DS91D176/DS91C176 100 MHz Single Channel M-LVDS Transceivers

Check for Samples: DS91C176, DS91D176

FEATURES

- **DC to 100+ MHz / 200+ Mbps Low Power, Low EMI Operation**
- **Optimal for ATCA, uTCA Clock Distribution Networks**
- **Meets or Exceeds TIA/EIA-899 M-LVDS Standard**
- **Wide Input Common Mode Voltage for Increased Noise Immunity**
- **DS91D176 has Type 1 Receiver Input**
- **DS91C176 has Type 2 Receiver with Fail-safe**
- **Industrial Temperature Range**
- **Space Saving SOIC-8 Package**

DESCRIPTION

The DS91C176 and DS91D176 are 100 MHz single channel M-LVDS (Multipoint Low Voltage Differential Signaling) transceivers designed for applications that utilize multipoint networks (e.g. clock distribution in ATCA and uTCA based systems). M-LVDS is a new bus interface standard (TIA/EIA-899) optimized for multidrop networks. Controlled edge rates, tight input receiver thresholds and increased drive strength are sone of the key enhancements that make M-LVDS devices an ideal choice for distributing signals via multipoint networks.

The DS91C176/DS91D176 are half-duplex transceivers that accept LVTTL/LVCMOS signals at the driver inputs and convert them to differential M-LVDS signals. The receiver inputs accept low voltage differential signals (LVDS, B-LVDS, M-LVDS, LV-PECL and CML) and convert them to 3V LVCMOS signals. The DS91D176 has a M-LVDS type 1 receiver input with no offset. The DS91C176 has an M-LVDS type 2 receiver which enable failsafe functionality.

Typical Application in an ATCA Clock Distribution Network

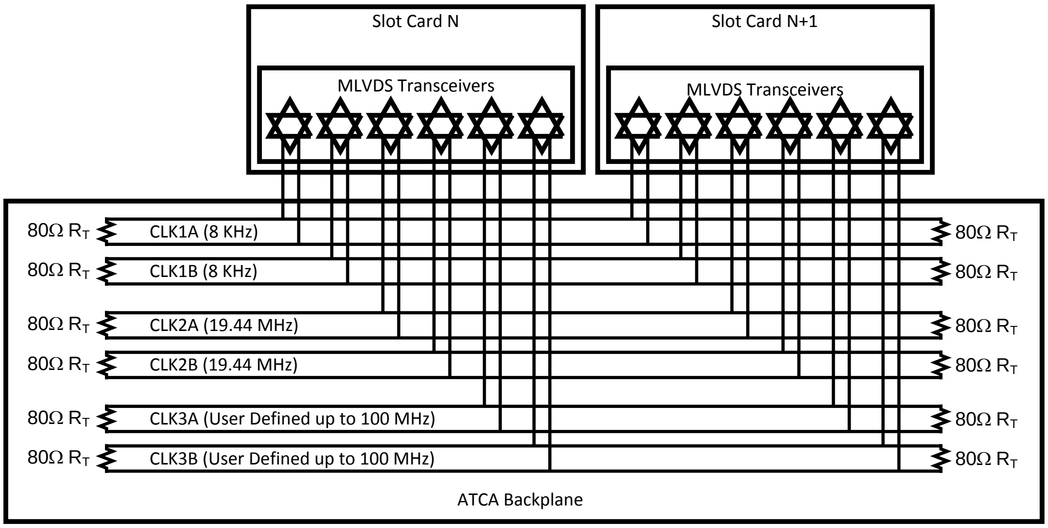

Figure 1. System Diagram

Connection and Logic Diagram

Top View

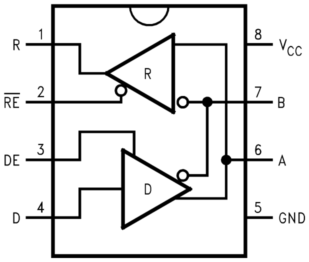

Figure 2. SOIC Package
See Package Number D0008A

M-LVDS Receiver Types

The EIA/TIA-899 M-LVDS standard specifies two different types of receiver input stages. A type 1 receiver has a conventional threshold that is centered at the midpoint of the input amplitude, $V_{ID}/2$. A type 2 receiver has a built in offset that is 100mV greater than $V_{ID}/2$. The type 2 receiver offset acts as a failsafe circuit where open or short circuits at the input will always result in the output stage being driven to a low logic state.

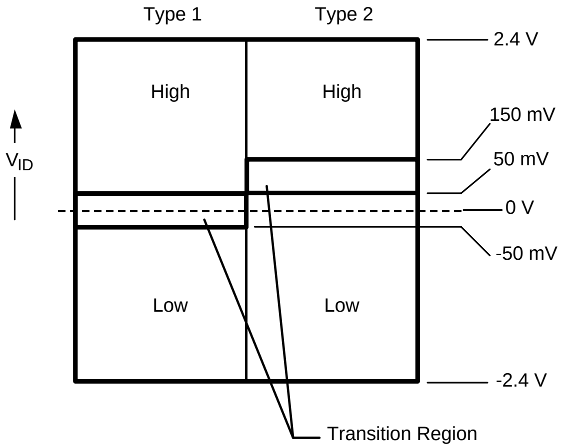

Figure 3. M-LVDS Receiver Input Thresholds

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage, V_{CC}	−0.3V to +4V
Control Input Voltages	−0.3V to (V_{CC} + 0.3V)
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltages	−1.8V to +4.1V
Receiver Input Voltages	−1.8V to +4.1V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation at +25°C	
SOIC Package	833 mW
Derate SOIC Package	6.67 mW/°C above +25°C
Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	150°C/W
θ_{JC}	63°C/W
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
ESD Ratings: (HBM 1.5kΩ, 100pF)	≥ 8 kV
(EIAJ 0Ω, 200pF)	≥ 250 V
(CDM 0Ω, 0pF)	≥ 1000 V

(1) "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	−1.4		+3.8	V
Differential Input Voltage V_{ID}			2.4	V
LVTTL Input Voltage High V_{IH}	2.0		V_{CC}	V
LVTTL Input Voltage Low V_{IL}	0		0.8	V
Operating Free Air Temperature T_A	−40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3) (4)

Parameter		Test Conditions	Min	Typ	Max	Units
M-LVDS Driver						
$\|V_{AB}\|$	Differential output voltage magnitude	R_L = 50Ω, C_L = 5pF See Figure 4 and Figure 6	480		650	mV
ΔV_{AB}	Change in differential output voltage magnitude between logic states		−50	0	+50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	R_L = 50Ω, C_L = 5pF See Figure 4 and Figure 5 ($V_{OS(PP)}$ @ 500KHz clock)	0.3	1.8	2.1	V
$\|\Delta V_{OS(SS)}\|$	Change in steady-state common-mode output voltage between logic states		0		+50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage			135		mV
$V_{A(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
$V_{B(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
(2) All typicals are given for V_{CC} = 3.3V and T_A = 25°C.
(3) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this datasheet.
(4) C_L includes fixture capacitance and C_D includes probe capacitance.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3) (4)

Parameter		Test Conditions		Min	Typ	Max	Units
$V_{P(H)}$	Voltage overshoot, low-to-high level output	R_L = 50Ω, C_L = 5pF,C_D = 0.5pF See Figure 9 and Figure 10 (5)				1.2V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output			−0.2V_{SS}			V
I_{IH}	High-level input current (LVTTL inputs)	V_{IH} = 2.0V		-15		15	μA
I_{IL}	Low-level input current (LVTTL inputs)	V_{IL} = 0.8V		-15		15	μA
V_{IKL}	Input Clamp Voltage (LVTTL inputs)	I_{IN} = -18mA		-1.5			V
I_{OS}	Differential short-circuit output current	See Figure 8		-43		43	mA
M-LVDS Receiver							
V_{IT+}	Positive-going differential input voltage threshold	See FUNCTION TABLES	Type 1		20	50	mV
			Type 2		94	150	mV
V_{IT-}	Negative-going differential input voltage threshold	See FUNCTION TABLES	Type 1	−50	20		mV
			Type 2	50	94		mV
V_{OH}	High-level output voltage (LVTTL output)	I_{OH} = −8mA		2.4	2.7		V
V_{OL}	Low-level output voltage (LVTTL output)	I_{OL} = 8mA			0.28	0.4	V
I_{OZ}	TRI-STATE output current	V_O = 0V or 3.6V		−10		10	μA
I_{OSR}	Short-circuit receiver output current (LVTTL output)	V_O = 0V			-48	-90	mA
M-LVDS Bus (Input and Output) Pins							
I_A	Transceiver input/output current	V_A = 3.8V, V_B = 1.2V				32	μA
		V_A = 0V or 2.4V, V_B = 1.2V		−20		+20	μA
		V_A = −1.4V, V_B = 1.2V		−32			μA
I_B	Transceiver input/output current	V_B = 3.8V, V_A = 1.2V				32	μA
		V_B = 0V or 2.4V, V_A = 1.2V		−20		+20	μA
		V_B = −1.4V, V_A = 1.2V		−32			μA
I_{AB}	Transceiver input/output differential current (I_A − I_B)	V_A = V_B, −1.4V ≤ V ≤ 3.8V		−4		+4	μA
$I_{A(OFF)}$	Transceiver input/output power-off current	V_A = 3.8V, V_B = 1.2V, DE = V_{CC} 0V ≤ V_{CC} ≤ 1.5V				32	μA
		V_A = 0V or 2.4V, V_B = 1.2V, DE = V_{CC} 0V ≤ V_{CC} ≤ 1.5V		−20		+20	μA
		V_A = −1.4V, V_B = 1.2V, DE =V_{CC} 0V ≤ V_{CC} ≤ 1.5V		−32			μA
$I_{B(OFF)}$	Transceiver input/output power-off current	V_B = 3.8V, V_A = 1.2V, DE = V_{CC} 0V ≤ V_{CC} ≤ 1.5V				32	μA
		V_B = 0V or 2.4V, V_A = 1.2V, DE = V_{CC} 0V ≤ V_{CC} ≤ 1.5V		−20		+20	μA
		V_B = −1.4V, V_A = 1.2V, DE = V_{CC} 0V ≤ V_{CC} ≤ 1.5V		−32			μA
$I_{AB(OFF)}$	Transceiver input/output power-off differential current ($I_{A(OFF)}$ − $I_{B(OFF)}$)	V_A = V_B, −1.4V ≤ V ≤ 3.8V, DE = V_{CC} 0V ≤ V_{CC} ≤ 1.5V		−4		+4	μA
C_A	Transceiver input/output capacitance	V_{CC} = OPEN			9		pF
C_B	Transceiver input/output capacitance				9		pF
C_{AB}	Transceiver input/output differential capacitance				5.7		pF
$C_{A/B}$	Transceiver input/output capacitance balance (C_A/C_B)				1.0		

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(5) Not production tested. Specified by a statistical analysis on a sample basis at the time of characterization.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3) (4)

Parameter		Test Conditions	Min	Typ	Max	Units
SUPPLY CURRENT (V_{CC})						
I_{CCD}	Driver Supply Current	R_L = 50Ω, DE = V_{CC}, $\overline{RE}$ = V_{CC}		20	29.5	mA
I_{CCZ}	TRI-STATE Supply Current	DE = GND, $\overline{RE}$ = V_{CC}		6	9.0	mA
I_{CCR}	Receiver Supply Current	DE = GND, $\overline{RE}$ = GND		14	18.5	mA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2)

Parameter		Test Conditions	Min	Typ	Max	Units
DRIVER AC SPECIFICATION						
t_{PLH}	Differential Propagation Delay Low to High	R_L = 50Ω, C_L = 5 pF, C_D = 0.5 pF Figure 9 and Figure 10	1.3	3.4	5.0	ns
t_{PHL}	Differential Propagation Delay High to Low		1.3	3.1	5.0	ns
t_{SKD1} ($t_{sk(p)}$)	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$ (3) (4)			300	420	ps
t_{SKD3}	Part-to-Part Skew (5) (5)				1.3	ns
t_{TLH} (t_r)	Rise Time (4)		1.0	1.8	3.0	ns
t_{THL} (t_f)	Fall Time (4)		1.0	1.8	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	R_L = 50Ω, C_L = 5 pF, C_D = 0.5 pF See Figure 11 and Figure 12			8	ns
t_{PZL}	Enable Time (Z to Active Low)				8	ns
t_{PLZ}	Disable Time (Active Low to Z)				8	ns
t_{PHZ}	Disable Time (Active High to Z)				8	ns
t_{JIT}	Random Jitter, RJ (4)	100 MHz Clock Pattern (6)		2.5	5.5	psrms
f_{MAX}	Maximum Data Rate		200			Mbps
RECEIVER AC SPECIFICATION						
t_{PLH}	Propagation Delay Low to High	C_L = 15 pF See Figure 13, Figure 14 and Figure 15	2.0	4.7	7.5	ns
t_{PHL}	Propagation Delay High to Low		2.0	5.3	7.5	ns
t_{SKD1} ($t_{sk(p)}$)	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$ (3) (4)			0.6	1.7	ns
t_{SKD3}	Part-to-Part Skew (5) (4)				1.3	ns
t_{TLH} (t_r)	Rise Time (4)		0.5	1.2	2.5	ns
t_{THL} (t_f)	Fall Time (4)		0.5	1.2	2.5	ns
t_{PZH}	Enable Time (Z to Active High)	R_L = 500Ω, C_L = 15 pF See Figure 16 and Figure 17			10	ns
t_{PZL}	Enable Time (Z to Active Low)				10	ns
t_{PLZ}	Disable Time (Active Low to Z)				10	ns
t_{PHZ}	Disable Time (Active High to Z)				10	ns
f_{MAX}	Maximum Data Rate		200			Mbps

(1) All typicals are given for V_{CC} = 3.3V and T_A = 25°C.
(2) C_L includes fixture capacitance and C_D includes probe capacitance.
(3) t_{SKD1}, $\lvert t_{PLHD} - t_{PHLD} \rvert$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(4) Not production tested. Specified by a statistical analysis on a sample basis at the time of characterization.
(5) t_{SKD3}, Part-to-Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(6) Stimulus and fixture Jitter has been subtracted.

Test Circuits and Waveforms

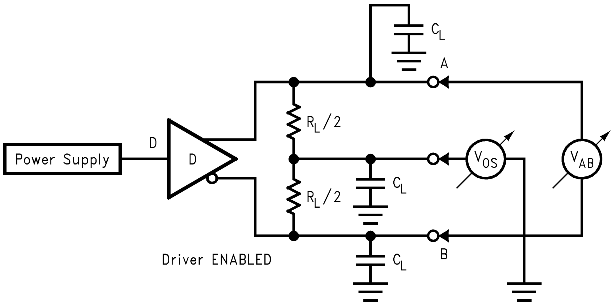


Figure 4. Differential Driver Test Circuit

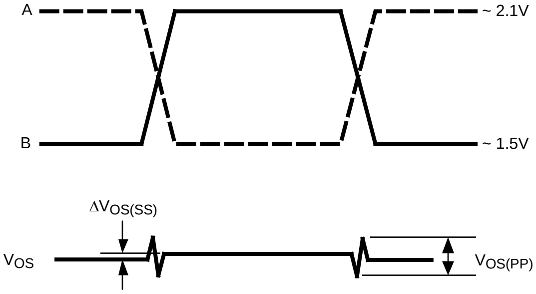


Figure 5. Differential Driver Waveforms

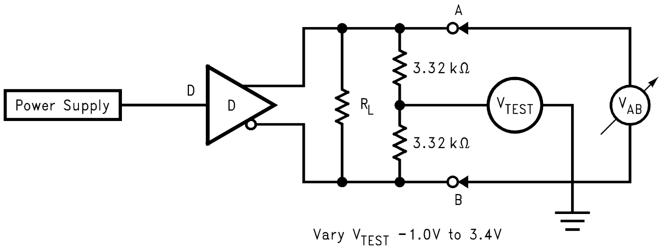


Figure 6. Differential Driver Full Load Test Circuit

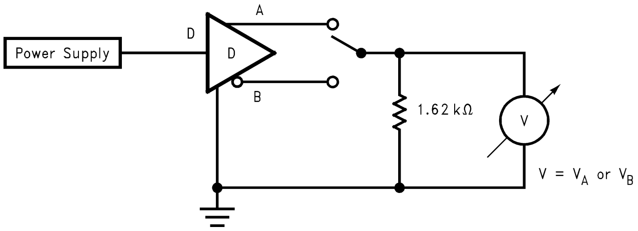


Figure 7. Differential Driver DC Open Test Circuit

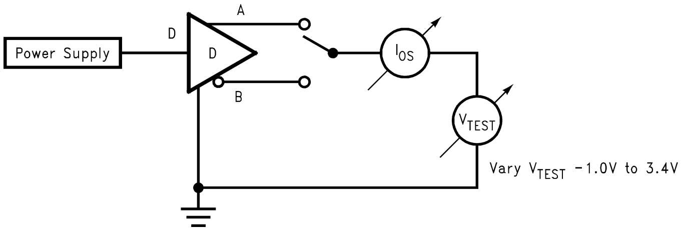


Figure 8. Differential Driver Short-Circuit Test Circuit

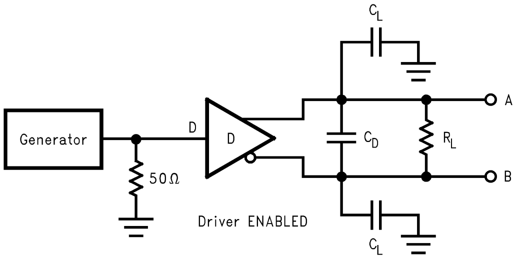


Figure 9. Driver Propagation Delay and Transition Time Test Circuit

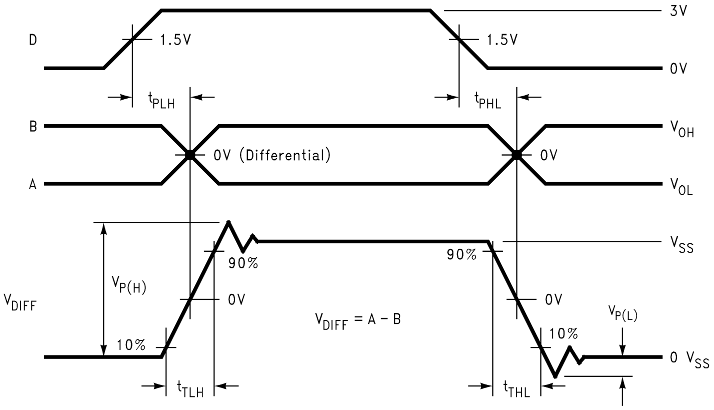


Figure 10. Driver Propagation Delays and Transition Time Waveforms

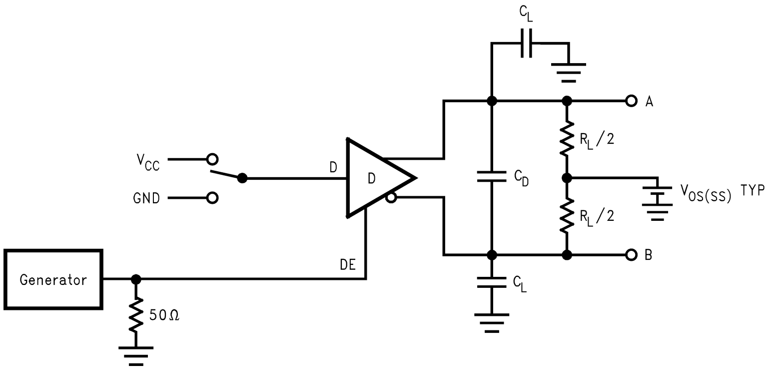


Figure 11. Driver TRI-STATE Delay Test Circuit

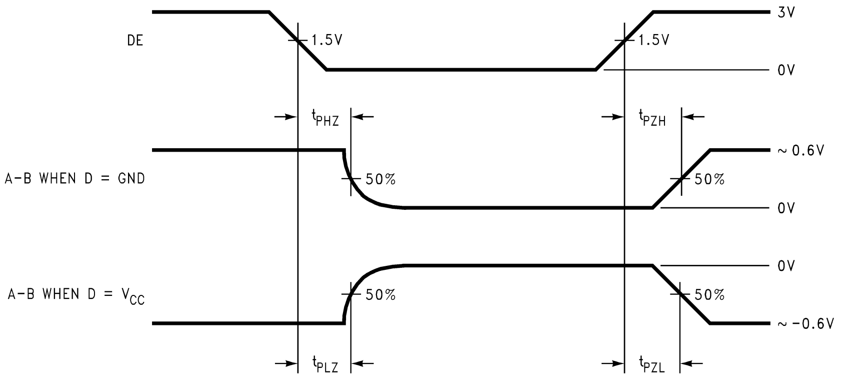


Figure 12. Driver TRI-STATE Delay Waveforms

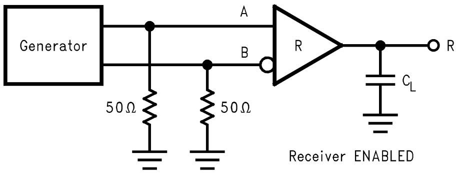


Figure 13. Receiver Propagation Delay and Transition Time Test Circuit

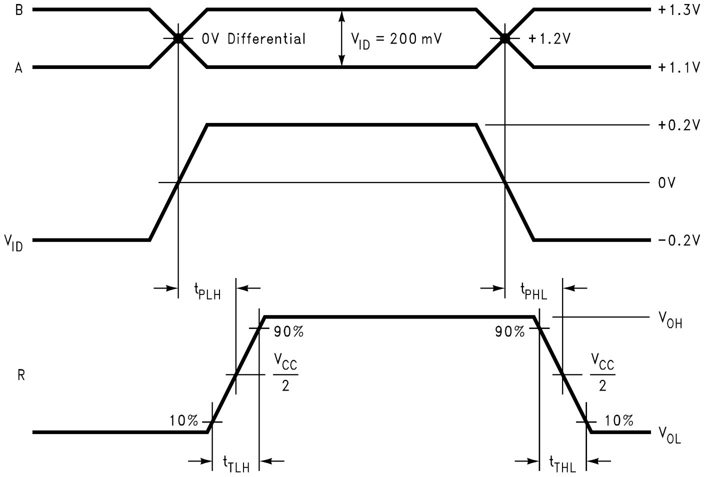


Figure 14. Type 1 Receiver Propagation Delay and Transition Time Waveforms

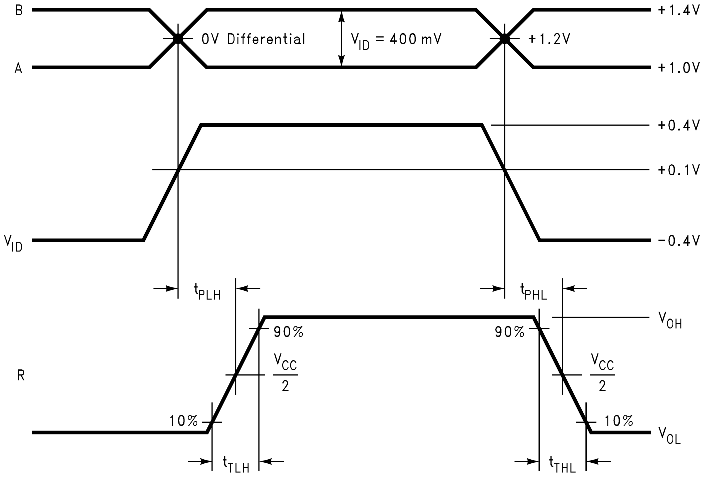


Figure 15. Type 2 Receiver Propagation Delay and Transition Time Waveforms

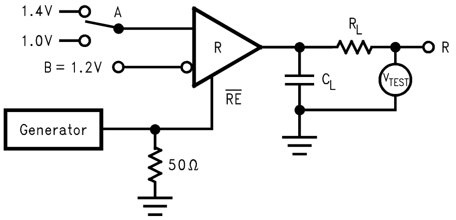


Figure 16. Receiver TRI-STATE Delay Test Circuit

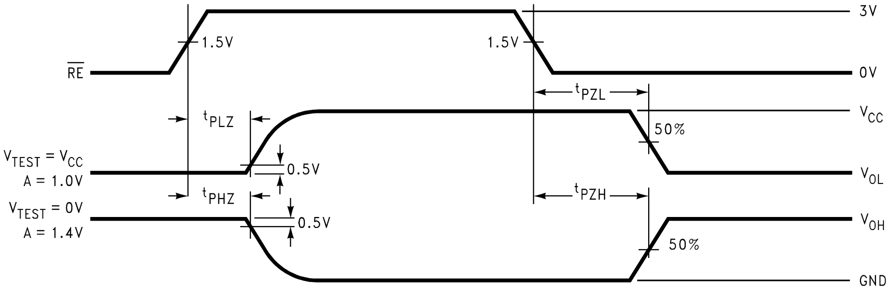


Figure 17. Receiver TRI-STATE Delay Waveforms

FUNCTION TABLES

Table 1. DS91D176/DS91C176 Transmitting[1]

Inputs			Outputs	
$\overline{RE}$	DE	D	B	A
X	2.0V	2.0V	L	H
X	2.0V	0.8V	H	L
X	0.8V	X	Z	Z

(1) X — Don't care condition
Z — High impedance state

Table 2. DS91D176 Receiving[1]

Inputs			Output
$\overline{RE}$	DE	A − B	R
0.8V	0.8V	≥ +0.05V	H
0.8V	0.8V	≤ −0.05V	L
0.8V	0.8V	0V	X
2.0V	0.8V	X	Z

(1) X — Don't care condition
Z — High impedance state

Table 3. DS91C176 Receiving[1]

Inputs			Output
$\overline{RE}$	DE	A − B	R
0.8V	0.8V	≥ +0.15V	H
0.8V	0.8V	≤ +0.05V	L
0.8V	0.8V	0V	L
2.0V	0.8V	X	Z

(1) X — Don't care condition
Z — High impedance state

Table 4. DS91D176 Receiver Input Threshold Test Voltages[1]

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	−2.400V	1.200V	L
3.800V	3.750V	0.050V	3.775V	H
3.750V	3.800V	−0.050V	3.775V	L
−1.400V	−1.350V	−0.050V	−1.375V	H
−1.350V	−1.400V	0.050V	−1.375V	L

(1) H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

Table 5. DS91C176 Receiver Input Threshold Test Voltages[1]

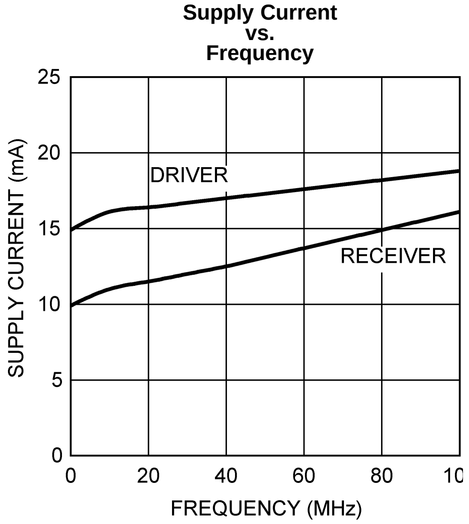
Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	−2.400V	1.200V	L
3.800V	3.650V	0.150V	3.725V	H
3.800V	3.750V	0.050V	3.775V	L
−1.250V	−1.400V	0.150V	−1.325V	H
−1.350V	−1.400V	0.050V	−1.375V	L

(1) H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

PIN DESCRIPTONS

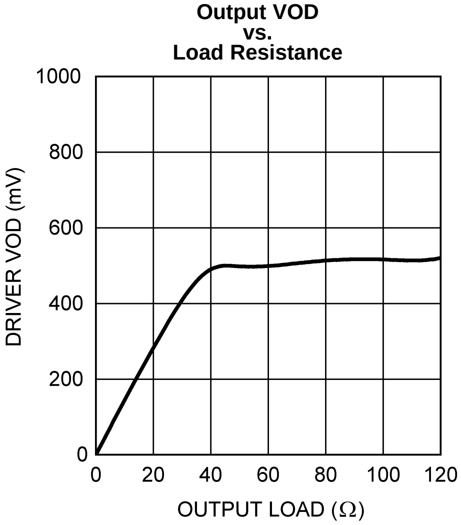
Pin No.	Name	Description
1	R	Receiver output pin
2	$\overline{\text{RE}}$	Receiver enable pin: When $\overline{\text{RE}}$ is high, the receiver is disabled. When $\overline{\text{RE}}$ is low or open, the receiver is enabled.
3	DE	Driver enable pin: When DE is low, the driver is disabled. When DE is high, the driver is enabled.
4	D	Driver input pin
5	GND	Ground pin
6	A	Non-inverting driver output pin/Non-inverting receiver input pin
7	B	Inverting driver output pin/Inverting receiver input pin
8	V_{CC}	Power supply pin, +3.3V ± 0.3V

Typical Performance Characteristics – DS91D176/DS91C176



Supply Current measured using a clock pattern with driver terminated to 50ohms . V_{CC} = 3.3V, T_A = +25°C.

Figure 18.



V_{CC} = 3.3V, T_A = +25°C

Figure 19.

REVISION HISTORY

Changes from Revision K (April 2013) to Revision L	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS91C176TMA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	DS91C 176MA	
DS91C176TMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS91C 176MA	Samples
DS91C176TMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	DS91C 176MA	Samples
DS91D176TMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS91D 176MA	Samples
DS91D176TMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS91D 176MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

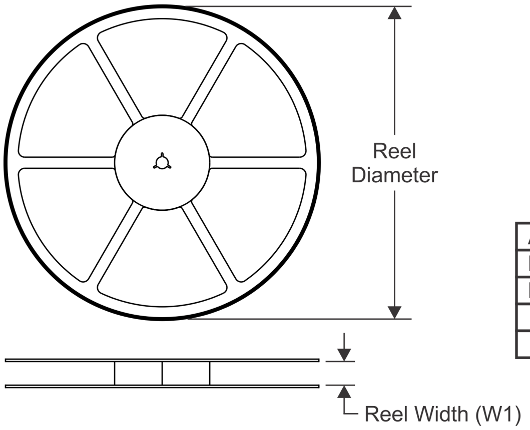
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

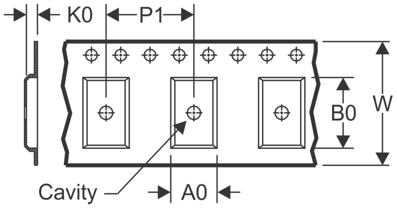
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

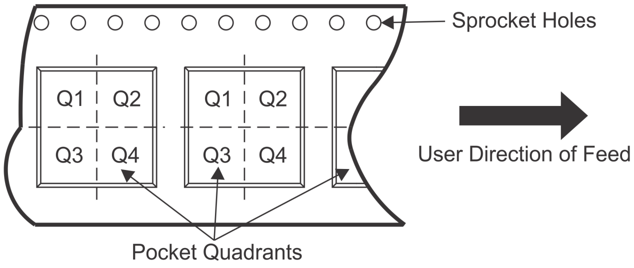


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

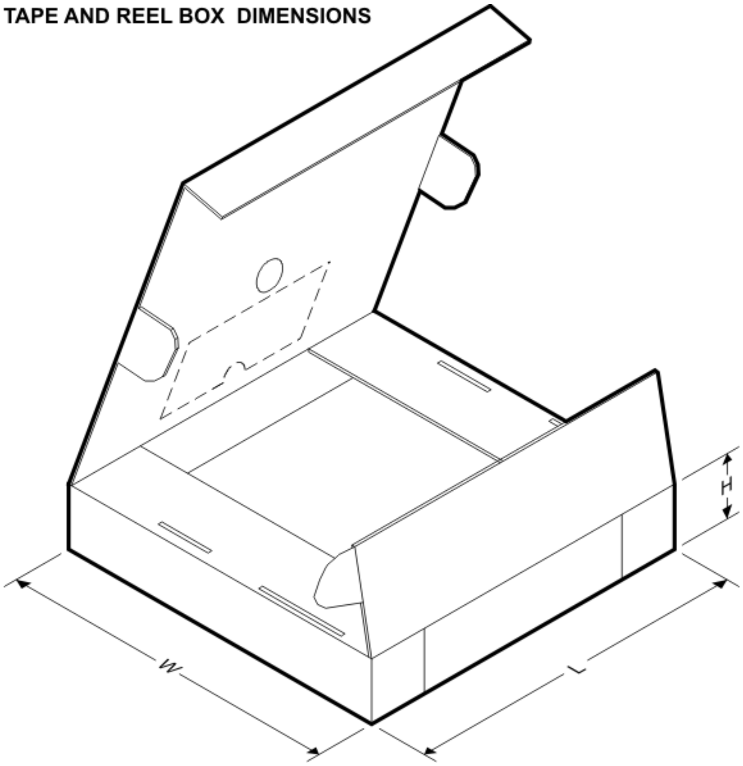
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS91C176TMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS91D176TMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

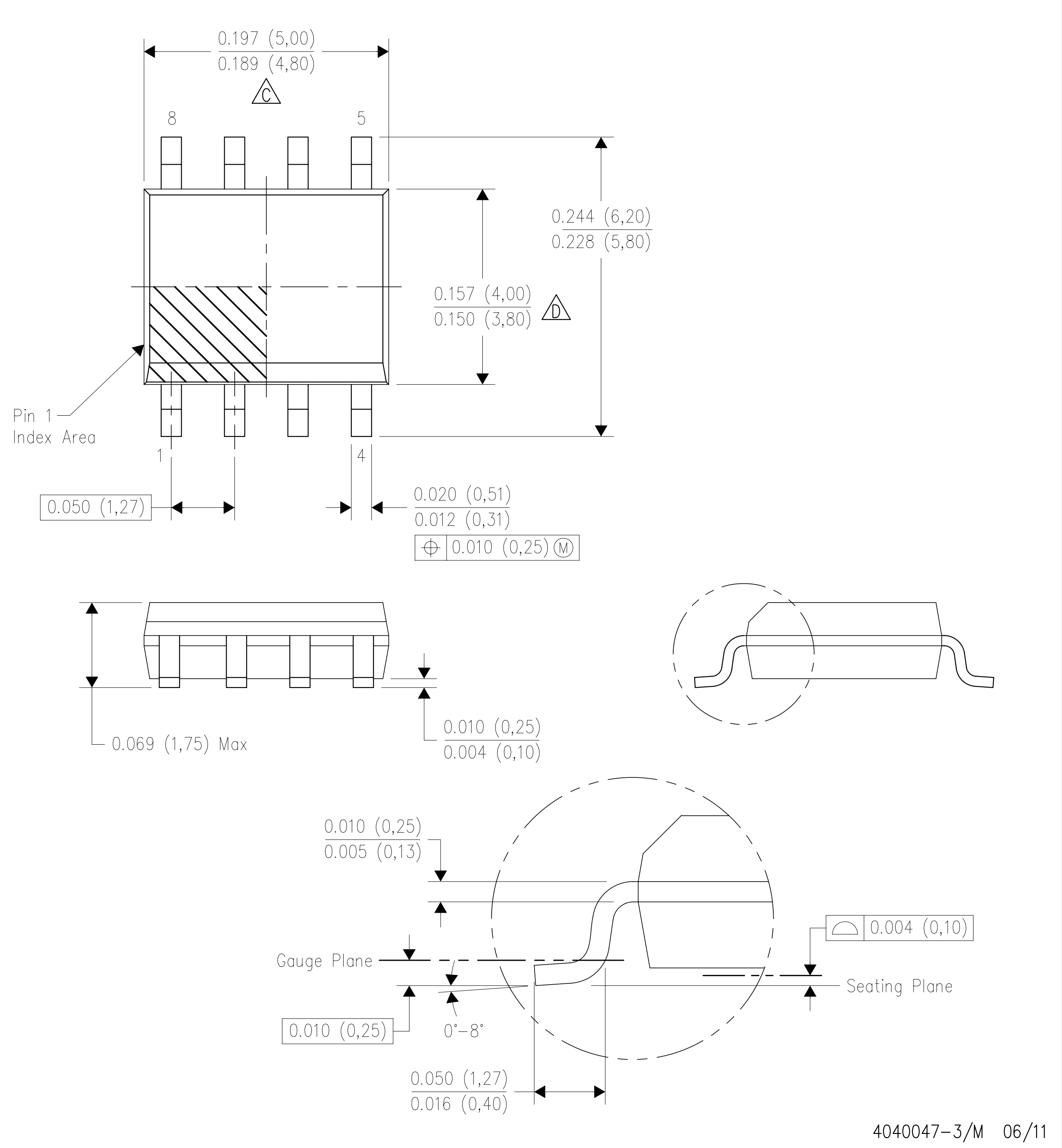
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS91C176TMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
DS91D176TMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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