- **Low Supply-Voltage Range, 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption:**
  - **Active Mode: 270 μA at 1 MHz, 2.2 V**
  - **Standby Mode (VLO): 0.3 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Internal Frequencies up to 16 MHz**
  - **Internal Very Low Power LF Oscillator**
  - **32-kHz Crystal (−40°C to 105°C only)**
  - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%**
  - **Resonator**
  - **External Digital Clock Source**
  - **External Resistor**
- **12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Seven Capture/Compare-With-Shadow Registers**

† The MSP430F24x1 devices are identical to the MSP430F24x devices, with the exception that the ADC12 module is not implemented.

- **Four Universal Serial Communication Interfaces (USCI)**
  - **USCI_A0 and USCI_A1**
    - **Enhanced UART Supporting Auto-Baudrate Detection**
    - **IrDA Encoder and Decoder**
    - **Synchronous SPI**
  - **USCI_B0 and USCI_B1**
    - **I²C™**
    - **Synchronous SPI**
- **On-Chip Comparator**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Brownout Detector**
- **Bootstrap Loader**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **Family Members Include:**
  - **MSP430F249**
    60KB+256B Flash Memory, 2KB RAM
- **Available in 64-Pin QFP Package (See Available Options)**
- **For Complete Module Descriptions, See *MSP430x2xx Family User's Guide*, Literature Number SLAU144**

description

The Texas Instruments MSP430 family of ultra-low power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The calibrated digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

description (continued)

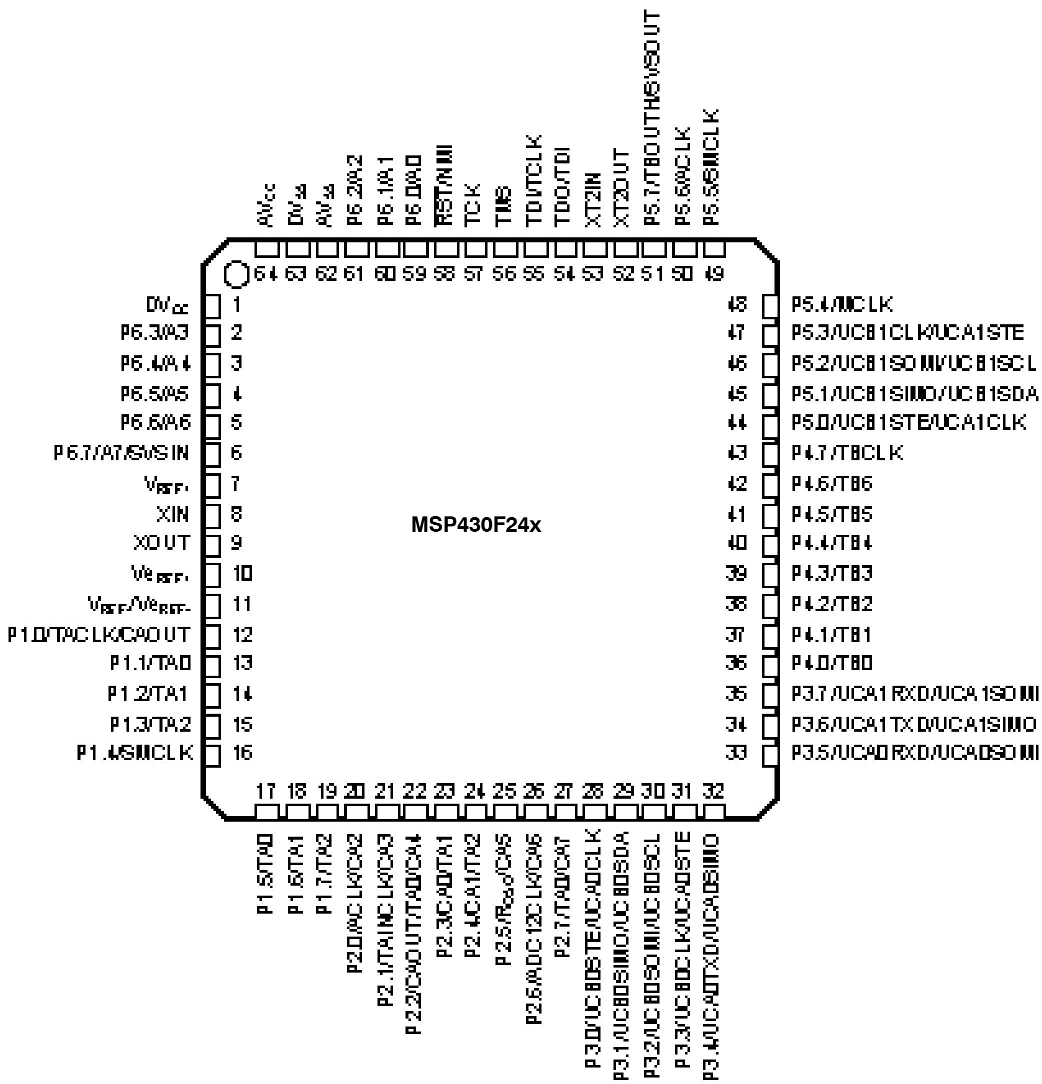
The MSP430F249 series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, a comparator, four universal serial communication interface (USCI) modules, and up to 48 I/O pins.

Typical applications include sensor systems, industrial control applications, hand-held meters, etc.

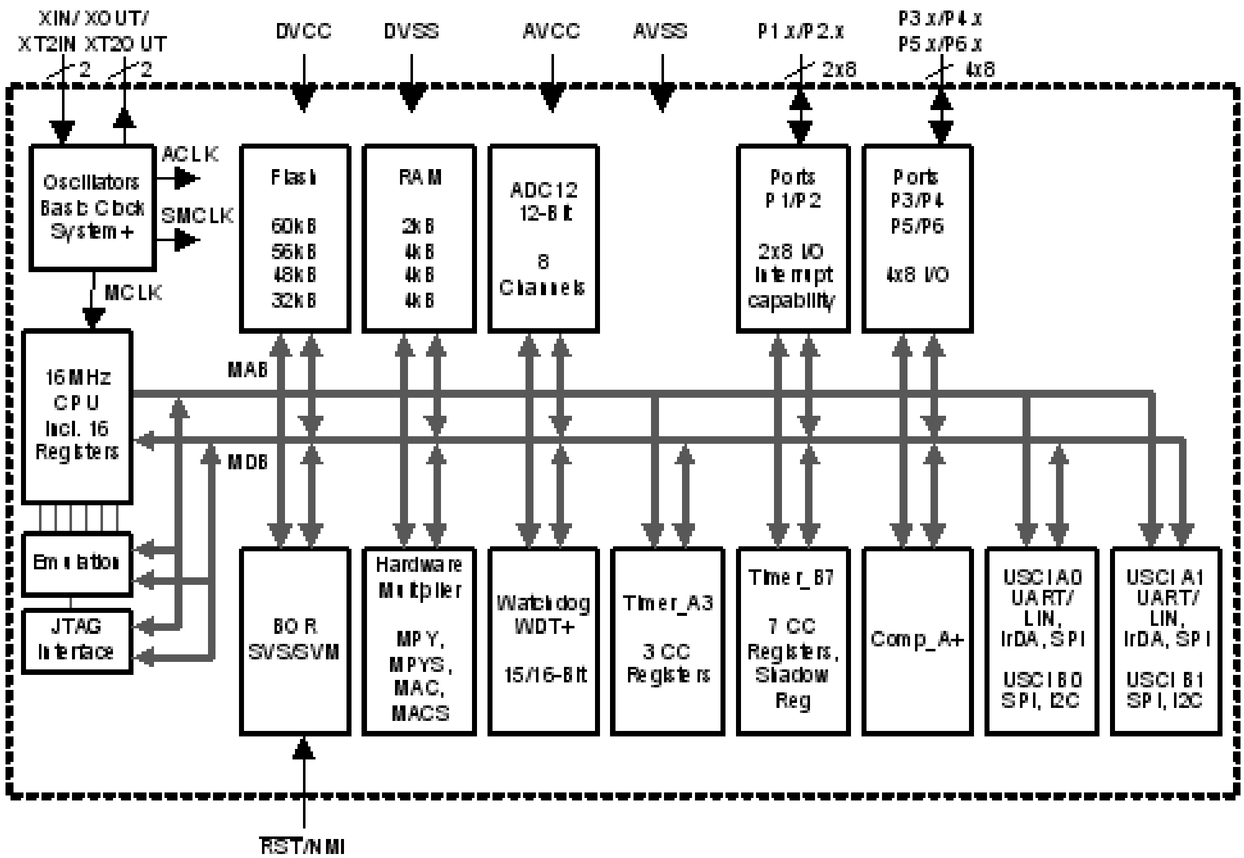
AVAILABLE OPTIONS

T_A	PACKAGE PLASTIC 64-PIN QFP (PM)
−55°C to 125°C	MSP430F249MPMEP

pin designation



functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK/ CAOUT	12	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input/Comparator_A output
P1.1/TA0	13	I/O	General-purpose digital I/O / Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O / Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O / Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O / SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O / Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O / Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O / Timer_A, compare: Out2 output
P2.0/ACLK/CA2	20	I/O	General-purpose digital I/O / ACLK output/Comparator_A input
P2.1/TAINCLK/ CA3	21	I/O	General-purpose digital I/O / Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0 /CA4	22	I/O	General-purpose digital I/O / Timer_A, capture: CCI0B input / Comparator_A output/BSL receive/Comparator_A input
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O / Timer_A, compare: Out1 output / Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O / Timer_A, compare: Out2 output / Comparator_A input
P2.5/R_{OSC}/CA5	25	I/O	General-purpose digital I/O / Input for external resistor defining the DCO nominal frequency / Comparator_A input
P2.6/ ADC12CLK/CA6	26	I/O	General-purpose digital I/O / Conversion clock – 12-bit ADC / Comparator_A input
P2.7/TA0/CA7	27	I/O	General-purpose digital I/O / Timer_A, compare: Out0 output / Comparator_A input
P3.0/UCB0STE/ UCA0CLK	28	I/O	General-purpose digital I/O / USCI B0 slave transmit enable / USCI A0 clock input/output
P3.1/UCB0SIMO/ UCB0SDA	29	I/O	General-purpose digital I/O / USCI B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/UCB0SOMI/ UCB0SCL	30	I/O	General-purpose digital I/O / USCI B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P3.3/UCB0CLK/ UCA0STE	31	I/O	General-purpose digital I/O / USCI B0 clock input/output, USCI A0 slave transmit enable
P3.4/UCA0TXD/ UCA0SIMO	32	I/O	General-purpose digital I/O / USCIA transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/UCA0RXD/ UCA0SOMI	33	I/O	General-purpose digital I/O / USCI A0 receive data input in UART mode, slave data out/master in in SPI mode
P3.6/UCA1TXD/ UCA1SIMO	34	I/O	General-purpose digital I/O / USCI A1 transmit data output in UART mode, slave data in/master out in SPI mode
P3.7/UCA1RXD/ UCA1SOMI	35	I/O	General-purpose digital I/O / USCIA1 receive data input in UART mode, slave data out/master in in SPI mode
P4.0/TB0	36	I/O	General-purpose digital I/O / Timer_B, capture: CCI0A/B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O / Timer_B, capture: CCI1A/B input, compare: Out1 output

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P4.2/TB2	38	I/O	General-purpose digital I/O / Timer_B, capture: CCI2A/B input, compare: Out2 output
P4.3/TB3	39	I/O	General-purpose digital I/O / Timer_B, capture: CCI3A/B input, compare: Out3 output
P4.4/TB4	40	I/O	General-purpose digital I/O / Timer_B, capture: CCI4A/B input, compare: Out4 output
P4.5/TB5	41	I/O	General-purpose digital I/O / Timer_B, capture: CCI5A/B input, compare: Out5 output
P4.6/TB6	42	I/O	General-purpose digital I/O / Timer_B, capture: CCI6A input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O / Timer_B, clock signal TBCLK input
P5.0/UCB1STE/ UCA1CLK	44	I/O	General-purpose digital I/O / USCI B1 slave transmit enable / USCI A1 clock input/output
P5.1/UCB1SIMO/ UCB1SDA	45	I/O	General-purpose digital I/O / USCI B1slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P5.2/UCB1SOMI/ UCB1SCL	46	I/O	General-purpose digital I/O / USCI B1slave out/master in in SPI mode, SCL I^2C clock in I^2C mode
P5.3/UCB1CLK/ UCA1STE	47	I/O	General-purpose digital I/O / USCI B1 clock input/output, USCI A1 slave transmit enable
P5.4/MCLK	48	I/O	General-purpose digital I/O / main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O / submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O / auxiliary clock ACLK output
P5.7/TBOUTH/ SVSOUT	51	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance − Timer_B TB0 to TB6/SVS comparator output
P6.0/A0	59	I/O	General-purpose digital I/O / analog input A0 – 12-bit ADC
P6.1/A1	60	I/O	General-purpose digital I/O / analog input A1 – 12-bit ADC
P6.2/A2	61	I/O	General-purpose digital I/O / analog input A2 – 12-bit ADC
P6.3/A3	2	I/O	General-purpose digital I/O / analog input A3 – 12-bit ADC
P6.4/A4	3	I/O	General-purpose digital I/O / analog input A4 – 12-bit ADC
P6.5/A5	4	I/O	General-purpose digital I/O / analog input A5 – 12-bit ADC
P6.6/A6	5	I/O	General-purpose digital I/O / analog input A6 – 12-bit ADC
P6.7/A7/SVSIN	6	I/O	General-purpose digital I/O / analog input A7 – 12-bit ADC/SVS input
XT2OUT	52	O	Output of crystal oscillator XT2
XT2IN	53	I	Input for crystal oscillator XT2
$\overline{RST}$/NMI	58	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in flash devices).
TCK	57	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output. TDO/TDI data output or programming data input terminal
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
Ve_{REF+}	10	I	Input for an external reference voltage
V_{REF+}	7	O	Output of positive of the reference voltage in the ADC12
V_{REF-}/Ve_{REF-}	11	I	Negativefor the reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output for crystal oscillator XT1. Standard or watch crystals can be connected.
QFN Pad	NA	NA	QFN package pad connection to DV_{SS} recommended (RTD package only)

short-form description

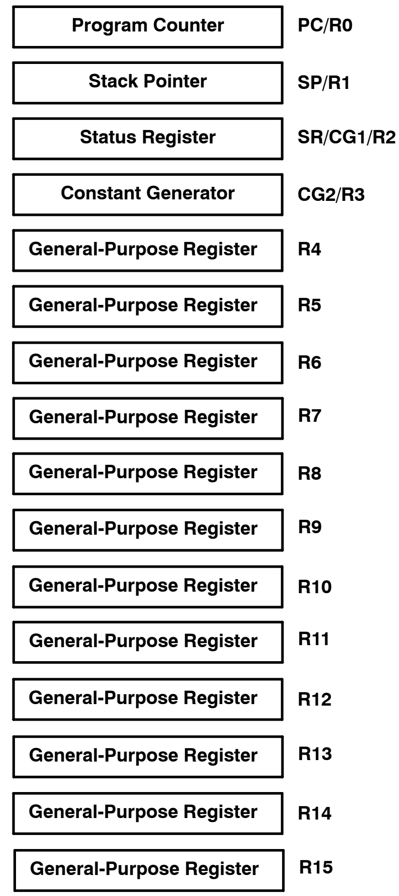
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 –––> R5
Single operands, destination only	e.g., CALL R8	PC ––>(TOS), R8––> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 ––> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)––> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) ––> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) ––> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) ––> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) ––> R11 R10 + 2––> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 ––> M(TONI)

NOTE: S = source, D = destination

operating modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is disabled
    DCO’s dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO’s dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO’s dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO’s dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. If the reset vector (0xFFFE) contains 0xFFFF (e.g., flash is not programmed) the CPU enters LPM4 after power-up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out of range (see Note 1)	PORIFG WDTIFG RSTIFG KEYV (see Note 2)	Reset	0xFFFE	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 and 7)	(Non)maskable (Non)maskable (Non)maskable	0xFFFC	30
Timer_B7 (see Note 3)	TBCCR0 CCIFG (see Note 4)	Maskable	0xFFFA	29
Timer_B7 (see Note 3)	TBCCR1 to TBCCR6 CCIFGs, TBIFG (see Notes 2 and 4)	Maskable	0xFFF8	28
Comparator_A+	CAIFG	Maskable	0xFFF6	27
Watchdog timer+	WDTIFG	Maskable	0xFFF4	26
Timer_A3	TACCR0 CCIFG (see Note 4)	Maskable	0xFFF2	25
Timer_A3	TACCR1 CCIFG TACCR2 CCIFG TAIFG (see Note 2 and 4)	Maskable	0xFFF0	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG (see Note 2 and 5)	Maskable	0xFFEE	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive / transmit	UCA0TXIFG, UCB0TXIFG (see Note 2 and 6)	Maskable	0xFFEC	22
ADC12 (see Note 8)	ADC12IFG (see Notes 2 and 4)	Maskable	0xFFEA	21
			0xFFE8	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 2 and 4)	Maskable	0xFFE6	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 and 4)	Maskable	0xFFE4	18
USCI A1/B1 receive	UCA1RXIFG, UCB1RXIFG (see Note 2)	Maskable	0xFFE2	17
USCI A1/B1 transmit	UCA1TXIFG, UCB1TXIFG (see Note 2)	Maskable	0xFFE0	16
Reserved (see Notes 9 and 10)	Reserved		0xFFDE to 0xFFC0	15 to 0, lowest

NOTES:
1. A reset is executed if the CPU tries to fetch instructions from within the module register memory address range (0x0000 −0x01FF) or from within unused address ranges.
2. Multiple source flags.
3. Timer_B7 in MSP430F24x(1), MSP430F2410 family has 7 CCRs, Timer_B3 in MSP430F23x family has three CCRs. In Timer_B3, there are only interrupt flags TBCCR0, 1, and 2 CCIFGs, and the interrupt enable bits TBCCTL0, 1, and 2 CCIE.
4. Interrupt flags are located in the module.
5. In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
6. In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
7. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot.
8. ADC12 is not implemented in the MSP430F24x1 family.
9. The address 0xFFDE is used as bootstrap loader security key (BSLSKEY).
   A 0xAA55 at this location disables the BSL completely.
   A zero disables the erasure of the flash if an invalid password is supplied.
10. The interrupt vectors at addresses 0xFFDE to 0xFFC0 are not used in this device and can be used for regular program code if necessary.

special function registers

Most interrupt enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0x0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

Interrupt Enable register 1

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as general-purpose timer.
OFIE	Oscillator-fault-interrupt enable
NMIIE	Nonmaskable-interrupt enable
ACCVIE	Flash memory access violation interrupt enable

Address	7	6	5	4	3	2	1	0
0x1h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

Interrupt Enable register 2

UCA0RXIE	USCI_A0 receive-interrupt enable
UCA0TXIE	USCI_A0 transmit-interrupt enable
UCB0RXIE	USCI_B0 receive-interrupt enable
UCB0TXIE	USCI_B0 transmit-interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
0x02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

Interrupt Flag register 1

WDTIFG Set on watchdog-timer overflow or security key violation.
Reset on V_{CC} power-on, or a reset condition at the $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault

PORIFG Power-on interrupt flag. Set on V_{CC} power-up.

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power−up.

NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
0x03h					UCB0TXIFG	UCB0RXIFG	UCA0TXIFG	UCA0RXIFG
					rw-1	rw-0	rw-1	rw-0

Interrupt Flag register 2

UCA0RXIFG USCI_A0 receive-interrupt flag

UCA0TXIFG USCI_A0 transmit-interrupt flag

UCB0RXIFG USCI_B0 receive-interrupt flag

UCB0TXIFG USCI_B0 transmit-interrupt flag

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0,1)	Bit can be read and written. It is Reset or Set by POR.
	(shaded box)	SFR bit is not present in device.

memory organization

Memory Main: interrupt vector Main: code memory	Size Flash Flash	60KB 0xFFFF to 0xFFC0 0xFFFF to 0x1100
RAM (total)	Size	2KB 0x09FF to 0x0200
Information memory	Size Flash	256 Byte 0x10FF to 0x1000
Boot memory	Size ROM	1KB 0x0FFF to 0x0C00
RAM	Size	2KB 0x09FF to 0x0200
Peripherals	16-bit 8-bit SFR	0x01FF to 0x0100 0x00FF to 0x0010 0x000F to 0x0000

bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader* (literature number SLAA089).

BSL FUNCTION	PM, RTD PACKAGE PINS
Data Transmit	13 - P1.1
Data Receive	22 - P2.2

flash memory

The flash memory can be programmed via the JTAG port, the BSL, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0−n.
  Segments A to D are also called information memory.
- Segment A contains calibration data. After reset segment A is protected against programming or erasing. It can be unlocked but care should be taken not to erase this segment if the calibration data is required.
- Flash content integrity check with marginal read modes.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide*, literature number SLAU144.

oscillator and system clock

The clock system in the MSP43F249 family of devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power, low-frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxillary clock (ACLK), sourced from a 32768−Hz watch crystal, high frequency crystal, or a very low power LF oscillator for −40°C to 105°C operation. For >105°C, use external clock source.
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules

calibration data stored in information memory segment A

Calibration data is stored for the DCO and for the ADC12. It is organized in a tag−length−value (TLV) structure.

TAGS USED BY THE ADC CALIBRATION TAGS			
NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at VCC = 3 V and T_A = 25°C at calibration
TAG_ADC12_1	0x10DA	0x10	ADC12_1 calibration tag
TAG_EMPTY	–	0xFE	Identifier for empty memory areas

LABELS USED BY THE ADC CALIBRATION TAGS			
LABEL	CONDITION AT CALIBRATION / DESCRIPTION	SIZE	ADDRESS OFFSET
CAL_ADC_25T85	INCHx = 0x1010; REF2_5 = 1, T_A = 125°C	word	0x000E
CAL_ADC_25T30	INCHx = 0x1010; REF2_5 = 1, T_A = 30°C	word	0x000C
CAL_ADC_25VREF_FACTOR	REF2_5 = 1, T_A = 30°C, I_{VREF+} = 1.0 mA	word	0x000A
CAL_ADC_15T85	INCHx = 0x1010; REF2_5 = 0, T_A = 125°C	word	0x0008
CAL_ADC_15T30	INCHx = 0x1010; REF2_5 = 0, T_A = 30°C	word	0x0006
CAL_ADC_15VREF_FACTOR	REF2_5 = 0, T_A = 30°C, I_{VREF+} = 0.5 mA	word	0x0004
CAL_ADC_OFFSET	External Vref = 1.5 V, $f_{ADC12CLK}$ = 5 MHz	word	0x0002
CAL_ADC_GAIN_FACTOR	External Vref = 1.5 V, $f_{ADC12CLK}$ = 5 MHz	word	0x0000
CAL_BC1_1MHz	–	byte	0x0007
CAL_DCO_1MHz	–	byte	0x0006
CAL_BC1_8MHz	–	byte	0x0005
CAL_DCO_8MHz	–	byte	0x0004
CAL_BC1_12MHz	–	byte	0x0003
CAL_DCO_12MHz	–	byte	0x0002
CAL_BC1_16MHz	–	byte	0x0001
CAL_DCO_16MHz	–	byte	0x0000

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure that the default DCO settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are up to six 8-bit I/O ports implemented—ports P1 through P6.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

watchdog timer + (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

hardware multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16, 16×8, 8×16, and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
12 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
21 - P2.1	TAINCLK	INCLK			
13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1
22 - P2.2	TA0	CCI0B			17 - P1.5
	DV_{SS}	GND			27 - P2.7
	DV_{CC}	V_{CC}			
14 - P1.2	TA1	CCI1A	CCR1	TA1	14 - P1.2
	CAOUT (internal)	CCI1B			18 - P1.6
	DV_{SS}	GND			23 - P2.3
	DV_{CC}	V_{CC}			ADC12† (internal)
15 - P1.3	TA2	CCI2A	CCR2	TA2	15 - P1.3
	ACLK (internal)	CCI2B			19 - P1.7
	DV_{SS}	GND			24 - P2.4
	DV_{CC}	V_{CC}			

† Not available in the MSP430F24x1 devices

timer_B7

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_B7 SIGNAL CONNECTIONS

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	$\overline{TBCLK}$	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12† (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12† (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3
39 - P4.3	TB3	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4
40 - P4.4	TB4	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5
41 - P4.5	TB5	CCI5B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6
	ACLK (internal)	CCI6B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

† Not available in the MSP430F24x1 devices

timer_B3 (MSP430F23x devices)

Timer_B3 is a 16-bit timer/counter with seven capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_B3 SIGNAL CONNECTIONS					
INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	$\overline{TBCLK}$	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

universal serial communications interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) or I^2C and asynchronous combination protocols such UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

The USCI A module provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

The USCI B module provides support for SPI (3 or 4 pin) and I^2C.

comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog−to−digital conversions, battery−voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

peripheral file map

PERIPHERAL FILE MAP			
ADC12	Interrupt-vector-word register	ADC12IV	0x01A8
	Inerrupt-enable register	ADC12IE	0x01A6
	Inerrupt-flag register	ADC12IFG	0x01A4
	Control register 1	ADC12CTL1	0x01A2
	Control register 0	ADC12CTL0	0x01A0
	Conversion memory 15	ADC12MEM15	0x015E
	Conversion memory 14	ADC12MEM14	0x015C
	Conversion memory 13	ADC12MEM13	0x015A
	Conversion memory 12	ADC12MEM12	0x0158
	Conversion memory 11	ADC12MEM11	0x0156
	Conversion memory 10	ADC12MEM10	0x0154
	Conversion memory 9	ADC12MEM9	0x0152
	Conversion memory 8	ADC12MEM8	0x0150
	Conversion memory 7	ADC12MEM7	0x014E
	Conversion memory 6	ADC12MEM6	0x014C
	Conversion memory 5	ADC12MEM5	0x014A
	Conversion memory 4	ADC12MEM4	0x0148
	Conversion memory 3	ADC12MEM3	0x0146
	Conversion memory 2	ADC12MEM2	0x0144
	Conversion memory 1	ADC12MEM1	0x0142
	Conversion memory 0	ADC12MEM0	0x0140
	ADC memory-control register15	ADC12MCTL15	0x008F
	ADC memory-control register14	ADC12MCTL14	0x008E
	ADC memory-control register13	ADC12MCTL13	0x008D
	ADC memory-control register12	ADC12MCTL12	0x008C
	ADC memory-control register11	ADC12MCTL11	0x008B
	ADC memory-control register10	ADC12MCTL10	0x008A
	ADC memory-control register9	ADC12MCTL9	0x0089
	ADC memory-control register8	ADC12MCTL8	0x0088
	ADC memory-control register7	ADC12MCTL7	0x0087
	ADC memory-control register6	ADC12MCTL6	0x0086
	ADC memory-control register5	ADC12MCTL5	0x0085
	ADC memory-control register4	ADC12MCTL4	0x0084
	ADC memory-control register3	ADC12MCTL3	0x0083
	ADC memory-control register2	ADC12MCTL2	0x0082
	ADC memory-control register1	ADC12MCTL1	0x0081
	ADC memory-control register0	ADC12MCTL0	0x0080

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
Timer_B7	Capture/compare register 6	TBCCR6	0x019E
	Capture/compare register 5	TBCCR5	0x019C
	Capture/compare register 4	TBCCR4	0x019A
	Capture/compare register 3	TBCCR3	0x0198
	Capture/compare register 2	TBCCR2	0x0196
	Capture/compare register 1	TBCCR1	0x0194
	Capture/compare register 0	TBCCR0	0x0192
	Timer_B register	TBR	0x0190
	Capture/compare control 6	TBCCTL6	0x018E
	Capture/compare control 5	TBCCTL5	0x018C
	Capture/compare control 4	TBCCTL4	0x018A
	Capture/compare control 3	TBCCTL3	0x0188
	Capture/compare control 2	TBCCTL2	0x0186
	Capture/compare control 1	TBCCTL1	0x0184
	Capture/compare control 0	TBCCTL0	0x0182
	Timer_B control	TBCTL	0x0180
	Timer_B interrupt vector	TBIV	0x011E
Timer_A3	Capture/compare register 2	TACCR2	0x0176
	Capture/compare register 1	TACCR1	0x0174
	Capture/compare register 0	TACCR0	0x0172
	Timer_A register	TAR	0x0170
	Reserved		0x016E
	Reserved		0x016C
	Reserved		0x016A
	Reserved		0x0168
	Capture/compare control 2	TACCTL2	0x0166
	Capture/compare control 1	TACCTL1	0x0164
	Capture/compare control 0	TACCTL0	0x0162
	Timer_A control	TACTL	0x0160
	Timer_A interrupt vector	TAIV	0x012E

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
Hardware Multiplier	Sum extend	SUMEXT	0x013E
	Result high word	RESHI	0x013C
	Result low word	RESLO	0x013A
	Second operand	OP2	0x0138
	Multiply signed +accumulate/operand1	MACS	0x0136
	Multiply+accumulate/operand1	MAC	0x0134
	Multiply signed/operand1	MPYS	0x0132
	Multiply unsigned/operand1	MPY	0x0130
Flash	Flash control 4	FCTL4	0x01BE
	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog	Watchdog Timer control	WDTCTL	0x0120
USCI A0/B0	USCI A0 auto baud rate control	UCA0ABCTL	0x005D
	USCI A0 transmit buffer	UCA0TXBUF	0x0067
	USCI A0 receive buffer	UCA0RXBUF	0x0066
	USCI A0 status	UCA0STAT	0x0065
	USCI A0 modulation control	UCA0MCTL	0x0064
	USCI A0 baud rate control 1	UCA0BR1	0x0063
	USCI A0 baud rate control 0	UCA0BR0	0x0062
	USCI A0 control 1	UCA0CTL1	0x0061
	USCI A0 control 0	UCA0CTL0	0x0060
	USCI A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI A0 IrDA transmit control	UCA0IRTCLT	0x005E
	USCI B0 transmit buffer	UCB0TXBUF	0x006F
	USCI B0 receive buffer	UCB0RXBUF	0x006E
	USCI B0 status	UCB0STAT	0x006D
	USCI B0 I2C Interrupt enable	UCB0CIE	0x006C
	USCI B0 baud rate control 1	UCB0BR1	0x006B
	USCI B0 baud rate control 0	UCB0BR0	0x006A
	USCI B0 control 1	UCB0CTL1	0x0069
	USCI B0 control 0	UCB0CTL0	0x0068
	USCI B0 I2C slave address	UCB0SA	0x011A
	USCI B0 I2C own address	UCB0OA	0x0118

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
USCI A1/B1	USCI A1 auto baud rate control	UCA1ABCTL	0x00CD
	USCI A1 transmit buffer	UCA1TXBUF	0x00D7
	USCI A1 receive buffer	UCA1RXBUF	0x00D6
	USCI A1 status	UCA1STAT	0x00D5
	USCI A1 modulation control	UCA1MCTL	0x00D4
	USCI A1 baud rate control 1	UCA1BR1	0x00D3
	USCI A1 baud rate control 0	UCA1BR0	0x00D2
	USCI A1 control 1	UCA1CTL1	0x00D1
	USCI A1 control 0	UCA1CTL0	0x00D0
	USCI A1 IrDA receive control	UCA1IRRCTL	0x00CF
	USCI A1 IrDA transmit control	UCA1IRTCLT	0x00CE
	USCI B1 transmit buffer	UCB1TXBUF	0x00DF
	USCI B1 receive buffer	UCB1RXBUF	0x00DE
	USCI B1 status	UCB1STAT	0x00DD
	USCI B1 I2C Interrupt enable	UCB1CIE	0x00DC
	USCI B1 baud rate control 1	UCB1BR1	0x00DB
	USCI B1 baud rate control 0	UCB1BR0	0x00DA
	USCI B1 control 1	UCB1CTL1	0x00D9
	USCI B1 control 0	UCB1CTL0	0x00D8
	USCI B1 I2C slave address	UCB1SA	0x017E
	USCI B1 I2C own address	UCB1OA	0x017C
	USCI A1/B1 interrupt enable	UC1IE	0x0006
	USCI A1/B1 interrupt flag	UC1IFG	0x0007
Comparator_A+	Comparator_A port disable	CAPD	0x005B
	Comparator_A control2	CACTL2	0x005A
	Comparator_A control1	CACTL1	0x0059
Basic Clock	Basic clock system control3	BCSCTL3	0x0053
	Basic clock system control2	BCSCTL2	0x0058
	Basic clock system control1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	0x0055
Port P6	Port P6 resistor enable	P6REN	0x0013
	Port P6 selection	P6SEL	0x0037
	Port P6 direction	P6DIR	0x0036
	Port P6 output	P6OUT	0x0035
	Port P6 input	P6IN	0x0034
Port P5	Port P5 resistor enable	P5REN	0x0012
	Port P5 selection	P5SEL	0x0033
	Port P5 direction	P5DIR	0x0032
	Port P5 output	P5OUT	0x0031
	Port P5 input	P5IN	0x0030
Port P4	Port P4 resistor enable	P4REN	0x0011
	Port P4 selection	P4SEL	0x001F
	Port P4 direction	P4DIR	0x001E
	Port P4 output	P4OUT	0x001D
	Port P4 input	P4IN	0x001C

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018
Port P2	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt-edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt-edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Functions	SFR interrupt flag2	IFG2	0x0003
	SFR interrupt flag1	IFG1	0x0002
	SFR interrupt enable2	IE2	0x0001
	SFR interrupt enable1	IE1	0x0000

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS}	−0.3 V to 4.1 V
Voltage applied to any pin‡	−0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal	±2 mA
Storage temperature§, T_{stg}: Unprogrammed device	−55°C to 150°C
Programmed device	−55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

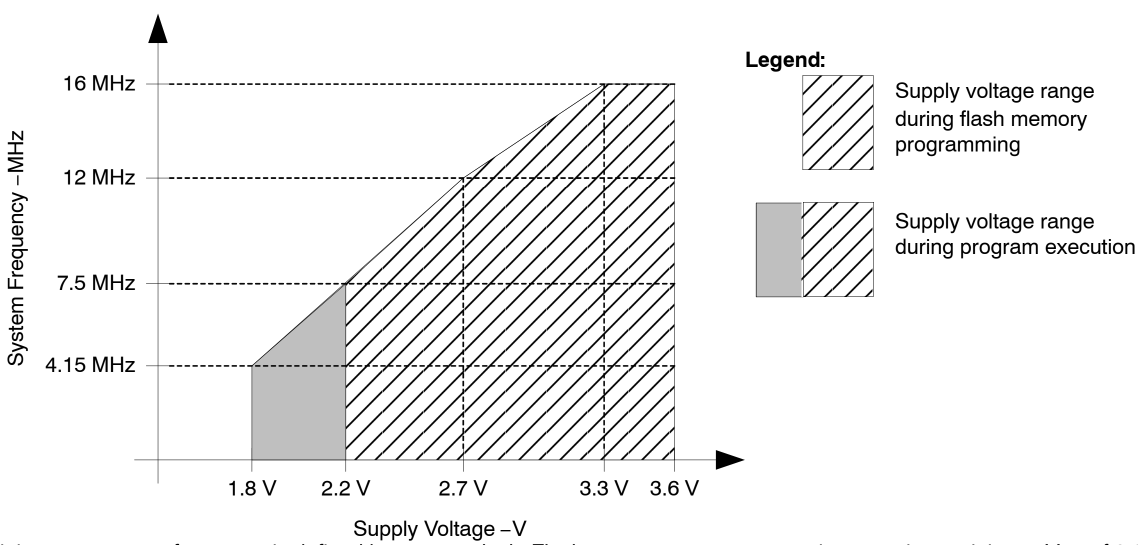
‡ All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

§ Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

recommended operating conditions

PARAMETER		MIN	MAX	UNITS
Supply voltage during program execution, V_{CC}	$AV_{CC} = DV_{CC} = V_{CC}$ (see Note 1)	1.8	3.6	V
Supply voltage during flash memory programming, V_{CC}	$AV_{CC} = DV_{CC} = V_{CC}$ (see Note 1)	2.2	3.6	V
Supply voltage, V_{SS}	$AV_{SS} = DV_{SS} = V_{SS}$	0.0	0.0	V
Operating free-air temperature range, T_A		−55	125	°C
Flash temperature range	Read	−55	125	°C
	Write	−55	125	°C
Processor frequency $f_{SYSYTEM}$ (maximum MCLK frequency) (see Notes 2 and 3 and Figure 1)	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc	4.15	MHz
	V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc	12	
	$V_{CC} \geq$ 3.3 V, Duty cycle = 50% ± 10%	dc	16	

NOTES: 1. It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power-up.
2. The MSP430 CPU is clocked directly with MCLK.
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
3. Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

active mode supply current into V_{CC} excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
$I_{AM, 1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes from flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	−55°C to 105°C	2.2 V		275		µA
			125°C			295	318	
			−55°C to 105°C	3 V		386		
			125°C			417	449	
$I_{AM, 1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1MHz, f_{ACLK} = 32,768Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	−55°C to 105°C	2.2 V		230		µA
			125°C			248	267	
			−55°C to 105°C	3 V		321		
			125°C			344	370	
$I_{AM, 4kHz}$	Active mode (AM) current (4 kHz)	$f_{MCLK} = f_{SMCLK} =$ f_{ACLK} = 32,768Hz/8 = 4,096Hz, f_{DCO} = 0Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	−55°C to 105°C	2.2 V		1.5		µA
			125°C			6	10.5	
			−55°C to 105°C	3 V		2		
			125°C			7	12.2	
$I_{AM,100kHz}$	Active mode (AM) current (100 kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \approx$ 100kHz, f_{ACLK} = 0Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	−55°C to 105°C	2.2 V		55		µA
			125°C			70	81	
			−55°C to 105°C	3 V		67		
			125°C			84	100	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

2. For < 105°C, the currents are characterized with a micro crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF. For > 105°C, the currents are characterized using a 32 kHz external clock source for ACLK..

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

typical characteristics – active mode supply current (into DV_{CC} + AV_{CC})

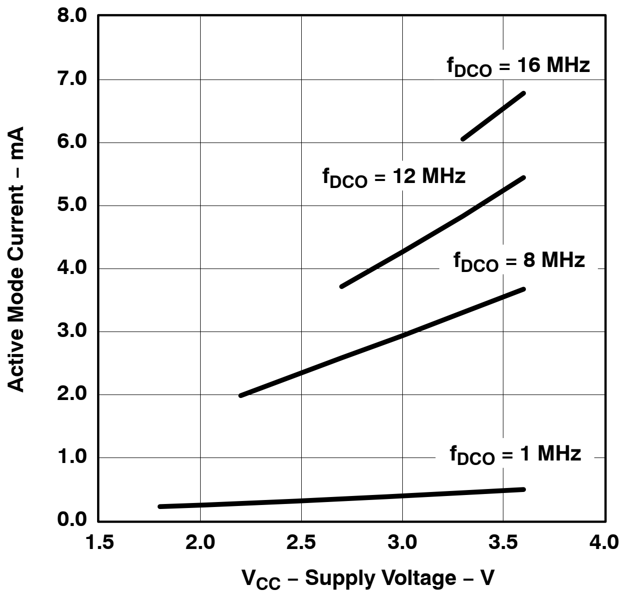


Figure 2. Active Mode Current vs V_{CC}, T_A = 25°C

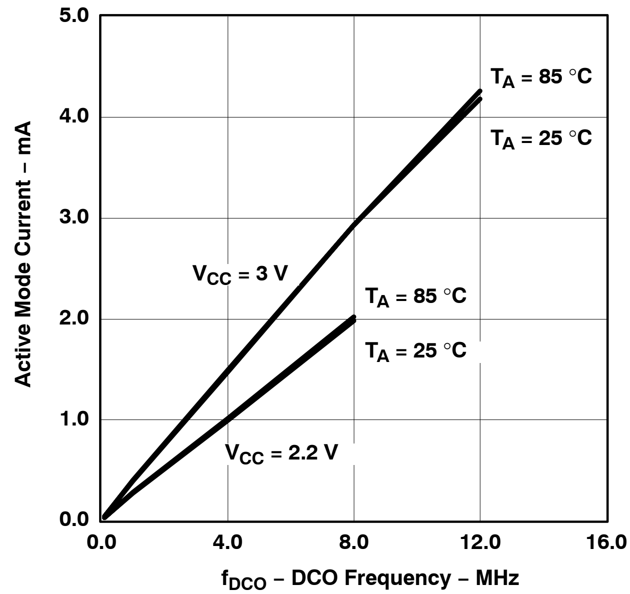


Figure 3. Active Mode Current vs DCO Frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

low-power mode supply current into V_{CC} excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
$I_{LPM0,\ 1MHz}$	Low-power mode 0 (LPM0) current (see Note 3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32,768Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	−55°C to 105°C	2.2 V		60		μA
			125°C			63	88	μA
			−55°C to 105°C	3 V		75		μA
			125°C			80	98	μA
$I_{LPM0,\ 100kHz}$	Low-power mode 0 (LPM0) current (see Note 3)	f_{MCLK} = 0MHz, f_{SMCLK} = $f_{DCO(0,\ 0)}$ ≈ 100kHz, f_{ACLK} = 0Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1	−55°C to 105°C	2.2 V		33		μA
			125°C			36	45	μA
			−55°C to 105°C	3 V		36		μA
			125°C			40	50	μA
I_{LPM2}	Low-power mode 2 (LPM2) current (see Note 4)	f_{MCLK} = f_{SMCLK} = 0MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	−55°C to 105°C	2.2 V		20		μA
			125°C			25	42	μA
			−55°C to 105°C	3 V		23		μA
			125°C				48	μA
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current (see Note 4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32,768Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	−55°C	2.2 V		0.8		μA
			25°C			0.9	1.3	
			105°C				15	
			125°C				22	
			−55°C	3 V		0.9		μA
			25°C			1	1.4	
			105°C				17	
			125°C				27	
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3) (see Note 4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	−55°C	2.2 V		0.3		μA
			25°C			0.3	0.9	
			105°C			2.5	4.5	
			125°C			8	15	
			−55°C	3 V		0.4		μA
			25°C			0.4	1	
			105°C			3.1	5.5	
			125°C			9	16	
I_{LPM4}	Low-power mode 4 (LPM4) current (see Note 5)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0MHz, f_{ACLK} = 0Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	−55°C	2.2 V and 3 V		0.1		μA
			25°C			0.1	0.5	
			105°C				13	
			125°C				22	

NOTES:
1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. For < 105°C, the currents are characterized with a micro crystal CC4V−T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF. For T_a > 105°C, ACLK was sourced from an external clock source.
3. Current for Brownout and WDT+ is included. The WDT+ is clocked by SMCLK.
4. Current for Brownout and WDT+ is included. The WDT+ is clocked by ACLK.
5. Current for Brownout included.

typical characteristics − LPM4 current

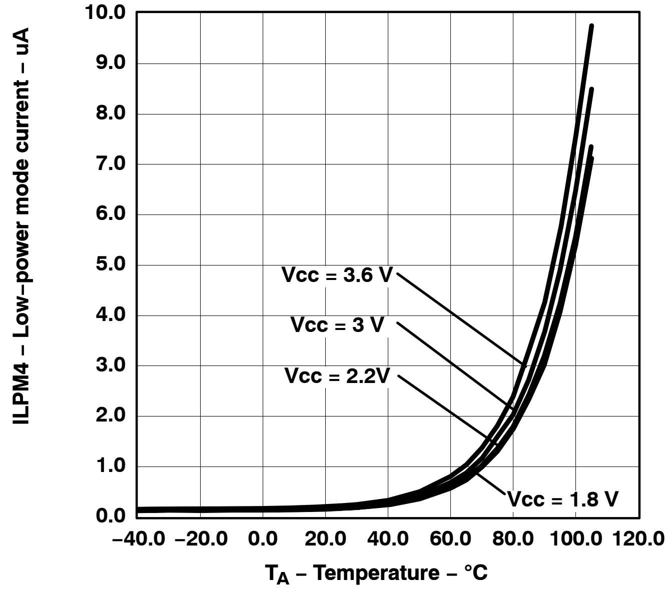


Figure 4. I_{LPM4} − LPM4 Current vs Temperature

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – ports P1, P2, P3, P4, P5, P6, RST/$\overline{NMI}$, JTAG, XIN, and XT2IN (see Note 6)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			2.2 V	1		1.65	
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			2.2 V	0.55		1.2	
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		2.2 V	0.2		1	V
			3 V	0.3		1	
R_{Pull}	Pullup/pulldown resistor	Pullup: $V_{IN} = V_{SS}$, Pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input Capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

NOTE 6: XIN and XT2IN only in bypass mode

inputs – ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	MAX	UNIT
t_{int}	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger pulse width to set the interrupt flag (see Note 1)	2.2 V/3 V	20		ns
t_{cap}	Timer_A, Timer_B capture timing	TA0, TA1, TA2	2.2 V	62		ns
		TB0, TB1, TB2, TB3, TB4, TB5, TB6	3 V	50		
f_{TAext} f_{TBext}	Timer_A, Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V		8	MHz
			3 V		10	
f_{TAint} f_{TBint}	Timer_A, Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V		8	MHz
			3 V		10	

NOTE 1: The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current – ports P1, P2, P3, P4, P5, and P6 (see Note 1 and 2)

PARAMETER		TEST CONDITIONS	VCC	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High impedance leakage current	See Notes 1 and 2	2.2 V/3 V		±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of digital port pins is measured individually. The port pin is selected for input and the pullup/pull−down resistor is disabled..

standard inputs – $\overline{RST}$/NMI

PARAMETER		TEST CONDITIONS	VCC	MIN	MAX	UNIT
V_{IL}	Low-level input voltage		2.2 V/3 V	V_{SS}	V_{SS} + 0.6	V
V_{IH}	High-level input voltage		2.2 V/3 V	0.8V_{CC}	V_{CC}	V

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs – ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS	VCC	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = −1.5 mA, (see Note 1)	2.2 V	V_{CC} − 0.25	V_{CC}	V
		$I_{OH(max)}$ = −6 mA, (see Note 2)	2.2 V	V_{CC} − 0.60	V_{CC}	
		$I_{OH(max)}$ = −1.5 mA, (see Note 1)	3 V	V_{CC} − 0.25	V_{CC}	
		$I_{OH(max)}$ = −6 mA, (see Note 2)	3 V	V_{CC} − 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA, (see Note 1)	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{OL(max)}$ = 6 mA, (see Note 2)	2.2 V	V_{SS}	V_{SS} + 0.60	
		$I_{OL(max)}$ = 1.5 mA, (see Note 1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{OL(max)}$ = 6 mA, (see Note 2)	3 V	V_{SS}	V_{SS} + 0.60	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum voltage drop specified.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum voltage drop specified.

output frequency – ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency with load	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ (see Notes 1 and 2)	2.2 V	DC		10	MHz
			3 V	DC		12	
f_{Port_CLK}	Clock output frequency	P2.0/ACLK/CA2, P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ (see Note 2)	2.2 V	DC		12	MHz
			3.3 V	DC		16	
$t_{(Xdc)}$	Duty cycle of output frequency	P1.0/TACLK/CAOUT, C_L = 20 pF, LF mode		30	50	70	%
		P1.0/TACLK/CAOUT, C_L = 20 pF, XT1 mode		40	50	60	
		P1.1/TA0, C_L = 20 pF, XT1 mode		40		60	
		P1.1/TA0, C_L = 20 pF, DCO		50% − 15 ns	50	50% + 15 ns	
		P1.4/SMCLK, C_L = 20 pF, XT2 mode		40		60	%
		P1.4/SMCLK, C_L = 20 pF, DCO		50% − 15 ns		50% + 15 ns	

NOTES: 1. A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
2. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − outputs

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE of one pin

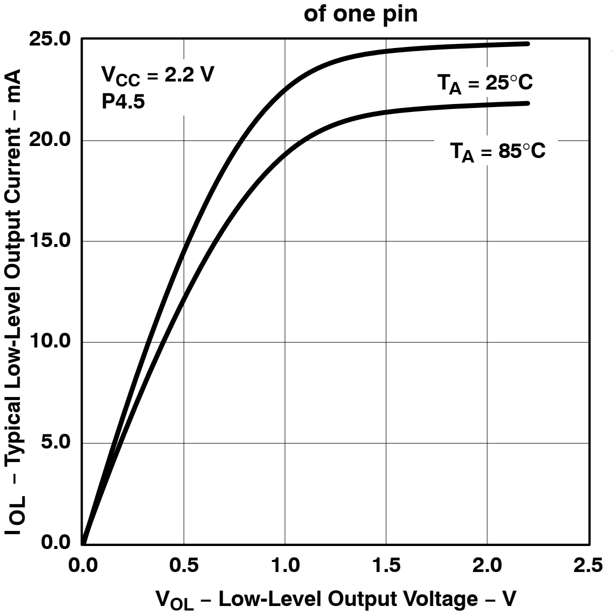


Figure 5

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE of one pin

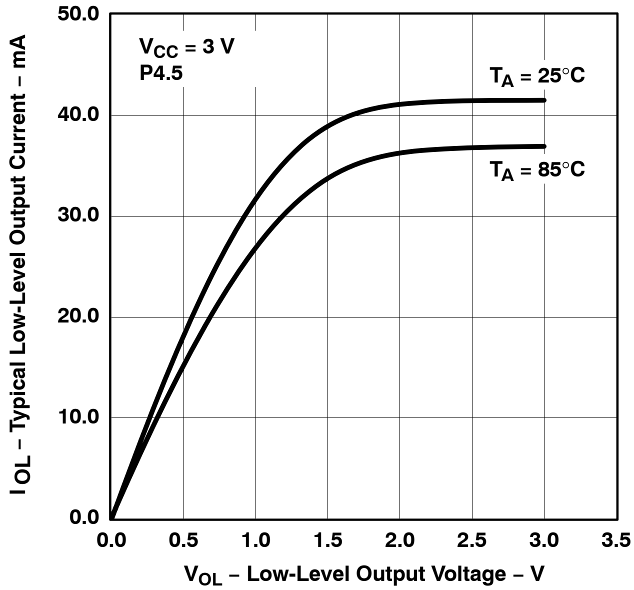


Figure 6

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE of one pin

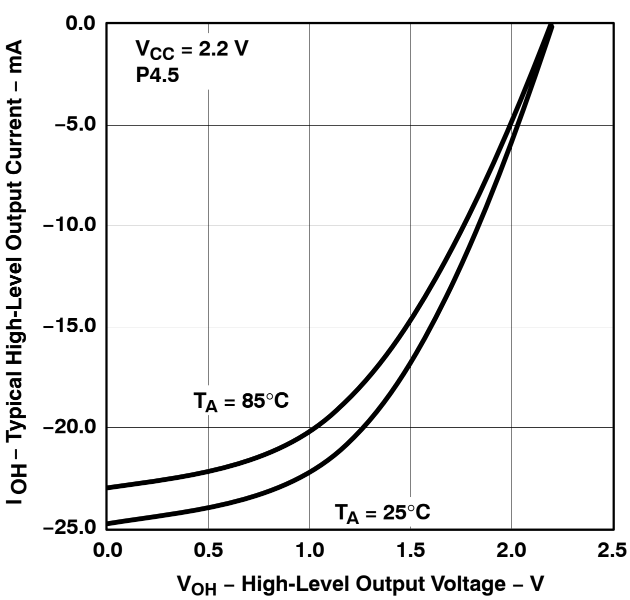


Figure 7

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE of one pin

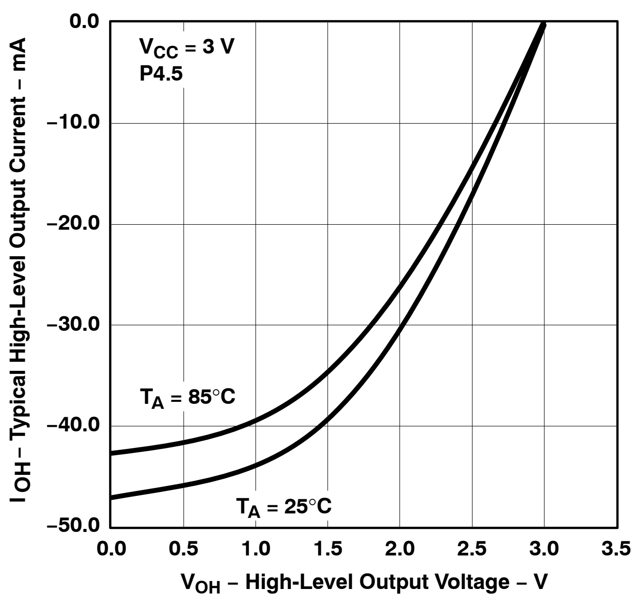


Figure 8

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	Operating voltage	$dV_{CC}/dt \leq 3$ V/s				$0.7 \times V_{(B\_IT-)}$	V
$V_{(B\_IT-)}$	Negative going V_{CC} reset threshold voltage	$dV_{CC}/dt \leq 3$ V/s				1.71	V
$V_{hys(B\_IT-)}$	V_{CC} reset threshold hysteresis	$dV_{CC}/dt \leq 3$ V/s		70	130	210	mV
$t_{d(BOR)}$	BOR reset release delay time					2000	µs
t_{reset}	Pulse length at $\overline{RST}$/NMI pin to accept a reset		2.2 V / 3 V	2			µs

NOTES: 3. The current consumption of the brownout module is included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

4. During power-up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \geq V_{CC(MIN)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

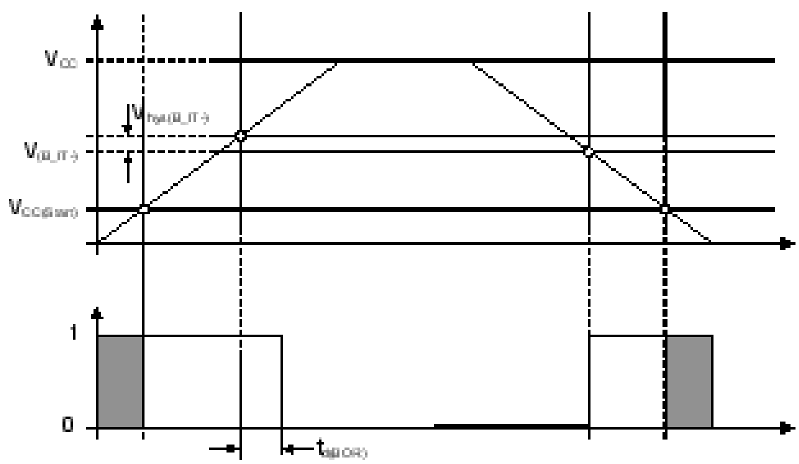


Figure 9. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – POR/brownout reset (BOR)

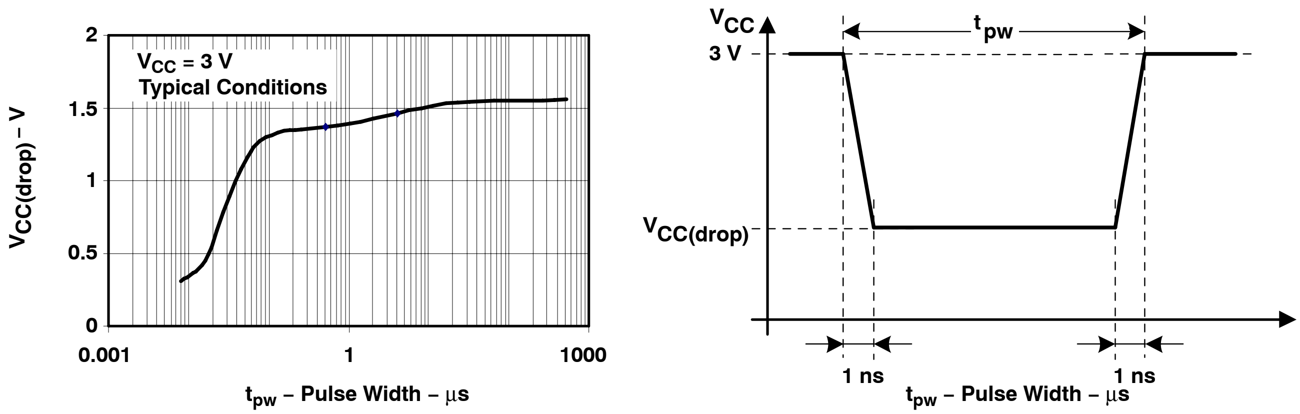


Figure 10. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

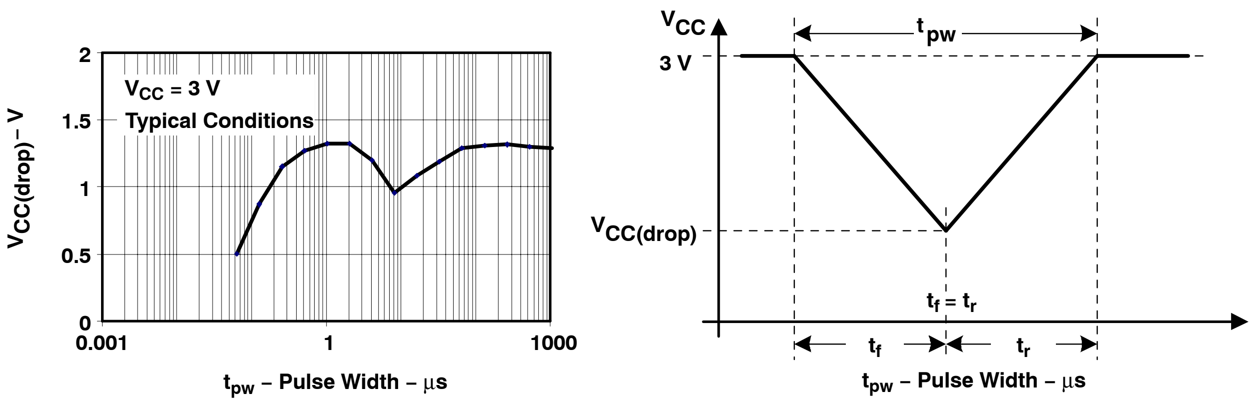


Figure 11. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

SVS (supply voltage supervisor/monitor)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt > 30$ V/ms (see Figure 12)		5		150	µs
	$dV_{CC}/dt \leq 30$ V/ms				2000	
$t_{d(SVSon)}$	SVSON, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V		20		150	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \leq 3$ V/s (see Figure 12)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 12)	VLD = 1	70	120	210	mV
		VLD = 2 to 14	0.001 x $V_{(SVS\_IT-)}$		0.016 x $V_{(SVS\_IT-)}$	
	$V_{CC}/dt \leq 3$ V/s (see Figure 12), External voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 12 and Figure 13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	$V_{CC}/dt \leq 3$ V/s (see Figure 12 and Figure 13), External voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$§	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.
‡ t_{settle} is the settling time that the comparator output must have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be >50 mV.
§ The current consumption of the SVS module is not included in the I_{CC} current consumption data.

typical characteristics

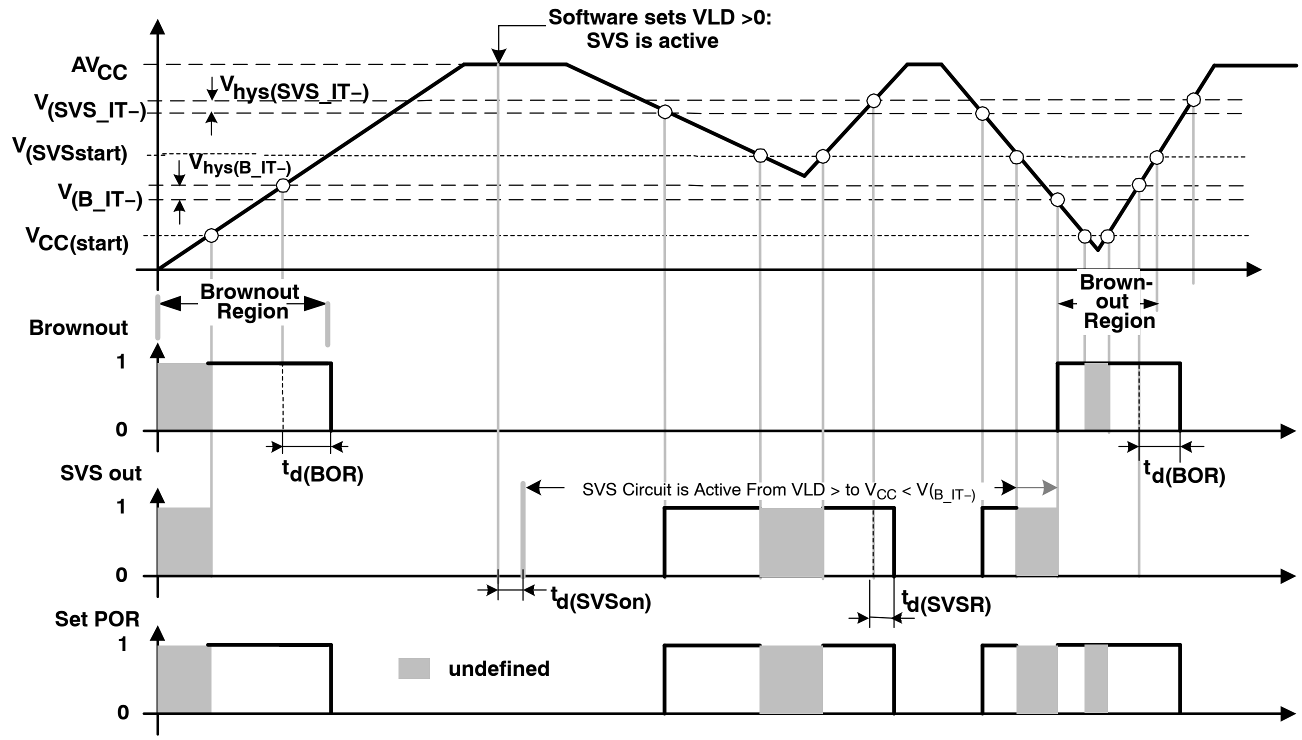
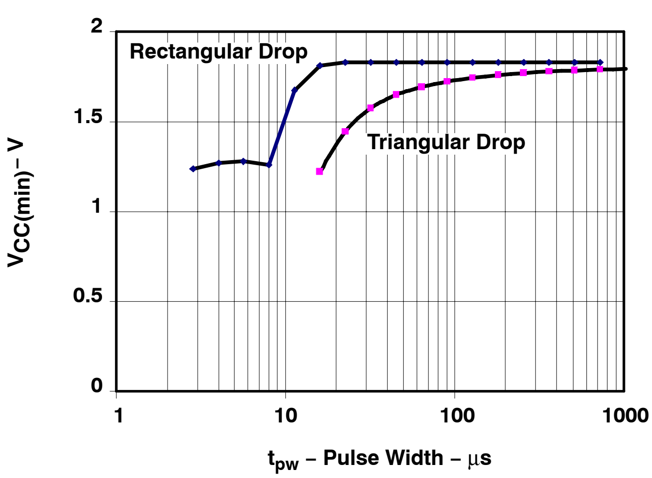


Figure 12. SVS Reset (SVSR) vs Supply Voltage



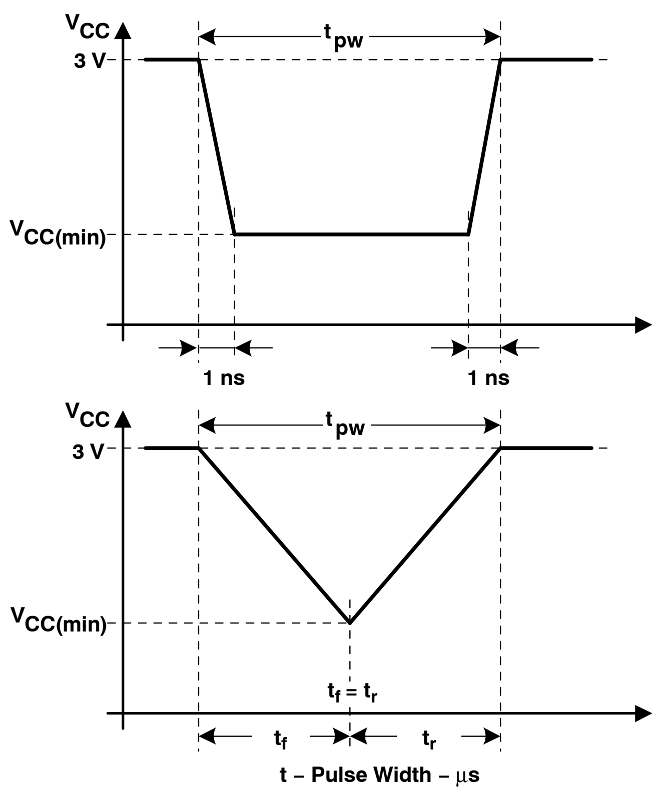


Figure 13. $V_{CC(min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal (VLD = 1)

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO frequency

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
Vcc	Supply voltage range	RSELx < 14		1.8		3.60	V
		RSELx = 14		2.2		3.60	
		RSELx = 15		3		3.60	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60		3	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60		13.90	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12		18.50	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16		26	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.35	1.55	2	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.07	1.08	1.16	ratio
Duty cycle		Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies – tolerance at calibration

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration			25°C	3 V	−1	±0.2	+1	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

calibrated DCO frequencies – tolerance over temperature –55°C to 125°C

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature			−55°C to 125°C	3 V	−2.5	±0.5	+2.5	%
8-MHz tolerance over temperature			−55°C to 125°C	3 V	−2.5	±1.0	+2.5	%
12-MHz tolerance over temperature			−55°C to 125°C	3 V	−2.5	±1.0	+2.5	%
16-MHz tolerance over temperature			−55°C to 125°C	3 V	−3.0	±2.0	+3.0	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms	−55°C to 125°C	2.2 V	0.970	1	1.030	MHz
				3 V	0.975	1	1.025	
				3.6 V	0.970	1	1.030	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	−55°C to 125°C	2.2 V	7.760	8	8.400	MHz
				3 V	7.800	8	8.200	
				3.6 V	7.600	8	8.240	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	−55°C to 125°C	2.2 V	11.64	12	12.36	MHz
				3 V	11.64	12	12.36	
				3.6 V	11.64	12	12.36	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	−55°C to 125°C	3 V	15.52	16	16.48	MHz
				3.6 V	15.00	16	16.48	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies – tolerance over supply voltage V_{CC}

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
1-MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	−3	±2	+3	%
8-MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	−3	±2	+3	%
12-MHz tolerance over V_{CC}			25°C	2.2 V to 3.6 V	−3	±2	+3	%
16-MHz tolerance over V_{CC}			25°C	3 V to 3.6 V	−6	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.970	1	1.030	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.760	8	8.240	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	25°C	3 V to 3.6 V	15.00	16	16.48	MHz

calibrated DCO frequencies – overall tolerance

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
1-MHz tolerance overall			−55°C to 125°C	1.8 V to 3.6 V	−5	±2	5	%
8-MHz tolerance overall			−55°C to 125°C	1.8 V to 3.6 V	−5	±2	5	%
12-MHz tolerance overall			−55°C to 125°C	2.2 V to 3.6 V	−5	±2	5	%
16-MHz tolerance overall			−55°C to 125°C	3 V to 3.6 V	−6	±3	6	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms	−55°C to 125°C	1.8 V to 3.6 V	0.950	1	1.05	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1= CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	−55°C to 125°C	1.8 V to 3.6 V	7.6	8	8.4	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1= CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	−55°C to 125°C	2.2 V to 3.6 V	11.40	12	12.6	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1= CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	−55°C to 125°C	3 V to 3.6 V	15	16	17	MHz

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − calibrated 1-MHz DCO frequency

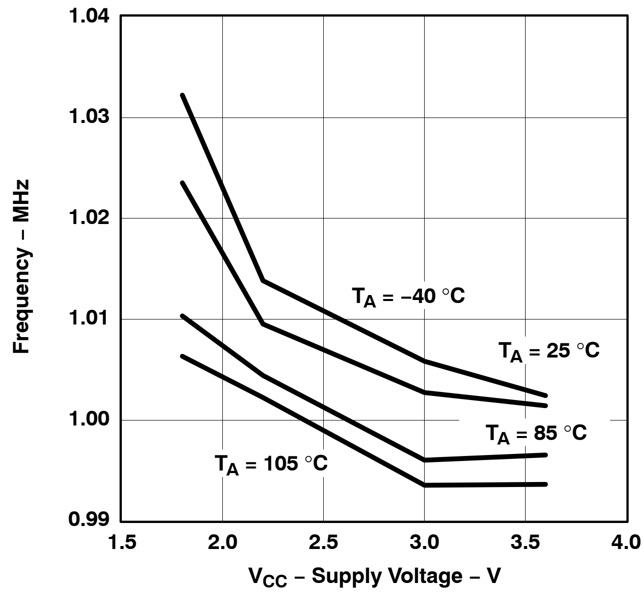


Figure 14. Calibrated 1 MHz Frequency vs. V_{CC}

typical characteristics − calibrated 8-MHz DCO frequency

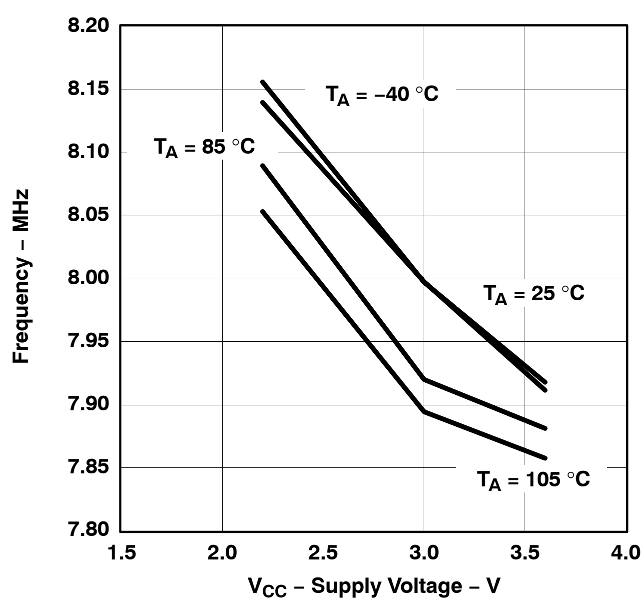


Figure 15. Calibrated 8 MHz Frequency vs. V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − calibrated 12-MHz DCO frequency

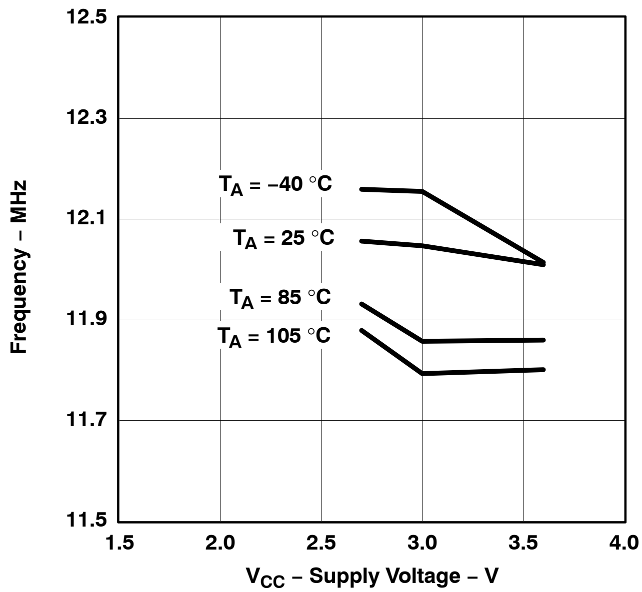


Figure 16. Calibrated 12-MHz Frequency vs V_{CC}

typical characteristics − calibrated 16-MHz DCO frequency

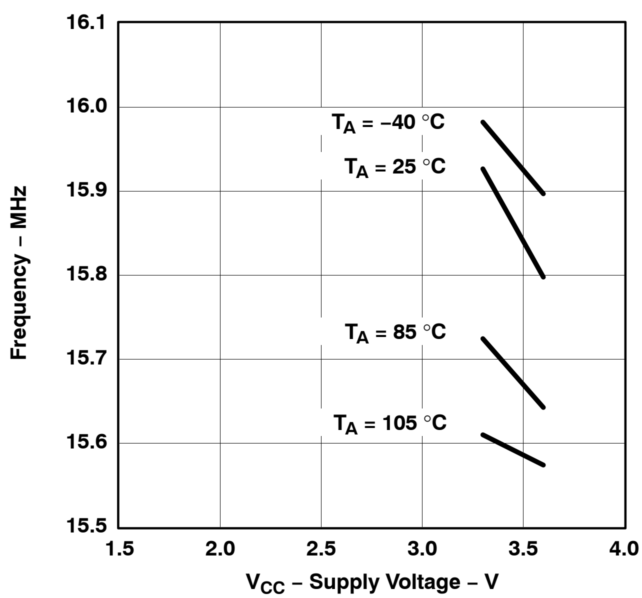


Figure 17. Calibrated 16-MHz Frequency vs V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

wake-up from lower power modes (LPM3/4)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake−up time from LPM3/4 (see Note 1)	BCSCTL1= CALBC1_1MHz, DCOCTL = CALDCO_1MHz	2.2 V/3 V			2	μs
		BCSCTL1= CALBC1_8MHz, DCOCTL = CALDCO_8MHz	2.2 V/3 V			1.5	
		BCSCTL1= CALBC1_12MHz, DCOCTL = CALDCO_12MHz	2.2 V/3 V			1	
		BCSCTL1= CALBC1_16MHz, DCOCTL = CALDCO_16MHz	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake−up time from LPM3/4 (see Note 2)					$1/f_{MCLK} + t_{Clock,LPM3/4}$	

NOTES: 1. The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
2. Parameter applicable only if DCOCLK is used for MCLK.

typical characteristics − DCO clock wake-up time from LPM3/4

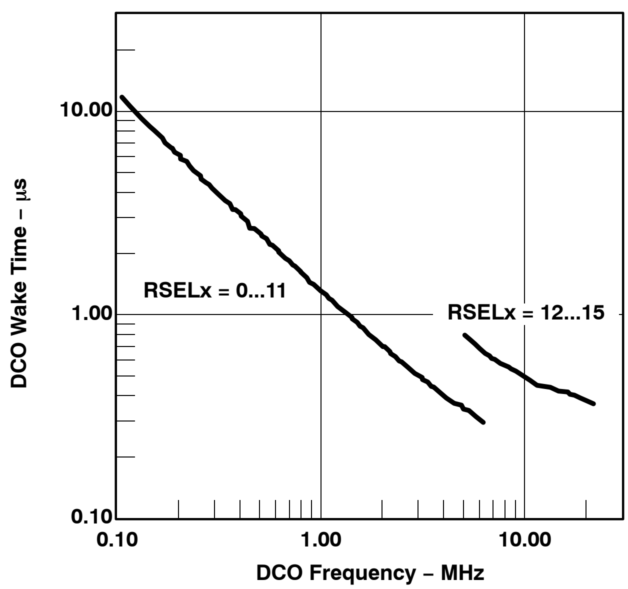


Figure 18. Clock Wake-Up Time From LPM3 vs DCO Frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO with external resistor R_{OSC} (see Note 1)

PARAMETER		TEST CONDITIONS	VCC	TYP	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V	1.8	MHz
			3 V	1.95	
D_t	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	±0.1	%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	10	%/V

NOTE 1: R_{OSC} = 100 kΩ, metal film resistor, type 0257. 0.6 W with 1% tolerance, and T_K = ±50 ppm/°C.

typical characteristics – DCO with external resistor R_{OSC}

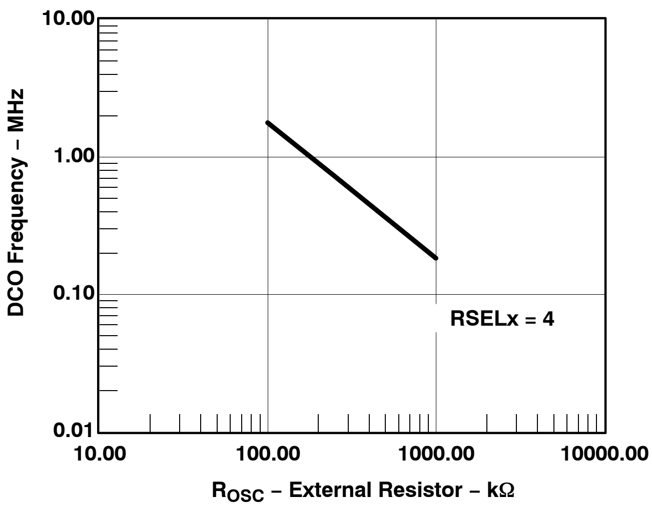


Figure 19. DCO Frequency vs R_{OSC}, V_{CC} = 2.2 V, T_A = 25°C

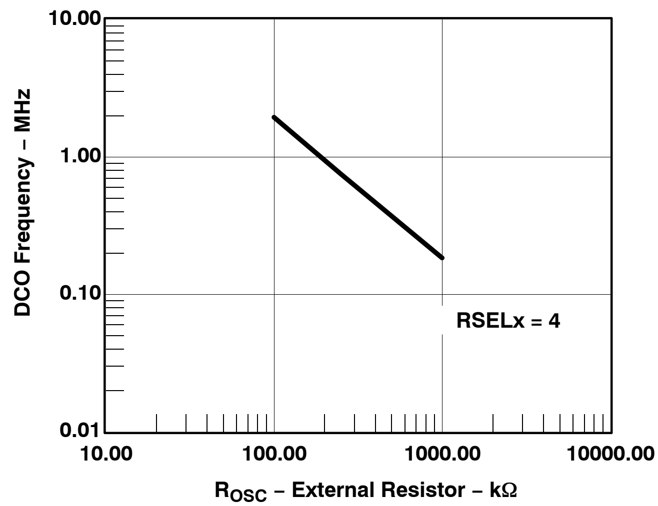


Figure 20. DCO Frequency vs R_{OSC}, V_{CC} = 3 V, T_A = 25°C

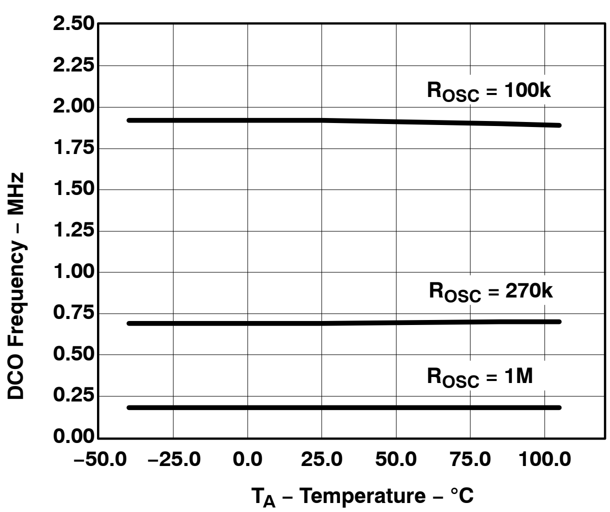


Figure 21. DCO Frequency vs Temperature, V_{CC} = 3 V

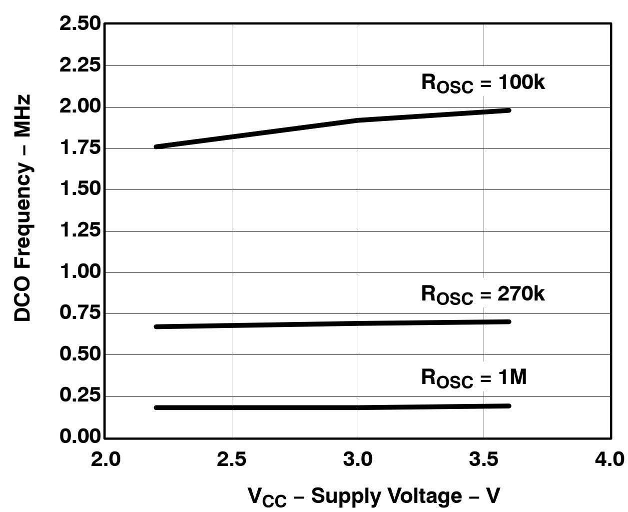


Figure 22. DCO Frequency vs V_{CC}, T_A = 25°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, low frequency modes (see Note 4 and 5)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32,768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	10,000	32,768	50,000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF			200		kΩ
$C_{L,eff}$	Integrated effective load capacitance, LF mode (see Note 1)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		pF
		XTS = 0, XCAPx = 2			8.5		pF
		XTS = 0, XCAPx = 3			11		pF
Duty cycle	LF mode	XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (see Note 3)	XTS = 0, LFXT1Sx = 3, XCAPx = 0 (see Notes 2)	2.2 V/3 V	10		10,000	Hz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
5. For T_a > 105°C: Applies only if using an external logic-level clock source. Not applicable when using a crystal or resonator.

internal very low power, low frequency oscillator (VLO)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency		2.2 V/3 V	4	12	22	kHz
df_{VLO}/dT	VLO frequency temperature drift	See Note 6	2.2 V/3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	See Note 7	1.8 V to 3.6 V		4		%/V

NOTES: 6. Calculated using the box method:
I version: (MAX(−40 to 85°C) − MIN(−40 to 85°C))/MIN(−40 to 85°C)/(85°C − (−40°C))
T version: (MAX(−40 to 105_C) − MIN(−40 to 105_C))/MIN(−40 to 105_C)/(105_C − (−40_C))
7. Calculated using the box method: (MAX(1.8 to 3.6 V) − MIN(1.8 to 3.6 V))/MIN(1.8 to 3.6 V)/(3.6 V − 1.8 V)

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, high frequency modes (see Note 5 and 6)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0, XCAPx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1, XCAPx = 0	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2, XCAPx = 0	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic level square wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation Allowance for HF crystals (refer to Figure 23 and Figure 24)	XTS = 1, XCAPx = 0, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 1, XCAPx = 0, LFXT1Sx = 1 $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 1, XCAPx = 0, LFXT1Sx = 2 $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode	XTS = 1, XCAPx = 0 (see Note 2)			1		pF
Duty cycle	HF mode	XTS = 1, XCAPx = 0, Measured at P1.4/SMCLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/3 V	40	50	60	%
		XTS = 1, XCAPx = 0, Measured at P1.4/SMCLK, $f_{LFXT1,HF}$ = 16 MHz		40	50	60	
$f_{Fault,HF}$	Oscillator fault frequency, HF mode (see Note 4)	XTS = 1, LFXT1Sx = 3, XCAPx = 0 (see Notes 3)	2.2 V/3 V	30		300	kHz

NOTES:
1. Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
3. Measured with logic level input frequency but also applies to operation with crystals.
4. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
5. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
6. For T_a > 105°C: Applies only if an external logic−lvel clock source is used. Not applicable when using a crystal or a resonator.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − LFXT1 oscillator in HF mode (XTS = 1)

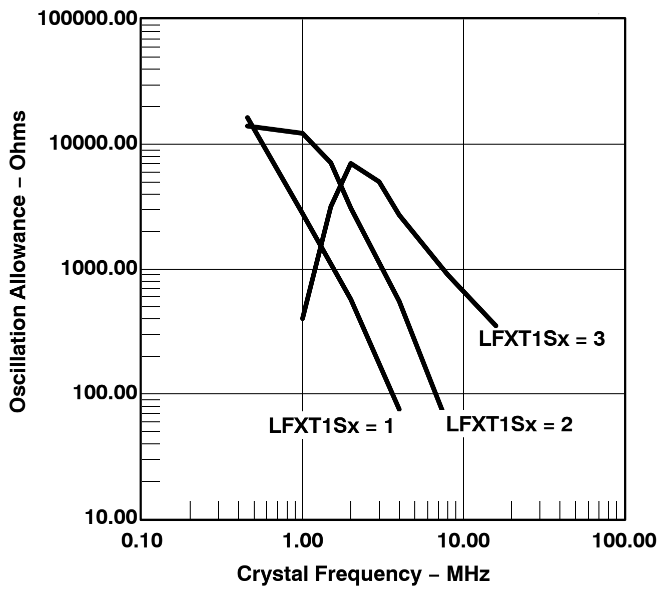


Figure 23. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

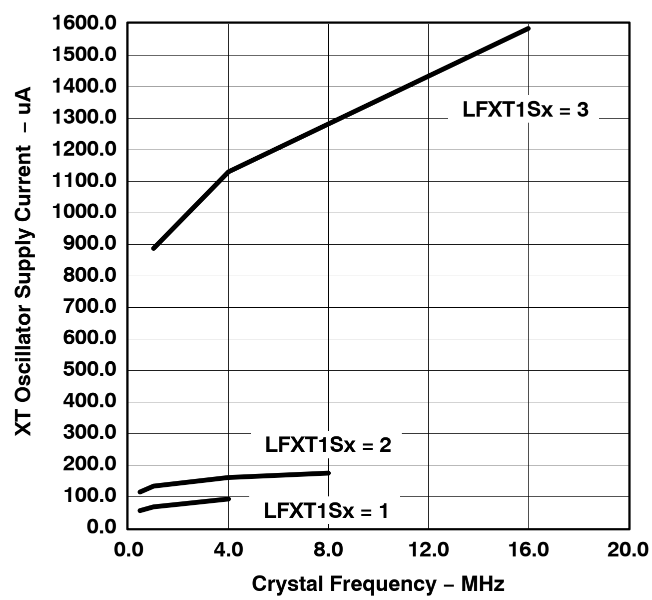


Figure 24. XT Oscillator Supply Current vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, XT2 (see Note 5)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{XT2}	XT2 oscillator crystal frequency, mode 0	XT2Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
f_{XT2}	XT2 oscillator crystal frequency, mode 1	XT2Sx = 1	1.8 V to 3.6 V	1		4	MHz
f_{XT2}	XT2 oscillator crystal frequency, mode 2	XT2Sx = 2	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
f_{XT2}	XT2 oscillator logic level square wave input frequency	XT2Sx = 3	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA	Oscillation allowance (see Figure 23 and Figure 24)	XT2Sx = 0, f_{XT2} = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XT2Sx = 1, f_{XT2} = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XT2Sx = 2, $f_{XT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode (see Note 1)	See Note 2			1		pF
Duty cycle		Measured at P1.4/SMCLK, f_{XT2} = 10 MHz	2.2 V/3 V	40	50	60	%
		Measured at P1.4/SMCLK, f_{XT2} = 16 MHz		40	50	60	
f_{Fault}	Oscillator fault frequency, HF mode (see Note 4)	XT2Sx = 3 (see Note 3)	2.2 V/3 V	30		300	kHz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
3. Measured with logic level input frequency but also applies to operation with crystals.
4. Frequencies below the MIN specification will set the fault flag, frequencies above the MAX specification will not set the fault flag. Frequencies in between might set the flag.
5. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − XT2 oscillator

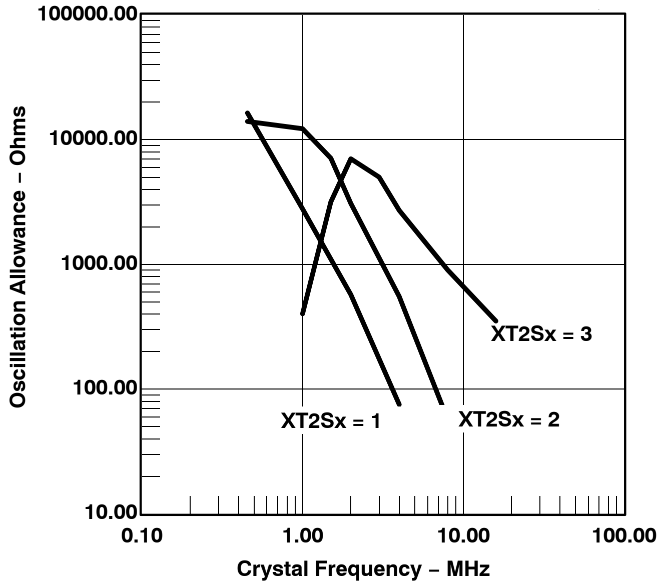


Figure 25. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

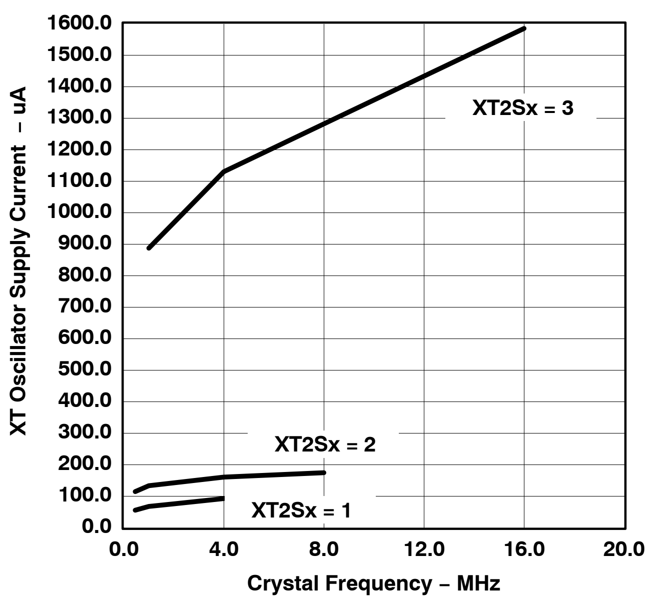


Figure 26. XT2 Oscillator Supply Current vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Timer_A

PARAMETER		TEST CONDITIONS	VCC	MIN	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ± 10%	2.2 V		7.5	MHz
			3.3 V		16	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1, TA2	2.2 V/3 V	20		ns

Timer_B

PARAMETER		TEST CONDITIONS	VCC	MIN	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ± 10%	2.2 V		7.5	MHz
			3.3 V		16	
$t_{TB,cap}$	Timer_B, capture timing	TBx	2.2 V/3 V	20		ns

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (UART mode)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals Baudrate in MBaud)		2.2 V/3 V			1	MHz
t_τ	UART receive deglitch time (see Note 1)		2.2 V	50	150	600	ns
			3 V	50	100	600	

NOTE 1: Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

USCI (SPI master mode) (see Figure 27 and Figure 28)

PARAMETER		TEST CONDITIONS	VCC	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110		ns
			3 V	75		
$t_{HD,MI}$	SOMI input data hold time		2.2 V			ns
			3 V			
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid; C_L = 20 pF	2.2 V		30	ns
			3 V		20	

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

USCI (SPI slave mode) (see Figure 29 and Figure 30)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time STE low to clock		2.2 V/3 V		50		ns
$t_{STE,LAG}$	STE lag time Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time STE low to SOMI data out		2.2 V/3 V		50		ns
$t_{STE,DIS}$	STE disable time STE high to SOMI high impedance		2.2 V/3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid; C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached master.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

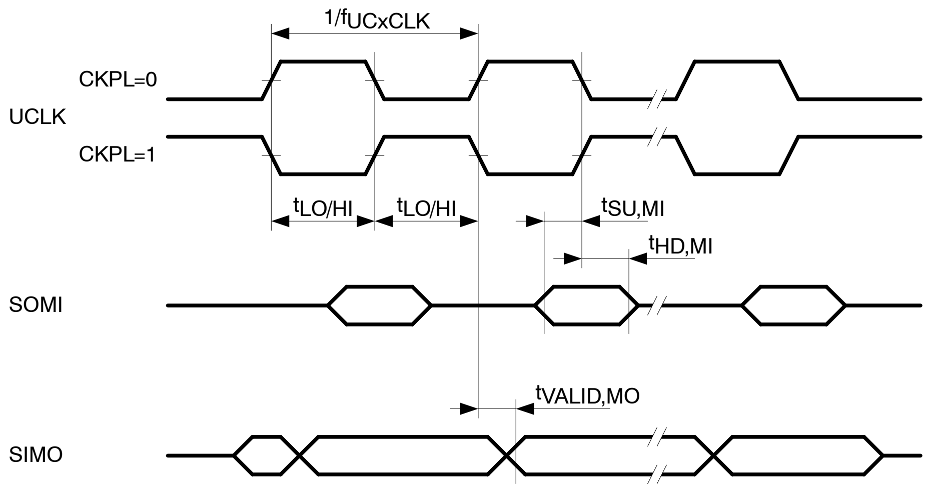


Figure 27. SPI Master Mode, CKPH = 0

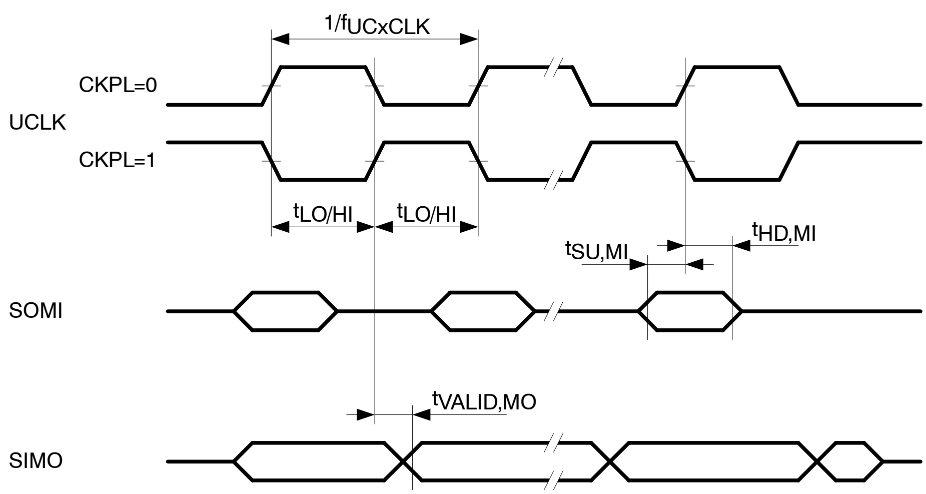


Figure 28. SPI Master Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

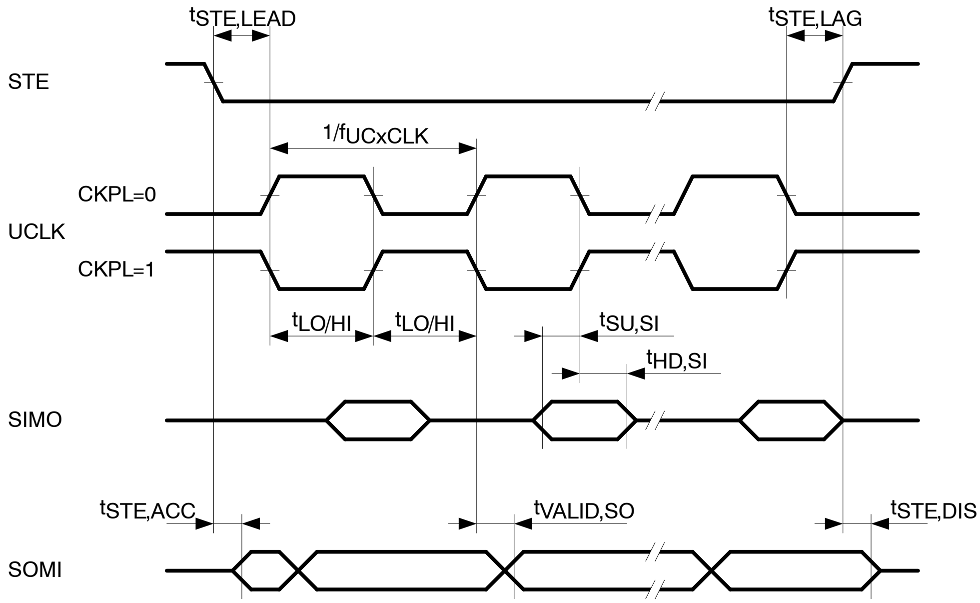


Figure 29. SPI Slave Mode, CKPH = 0

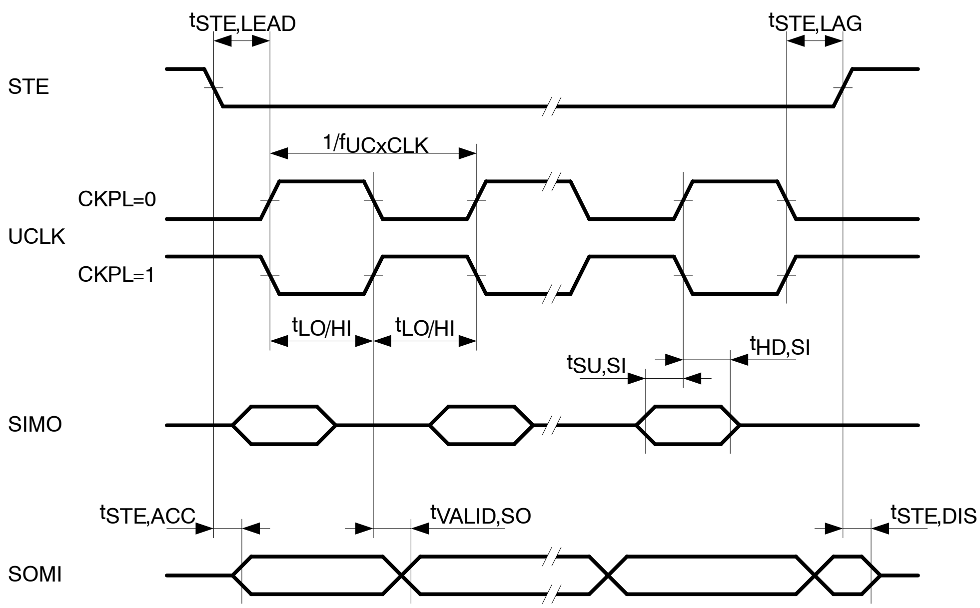


Figure 30. SPI Slave Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (I^{2}C mode) (see Figure 31)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \leq 100kHz$	2.2 V/3 V	4.0			µs
		$f_{SCL} > 100kHz$		0.6			
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \leq 100kHz$	2.2 V/3 V	4.7			µs
		$f_{SCL} > 100kHz$		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V/3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V/3 V	4.0			µs
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

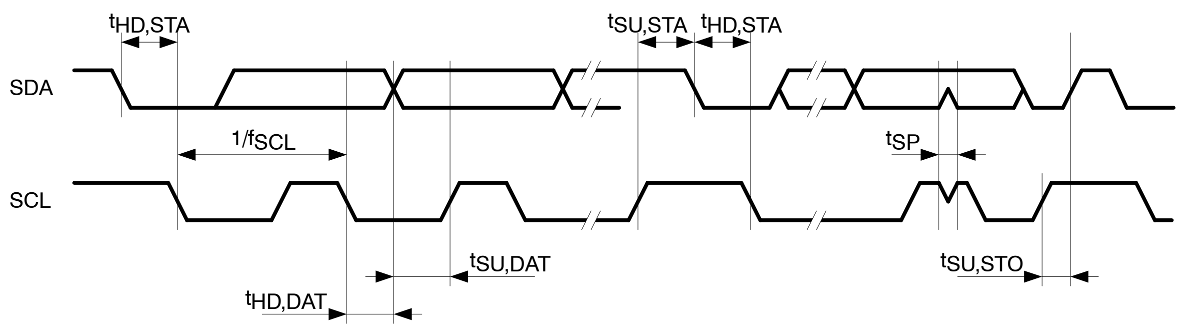


Figure 31. I^{2}C Mode Timing

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Comparator_A+ (see Note 1)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	μA
			3 V		45	60	
$I_{(Refladder/Refdiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	μA
			3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON = 1	2.2 V/3 V	0		$V_{CC}-1$	V
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5} V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	.47	0.48	0.5	
$V_{(RefVT)}$	(see Figure 35 and Figure 36)	PCA0 = 1, CARSEL = 1, CAREF = 3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	2.2 V/3 V	−30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V/3 V	0	0.7	1.4	mV
$t_{(response)}$	Low to high and high to low (see Note 3)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	2.2 V	80	165	300	ns
			3 V	70	120	270	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF = 1	2.2 V	1.4	1.9	2.8	μs
			3 V	0.9	1.5	2.2	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.
3. The response time is measured at P2.2/CAOUT/TA0/CA4 with an input voltage step, with Comparator_A+ already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

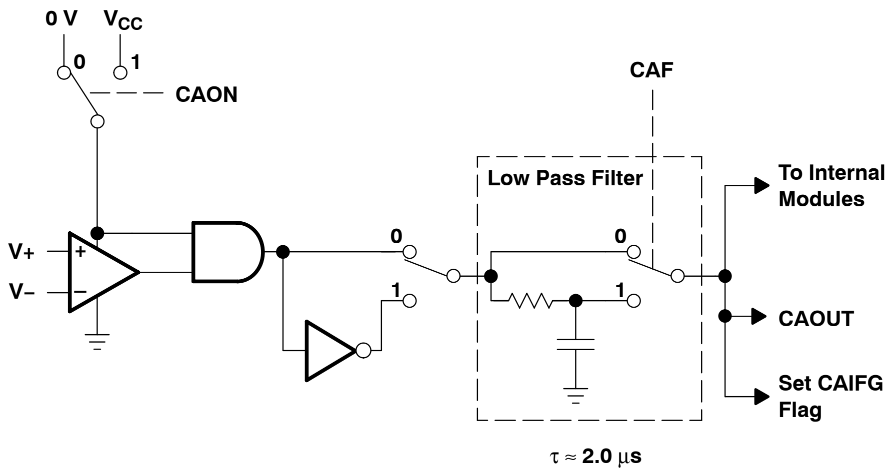


Figure 32. Block Diagram of Comparator_A Module

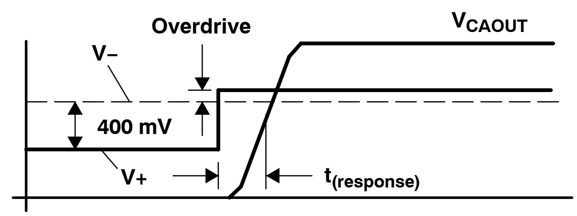


Figure 33. Overdrive Definition

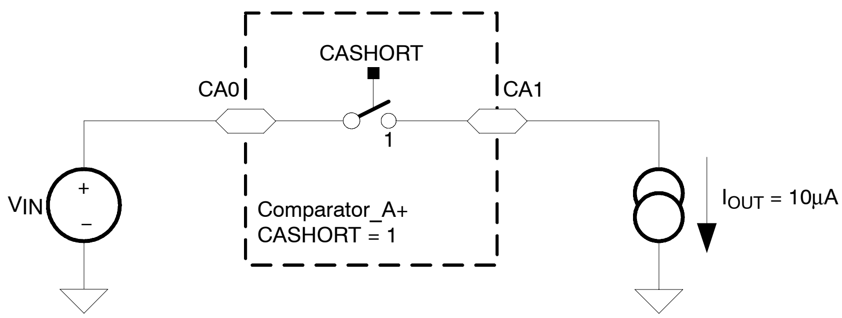


Figure 34. Comparator_A+ Short Resistance Test Condition

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

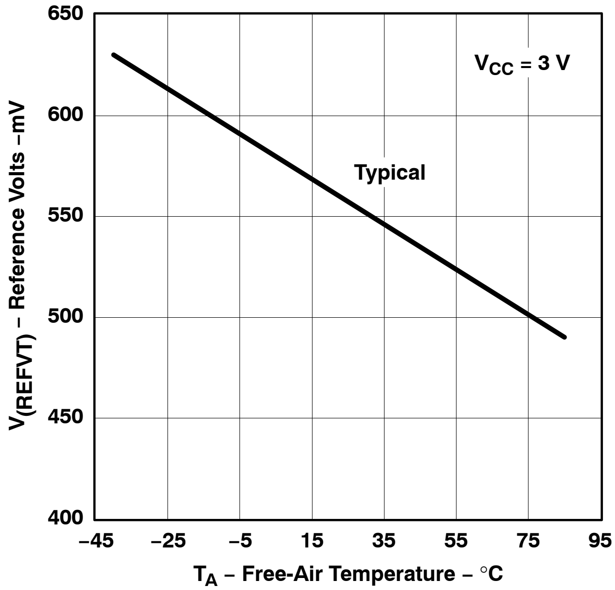


Figure 35. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

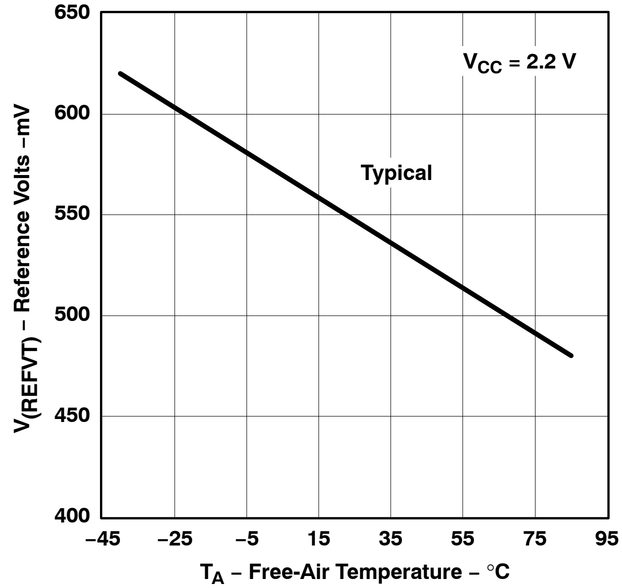


Figure 36. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

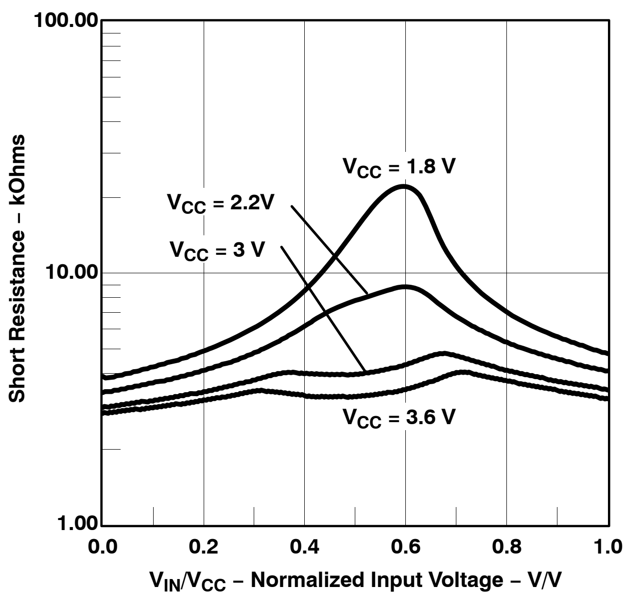


Figure 37. Short Resistance vs V_{IN}/V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range (see Note 2)	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register, P6Sel.x = 1, $0 \le x \le 7$, $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal (see Note 3)	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V		0.65	0.8	mA
			3 V		0.8	1	
I_{REF+}	Operating supply current into AV_{CC} terminal (see Note 4)	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		0.5	0.7	mA
		$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V		0.5	0.7	mA
			3 V		0.5	0.7	
C_I †	Input capacitance	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
R_I†	Input MUX ON resistance	$0V \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω

† Not production tested, limits verified by design

NOTES: 1. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC12}.
4. The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC, external reference (see Note 1)

PARAMETER		TEST CONDITIONS	VCC	MIN	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2)		1.4	V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3)		0	1.2	V
(V_{eREF+} − V_{REF-}/V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4)		1.4	V_{AVCC}	V
I_{VeREF+}	Static input current	$0V \le V_{eREF+} \le V_{AVCC}$	2.2 V/3 V		±1	µA
$I_{VREF-/VeREF-}$	Static input current	$0V \le V_{eREF-} \le V_{AVCC}$	2.2 V/3 V		±1	µA

NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, built-in reference

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 (2.5 V), $I_{VREF+}max \leq I_{VREF+} \leq I_{VREF+}min$	−55°C to 105°C	3 V	2.4	2.5	2.6	V
			125°C	3 V	2.37	2.5	2.64	
		REF2_5V = 0 (1.5 V), $I_{VREF+}max \leq I_{VREF+} \leq I_{VREF+}min$	−55°C to 105°C	2.2 V/3 V	1.44	1.5	1.56	
			125°C	2.2V / 3 V	1.42	1.5	1.57	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built-in reference active	REF2_5V = 0, $I_{VREF+}max \leq I_{VREF+} \leq I_{VREF+}min$			2.2			V
		REF2_5V = 1, $-0.5mA \leq I_{VREF+} \leq I_{VREF+}min$			2.8			
		REF2_5V = 1, $-1mA \leq I_{VREF+} \leq I_{VREF+}min$			2.9			
I_{VREF+}	Load current out of V_{REF+} terminal			2.2 V	0.01		−0.5	mA
				3 V	0.01		−1	
$I_{L(VREF)+}$ †	Load-current regulation V_{REF+} terminal	I_{VREF+} = 500 µA ± 100 µA Analog input voltage ~0.75 V; REF2_5V = 0		2.2 V			±2	LSB
				3 V			±2	
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage ~1.25 V, REF2_5V = 1		3 V			±2	
$I_{DL(VREF)+}$ ‡	Load current regulation V_{REF+} terminal	I_{VREF+} =100 µA → 900 µA, C_{VREF+}=5 µF, ax ~0.5 × V_{REF+} Error of conversion result ≤ 1 LSB		3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (see Note 1)	REFON =1, 0 mA ≤ I_{VREF+} ≤ $I_{VREF+}max$		2.2 V/3 V	5	10		µF
T_{REF+} †	Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA		2.2 V/3 V			±100	ppm/°C
t_{REFON} †	Settle time of internal reference voltage (see Figure 38 and Note 2)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V					17	ms

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10-µF tantalum and 100-nF ceramic.
2. The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

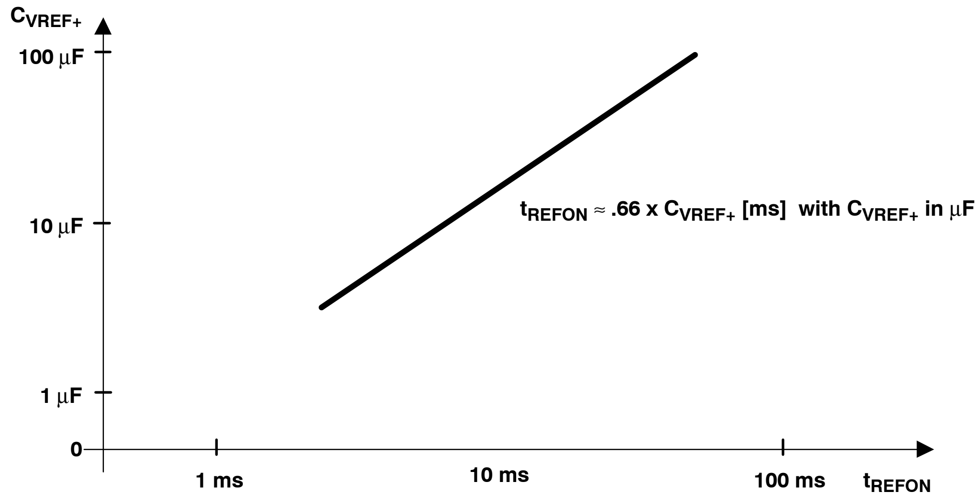


Figure 38. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on $V_{REF}+$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

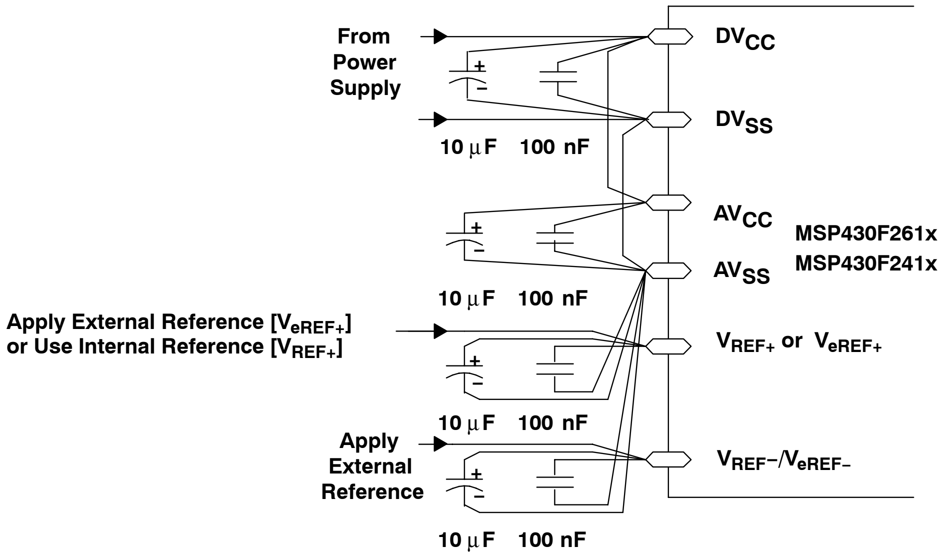


Figure 39. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

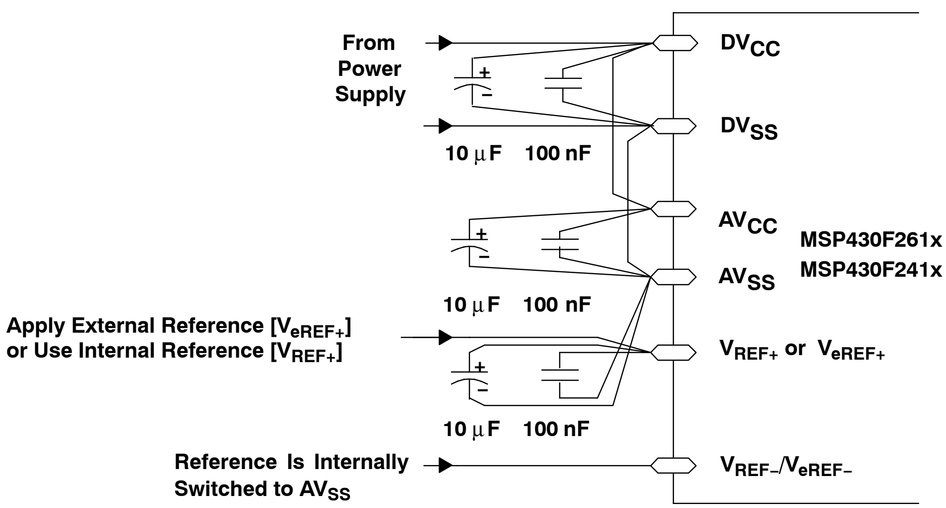


Figure 40. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} = AV_{SS}, Internally Connected

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	2.2V/3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV=0, $f_{ADC12CLK}$=$f_{ADC12OSC}$	2.2 V/ 3 V	3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	C_{VREF+} ≥ 5 μF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V/ 3 V	2.06		3.51	μs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK: ADC12SSEL ≠ 0		13 × ADC12DIV × 1 /$f_{ADC12CLK}$			
$t_{ADC12ON}$†	Turn-on settling time of the ADC	See Note 1				100	ns
t_{Sample}†	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF $\tau = [R_S + R_I] \times C_I$;(see Note 2)	3 V	1220			ns
			2.2 V	1400			

† Limits verified by design

NOTES: 1. The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns where n = ADC resolution = 12, R_S = external source resistance.

12-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ 1.6 V	2.2 V/3 V			±1.7	LSB
		1.6 V < (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ [V_{AVCC}]				±1.7	
E_D	Differential linearity error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V			±1	LSB
E_O	Offset error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), Internal impedance of source R_S < 100 Ω, C_{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±4	LSB
E_G	Gain error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±5	LSB

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in V_{MID}

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (see Note 1)	REFON = 0, INCH = 0Ah, ADC12ON = 1, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}†	See Note 2	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986		mV
			3 V		986		
TC_{SENSOR}†		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55 ± 3%	mV/°C
			3 V		3.55	3.55 ± 3%	
$t_{SENSOR(sample)}$†	Sample time required if channel 10 is selected (see Note 3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11 (see Note 4)	ADC12ON = 1, INCH = 0Bh,	2.2 V			NA	µA
			3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 × V_{AVCC}	2.2 V		1.1	1.1 ± 0.04	V
			3 V		1.5	1.5 ± 0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

† Limits characterized

NOTES:
1. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON=1) or (ADC12ON=1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
2. The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
3. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
4. No additional current is needed. The V_{MID} is used during sampling.
5. The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.7 V/ 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	See Note 1	2.7 V/ 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time	See Note 2	2.7 V/ 3.6 V	200			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time (see Note 4)				10593		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297×1/f_{FTG},max = 5297×1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).
4. To erase the complete code area the mass erase has to be performed once with a dummy address in the range of the lower 64kB Flash addresses and once with the dummy address in the upper 64kB Flash addresses.
5. Additional Flash retention documentation located in application report (SLAA392)

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

RAM

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
VRAMh	See Note 1	CPU halted	1.6		V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

JTAG interface

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	See Note 1	2.2 V	0		5	MHz
			3 V	0		10	
$R_{Internal}$	Internal pullup resistance on TMS, TCK, TDI/TCLK	See Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

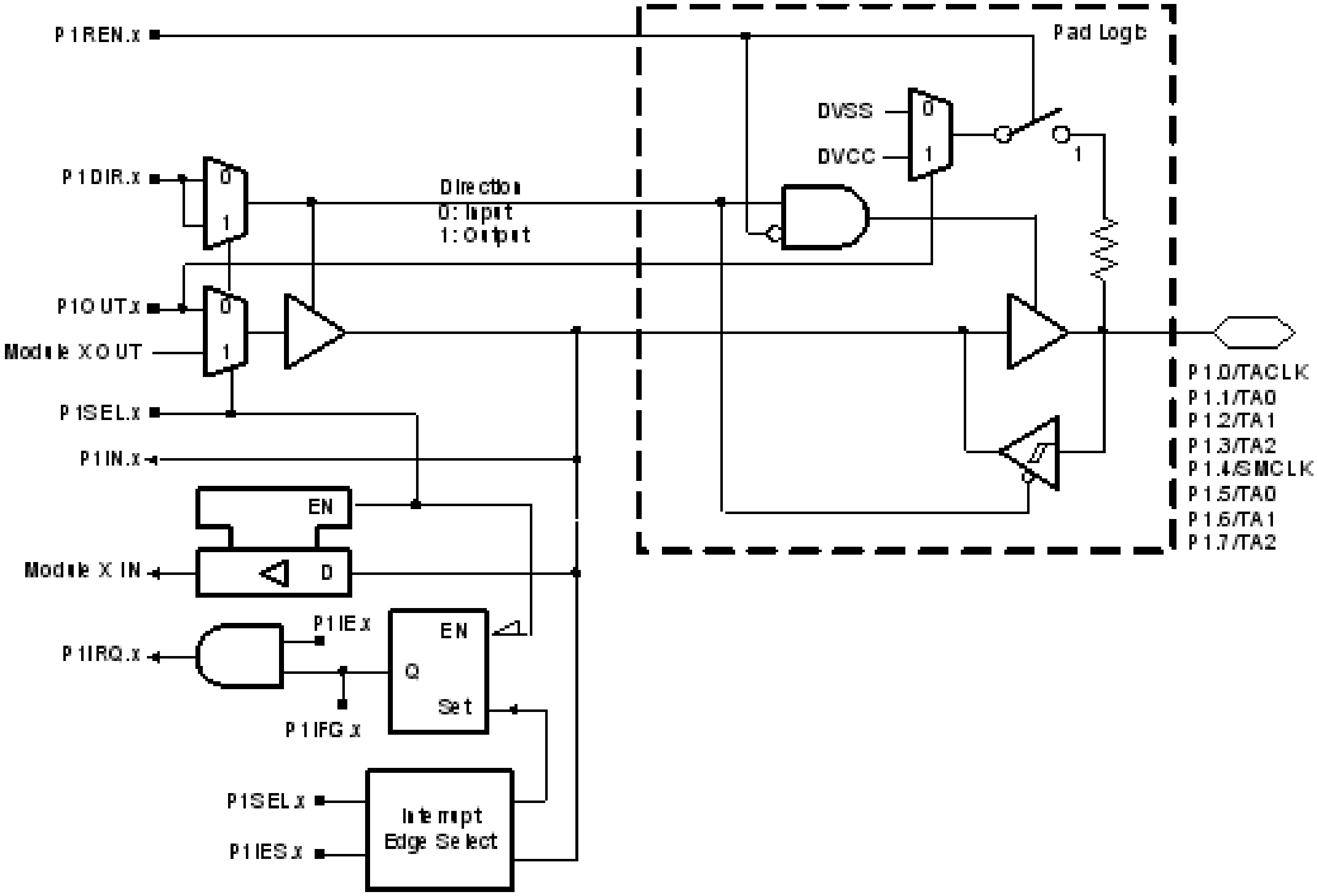
JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	$T_A = 25°C$	2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse blow: F versions		6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

NOTE 1: Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

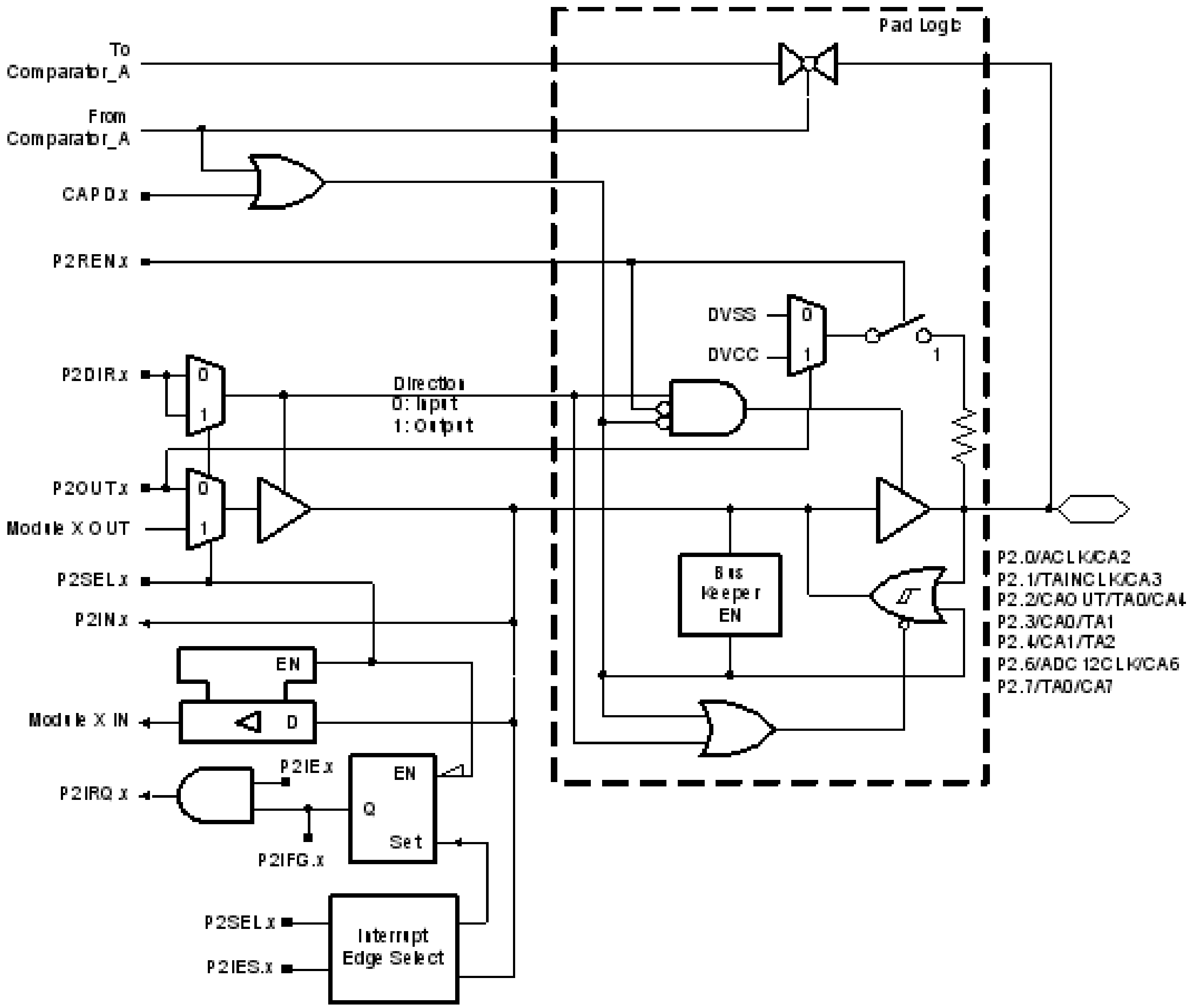
Port P1 pin schematic: P1.0 to P1.7, input/output with Schmitt trigger



Port P1.0 to P1.7 pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		CAOUT	1	1
P1.1/TA0	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.3/TA2	3	P1.3 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.4/SMCLK	4	P1.4 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P1.5/TA0	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.6/TA1	6	P1.6 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA1	1	1
P1.7/TA2	7	P1.7 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA2	1	1

Port P2 pin schematic: P2.0 to P2.4, P2.6, and P2.7, input/output with Schmitt trigger

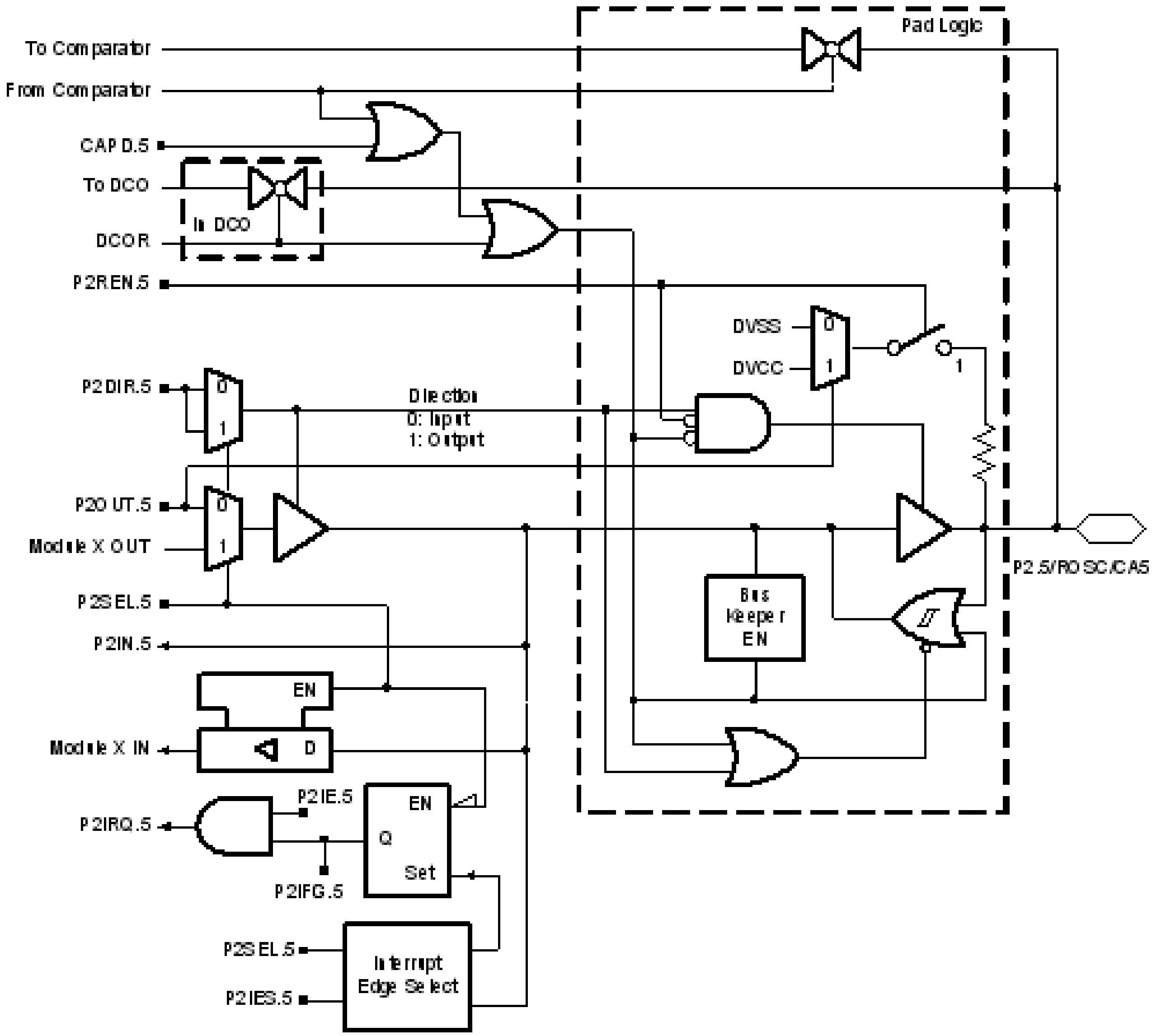


Port P2.0 to P2.4, P2.6, and P2.7 pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			CAPD.x	P2DIR.x	P2SEL.x
P2.0/ACLK/CA2	0	P2.0 (I/O)	0	I: 0; O: 1	0
		ACLK	0	1	1
		CA2	1	X	X
P2.1/TAINCLK/CA3	1	P2.1 (I/O)	0	I: 0; O: 1	0
		Timer_A3.INCLK	0	0	1
		DV_{SS}	0	1	1
		CA3	1	X	X
P2.2/CAOUT/TA0/ CA4	2	P2.2 (I/O)	0	I: 0; O: 1	0
		CAOUT	0	1	1
		TA0	0	0	1
		CA4	1	X	X
P2.3/CA0/TA1	3	P2.3 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA1	0	1	1
		CA0	1	X	X
P2.4/CA1/TA2	4	P2.4 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA2	0	1	X
		CA1	1	X	1
P2.6/ADC12CLK†/ CA6	6	P2.6 (I/O)	0	I: 0; O: 1	0
		ADC12CLK†	0	1	1
		CA6	1	X	X
P2.7/TA0/CA7	7	P2.7 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA0	0	1	1
		CA7	1	X	X

† MSP430F24x and MSP430F23x devices only
NOTE: X: Don’t care.

Port P2 pin schematic: P2.5, input/output with Schmitt trigger

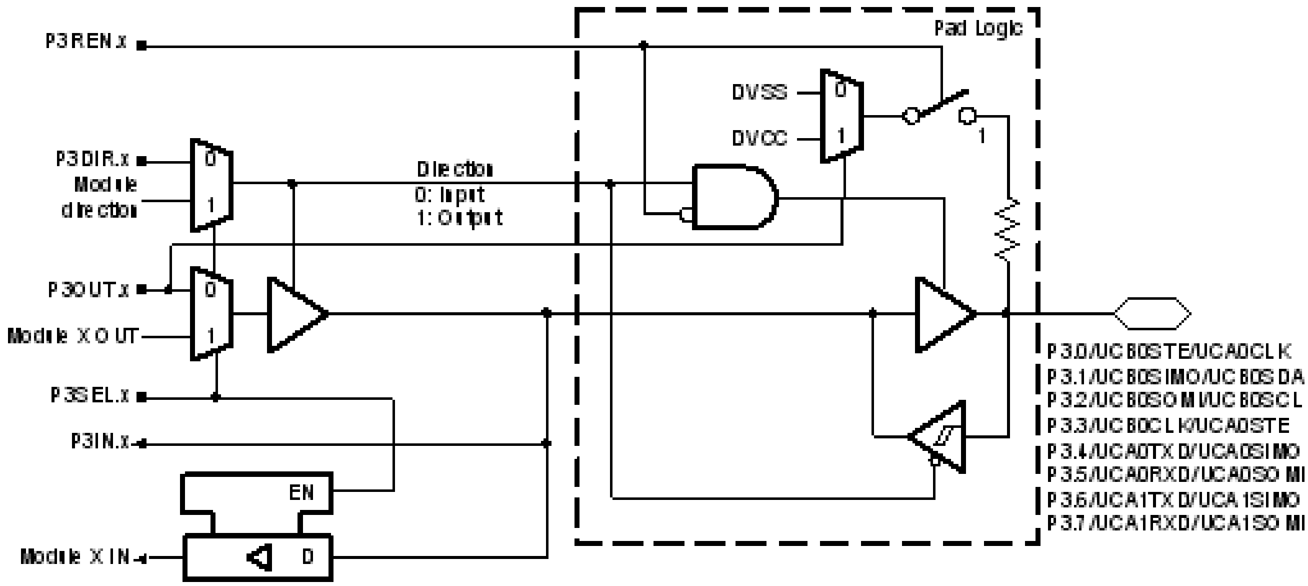


Port P2.5 pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD	DCOR	P2DIR.5	P2SEL.5
P2.5/R_{OSC}/CA5	5	P2.5 (I/O)	0	0	I: 0; O: 1	0
		R_{OSC}	0	1	X	X
		DV_{SS}	0	0	1	1
		CA5	1 or selected	0	X	X

NOTE: X: Don't care.

Port P3 pin schematic: P3.0 to P3.7, input/output with Schmitt trigger



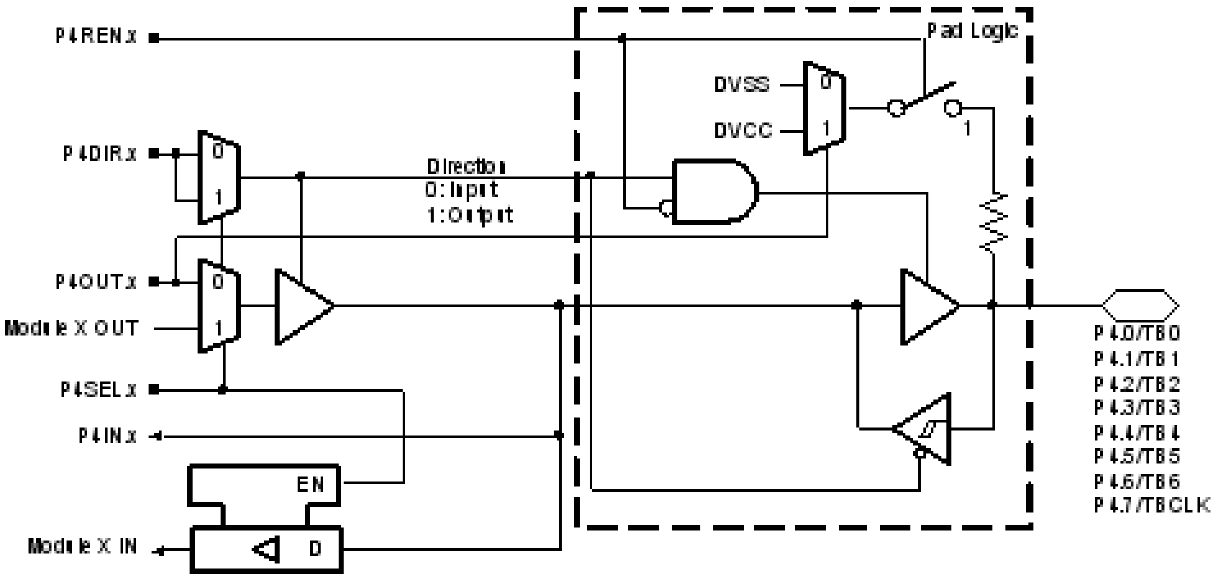
Port P3.0 to P3.7 pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/ UCA0CLK	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK (see Notes 2 and 4)	X	1
P3.1/UCB0SIMO/ UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA (see Notes 2 and 3)	X	1
P3.2/UCB0SOMI/ UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL (see Notes 2 and 3)	X	1
P3.3/UCB0CLK/ UCA0STE	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE (see Note 2)	X	1
P3.4/UCA0TXD/ UCA0SIMO	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO (see Note 2)	X	1
P3.5/UCA0RXD/ UCA0SOMI	5	P3.5 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI (see Note 2)	X	1
P3.6/UCA1TXD†/ UCA1SIMO†	6	P3.6 (I/O)	I: 0; O: 1	0
		UCA1TXD†/UCA1SIMO† (see Note 2)	X	1
P3.7/UCA1RXD†/ UCA1SOMI†	7	P3.7 (I/O)	I: 0; O: 1	0
		UCA1RXD†/UCA1SOMI† (see Note 2)	X	1

† MSP430F24x and MSP430F24x1 devices only

NOTES: 1. X: Don't care.
2. The pin direction is controlled by the USCI module.
3. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.
4. UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output USCI A/B0 will be forced to 3−wire SPI mode if 4−wire SPI mode is selected.

Port P4 pin schematic: P4.0 to P4.7, input/output with Schmitt trigger

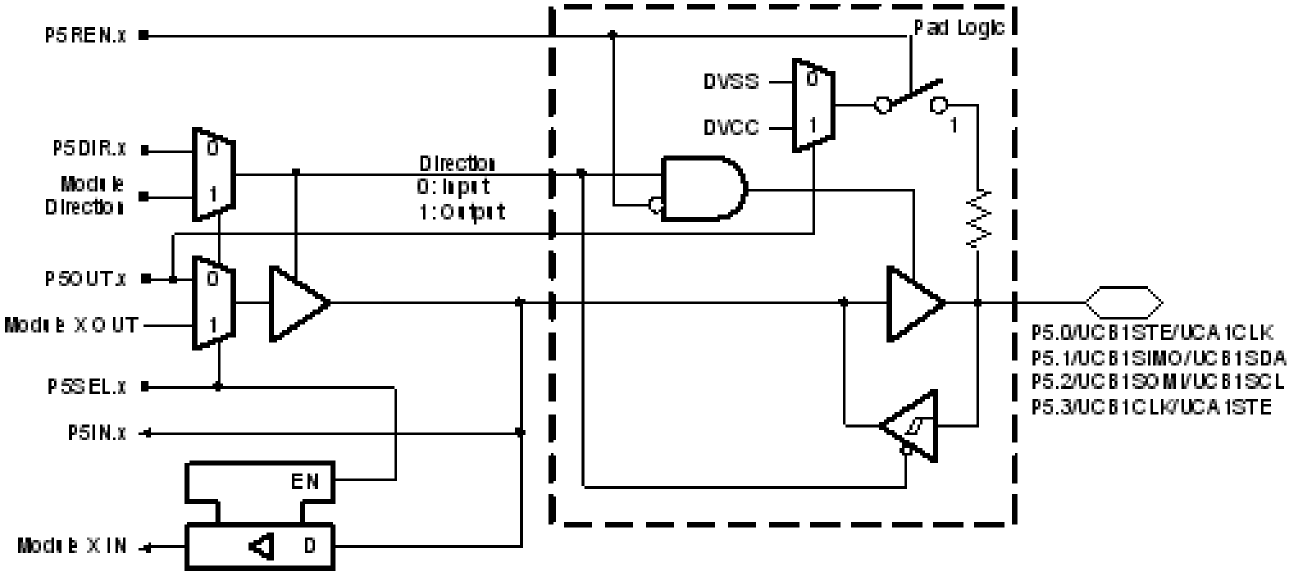


Port P4.0 to P4.7 pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0	1	1
P4.1/TB1	1	P4.1 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1	1	1
P4.2/TB2	2	P4.2 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB2	1	1
P4.3/TB3†	3	P4.3 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI3A and Timer_B7.CCI3B†	0	1
		Timer_B7.TB3†	1	1
P4.4/TB4†	4	P4.4 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI4A and Timer_B7.CCI4B†	0	1
		Timer_B7.TB4†	1	1
P4.5/TB5†	5	P4.5 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI5A and Timer_B7.CCI5B†	0	1
		Timer_B7.TB5†	1	1
P4.6/TB6†	6	P4.6 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI6A and Timer_B7.CCI6B†	0	1
		Timer_B7.TB6†	1	1
P4.7/TBCLK	7	P4.7 (I/O)	I: 0; O: 1	0
		Timer_B7.TBCLK	0	1

† MSP430F24x and MSP430F24x1 devices only

Port P5 pin schematic: P5.0 to P5.3, input/output with Schmitt trigger



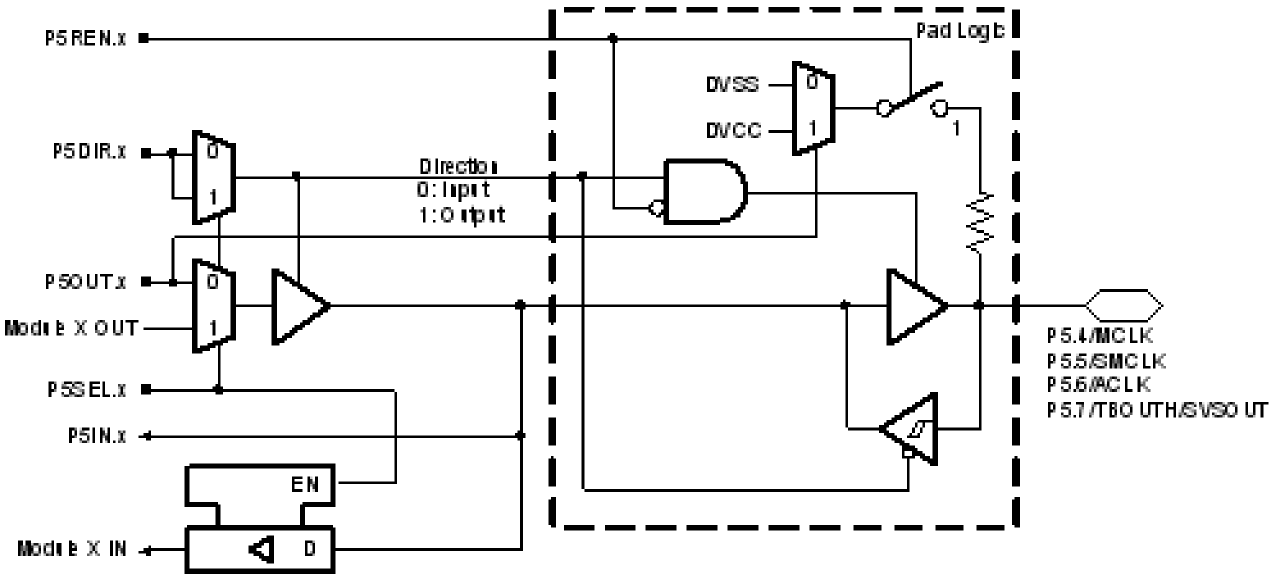
Port P5.0 to P5.3 pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.0/UCB1STE†/ UCA1CLK†	0	P5.0 (I/O)	I: 0; O: 1	0
		UCB1STE†/UCA1CLK† (see Notes 2 and 4)	X	1
P5.1/UCB1SIMO†/ UCB1SDA†	1	P5.1 (I/O)	I: 0; O: 1	0
		UCB1SIMO†/UCB1SDA† (see Notes 2 and 3)	X	1
P5.2/UCB1SOMI†/ UCB1SCL†	2	P5.2 (I/O)	I: 0; O: 1	0
		UCB1SOMI†/UCB1SCL† (see Notes 2 and 3)	X	1
P5.3/UCB1CLK†/ UCA1STE†	3	P5.3 (I/O)	I: 0; O: 1	0
		UCB1CLK†/UCA1STE† (see Note 2)	X	1

† † MSP430F24x and MSP430F24x1 devices only

NOTES: 1. X: Don't care.
2. The pin direction is controlled by the USCI module.
3. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.
4. UCA01CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output USCI A/B1 will be forced to 3−wire SPI mode if 4−wire SPI mode is selected.

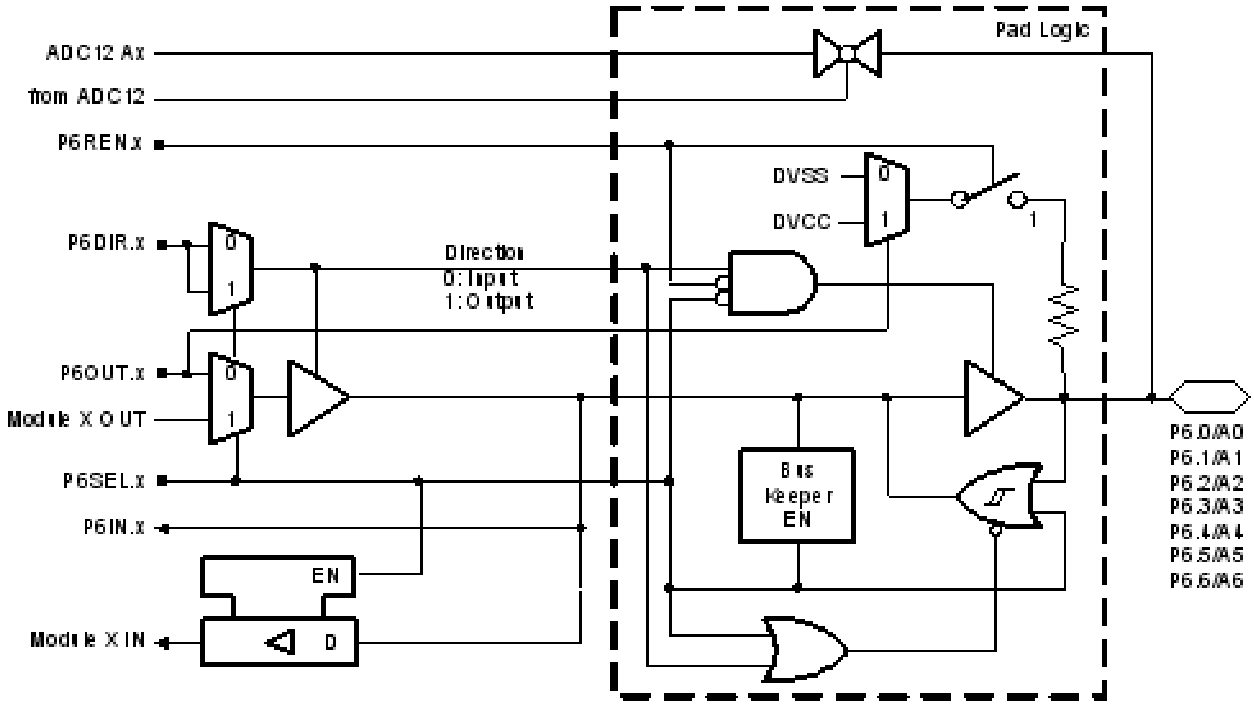
Port P5 pin schematic: P5.4 to P5.7, input/output with Schmitt trigger



Port P5.4 to P5.7 pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.4/MCLK	4	P5.4 (I/O)	I: 0; O: 1	0
		MCLK	1	1
P5.5/SMCLK	5	P5.5 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P5.6/ACLK	6	P5.6 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P5.7/TBOUTH/ SVSOUT	7	P5.7 (I/O)	I: 0; O: 1	0
		Timer_B7.TBOUTH	0	1
		SVSOUT	1	1

Port P6 pin schematic: P6.0 to P6.6, input/output with Schmitt trigger

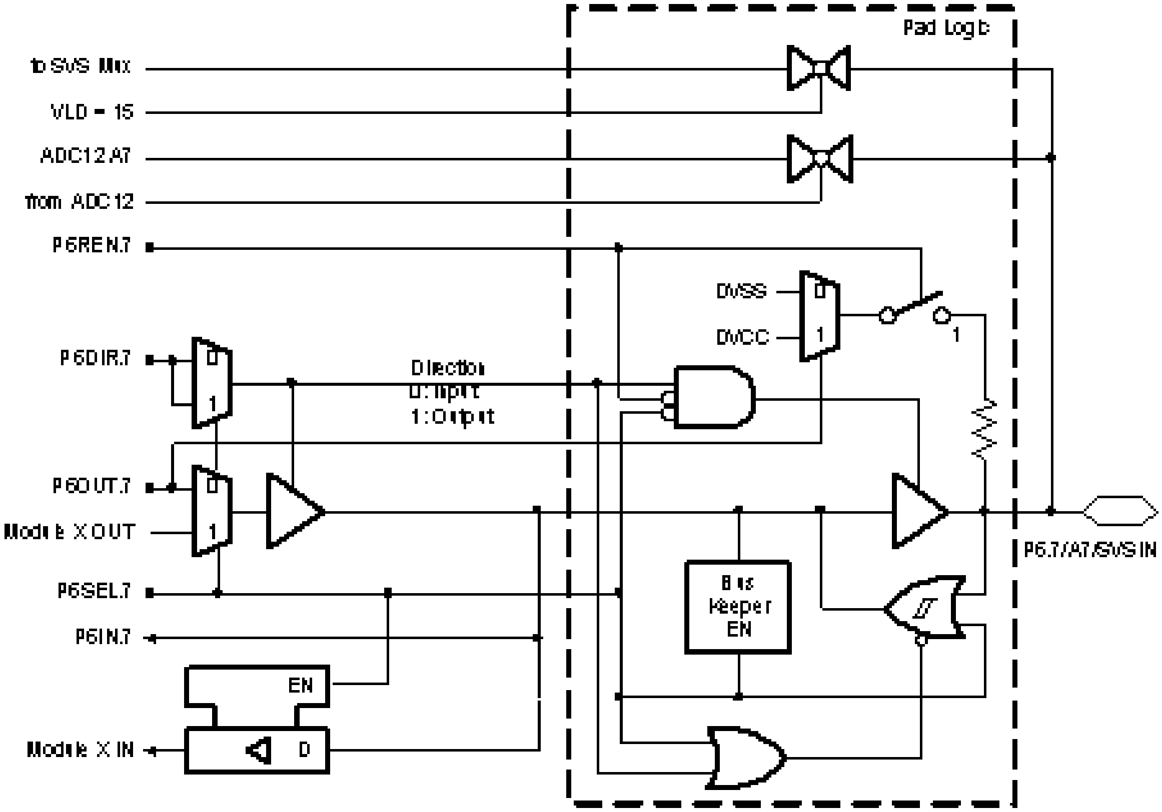


Port P6.0 to P6.6 pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P6DIR.x	P6SEL.x	CAPD.x
P6.0/A0†	0	P5.0 (I/O)	I: 0; O: 1	0	0
		A0†	X	X	1
P6.1/A1†	1	P5.1 (I/O)	I: 0; O: 1	0	0
		A1†	X	X	1
P6.2/A2†	2	P5.2 (I/O)	I: 0; O: 1	0	0
		A2†	X	X	1
P6.3/A3†	3	P5.3 (I/O)	I: 0; O: 1	0	0
		A3†	X	X	1
P6.4/A4†	4	P5.4 (I/O)	I: 0; O: 1	0	0
		A4†	X	X	1
P6.5/A5†	5	P5.5 (I/O)	I: 0; O: 1	0	0
		A5†	X	X	1
P6.6/A6†	6	P6.6 (I/O)	I: 0; O: 1	0	0
		A6†	X	X	1

† MSP430F24x and MSP430F23x devices only

Port P6 pin schematic: P6.7, input/output with Schmitt trigger

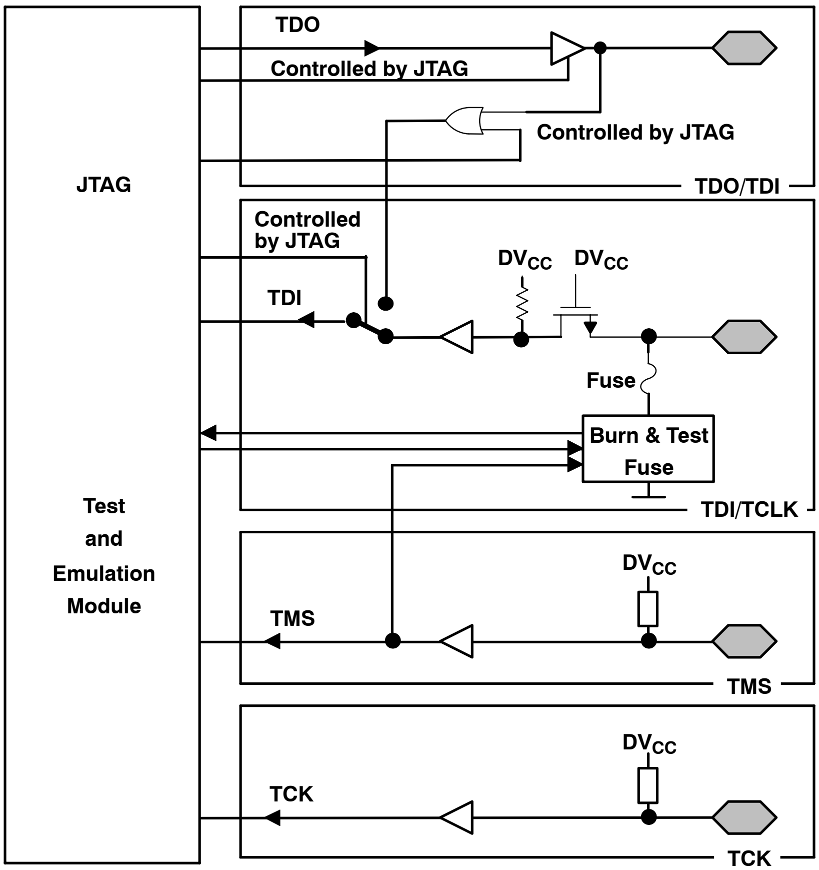


Port P6.7 pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P6DIR.x	P6SEL.x	CAPD.x
P6.7/A7/SVSIN	7	P6.7 (I/O)	I: 0; O: 1	0	0
		DV_{SS}	1	1	0
		A7	X	X	1
		SVSIN (VLD = 15)	X	X	1

APPLICATION INFORMATION

JTAG pins (TMS, TCK, TDI/TCLK, TDO/TDI), input/output with Schmitt trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 41). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

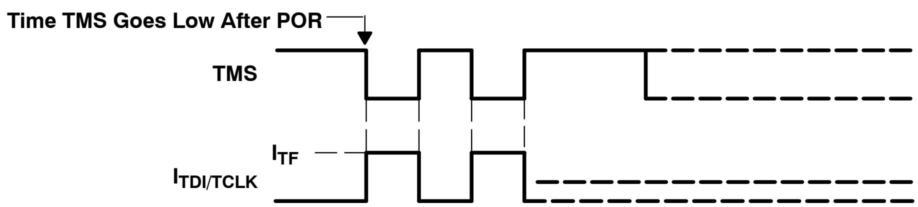


Figure 41. Fuse Check Mode Current

Data Sheet Revision History

LITERATURE NUMBER	SUMMARY
SLAS584	Product Preview release

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430F249MPMEP	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Contact TI Distributor or Sales Office
V62/09601-01XE	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Contact TI Distributor or Sales Office

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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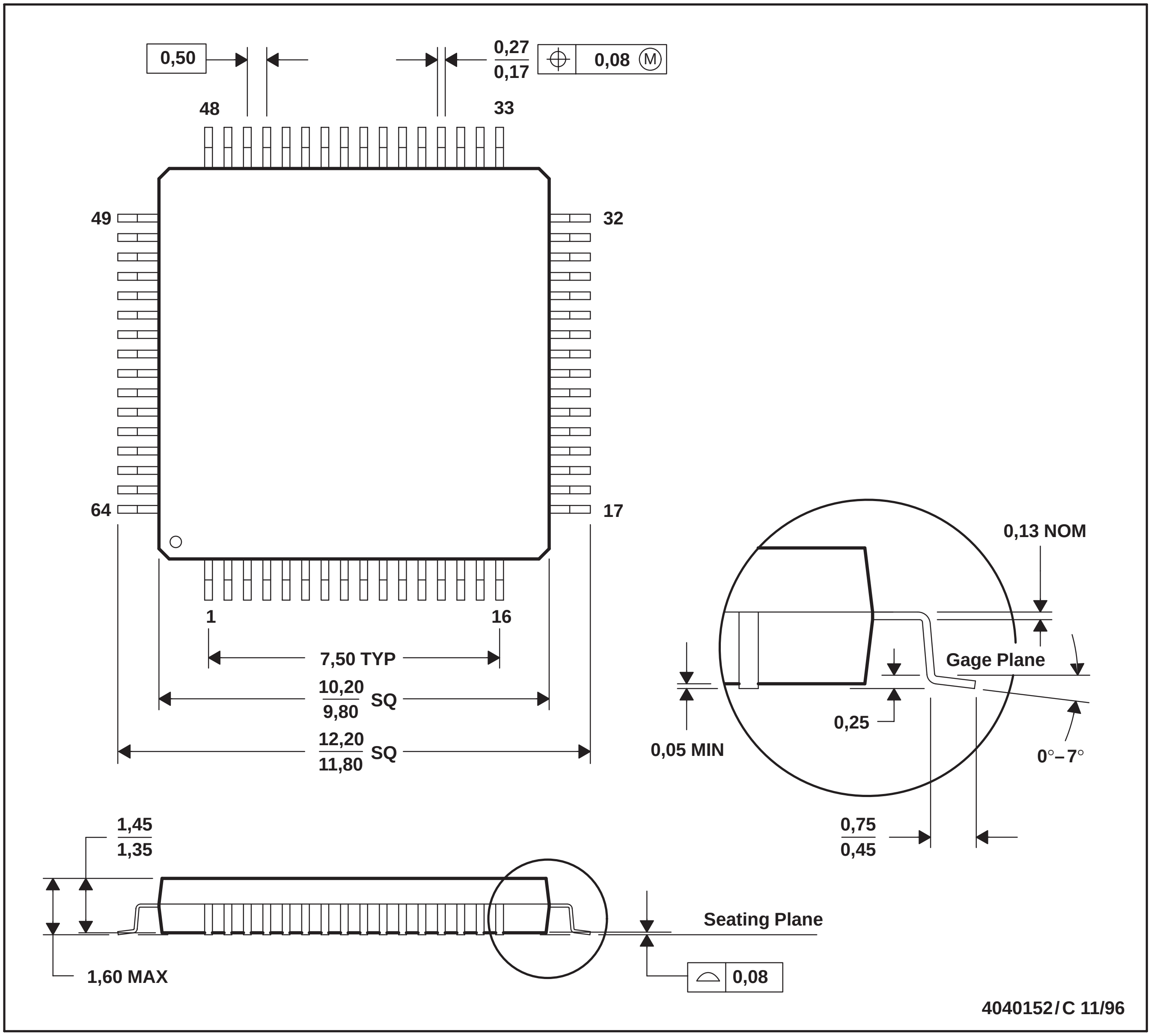
OTHER QUALIFIED VERSIONS OF MSP430F249-EP :

- Catalog: MSP430F249

NOTE: Qualified Version Definitions:

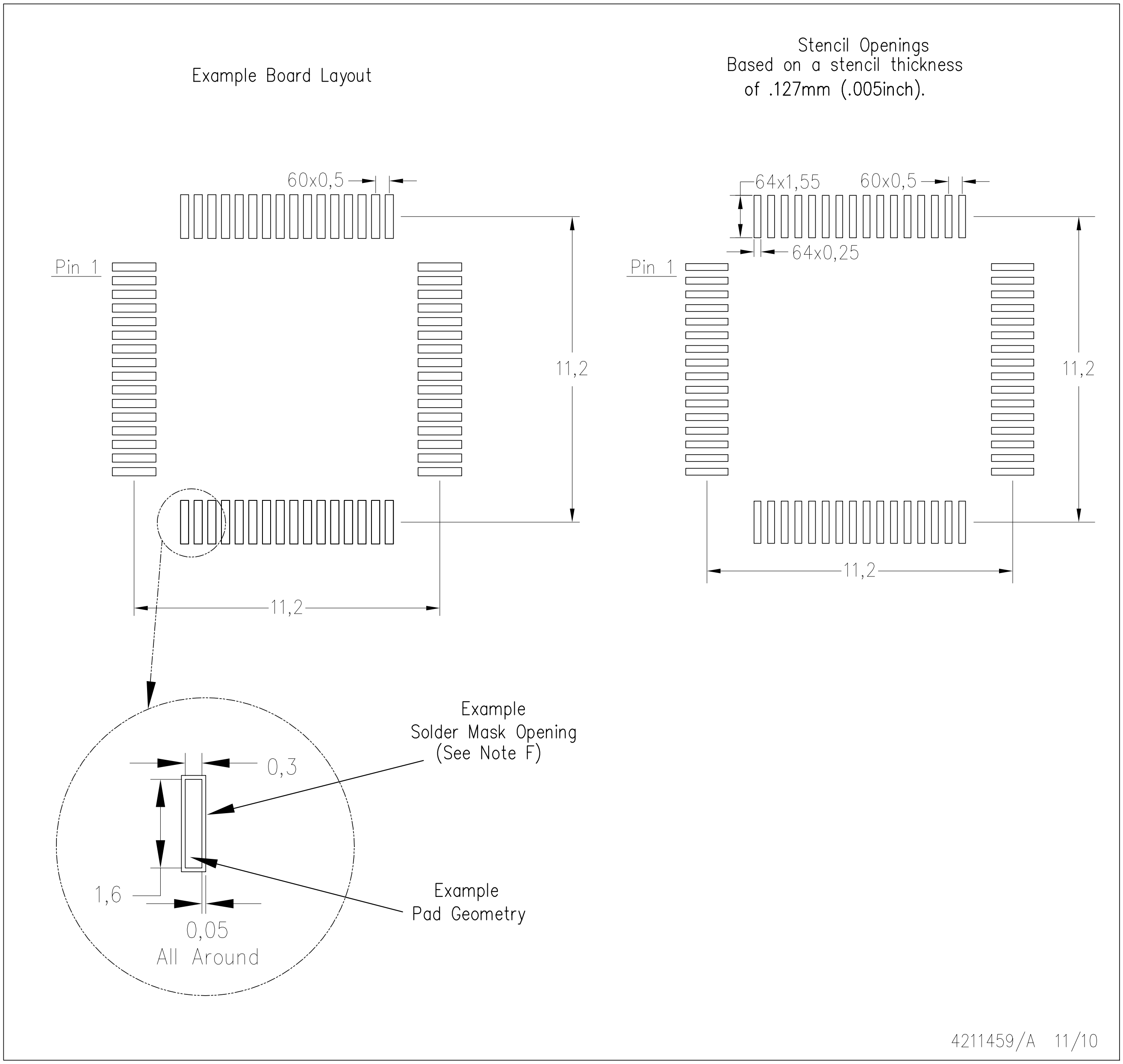
- Catalog - TI's standard catalog product

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S-PQFP-G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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