

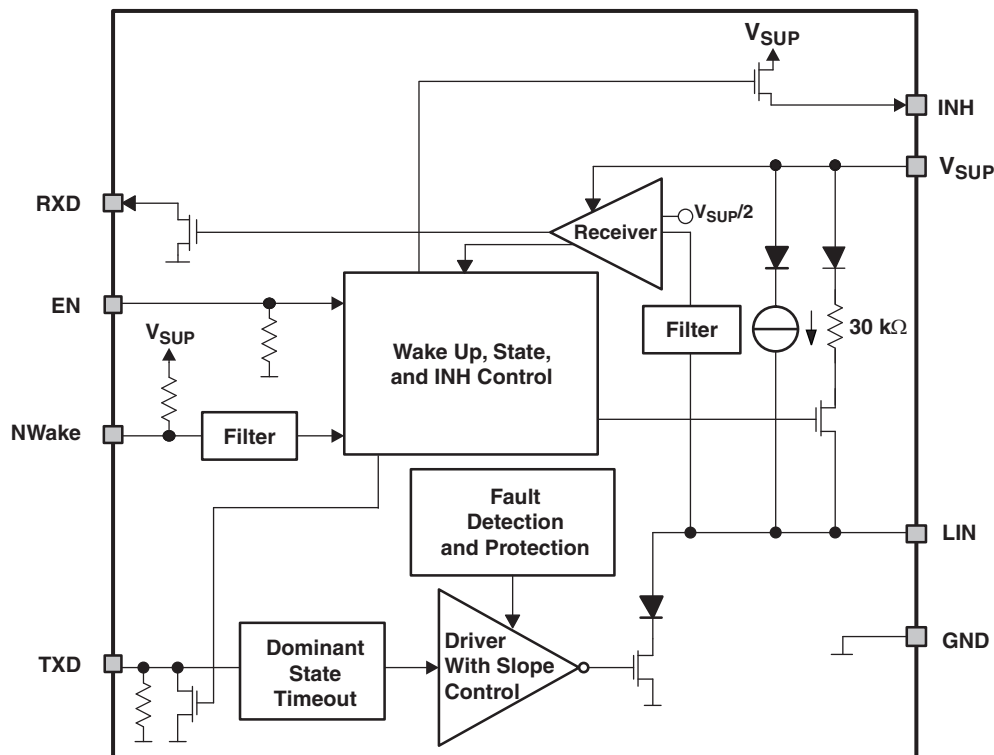
## LIN PHYSICAL INTERFACE

 Check for Samples: [SN65HVDA100-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- Local Interconnect Network (LIN) Physical Layer Specification Revision 2.1 Compliant and Conforms to SAEJ2602 Recommended Practice for LIN
- Extended Operation With Supply From 5 V to 27 V DC (LIN Specification 7 V to 18 V)
- LIN Transmit Speed up to 20-kbps LIN Specified Maximum, High-Speed Receive Capable
- Sleep Mode: Ultralow Current Consumption Allows Wake-Up Events From: LIN Bus, Wake-Up Input (External Switch) or Host MCU
- Wake-Up Request on RXD Pin
- Wake-Up Source Recognition on TXD Pin
- Interfaces to MCU With 5-V or 3.3-V I/O Pins
- High Electromagnetic Compatibility (EMC)
- Control of External Voltage Regulator (INH Pin)
- Supports ISO9141 (K-Line) -Like Functions
- Protection
- ESD Protection to  $\pm 12$  kV (Human-Body Model) on LIN Pin
- LIN Pin Handles Voltage From  $-27$  V to 45 V (Short to Battery or Ground)
- Survives Transient Damage in Automotive Environment (ISO 7637)
- Undervoltage Protection on  $V_{SUP}$
- TXD Dominant State Time-Out Protection
- Prevention of False Wake-Ups With Bus Stuck Dominant Fault
- Thermal Shutdown
- Unpowered Node or Ground Disconnection Failsafe at System Level, Node Does Not Disturb Bus (No load on bus)

### FUNCTIONAL BLOCK DIAGRAM



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

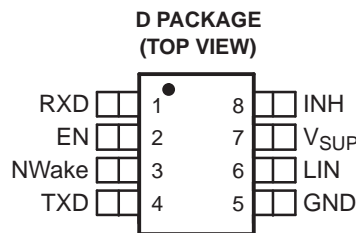
## DESCRIPTION

The SN65HVDA100 is the Local Interconnect Network (LIN) physical interface, which integrates the serial transceiver with wake-up and protection features. The LIN bus is a single-wire bidirectional bus typically used for low-speed in-vehicle networks using data rates between 2.4 kbps and 20 kbps. The LIN protocol output data stream on TXD is converted by the SN65HVDA100 into the LIN bus signal through a current-limited wave-shaping driver as outlined by the LIN Physical Layer Specification. The receiver converts the data stream from the LIN bus and outputs the data stream via RXD. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pullup resistor (30 k $\Omega$ ) and series diode, so no external pullup components are required for slave applications. Master applications require an external pullup resistor (1 k $\Omega$ ) plus a series diode per the LIN specification.

In sleep mode, low quiescent current is needed even though the wake-up circuits remain active and allow for remote wake up via the LIN bus or local wake up via the NWake or EN pins.

The SN65HVDA100 has been designed for operation in the harsh automotive environment. The device also prevents back-feed current through LIN to the supply input in case of a ground shift or supply-voltage disconnection. It also features undervoltage, overtemperature, and loss-of-ground protection. In the event of a fault condition, the transmitter is immediately switched off and remains off until the fault condition is removed.

## PIN FUNCTIONS



## PIN ASSIGNMENTS

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	2	I	Enable input
GND	5	GND	Ground
INH	8	O	Inhibit controls external voltage regulator with inhibit input
LIN	6	I/O	LIN bus single-wire transmitter and receiver
NWAKE	3	I	High voltage input for device wake up
RXD	1	O	RXD output (open drain) interface reporting state of LIN bus voltage
TXD	4	I	TXD input interface to control state of LIN output
V <sub>SUP</sub>	7	Supply	Device supply voltage (connected to battery in series with external reverse blocking diode)

## ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	SN65HVDA100QDRQ1	A100Q

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).  
 (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



### TXD (Transmit Input / Output)

TXD is the interface to the MCU's LIN protocol controller or SCI/UART that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near battery). The TXD input structure is compatible with microcontrollers with 3.3-V and 5-V I/O. TXD has an internal pulldown resistor. The LIN bus is protected from being stuck dominant via a system failure driving TXD low via the dominant state timeout timer. The TXD pin is pulled down strongly in standby mode after a wake-up event on the NWake pin.

### RXD (Receive Output)

RXD is the interface to the MCU's LIN protocol controller or SCI/UART, which reports the state of the LIN bus voltage. LIN recessive (near battery) is represented by a high level on RXD and LIN dominant (near ground) is represented by a low level on RXD. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3-V and 5-V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pullup, an external pullup resistor to the microcontroller I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake up request from LIN or NWake.

### V<sub>SUP</sub> (Supply Voltage)

V<sub>SUP</sub> is the power supply pin. V<sub>SUP</sub> is connected to the battery through an external reverse battery blocking diode. If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

### GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce V<sub>SUP</sub> below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

### EN (Enable Input)

EN controls the operational modes of the device. When EN is high, the device is in normal mode, allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pulldown resistor to ensure the device remains in low-power mode even if EN floats.

### NWake (High Voltage Wake Up Input)

NWake is a high-voltage input used to wake up from sleep mode. NWake is usually connected to an external switch in the application. A low on NWake that is asserted longer than the filter time (t<sub>NWAKE</sub>) results in a local wake-up. NWake provides an internal pullup source to V<sub>SUP</sub>.

### INH (Inhibit Output)

INH is used to control an external voltage regulator that has an inhibit or enable input. When the device is in normal operating mode, the inhibit switch is enabled and the external voltage regulator is activated. When device is in sleep mode, the inhibit switch is disabled, which turns off the system voltage regulator. A wake-up event transitions the device to standby by mode and re-enables INH which, in turn, restarts the system by turning on the voltage regulators. INH can also drive an external transistor connected to an MCU interrupt input.

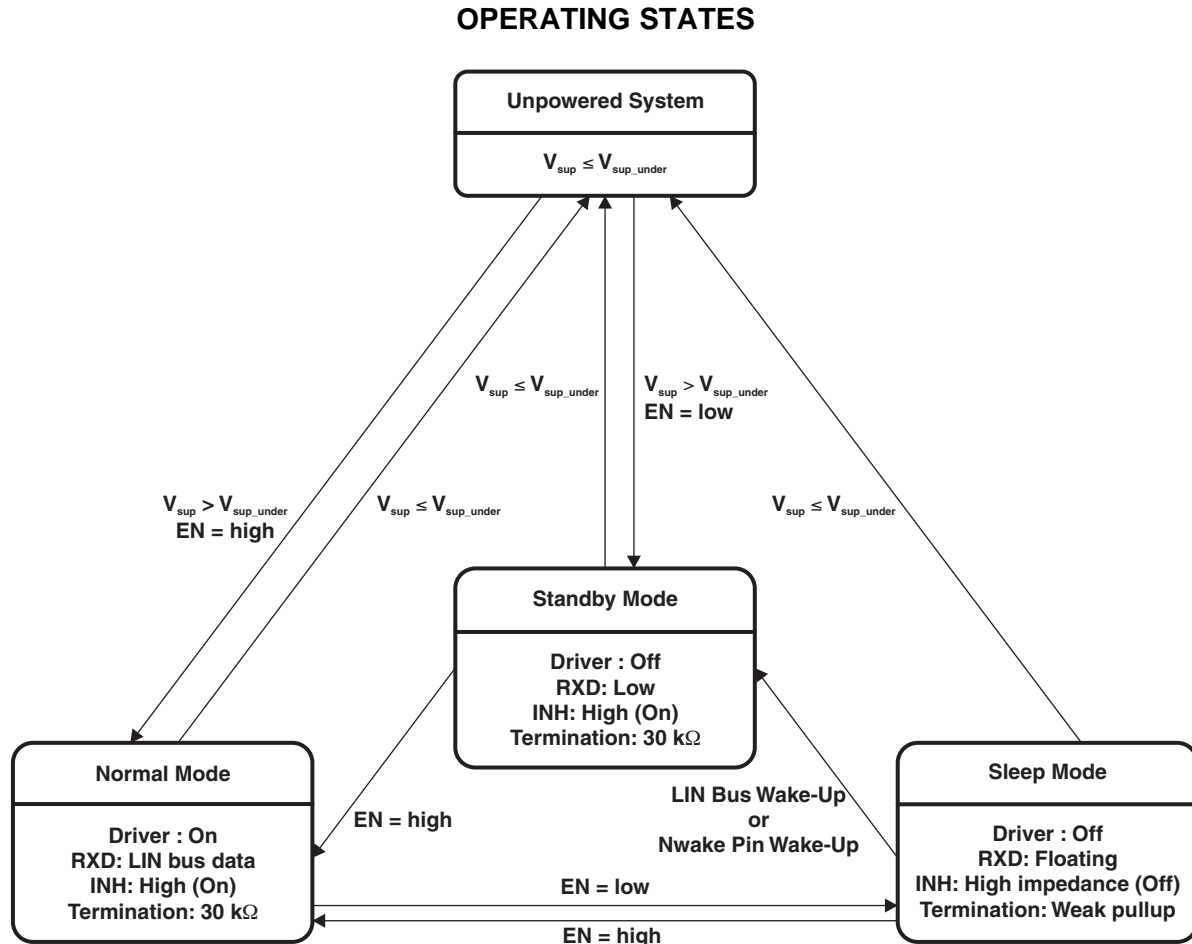


Figure 2. Operating States Diagram

Table 1. Operating Modes

MODE	EN	RXD	LIN BUS TERMINATION	INH	TRANSMITTER	COMMENTS
Sleep	Low	Floating	Weak current pullup	High impedance	Off	
Standby	Low	Low	30 kΩ (typ)	High	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	LIN bus data	30 kΩ (typ)	High	On	LIN transmission up to 20 kbps

**Normal Mode**

This is the normal operational mode, in which the receiver and driver are active, and LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller, where recessive on the LIN bus is a digital high, and dominate on the LIN bus is digital low. The driver transmits input data on TXD to the LIN bus. Normal mode is entered as EN transitions high while the SN65HVDA100 is in sleep or standby mode.

## Sleep Mode

Sleep mode is the power saving mode for the SN65HVDA100. Even with the extremely low current consumption in this mode, the SN65HVDA100 can still wake up from LIN bus via a wake-up signal, a low on NWake, or if EN is set high. The LIN bus and NWake are filtered to prevent false wake-up events. The wake-up events must be active for their respective time periods ( $t_{LINBUS}$ ,  $t_{NWake}$ ).

The sleep mode is entered by setting EN low.

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pullup is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- INH is high impedance.
- EN input, NWake input, and the LIN wake-up receiver are active.

## Wake-Up Events

There are three ways to wake up from sleep mode:

- Remote wake-up via recessive (high) to dominant (low) state transition on LIN bus. The dominant state must be held for  $t_{LINBUS}$  filter time and then the bus must return to the recessive state (to eliminate false wake-ups from disturbances on the LIN bus or if the bus is shorted to ground).
- Local wake-up via a low on NWake, which is asserted low longer than the filter time  $t_{NWake}$  (to eliminate false wake-ups from disturbances on NWake)
- Local wake-up via EN being set high

## Wake-Up Request (RXD)

When the device encounters a wake-up event from the LIN bus or NWake pin, RXD goes low, and the device transitions to standby mode (until EN is reasserted high and the device enters normal mode). Once the device enters normal mode, the RXD pin is releasing the wake-up request signal, and the RXD pin then reflects the receiver output from the bus.

## Wake-Up Source Recognition (TXD)

When the device encounters a wake-up event from the LIN bus or NWake pin, TXD indicates the source while the device enters and remains in standby mode (until EN is reasserted high and the device enters normal mode). In addition to the internal pullup resistor on TXD, typically an external pullup resistor (~5 k $\Omega$ ) is used in the system's I/O supply voltage. A high on TXD in standby mode indicates a remote wake-up via the LIN bus, and a low (strong pulldown) on the TXD pin indicates a local wake-up via the NWAKE pin.

## Standby Mode

This mode is entered whenever a wake-up event occurs via LIN bus or NWake while the device is in sleep mode. The LIN bus slave termination circuit and INH are turned on when standby mode is entered. The application system powers up once INH is turned on, assuming the system is using a voltage regulator connected via INH. Standby mode is signaled via a low level on RXD.

When EN is set high while the device is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

During power up if EN is low the device goes into Standby mode and if EN is high the device goes into Normal mode. EN has an internal pull down resistor, so if the pin is floating in the system, the internal pull down will ensure it is pulled low.

**Application Hint:** If the INH output of the HVDA100 is not used to control the system power management (voltage regulators) and monitor wake up sources, but sleep mode is used to reduce system current the RXD pin can be monitored to ensure HVDA100 remains in sleep mode. If the HVDA100 detects an undervoltage on  $V_{SUP}$  the RXD pin transitions low and would signal to the software that the HVDA100 is in standby mode and should be returned to sleep mode to return to the lowest power state.

### Mode Transitions

When the device is transitioning between modes the device needs the time,  $t_{MODE\_CHANGE}$ , to allow the change to fully propagate from the EN pin through the device into the new state.

**Application Hint:** When using the HVDA100 in systems which are not controlled via the INH output, but rather are monitoring the RXD pin for a wake-up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake-up request until  $t_{MODE\_CHANGE}$ . This is shown in Figure 3.

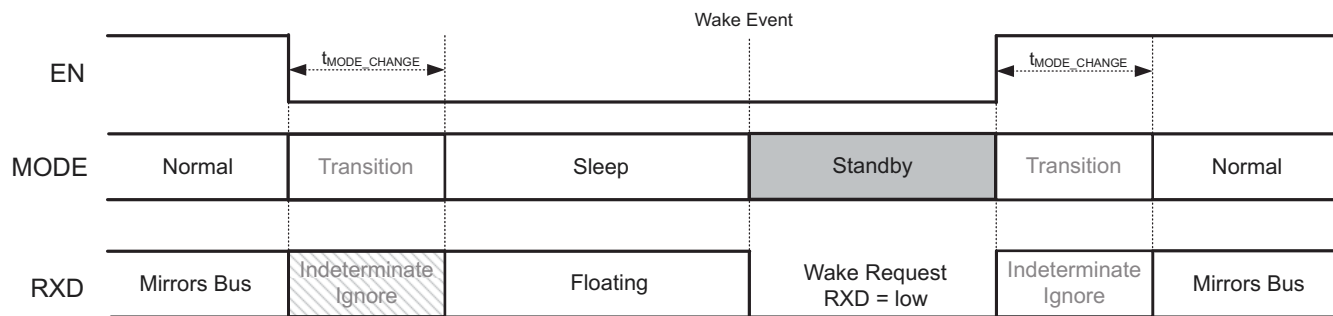


Figure 3. Mode Transitions

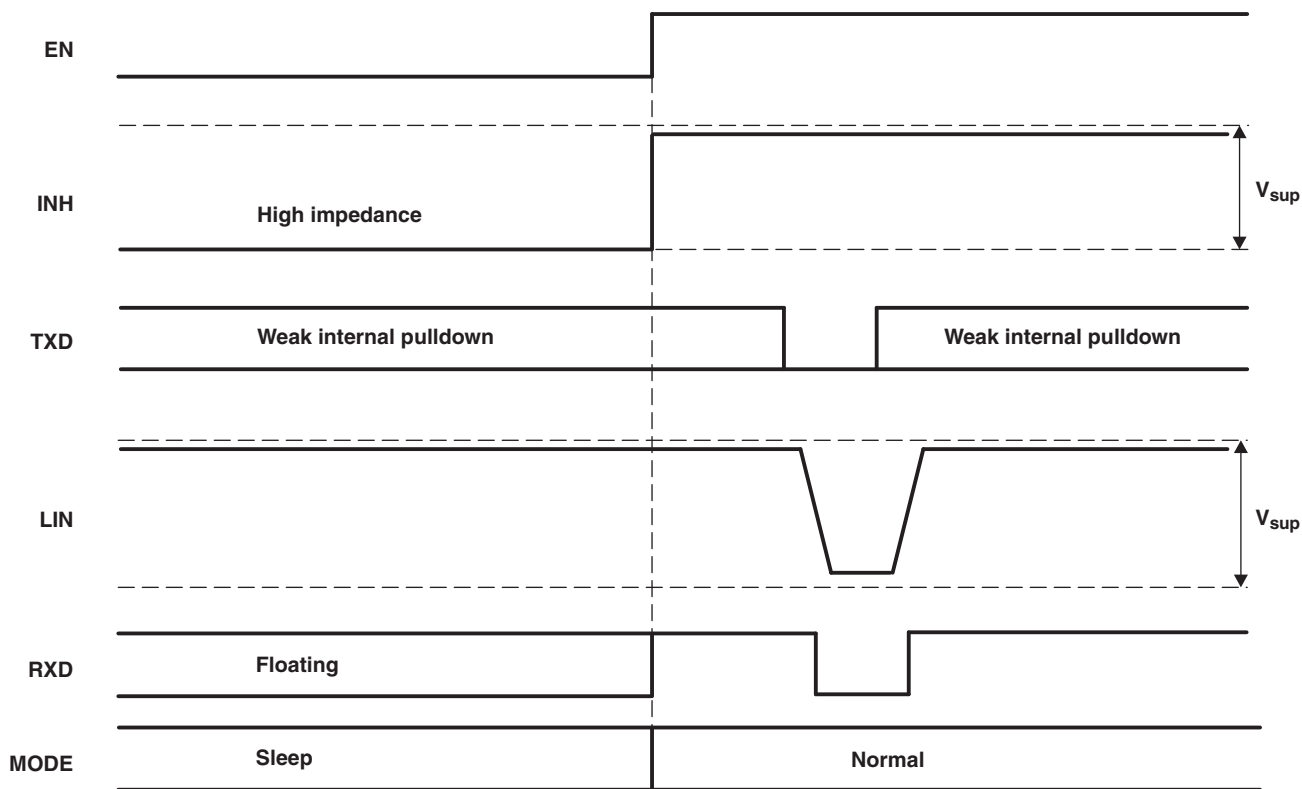


Figure 4. Wake-Up Via EN

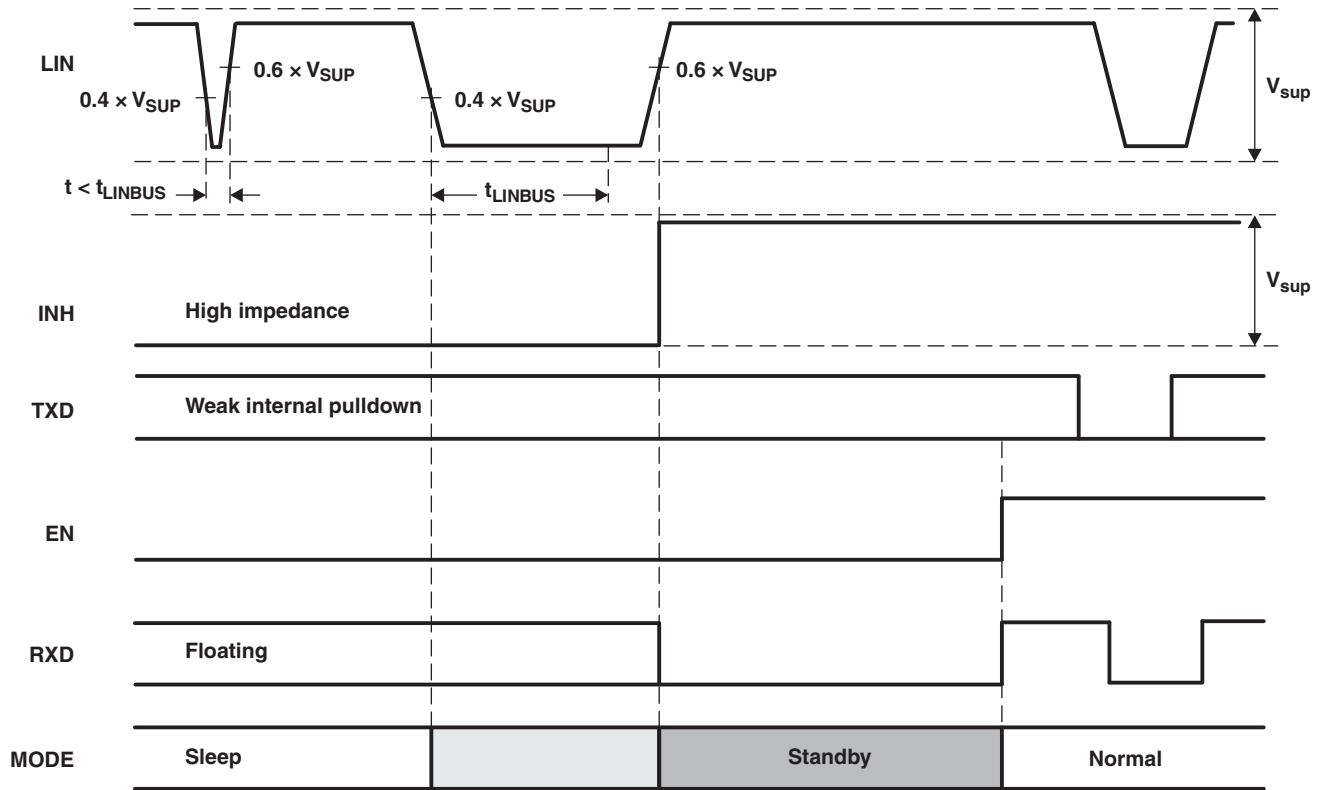


Figure 5. Wake-Up Via LIN

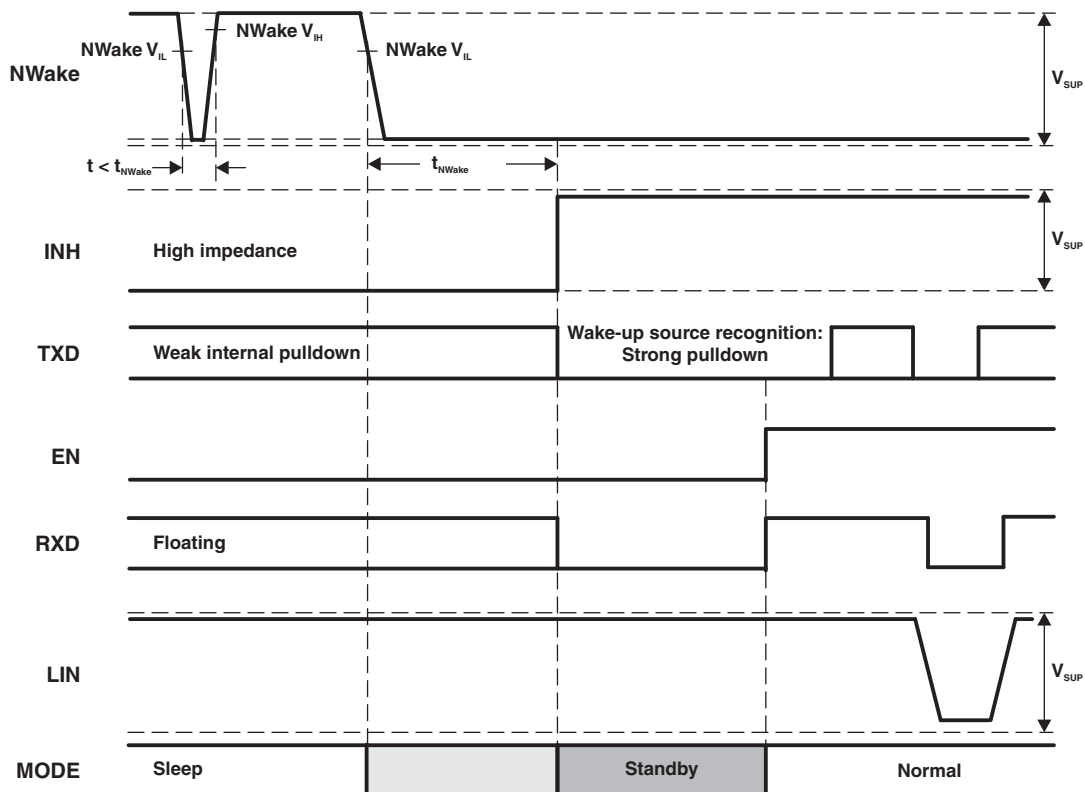


Figure 6. Wake-Up Via NWake



## PROTECTION AND FAILSAFE FEATURES

### TXD Dominant State Timeout

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on TXD. If the low signal remains on TXD for longer than  $t_{DST}$ , the transmitter is disabled, thus allowing the LIN bus to return to the recessive state and communication to resume on the bus. The protection is cleared and the  $t_{DST}$  timer is reset by a rising edge on TXD. The TXD pin has an internal pulldown to ensure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus, INH remains on, and the LIN bus pullup termination remains on.

**APPLICATION HINT:** The maximum dominant TXD time allowed by the TXD Dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for master and slave applications thus there are different the maximum consecutive dominant bits for each application case and thus different minimum data rates.

**Master node:** The maximum continuous dominant is the maximum dominant of the SYNC BREAK FIELD,  $t_{SYNC\_DOM(max)}$ . The SYNC BREAK FIELD notifies the 'start of frame' to all LIN slaves. It consists of 13 to 26 dominant bits (low phase) followed by a delimiter. Thus the minimum TXD dominant time out,  $t_{DST(min)}$  and the maximum SYNC BREAK FIELD for the master determine the minimum data rate for a master node, which may be calculated by the following equation:

$$DataRate_{Master(min)} = t_{SYNC\_DOM(max)} / t_{DST(min)}$$

**Slave node:** sends the response part of the LIN message frame which has a maximum consecutive dominant length of 9 bits (start bit + 8 data bits). As a result the minimum baud rate of a slave can be calculated by the following equation:

$$DataRate_{Slave(min)} = 9 + n_{margin} / t_{DST(min)} \text{ where } n_{margin} \text{ is a safety margin.}$$

### Thermal Shutdown

The LIN transmitter is protected via a current limit, however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device turns off the LIN transmitter circuit. Once the overtemperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus, INH remains on, and the LIN bus pullup termination remains on.

## Bus Stuck Dominant System Fault: False Wake Up Lock Out

The device contains logic to detect bus stuck dominant system faults and prevent the device from waking up falsely during this system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake up logic is locked out until a valid recessive on the bus "clears" the bus stuck dominant condition. This logic prevents the potential for a cyclical false wake up of the system if the bus is stuck dominant, preventing excessive current use. Figure 7 and Figure 8 show the behavior of this protection feature.

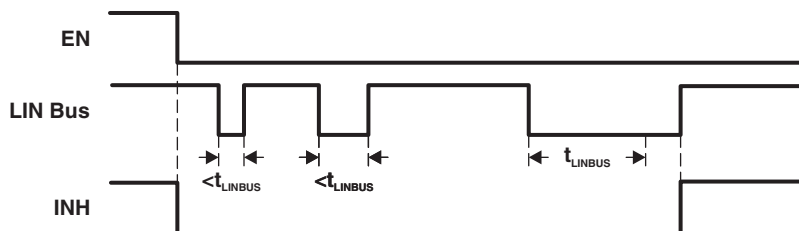


Figure 7. No Bus Fault: Entering Sleep Mode With Bus Recessive Condition and Wake Up

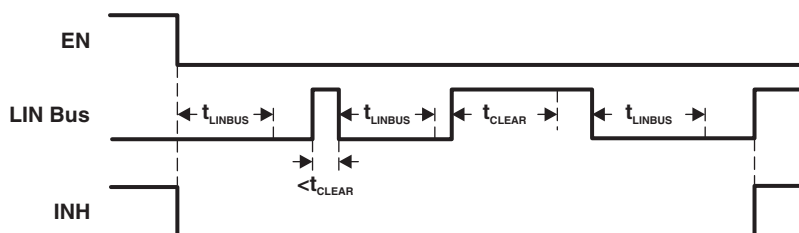


Figure 8. Bus Fault: Entering Sleep Mode With Bus Stuck Dominant Fault, Clearing, and Wake Up

## Undervoltage on $V_{SUP}$

The device contains a power-on reset circuit to avoid false bus messages during undervoltage conditions when  $V_{SUP}$  is less than  $UV_{VSUP}$ .

## Unpowered Device Does Not Affect the LIN Bus

The device has extremely low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

**ABSOLUTE MAXIMUM RATINGS<sup>(1) (2)</sup>**

			UNITS
1.1	V <sub>SUP</sub>	Supply line supply voltage (LIN 2.1 Param 11)	–0.3 V to 45 V
1.2	V <sub>LIN</sub>	LIN input voltage	–27 V to 45 V
1.3	V <sub>NWAKE</sub>	NWake input voltage (via serial resistor ≥ 2kΩ)	–0.3 V to 45 V
1.4	I <sub>O</sub>	Output current	–50 mA to 2 mA
1.5	V <sub>INH</sub>	INH voltage	–0.3 V to V <sub>sup</sub> + 0.3 V
1.6	V <sub>Logic</sub>	Logic pin voltage	RXD, TXD, EN –0.3 V to 5.5 V
1.7	T <sub>A</sub>	Operational free-air (ambient) temperature range	–40°C to 125°C
1.8	T <sub>J</sub>	Junction temperature range	–40°C to 150°C
1.9	T <sub>LEAD</sub>	Lead temperature (soldering, 10 seconds)	260°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

**TRANSIENT AND ELECTROSTATIC DISCHARGE PROTECTION**

2.1	Electrostatic discharge	Human-Body Model <sup>(1)</sup>	All pins	–4 kV to 4 kV
2.2			LIN bus pin <sup>(2)</sup>	–12 kV to 12 kV
2.3			NWake pin <sup>(3)</sup>	–11 kV to 11 kV
2.4		Charged-Device Model	All pins <sup>(4)</sup>	–1.5 kV to 1.5 kV

- (1) Tested in accordance to AEC-Q100-002.
- (2) Test method based upon AEC-Q100-002, LIN bus pin stressed with respect to GND.
- (3) Test method based upon AEC-Q100-002, NWake pin stressed with respect to GND.
- (4) Tested in accordance to AEC-Q100-011.

**RECOMMENDED OPERATING CONDITIONS**

			MIN	MAX	UNIT
3.1	V <sub>SUP</sub>	Supply line supply voltage (LIN 2.1 Param 10)	5	27	V
3.2	V <sub>LIN</sub>	LIN input voltage	0	18	V
3.3	V <sub>NWake</sub>	NWake input voltage	0	27	V
3.4	V <sub>INH</sub>	INH voltage	0	27	V
3.5	V <sub>Logic</sub>	Logic voltage	0	5.25	V
3.6	T <sub>A</sub>	Operational free-air temperature (see Thermal Characteristics table)	–40	125	°C

## ELECTRICAL CHARACTERISTICS

$V_{SUP} = 5V$  to  $27V$ ,  $T_J = -40^{\circ}C$  to  $150^{\circ}C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS / COMMENT		MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b><math>V_{SUP}</math> SUPPLY</b>							
4.1	$V_{SUP}$	Operational supply voltage (LIN 2.1 Param 10) <sup>(2)</sup>	Device is operational beyond the LIN defined nominal supply line voltage range of $5V < V_{SUP} < 27V$	5	14	27	V
4.2	$V_{SUP}$	Nominal supply voltage (LIN 2.1 Param 10)	Normal and standby modes	7	14	18	V
			Sleep mode	7	12	18	
4.3	$UV_{SUP}$	Undervoltage $V_{SUP}$ threshold		4.35		4.65	V
4.4	$UV_{HYS}$	Delta hysteresis voltage for $V_{SUP}$ undervoltage threshold			0.2		V
4.5	$I_{SUP}$	Supply current	Normal mode, EN = high, Bus dominant (total bus load where $R_{LIN} \geq 500\Omega$ and $C_{LIN} \leq 10nF$ (see Figure 11) <sup>(3)</sup> , INH = $V_{SUP}$ , NWake = $V_{SUP}$		1.2	7.5	mA
4.6			Standby mode, EN = low, Bus dominant (total bus load where $R_{LIN} \geq 500\Omega$ and $C_{LIN} \leq 10nF$ (see Figure 11) <sup>(3)</sup> , INH = $V_{SUP}$ , NWake = $V_{SUP}$		1	2.1	mA
4.7			Normal mode, EN = high, Bus recessive, LIN = $V_{SUP}$ , INH = $V_{SUP}$ , NWake = $V_{SUP}$		450	775	$\mu A$
4.8			Standby mode, EN = low, Bus recessive, LIN = $V_{SUP}$ , INH = $V_{SUP}$ , NWake = $V_{SUP}$		450	775	$\mu A$
4.9			Sleep mode, $7V < V_{SUP} \leq 14V$ , LIN = $V_{SUP}$ , NWake = $V_{SUP}$ , EN = 0V, TXD and RXD floating		10	20	$\mu A$
4.10			Sleep mode, $14V < V_{SUP} < 27V$ , LIN = $V_{SUP}$ , NWake = $V_{SUP}$ , EN = 0V, TXD and RXD floating				30
<b>RXD Output Pin (open drain)</b>							
5.1	$V_O$	Output voltage <sup>(4)</sup>		-0.3		5.5	V
5.2	$I_{OL}$	Low-level output current, open drain	LIN = 0V, RXD = 0.4V	3.5			mA
5.3	$I_{IKG}$	Leakage current, high-level	LIN = $V_{SUP}$ , RXD = 5V	-5	0	5	$\mu A$
<b>TXD Input / Output Pin</b>							
6.1	$V_{IL}$	Low-level input voltage		-0.3		0.8	V
6.2	$V_{IH}$	High-level input voltage		2		5.5	V
6.3	$V_{IT}$	Input threshold hysteresis voltage		30		500	mV
6.4		Pull-down resistor		125	350	800	k $\Omega$
6.5	$I_{IL}$	Low-level input leakage current	TXD = Low	-5	0	5	$\mu A$
6.6	$I_{TXD\_Wake}$	Local wake up source re recognition TXD open drain drive	Standby mode after a local wake up event, $V_{LIN} = V_{SUP}$ , NWake = 0V, TXD = 1V	1.3	4.6	8	mA

(1) Typical values are given for  $V_{SUP} = 14V$  at  $25^{\circ}C$ , except for low power mode where typical values are given for  $V_{SUP} = 12V$  at  $25^{\circ}C$ .

(2) All voltages are defined with respect to ground; positive currents flow into the SN65HVDA100 device.

(3) In the dominant state, the supply current increases as the supply voltage increases due to the integrated LIN slave termination resistance. At higher voltages the majority of supply current is through the termination resistance. The minimum resistance of the LIN slave termination is 20 k $\Omega$ , so the maximum supply current attributed to the termination is:  $I_{SUP} (dom) \max \text{ termination} \neq (V_{SUP} - (V_{LIN\_Dominant} + 0.7V)) / 20k\Omega$

(4) RXD pin output is open drain. Output voltage is via external pull up resistance to logic supply of the system and impedance of the RXD pin.

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{SUP} = 5V$  to  $27V$ ,  $T_J = -40^{\circ}C$  to  $150^{\circ}C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS / COMMENT	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>LIN Pin (Referenced to <math>V_{SUP}</math>)</b>						
7.1	$V_{OH}$	High-level output voltage	LIN recessive, TXD = high, $I_O = 0$ mA, $V_{SUP} = 14$ V		$V_{SUP} - 1$	V
7.2	$V_{OL}$	Low-level output voltage	LIN dominant, TXD = low, $I_O = 40$ mA, $V_{SUP} = 14$ V		$0.2 \times V_{SUP}$	V
7.3	$I_L$	Limiting current (LIN 2.1 Param 12)	TXD = 0 V, $V_{LIN} = 7$ V to $27$ V		40      90      200	mA
7.4	$I_{LKG}$	Receiver leakage current, dominant (LIN 2.1 Param 13)	LIN = 0 V, $7V \leq V_{SUP} \leq 18$ V, Driver off		-1	mA
7.5		Receiver leakage current, recessive (LIN 2.1 Param 14)	LIN $\geq V_{SUP}$ , $7 \leq V_{SUP} \leq 18$ V, Driver off		20	$\mu$ A
7.6			LIN = $V_{SUP}$ , driver off		-5	
7.7	$I_{LKG}$	Leakage current, loss of ground (LIN 2.1 Param 15)	GND = $V_{SUP}$ , $V_{SUP} = 12$ V, $0 V < V_{LIN} < 18$ V		-1	1 mA
7.8	$I_{LKG}$	Leakage current, loss of supply (LIN 2.1 Param 16)	$7 V < LIN \leq 12$ V, $V_{SUP} = GND$		5	$\mu$ A
7.9			$12 V < LIN \leq 18$ V, $V_{SUP} = GND$		10	
7.10	$V_{IL}$	Low-level input voltage (LIN 2.1 Param 17)	LIN dominant (including LIN dominant for wake up)		$0.4 \times V_{SUP}$	V
7.11	$V_{IH}$	High-level input voltage (LIN 2.1 Param 18)	LIN recessive		$0.6 \times V_{SUP}$	V
7.12	$V_{BUS\_CNT}$	Receiver center threshold (LIN 2.1 Param 19)	$V_{BUS\_CNT} = (V_{IL} + V_{IH}) / 2$		$0.475 \times V_{SUP}$ $0.5 \times V_{SUP}$ $0.525 \times V_{SUP}$	V
7.13	$V_{HYS}$	Hysteresis voltage (LIN 2.1 Param 20)	$V_{HYS} = (V_{IL} - V_{IH})$		$0.05 \times V_{SUP}$ $0.175 \times V_{SUP}$	V
7.14	$V_{SERIAL\_DIODE}$	Serial diode in LIN termination pull up path (LIN 2.1 Param 21)	By design and characterization		0.4      0.7      1.0	V
7.15	$R_{SLAVE}$	Pullup resistor to $V_{SUP}$ (LIN 2.1 Param 26)	Normal and standby modes		20      30      60	k $\Omega$
7.16	$R_{SLEEP}$	Pullup current source to $V_{SUP}$	Sleep mode, $V_{SUP} = 14$ V, LIN = GND		-2	-20 $\mu$ A
<b>EN Input Pin</b>						
8.1	$V_{IL}$	Low-level input voltage			-0.3	0.8 V
8.2	$V_{IH}$	High-level input voltage			2	5.5 V
8.3	$V_{hys}$	Hysteresis voltage	By design and characterization		30	500 mV
8.4		Pulldown resistor			125      350      800	k $\Omega$
8.5	$I_{IL}$	Low-level input current	EN = Low		-5	0      5 $\mu$ A
<b>INH Output Pin</b>						
9.1	$R_{DS(on)}$	On-state resistance	Between $V_{SUP}$ and INH, INH = 2-mA drive, Normal or standby mode		25	50 $\Omega$
9.2	$I_{IKG}$	Leakage current	Low-power mode, $0 < INH < V_{SUP}$		-5	0      5 $\mu$ A

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{SUP} = 5V$  to  $27V$ ,  $T_J = -40^{\circ}C$  to  $150^{\circ}C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS / COMMENT	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>NWake Input Pin</b>						
10.1	$V_{IL}$	Low-level input voltage	-0.3		$V_{SUP} - 3.3$	V
10.2	$V_{IH}$	High-level input voltage	$V_{SUP} - 1$		$V_{SUP} + 0.3$	V
10.3		Pullup current	-45	-10	-2	$\mu A$
10.4	$I_{IKG}$	Leakage current	-5	0	5	$\mu A$
<b>AC Characteristics</b>						
11.1	D1	Duty cycle 1 <sup>(5)</sup> (LIN 2.1 Param 27)	$TH_{REC(max)} = 0.744 \times V_{SUP}$ , $TH_{DOM(max)} = 0.581 \times V_{SUP}$ , $V_{SUP} = 7V$ to $18V$ , $t_{BIT} = 50 \mu s$ (20 kbps), $D1 = t_{Bus\_rec(min)} / (2 \times t_{BIT})$ (see Figure 9)		0.396	
11.2	D2	Duty cycle 2 <sup>(5)</sup> (LIN 2.1 Param 28)	$TH_{REC(min)} = 0.422 \times V_{SUP}$ , $TH_{DOM(min)} = 0.284 \times V_{SUP}$ , $V_{SUP} = 7.6V$ to $18V$ , $t_{BIT} = 50 \mu s$ (20 kbps), $D2 = t_{Bus\_rec(max)} / (2 \times t_{BIT})$ (see Figure 9)			0.581
11.3	D3	Duty cycle 3 <sup>(5)</sup> (LIN 2.1 Param 29)	$TH_{REC(max)} = 0.778 \times V_{SUP}$ , $TH_{DOM(max)} = 0.616 \times V_{SUP}$ , $V_{SUP} = 7V$ to $18V$ , $t_{BIT} = 96 \mu s$ (10.4 kbps), $D3 = t_{Bus\_rec(min)} / (2 \times t_{BIT})$ (see Figure 9)		0.417	
11.4	D4	Duty cycle 4 <sup>(5)</sup> (LIN 2.1 Param 30)	$TH_{REC(min)} = 0.389 \times V_{SUP}$ , $TH_{DOM(min)} = 0.251 \times V_{SUP}$ , $V_{SUP} = 7.6V$ to $18V$ , $t_{BIT} = 96 \mu s$ (10.4 kbps), $D4 = t_{Bus\_rec(max)} / (2 \times t_{BIT})$ (see Figure 9)			0.59
11.5	$t_{rx\_pdr}$	Receiver rising propagation delay time (LIN 2.1 Param 31)	$R_{RXD} = 2.4 k\Omega$ , $C_{RXD} = 20 pF$ (see Figure 10 and Figure 11)			6 $\mu s$
11.6	$t_{rx\_pdf}$	Receiver falling propagation delay time (LIN 2.1 Param 31)	$R_{RXD} = 2.4 k\Omega$ , $C_{RXD} = 20 pF$ (see Figure 10 and Figure 11)			6 $\mu s$
11.7	$t_{rx\_sym}$	Symmetry of receiver propagation delay time (LIN 2.1 Param 32)	Rising edge with respect to falling edge $(t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdr})$ $R_{RXD} = 2.4 k\Omega$ , $C_{RXD} = 20 pF$ (see Figure 10 and Figure 11)		-2	2 $\mu s$
11.8	$t_{NWake}$	NWake filter time for local wake-up	See Figure 6		25	50 150 $\mu s$
11.9	$t_{LINBUS}$	LIN wake-up time (Minimum dominant time on LIN bus for wake-up)	See Figure 7, Figure 8, and Figure 5		25	100 150 $\mu s$

(5) Duty cycles: LIN driver bus load conditions ( $C_{LINBUS}$ ,  $R_{LINBUS}$ ): Load1 = 1 nF, 1 k $\Omega$ ; Load2 = 10 nF, 500  $\Omega$ . Duty cycles 3 and 4 are defined for 10.4-kbps operation. The SN65HVDA100 also meets these lower data rate requirements, while it is capable of the higher speed 20-kbps operation as specified by duty cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details see the SAEJ2602 specification.

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{SUP} = 5V$  to  $27V$ ,  $T_J = -40^{\circ}C$  to  $150^{\circ}C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS / COMMENT	MIN	TYP <sup>(1)</sup>	MAX	UNIT
11.10	t <sub>CLEAR</sub>	Time to clear false wake-up prevention logic if LIN Bus had bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	8	17	50	μs
11.11	t <sub>DST</sub>	Dominant state timeout <sup>(6)</sup>	20	34	80	ms
11.12	t <sub>MODE_CHANGE</sub>	Mode change delay time			5	μs
		Time to change from standby mode to normal mode or normal mode to sleep mode via EN pin				

- (6) TXD Dominant state timeout limits the minimum data rate to 650bps. The minimum datarates may be calculated by the following formulas.  $DataRate_{Master(min)} = t_{SYNC\_DOM(max)} / t_{DST(min)}$  and  $DataRate_{Slave(min)} = 9 + n_{margin} / t_{DST(min)}$  where  $n_{margin}$  is a safety margin. For slave node cases where  $n_{margin} \leq 4$ , the master node case will be the limiting calculation.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		SN65HVDA100-Q1		UNITS
		D (8 PINS)		
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	112.5		°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	66.3		
θ <sub>JB</sub>	Junction-to-board thermal resistance	52.9		
ψ <sub>JT</sub>	Junction-to-top characterization parameter	19.3		
ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.4		
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	N/A		
	Thermal shutdown temperature	180		°C
	Thermal shutdown hysteresis	15		°C
P <sub>D</sub>	Power Dissipation in normal mode (dominant)	Typ 17	Max 230	mW

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

TIMING DIAGRAMS

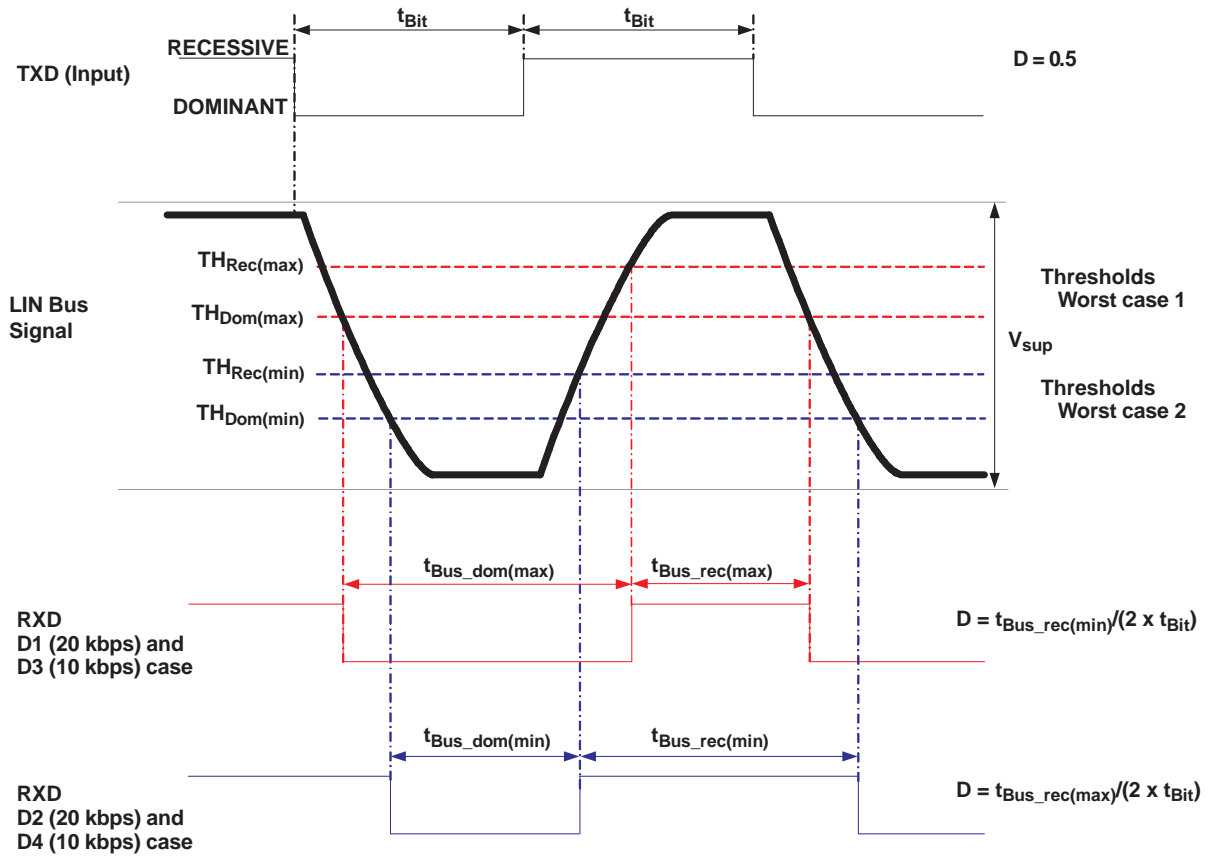


Figure 9. Definition of Bus Timing Parameters



TIMING DIAGRAMS (continued)

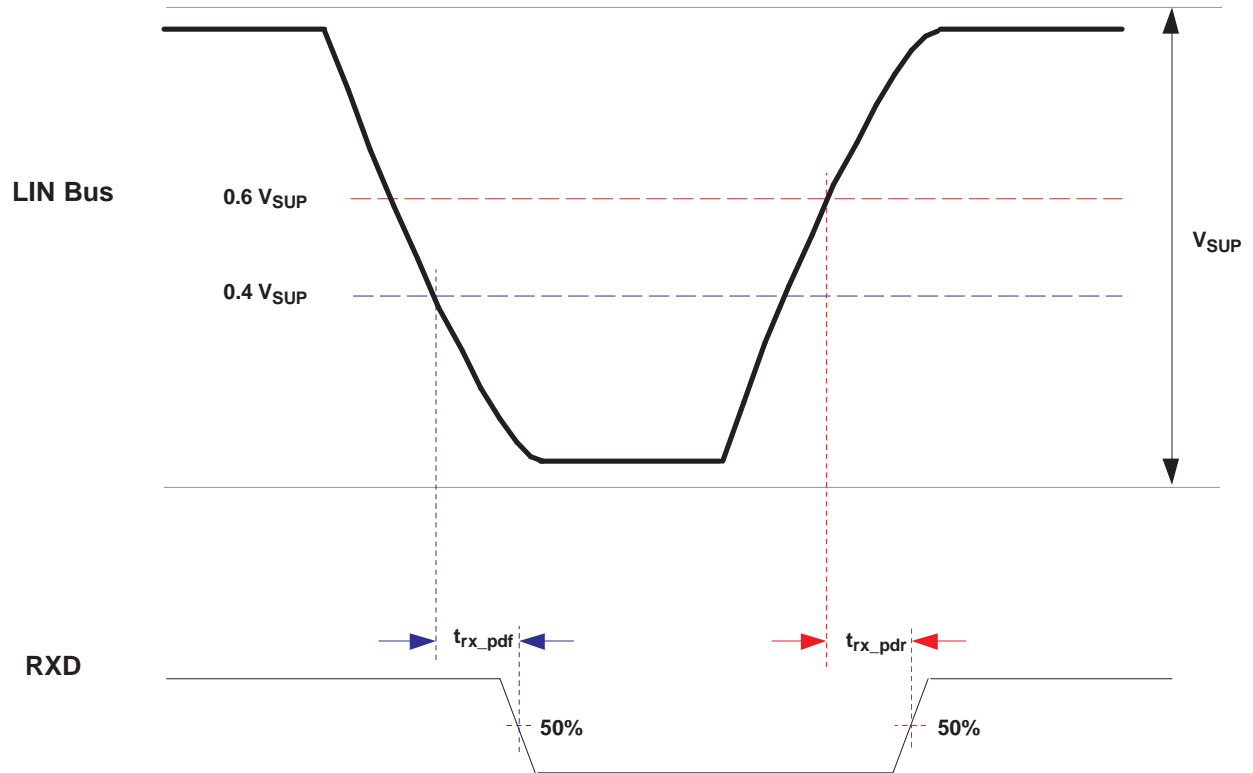


Figure 10. Propagation Delay

TIMING DIAGRAMS (continued)

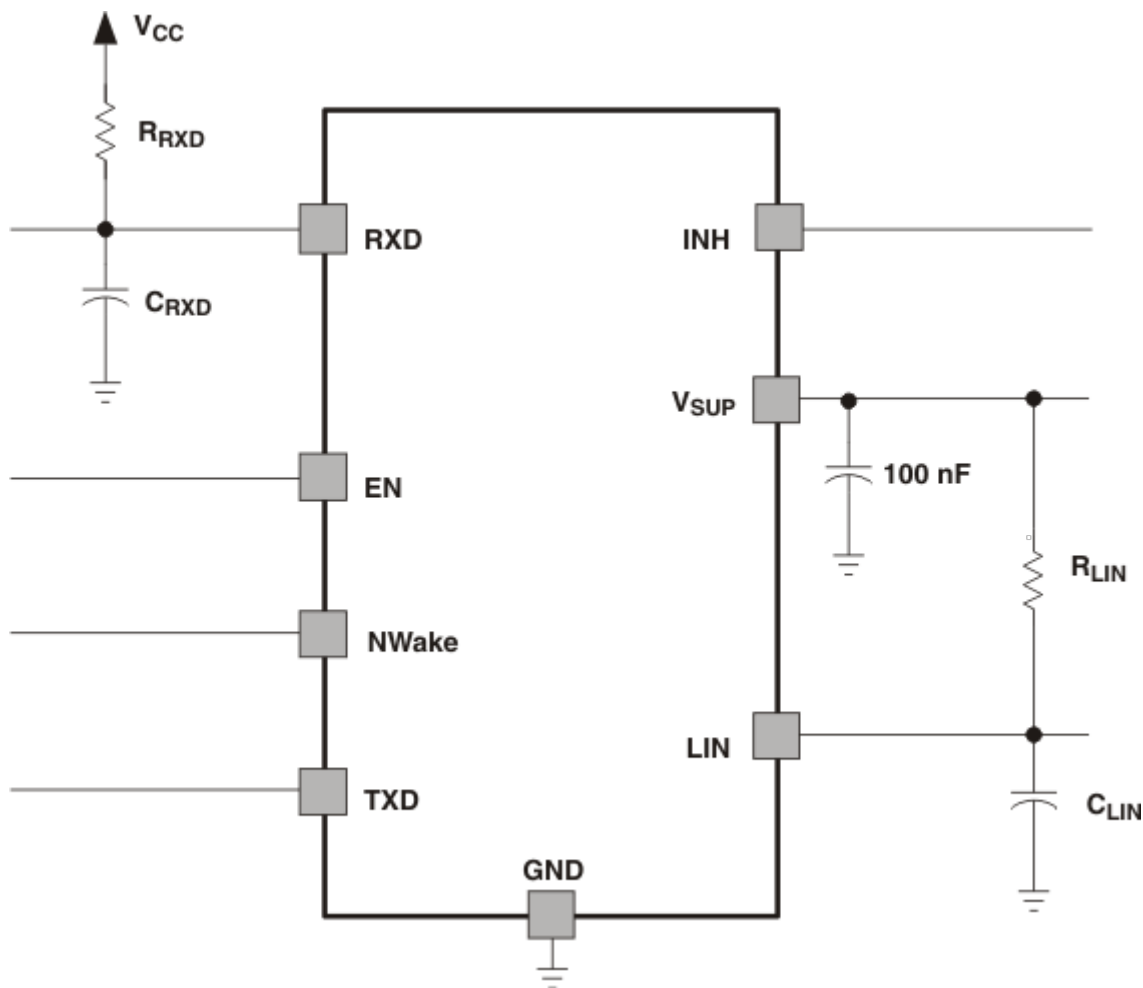
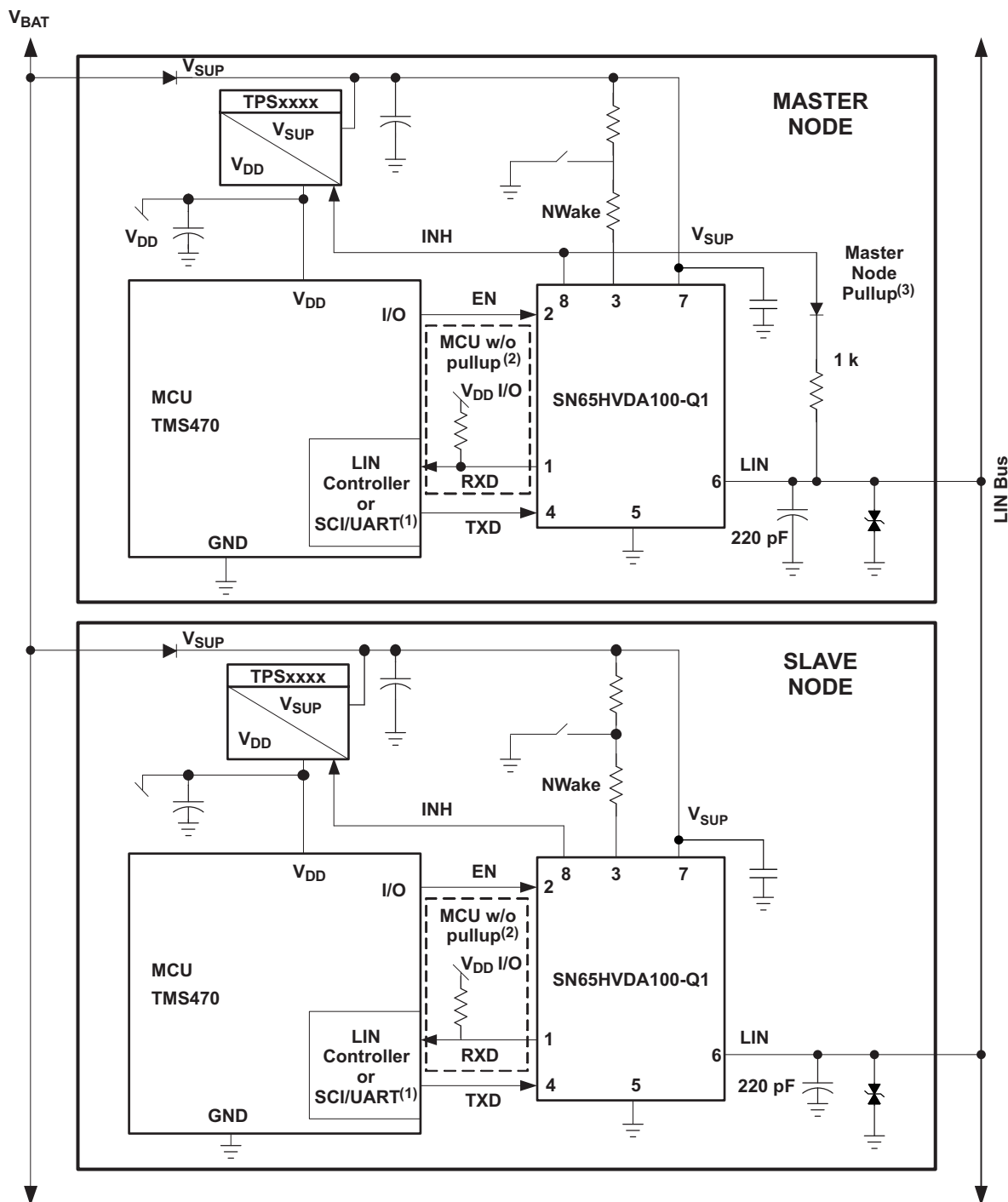


Figure 11. Test Circuit for AC Characteristics

APPLICATION INFORMATION



- (1) RXD on MCU or LIN slave has internal pullup, no external pullup resistor is needed.
- (2) RXD on MCU or LIN slave without internal pullup, requires external pullup resistor.
- (3) Master node applications require an external 1-kΩ pullup resistor and serial diode.

Figure 12. SN65HVDA100-Q1 Application Diagram

## Device Comparison: TPIC1021 versus SN65HVDA100

The SN65HVDA100 is pin-to-pin compatible to the TPIC1021 device. The SN65HVDA100 is an enhanced LIN transceiver, including enhanced immunity to RF disturbances. [Table 2](#) is a summary of the differences between the two devices.

**Table 2. SN65HVDA100 versus TPIC1021 Differences**

SPECIFICATION	SN65HVDA100	TPIC1021
LIN termination	Weak current pullup in sleep mode	High $\Omega$ in low-power mode
LIN receiver	Enhanced high-speed receive capable	High-speed receive capable
LIN leakage current (unpowered device): $7\text{ V} < \text{LIN} < 12\text{ V}$ , $V_{\text{SUP}} = \text{GND}$	$<5\ \mu\text{A}$ at 12 V (max)	$<10\ \mu\text{A}$ at 12 V (typ)
LIN bus wake-up	Remote wake-up via recessive-to-dominant transition on LIN bus where dominant bus state is held for at least $t_{\text{LINBUS}}$ time followed by a transition back to the recessive state	Remote wake-up via recessive-to-dominant transition on LIN bus where dominant bus state is held for at least $t_{\text{LINBUS}}$ time
Low-power current	$<20\ \mu\text{A}$ at 14 V (max)	$<50\ \mu\text{A}$ at 14 V (max)
INH pin	Enhanced driving of bus master termination via lower $R_{\text{on}}$	Driving of bus master termination
Source wake up recognition (TXD pin)	TXD pin reflects the source of the wake-up event (LIN or NWake)	Not applicable
Default power up state	Standby mode	Sleep mode

## REVISION HISTORY

<b>Changes from Revision A (January 2013) to Revision B</b>	<b>Page</b>
• Ordered PIN ASSIGNMENTS table alphabetically by pin name .....	2
• Changed "Application Note" to "Application Hint" .....	6
• Added new Mode Transitions section, including a new figure .....	7
• Revised the application schematic diagram .....	19

<b>Changes from Original (November 2011) to Revision A</b>	<b>Page</b>
• Added 1.4 row to the abs max table by copying from the 9.2 row in the elec char table .....	11
• Deleted -03V to 45V from the 1.5 row in the abs max table, units column .....	11
• Changed added Delta and corrected Hysteresis in elec chara table, row 4.4 and changed the TYP column from 4.5 to 0.2 .....	12
• Deleted rows 9.1 and 9.2 from the elec chara table .....	13
• Added Minimum to the statement in parens in front of dominant, row 11.9 of elec chara table .....	14

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVDA100QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	A100Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVDA100QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVDA100QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
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  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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