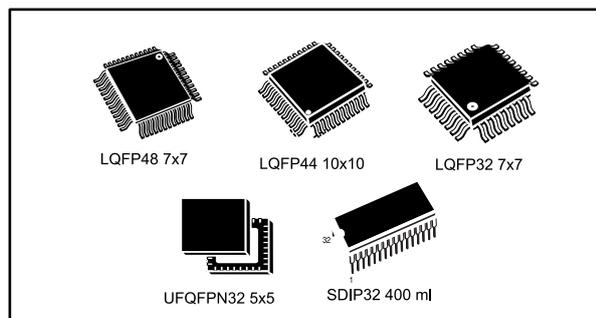


Access line, 16 MHz STM8S 8-bit MCU, up to 32 Kbytes Flash, integrated EEPROM, 10-bit ADC, timers, UART, SPI, I²C

Datasheet - production data



Features

Core

- 16 MHz advanced STM8 core with Harvard architecture and 3-stage pipeline
- Extended instruction set

Memories

- Medium-density Flash/EEPROM:
 - Program memory up to 32 Kbytes; data retention 20 years at 55°C after 10 kcycles
 - Data memory up to 1 Kbytes true data EEPROM; endurance 300 kcycles
- RAM: Up to 2 Kbytes

Clock, reset and supply management

- 2.95 V to 5.5 V operating voltage
- Flexible clock control, 4 master clock sources:
 - Low power crystal resonator oscillator
 - External clock input
 - Internal, user-trimmable 16 MHz RC
 - Internal low power 128 kHz RC
- Clock security system with clock monitor
- Power management:
 - Low power modes (wait, active-halt, halt)
 - Switch-off peripheral clocks individually
- Permanently active, low consumption power-on and power-down reset

Interrupt management

- Nested interrupt controller with 32 interrupts
- Up to 37 external interrupts on 6 vectors

Timers

- 2x 16-bit general purpose timers, with 2+3 CAPCOM channels (IC, OC or PWM)
- Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
- 8-bit basic timer with 8-bit prescaler
- Auto wake-up timer
- Window and independent watchdog timers

Communications interfaces

- UART with clock output for synchronous operation, Smartcard, IrDA, LIN
- SPI interface up to 8 Mbit/s
- I²C interface up to 400 Kbit/s

Analog-to-digital converter (ADC)

- 10-bit, ± 1 LSB ADC with up to 10 multiplexed channels, scan mode and analog watchdog

I/Os

- Up to 38 I/Os on a 48-pin package including 16 high sink outputs
- Highly robust I/O design, immune against current injection

Development support

- Embedded single wire interface module (SWIM) for fast on-chip programming and non-intrusive debugging

Unique ID

- 96-bit unique key for each device

Table 1: Device summary

| Reference | Part number |
|------------|--|
| STM8S105xx | STM8S105K4, STM8S105K6, STM8S105S4, STM8S105S6, STM8S105C4, STM8S105C6 |

Contents

| | | |
|----------|--|-----------|
| 1 | Introduction..... | 8 |
| 2 | Description..... | 9 |
| 3 | Block diagram..... | 10 |
| 4 | Product overview..... | 11 |
| 4.1 | Single wire interface module (SWIM) and debug module (DM)..... | 11 |
| 4.2 | Interrupt controller | 12 |
| 4.3 | Flash program and data EEPROM memory..... | 12 |
| 4.4 | Clock controller | 13 |
| 4.5 | Power management | 14 |
| 4.6 | Watchdog timers | 14 |
| 4.7 | Auto wakeup counter | 15 |
| 4.8 | Beeper | 15 |
| 4.9 | TIM1 - 16-bit advanced control timer..... | 15 |
| 4.10 | TIM2, TIM3 - 16-bit general purpose timers | 15 |
| 4.11 | TIM4 - 8-bit basic timer | 16 |
| 4.12 | Analog-to-digital converter (ADC1) | 16 |
| 4.13 | Communication interfaces..... | 17 |
| 4.13.1 | UART2..... | 17 |
| 4.13.2 | SPI..... | 17 |
| 4.13.3 | I ² C..... | 18 |
| 5 | Pinout and pin description | 19 |
| 5.1 | STM8S105 pinouts and pin description..... | 19 |
| 5.1.1 | Alternate function remapping | 24 |
| 6 | Memory and register map..... | 25 |
| 6.1 | Memory map | 25 |
| 6.2 | Register map..... | 26 |
| 6.2.1 | I/O port hardware register map | 26 |
| 6.2.2 | General hardware register map..... | 27 |
| 6.2.3 | CPU/SWIM/debug module/interrupt controller registers | 34 |
| 7 | Interrupt vector mapping | 36 |
| 8 | Option bytes..... | 37 |
| 9 | Unique ID..... | 41 |

| | | |
|-----------|---|-----------|
| 10 | Electrical characteristics | 42 |
| 10.1 | Parameter conditions | 42 |
| 10.1.1 | Minimum and maximum values | 42 |
| 10.1.2 | Typical values..... | 42 |
| 10.1.3 | Typical curves..... | 42 |
| 10.1.4 | Typical current consumption | 42 |
| 10.1.5 | Loading capacitor | 43 |
| 10.1.6 | Pin input voltage | 43 |
| 10.2 | Absolute maximum ratings | 43 |
| 10.3 | Operating conditions | 45 |
| 10.3.1 | VCAP external capacitor | 46 |
| 10.3.2 | Supply current characteristics | 47 |
| 10.3.3 | External clock sources and timing characteristics..... | 56 |
| 10.3.4 | Internal clock sources and timing characteristics..... | 58 |
| 10.3.5 | Memory characteristics..... | 60 |
| 10.3.6 | I/O port pin characteristics..... | 61 |
| 10.3.7 | Typical output level curves | 64 |
| 10.3.8 | Reset pin characteristics | 68 |
| 10.3.9 | SPI serial peripheral interface | 70 |
| 10.3.10 | I2C interface characteristics | 73 |
| 10.3.11 | 10-bit ADC characteristics..... | 74 |
| 10.3.12 | EMC characteristics..... | 77 |
| 11 | Package information | 80 |
| 11.1 | 48-pin LQFP package mechanical data | 80 |
| 11.2 | 44-pin LQFP package mechanical data | 81 |
| 11.3 | 32-pin LQFP package mechanical data | 82 |
| 11.4 | 32-lead UFQFPN package mechanical data..... | 84 |
| 11.5 | SDIP32 package mechanical data | 85 |
| 12 | Thermal characteristics | 87 |
| 12.1 | Reference document..... | 87 |
| 12.2 | Selecting the product temperature range | 87 |
| 13 | Ordering information..... | 89 |
| 14 | STM8S105 FASTROM microcontroller option list | 90 |
| 15 | STM8 development tools | 94 |
| 15.1 | Emulation and in-circuit debugging tools..... | 94 |

| | | |
|-----------|---------------------------------|-----------|
| 15.2 | Software tools | 94 |
| 15.2.1 | STM8 toolset | 94 |
| 15.2.2 | C and assembly toolchains | 95 |
| 15.3 | Programming tools | 95 |
| 16 | Revision history | 96 |
| 17 | Disclaimer | 99 |

List of tables

| | |
|--|----|
| Table 1: Device summary | 1 |
| Table 2: STM8S105xx access line features | 9 |
| Table 3: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers | 14 |
| Table 4: TIM timer features..... | 16 |
| Table 5: Legend/abbreviations for pinout tables..... | 19 |
| Table 6: Pin description for STM8S105 microcontrollers | 22 |
| Table 7: Flash, Data EEPROM and RAM boundary addresses | 26 |
| Table 8: I/O port hardware register map..... | 26 |
| Table 9: General hardware register map | 27 |
| Table 10: CPU/SWIM/debug module/interrupt controller registers | 34 |
| Table 11: Interrupt mapping..... | 36 |
| Table 12: Option bytes..... | 37 |
| Table 13: Option byte description | 38 |
| Table 14: Description of alternate function remapping bits [7:0] of OPT2..... | 39 |
| Table 15: Unique ID registers (96 bits) | 41 |
| Table 16: Voltage characteristics..... | 43 |
| Table 17: Current characteristics..... | 44 |
| Table 18: Thermal characteristics..... | 45 |
| Table 19: General operating conditions..... | 45 |
| Table 20: Operating conditions at power-up/power-down | 46 |
| Table 21: Total current consumption with code execution in run mode at VDD = 5 V | 47 |
| Table 22: Total current consumption with code execution in run mode at VDD = 3.3 V | 48 |
| Table 23: Total current consumption in wait mode at VDD = 5 V..... | 49 |
| Table 24: Total current consumption in wait mode at VDD = 3.3 V..... | 49 |
| Table 25: Total current consumption in active halt mode at VDD = 5 V..... | 50 |
| Table 26: Total current consumption in active halt mode at VDD = 3.3 V..... | 51 |
| Table 27: Total current consumption in halt mode at VDD = 5 V | 51 |
| Table 28: Total current consumption in halt mode at VDD = 3.3 V | 52 |
| Table 29: Wakeup times | 52 |
| Table 30: Total current consumption and timing in forced reset state..... | 53 |
| Table 31: Peripheral current consumption..... | 53 |
| Table 32: HSE user external clock characteristics | 56 |
| Table 33: HSE oscillator characteristics | 56 |
| Table 34: HSI oscillator characteristics..... | 58 |
| Table 35: LSI oscillator characteristics | 59 |
| Table 36: RAM and hardware registers..... | 60 |
| Table 37: Flash program memory/data EEPROM memory..... | 60 |
| Table 38: I/O static characteristics..... | 61 |
| Table 39: Output driving current (standard ports)..... | 63 |
| Table 40: Output driving current (true open drain ports) | 63 |
| Table 41: Output driving current (high sink ports) | 63 |
| Table 42: NRST pin characteristics | 68 |
| Table 43: SPI characteristics | 71 |
| Table 44: I2C characteristics | 73 |
| Table 45: ADC characteristics | 74 |
| Table 46: ADC accuracy with RAIN < 10 k Ω , VDDA= 5 V | 75 |
| Table 47: ADC accuracy with RAIN < 10 k Ω RAIN, VDDA = 3.3 V..... | 76 |
| Table 48: EMS data | 78 |
| Table 49: EMI data..... | 78 |
| Table 50: ESD absolute maximum ratings | 79 |
| Table 51: Electrical sensitivities..... | 79 |
| Table 52: 48-pin low profile quad flat package mechanical data..... | 80 |
| Table 53: 44-pin low profile quad flat package mechanical data..... | 81 |

| | |
|---|----|
| Table 54: 32-pin low profile quad flat package mechanical data..... | 82 |
| Table 55: 32-lead ultra thin fine pitch quad flat no-lead package mechanical data | 84 |
| Table 56: 32-lead shrink plastic DIP (400 ml) package mechanical data..... | 86 |
| Table 57: Thermal characteristics (1) | 87 |
| Table 58: Document revision history | 96 |

List of figures

| | |
|--|----|
| Figure 1: STM8S105xx access line block diagram..... | 10 |
| Figure 2: Flash memory organization | 13 |
| Figure 3: LQFP 48-pin pinout | 19 |
| Figure 4: LQFP 44-pin pinout | 20 |
| Figure 5: LQFP/UFQFPN 32-pin pinout..... | 21 |
| Figure 6: SDIP 32-pin pinout | 21 |
| Figure 7: Memory map..... | 25 |
| Figure 8: Supply current measurement conditions | 42 |
| Figure 9: Pin loading conditions..... | 43 |
| Figure 10: Pin input voltage | 43 |
| Figure 11: fCPU _{max} versus VDD | 46 |
| Figure 12: External capacitor CEXT | 47 |
| Figure 13: Typ. IDD(RUN) vs. VDD, HSE user external clock, fCPU = 16 MHz | 54 |
| Figure 14: Typ. IDD(RUN) vs. fCPU, HSE user external clock, VDD= 5 V | 54 |
| Figure 15: Typ. IDD(RUN) vs. VDD, HSI RC osc, fCPU = 16 MHz..... | 54 |
| Figure 16: Typ. IDD(WFI) vs. VDD, HSE user external clock, fCPU = 16 MHz | 55 |
| Figure 17: Typ. IDD(WFI) vs. fCPU, HSE user external clock VDD = 5 V | 55 |
| Figure 18: Typ. IDD(WFI) vs. VDD, HSI RC osc, fCPU = 16 MHz | 55 |
| Figure 19: HSE external clocksource | 56 |
| Figure 20: HSE oscillator circuit diagram..... | 57 |
| Figure 21: Typical HSI accuracy at VDD = 5 V vs 5 temperatures..... | 58 |
| Figure 22: Typical HSI accuracy vs VDD @ 4 temperatures | 59 |
| Figure 23: Typical LSI accuracy vs VDD @ 4 temperatures | 59 |
| Figure 24: Typical VIL and VIH vs VDD @ 4 temperatures | 62 |
| Figure 25: Typical pull-up resistance vs VDD @ 4 temperatures..... | 62 |
| Figure 26: Typical pull-up current vs VDD @ 4 temperatures..... | 63 |
| Figure 27: Typ. VOL @ VDD = 5 V (standard ports) | 64 |
| Figure 28: Typ. VOL @ VDD = 3.3 V (standard ports)..... | 65 |
| Figure 29: Typ. VOL @ VDD = 5 V (true open drain ports)..... | 65 |
| Figure 30: Typ. VOL @ VDD = 3.3 V (true open drain ports)..... | 66 |
| Figure 31: Typ. VOL @ VDD = 5 V (high sink ports)..... | 66 |
| Figure 32: Typ. VOL @ VDD = 3.3 V (high sink ports)..... | 67 |
| Figure 33: Typ. VDD - VOH @ VDD = 5 V (standard ports)..... | 67 |
| Figure 34: Typ. VDD - VOH @ VDD = 3.3 V (standard ports)..... | 67 |
| Figure 35: Typ. VDD - VOH @ VDD = 5 V (high sink ports) | 68 |
| Figure 36: Typ. VDD - VOH @ VDD = 3.3 V (high sink ports) | 68 |
| Figure 37: Typical NRST VIL and VIH vs VDD @ 4 temperatures..... | 69 |
| Figure 38: Typical NRST pull-up resistance vs VDD @ 4 temperatures..... | 69 |
| Figure 39: Typical NRST pull-up current vs VDD @ 4 temperatures | 70 |
| Figure 40: Recommended reset pin protection | 70 |
| Figure 41: SPI timing diagram - slave mode and CPHA = 0 | 72 |
| Figure 42: SPI timing diagram - slave mode and CPHA = 1(1)..... | 72 |
| Figure 43: SPI timing diagram - master mode(1) | 73 |
| Figure 44: Typical application with I2C bus and timing diagram (1)..... | 74 |
| Figure 45: ADC accuracy characteristics..... | 76 |
| Figure 46: Typical application with ADC | 77 |
| Figure 47: 48-pin low profile quad flat package (7 x 7)..... | 80 |
| Figure 48: 44-pin low profile quad flat package | 81 |
| Figure 49: 32-pin low profile quad flat package (7 x 7)..... | 82 |
| Figure 50: 32-lead, ultra thin, fine pitch quad flat no-lead package (5 x 5) | 84 |
| Figure 51: 32-lead shrink plastic DIP (400 ml) package..... | 85 |
| Figure 52: STM8S105xx access line ordering information scheme | 89 |

1 Introduction

This datasheet contains the description of the device features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8S105xx access line 8-bit microcontrollers offer from 16 to 32 Kbytes Flash program memory, plus integrated true data EEPROM. They are referred to as medium-density devices in the STM8S microcontroller family reference manual (RM0016).

All devices of the STM8S105xx access line provide the following benefits: reduced system cost, performance and robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300k write/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Device performance is ensured by a 16 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

Short development cycles are guaranteed due to application scalability across common family product architecture with compatible pinout, memory map and modular peripherals. Full documentation is offered with a wide choice of development tools.

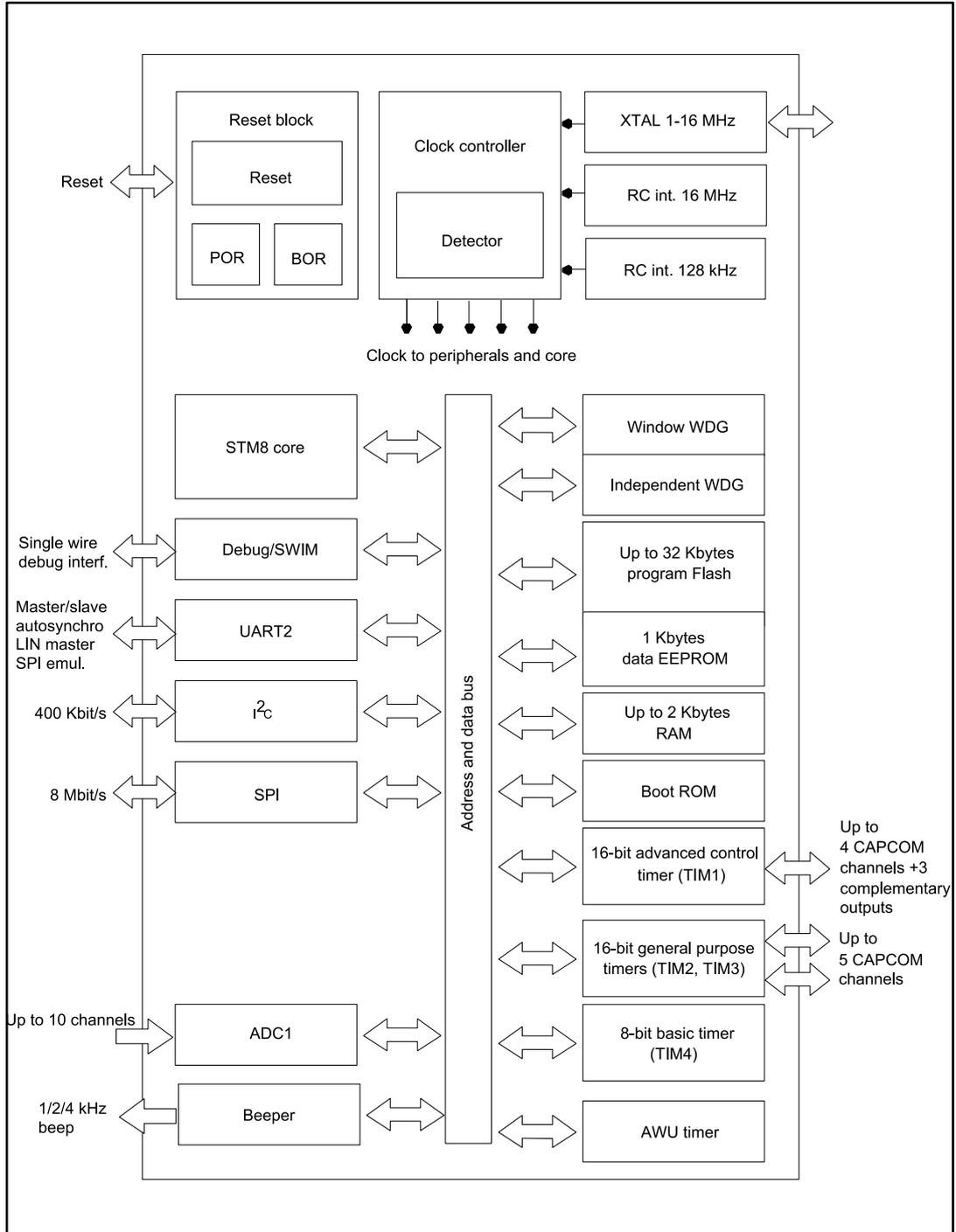
Product longevity is ensured in the STM8S family thanks to their advanced core which is made in a state-of-the art technology for applications with 2.95 V to 5.5 V operating supply.

Table 2: STM8S105xx access line features

| Device | STM8S105C6 | STM8S105C4 | STM8S105S6 | STM8S105S4 | STM8S105K6 | STM8S105K4 |
|---|---|------------|------------|------------|------------|------------|
| Pin count | 48 | 48 | 44 | 44 | 32 | 32 |
| Maximum number of GPIOs | 38 | 38 | 34 | 34 | 25 | 25 |
| Ext. Interrupt pins | 35 | 35 | 31 | 31 | 23 | 23 |
| Timer CAPCOM channels | 9 | 9 | 8 | 8 | 8 | 8 |
| Timer complementary outputs | 3 | 3 | 3 | 3 | 3 | 3 |
| A/D Converter channels | 10 | 10 | 9 | 9 | 7 | 7 |
| High sink I/Os | 16 | 16 | 15 | 15 | 12 | 12 |
| Medium density Flash Program memory (bytes) | 32K | 16K | 32K | 16K | 32K | 16K |
| Data EEPROM (bytes) | 1024 | 1024 | 1024 | 1024 | 1024 | 1024 |
| RAM (bytes) | 2K | 2K | 2K | 2K | 2K | 2K |
| Peripheral set | Advanced control timer (TIM1), General-purpose timers (TIM2 and TIM3), Basic timer (TIM4) SPI, I ² C, UART, Window WDG, Independent WDG, ADC | | | | | |

3 Block diagram

Figure 1: STM8S105xx access line block diagram



4 Product overview

The following section intends to give an overview of the basic features of the device functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

4.1 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

4.2 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 37 external interrupts on 6 vectors including TLI
- Trap and reset interrupts

4.3 Flash program and data EEPROM memory

- Up to 32 Kbytes of Flash program single voltage Flash memory
- Up to 1 Kbytes true data EEPROM
- Read while write: Writing in data memory possible while executing code in program memory
- User option byte area

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to the figure below.

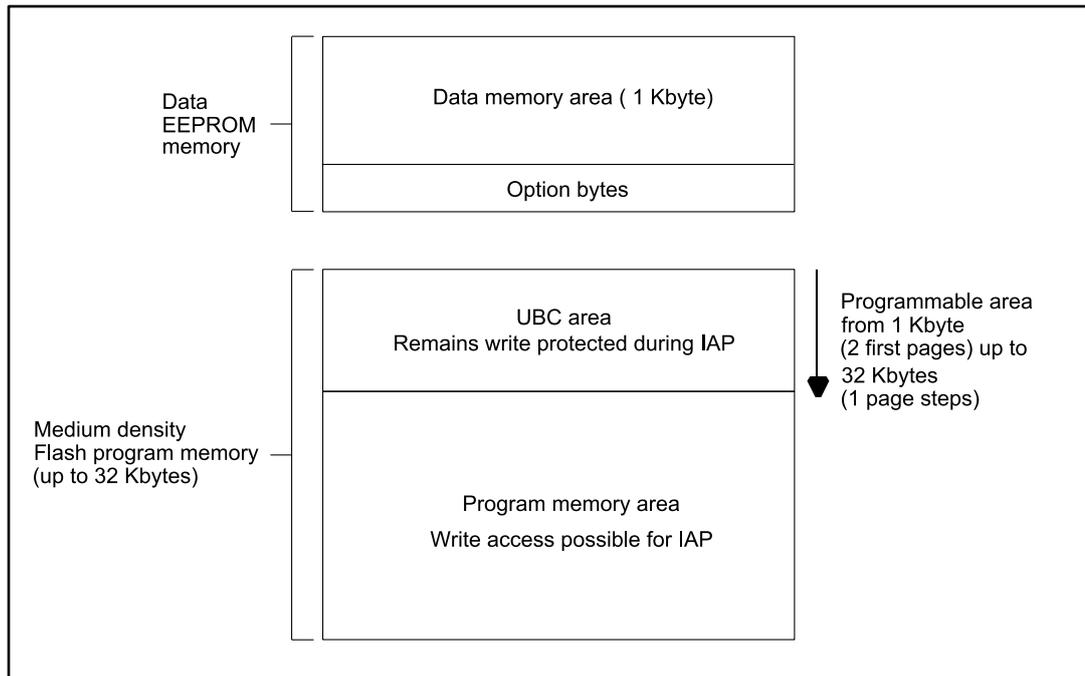
The size of the UBC is programmable through the UBC option byte, in increments of 1 page (512 bytes) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 32 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 32 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2: Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.4 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** Four different clock sources can be used to drive the master clock:
 - 1-16 MHz high-speed external crystal (HSE)
 - Up to 16 MHz high-speed user-external clock (HSE user-ext)
 - 16 MHz high-speed internal RC oscillator (HSI)
 - 128 kHz low-speed internal RC (LSI)

- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 3: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

| Bit | Peripheral clock |
|---------|------------------|---------|------------------|---------|------------------|---------|------------------|
| PCKEN17 | TIM1 | PCKEN13 | UART2 | PCKEN27 | Reserved | PCKEN23 | ADC |
| PCKEN16 | TIM3 | PCKEN12 | Reserved | PCKEN26 | Reserved | PCKEN22 | AWU |
| PCKEN15 | TIM2 | PCKEN11 | SPI | PCKEN25 | Reserved | PCKEN21 | Reserved |
| PCKEN14 | TIM4 | PCKEN10 | I ² C | PCKEN24 | Reserved | PCKEN20 | Reserved |

4.5 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode:** In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active halt mode with regulator on:** In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active halt mode with regulator off:** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode :** In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.6 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 μ s up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 μ s to 1 s.

4.7 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM3 input capture channel 1 for calibration

4.8 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.9 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.10 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1...32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

4.11 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 4: TIM timer features

| Timer | Counter size (bits) | Prescaler | Counting mode | CAPCOM channels | Complem. outputs | Ext. trigger | Timer synchronization/chaining |
|-------|---------------------|--------------------------------|---------------|-----------------|------------------|--------------|--------------------------------|
| TIM1 | 16 | Any integer from 1 to 65536 | Up/Down | 4 | 3 | Yes | No |
| TIM2 | 16 | Any power of 2 from 1 to 32768 | Up | 3 | 0 | No | |
| TIM3 | 16 | Any power of 2 from 1 to 32768 | Up | 2 | 0 | No | |
| TIM4 | 8 | Any power of 2 from 1 to 128 | Up | 0 | 0 | No | |

4.12 Analog-to-digital converter (ADC1)

The STM8S105xx products contain a 10-bit successive approximation A/D converter (ADC1) with up to 10 multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DD}
- Input voltage range: 0 to V_{DDA}
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size ($n \times 10$ bits) where n = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt



Additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC_DRH/ADC_DRL registers.

4.13 Communication interfaces

The following communication interfaces are implemented:

- UART2: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, LIN2.1 master/slave capability
- SPI : Full and half-duplex, 8 Mbit/s
- I²C: Up to 400 Kbit/s

4.13.1 UART2

Main features

- One Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- LIN slave mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s ($f_{CPU}/16$) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
 - Address bit (MSB)
 - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz ($f_{CPU}/16$)

LIN master mode

- Emission: Generates 13-bit synch break frame
- Reception: Detects 11-bit break frame

LIN slave mode

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation $\pm 15\%$
- Synch delimiter checking
- 11-bit LIN synch break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

4.13.2 SPI

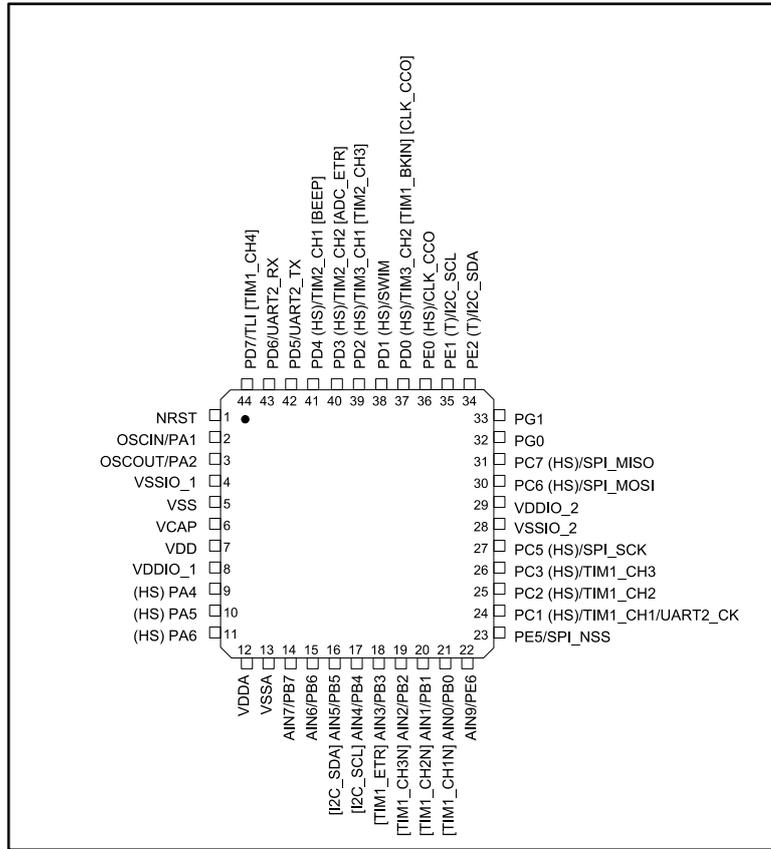
- Maximum speed: 8 Mbit/s ($f_{MASTER}/2$) both for master and slave
- Full duplex synchronous transfers

- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

4.13.3 I²C

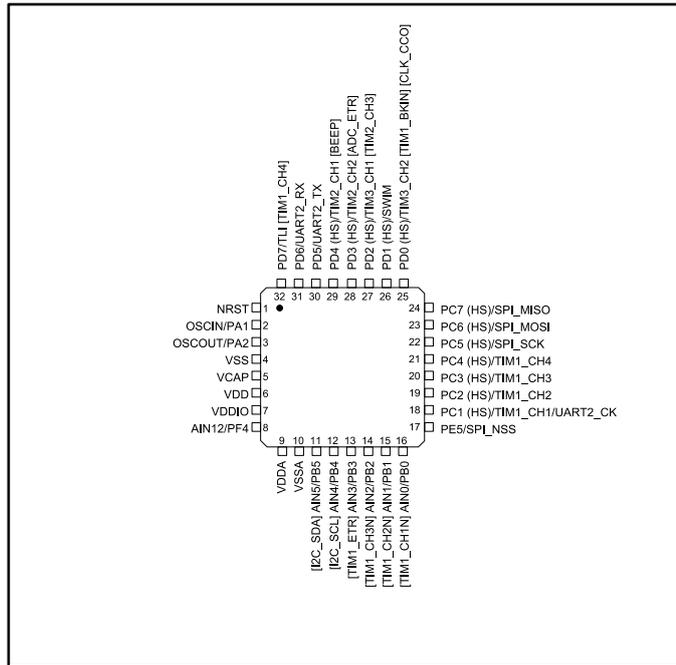
- I²C master features:
 - Clock generation
 - Start and stop generation
- I²C slave features:
 - Programmable I2C address detection
 - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
 - Standard speed (up to 100 kHz)
 - Fast speed (up to 400 kHz)

Figure 4: LQFP 44-pin pinout



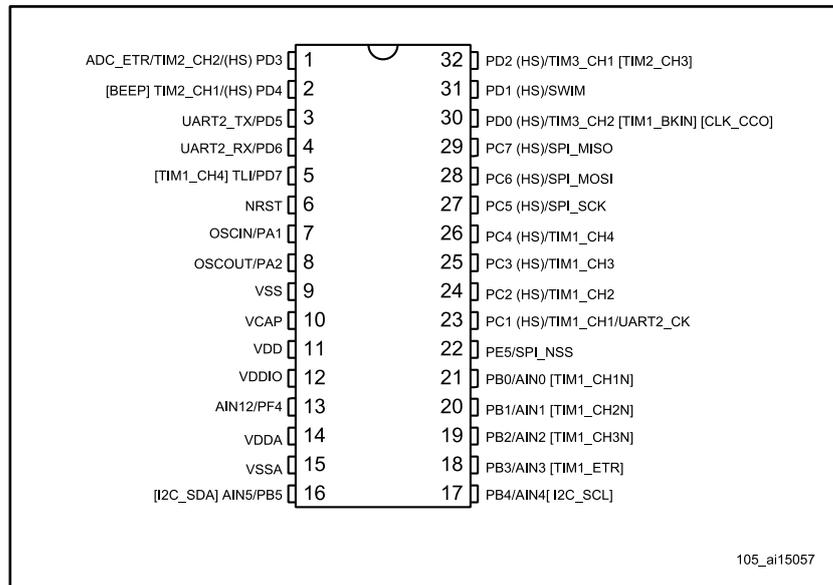
1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 5: LQFP/UFQFPN 32-pin pinout



1. (HS) high sink capability.
2. [] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 6: SDIP 32-pin pinout



105_ai15057

1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6: Pin description for STM8S105 microcontrollers

| Pin number | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|------------|--------|-----------------|--------|-------------------------------------|------|----------|-----|----------------|-----------|-------|----|---------|--------------------------------|---|---|
| LQFP48 | LQFP44 | LQFP32/UFQFPN32 | SDIP32 | | | floating | wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 1 | 1 | 1 | 6 | NRST | I/O | | X | | | | | | Reset | | |
| 2 | 2 | 2 | 7 | PA1/ OSC IN | I/O | X | X | | O1 | X | X | Port A1 | Resonator crystal in | | |
| 3 | 3 | 3 | 8 | PA2/ OSC OUT | I/O | X | X | X | O1 | X | X | Port A2 | Resonator crystal out | | |
| 4 | 4 | - | - | V _{SSIO_1} | S | | | | | | | | I/O ground | | |
| 5 | 5 | 4 | 9 | V _{SS} | S | | | | | | | | Digital ground | | |
| 6 | 6 | 5 | 10 | VCAP | S | | | | | | | | 1.8 V regulator capacitor | | |
| 7 | 7 | 6 | 11 | V _{DD} | S | | | | | | | | Digital power supply | | |
| 8 | 8 | 7 | 12 | V _{DDIO_1} | S | | | | | | | | I/O power supply | | |
| 9 | - | - | - | PA3/ TIM2_CH3 [TIM3_CH1] | I/O | X | X | X | O1 | X | X | Port A3 | Timer 2 - channel 3 | TIM3_CH1 [AFR1] | |
| 10 | 9 | - | - | PA4 | I/O | X | X | X | HS | O3 | X | X | Port A4 | | |
| 11 | 10 | - | - | PA5 | I/O | X | X | X | HS | O3 | X | X | Port A5 | | |
| 12 | 11 | - | - | PA6 | I/O | X | X | X | HS | O3 | X | X | Port A6 | | |
| - | - | 8 | 13 | PF4/ AIN12 ⁽¹⁾ | I/O | X | X | | O1 | X | X | Port F4 | Analog input 12 ⁽²⁾ | | |
| 13 | 12 | 9 | 14 | V _{DDA} | S | | | | | | | | Analog power supply | | |
| 14 | 13 | 10 | 15 | V _{SSA} | S | | | | | | | | Analog ground | | |
| 15 | 14 | - | - | PB7/ AIN7 | I/O | X | X | X | O1 | X | X | Port B7 | Analog input 7 | | |
| 16 | 15 | - | - | PB6/ AIN6 | I/O | X | X | X | O1 | X | X | Port B6 | Analog input 6 | | |
| 17 | 16 | 11 | 16 | PB5/ AIN5 [I ² C_SDA] | I/O | X | X | X | O1 | X | X | Port B5 | Analog input 5 | I ² C_SDA [AFR6] | |
| 18 | 17 | 12 | 17 | PB4/ AIN4 [I ² C_SCL] | I/O | X | X | X | O1 | X | X | Port B4 | Analog input 4 | I ² C_SCL [AFR6] | |
| 19 | 18 | 13 | 18 | PB3/ AIN3 [TIM1_ETR] | I/O | X | X | X | O1 | X | X | Port B3 | Analog input 3 | TIM1_ETR [AFR5] | |
| 20 | 19 | 14 | 19 | PB2/ AIN2 [TIM1_CH3N] | I/O | X | X | X | O1 | X | X | Port B2 | Analog input 2 | TIM1_CH3N [AFR5] | |
| 21 | 20 | 15 | 20 | PB1/ AIN1 [TIM1_CH2N] | I/O | X | X | X | O1 | X | X | Port B1 | Analog input 1 | TIM1_CH2N [AFR5] | |
| 22 | 21 | 16 | 21 | PB0/ AIN0 [TIM1_CH1N] | I/O | X | X | X | O1 | X | X | Port B0 | Analog input 0 | TIM1_CH1N [AFR5] | |
| 23 | - | - | - | PE7/ AIN8 | I/O | X | X | X | O1 | X | X | Port E7 | Analog input 8 | | |
| 24 | 22 | - | - | PE6/ AIN9 | I/O | X | X | X | O1 | X | X | Port E6 | Analog input 9 ⁽³⁾ | | |
| 25 | 23 | 17 | 22 | PE5/SPI_NSS | I/O | X | X | X | O1 | X | X | Port E5 | SPI master/slave select | | |
| 26 | 24 | 18 | 23 | PC1/ TIM1_CH1 UART2_CK | I/O | X | X | X | HS | O3 | X | X | Port C1 | Timer 1 – channel 1/ UART2 synchronous clock | |

| Pin number | | | | Pin name | Type | Input | | | Output | | | | Main function (after reset) | Default alternate function | Alternate function after remap [option bit] |
|------------|--------|---------------------|--------|---|------|----------|-----|----------------|-----------|-------|------------------|----|-----------------------------|----------------------------|---|
| LQFP48 | LQFP44 | LQFP32/ UFQFPN32 | SDIP32 | | | floating | wpu | Ext. interrupt | High sink | Speed | OD | PP | | | |
| 27 | 25 | 19 | 24 | PC2/ TIM1_CH2 | I/O | X | X | X | HS | O3 | X | X | Port C2 | Timer 1 - channel 2 | |
| 28 | 26 | 20 | 25 | PC3/ TIM1_CH3 | I/O | X | X | X | HS | O3 | X | X | Port C3 | Timer 1 - channel 3 | |
| 29 | - | 21 | 26 | PC4/ TIM1_CH4 | I/O | X | X | X | HS | O3 | X | | Port C4 | Timer 1 - channel 4 | |
| 30 | 27 | 22 | 27 | PC5/ SPI_SCK | I/O | X | X | X | HS | O3 | X | X | Port C5 | SPI clock | |
| 31 | 28 | - | - | V _{SSIO_2} | S | | | | | | | | | I/O ground | |
| 32 | 29 | - | - | V _{DDIO_2} | S | | | | | | | | | I/O power supply | |
| 33 | 30 | 23 | 28 | PC6/ SPI_MOSI | I/O | X | X | X | HS | O3 | X | X | Port C6 | SPI master out/slave in | |
| 34 | 31 | 24 | 29 | PC7/ SPI_MISO | I/O | X | X | X | HS | O3 | X | X | Port C7 | SPI master in/ slave out | |
| 35 | 32 | - | - | PG0 | I/O | X | X | | | O1 | X | X | Port G0 | | |
| 36 | 33 | - | - | PG1 | I/O | X | X | | | O1 | X | X | Port G1 | | |
| 37 | - | - | - | PE3/ TIM1_BKIN | I/O | X | X | X | | O1 | X | X | Port E3 | Timer 1 - break input | |
| 38 | 34 | - | - | PE2/ I ² C_SDA | I/O | X | | X | | O1 | T ⁽⁴⁾ | | Port E2 | I ² C data | |
| 39 | 35 | - | - | PE1/ I ² C_SCL | I/O | X | | X | | O1 | T ⁽⁴⁾ | | Port E1 | I ² C clock | |
| 40 | 36 | - | - | PE0/ CLK_CCO | I/O | X | X | X | HS | O3 | X | X | Port E0 | Configurable clock output | |
| 41 | 37 | 25 | 30 | PD0/ TIM3_CH2 [TIM1_BKIN] [CLK_CCO] | I/O | X | X | X | HS | O3 | X | X | Port D0 | Timer 3 - channel 2 | TIM1_BKIN [AFR3]/ CLK_CCO [AFR2] |
| 42 | 38 | 26 | 31 | PD1/ SWIM ⁽⁵⁾ | I/O | X | X | X | HS | O4 | X | X | Port D1 | SWIM data interface | |
| 43 | 39 | 27 | 32 | PD2/ TIM3_CH1 [TIM2_CH3] | I/O | X | X | X | HS | O3 | X | X | Port D2 | Timer 3 - channel 1 | TIM2_CH3 [AFR1] |
| 44 | 40 | 28 | 1 | PD3/ TIM2_CH2 [ADC_ETR] | I/O | X | X | X | HS | O3 | X | X | Port D3 | Timer 2 - channel 2 | ADC_ETR [AFR0] |
| 45 | 41 | 29 | 2 | PD4/ TIM2_CH1 [BEEP] | I/O | X | X | X | HS | O3 | X | X | Port D4 | Timer 2 - channel 1 | BEEP output [AFR7] |
| 46 | 42 | 30 | 3 | PD5/ UART2_TX | I/O | X | X | X | | O1 | X | X | Port D5 | UART2 data transmit | |
| 47 | 43 | 31 | 4 | PD6/ UART2_RX | I/O | X | X | X | | O1 | X | X | Port D6 | UART2 data receive | |
| 48 | 44 | 32 | 5 | PD7/ TLI [TIM1_CH4] | I/O | X | X | X | | O1 | X | X | Port D7 | Top level interrupt | TIM1_CH4 [AFR4] |

Notes:

- (1) A pull-up is applied to PF4 during the reset phase. This pin is input floating after reset release.
- (2) AIN12 is not selectable in ADC scan mode or with analog watchdog.
- (3) In 44-pin package, AIN9 cannot be used by ADC scan mode.
- (4) In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
- (5) The PD1 pin is in input pull-up during the reset phase and after internal reset release.



5.1.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. When the remapping option is active, the default alternate function is no longer available.

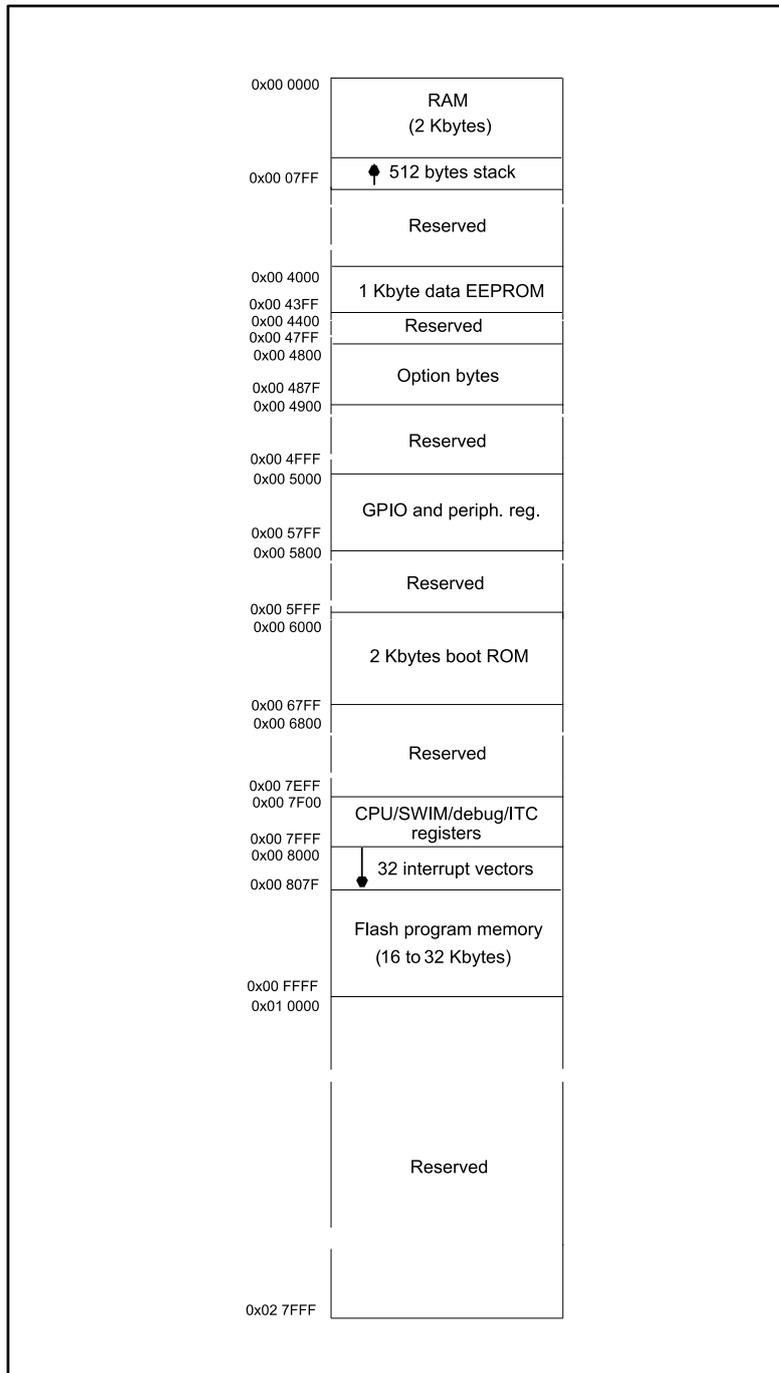
To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not affect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

6 Memory and register map

6.1 Memory map

Figure 7: Memory map



The following table lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

Table 7: Flash, Data EEPROM and RAM boundary addresses

| Memory area | Size (bytes) | Start address | End address |
|----------------------|--------------|---------------|-------------|
| Flash program memory | 32K | 0x00 8000 | 0x00 FFFF |
| | 16K | 0x00 8000 | 0x00 BFFF |
| RAM | 2K | 0x00 0000 | 0x00 07FF |
| Data EEPROM | 1024 | 0x00 4000 | 0x00 43FF |

6.2 Register map

6.2.1 I/O port hardware register map

Table 8: I/O port hardware register map

| Address | Block | Register label | Register name | Reset status |
|-----------|--------|----------------|-----------------------------------|--------------|
| 0x00 5000 | Port A | PA_ODR | Port A data output latch register | 0x00 |
| 0x00 5001 | | PA_IDR | Port A input pin value register | 0xXX |
| 0x00 5002 | | PA_DDR | Port A data direction register | 0x00 |
| 0x00 5003 | | PA_CR1 | Port A control register 1 | 0x00 |
| 0x00 5004 | | PA_CR2 | Port A control register 2 | 0x00 |
| 0x00 5005 | Port B | PB_ODR | Port B data output latch register | 0x00 |
| 0x00 5006 | | PB_IDR | Port B input pin value register | 0xXX |
| 0x00 5007 | | PB_DDR | Port B data direction register | 0x00 |
| 0x00 5008 | | PB_CR1 | Port B control register 1 | 0x00 |
| 0x00 5009 | | PB_CR2 | Port B control register 2 | 0x00 |
| 0x00 500A | Port C | PC_ODR | Port C data output latch register | 0x00 |
| 0x00 500B | | PC_IDR | Port C input pin value register | 0xXX |
| 0x00 500C | | PC_DDR | Port C data direction register | 0x00 |
| 0x00 500D | | PC_CR1 | Port C control register 1 | 0x00 |
| 0x00 500E | | PC_CR2 | Port C control register 2 | 0x00 |
| 0x00 500F | Port D | PD_ODR | Port D data output latch register | 0x00 |
| 0x00 5010 | | PD_IDR | Port D input pin value register | 0xXX |
| 0x00 5011 | | PD_DDR | Port D data direction register | 0x00 |
| 0x00 5012 | | PD_CR1 | Port D control register 1 | 0x02 |
| 0x00 5013 | | PD_CR2 | Port D control register 2 | 0x00 |
| 0x00 5014 | Port E | PE_ODR | Port E data output latch register | 0x00 |
| 0x00 5015 | | PE_IDR | Port E input pin value register | 0xXX |
| 0x00 5016 | | PE_DDR | Port E data direction register | 0x00 |
| 0x00 5017 | | PE_CR1 | Port E control register 1 | 0x00 |
| 0x00 5018 | | PE_CR2 | Port E control register 2 | 0x00 |
| 0x00 5019 | Port F | PF_ODR | Port F data output latch register | 0x00 |

| Address | Block | Register label | Register name | Reset status |
|-----------|--------|----------------|-----------------------------------|--------------|
| 0x00 501A | | PF_IDR | Port F input pin value register | 0xXX |
| 0x00 501B | | PF_DDR | Port F data direction register | 0x00 |
| 0x00 501C | | PF_CR1 | Port F control register 1 | 0x00 |
| 0x00 501D | | PF_CR2 | Port F control register 2 | 0x00 |
| 0x00 501E | Port G | PG_ODR | Port G data output latch register | 0x00 |
| 0x00 501F | | PG_IDR | Port G input pin value register | 0xXX |
| 0x00 5020 | | PG_DDR | Port G data direction register | 0x00 |
| 0x00 5021 | | PG_CR1 | Port G control register 1 | 0x00 |
| 0x00 5022 | | PG_CR2 | Port G control register 2 | 0x00 |
| 0x00 5023 | Port H | PH_ODR | Port H data output latch register | 0x00 |
| 0x00 5024 | | PH_IDR | Port H input pin value register | 0xXX |
| 0x00 5025 | | PH_DDR | Port H data direction register | 0x00 |
| 0x00 5026 | | PH_CR1 | Port H control register 1 | 0x00 |
| 0x00 5027 | | PH_CR2 | Port H control register 2 | 0x00 |
| 0x00 5028 | Port I | PI_ODR | Port I data output latch register | 0x00 |
| 0x00 5029 | | PI_IDR | Port I input pin value register | 0xXX |
| 0x00 502A | | PI_DDR | Port I data direction register | 0x00 |
| 0x00 502B | | PI_CR1 | Port I control register 1 | 0x00 |
| 0x00 502C | | PI_CR2 | Port I control register 2 | 0x00 |

6.2.2 General hardware register map

Table 9: General hardware register map

| Address | Block | Register label | Register name | Reset status |
|---------------------------|--------------------------|----------------|--|--------------|
| 0x00 5050 to 0x00 5059 | Reserved area (10 bytes) | | | |
| 0x00 505A | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 505B | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 505C | | FLASH_NCR2 | Flash complementary control register 2 | 0xFF |
| 0x00 505D | | FLASH_FPR | Flash protection register | 0x00 |
| 0x00 505E | | FLASH_NFPR | Flash complementary protection register | 0xFF |
| 0x00 505F | | FLASH_IAPSR | Flash in-application programming status register | 0x00 |
| 0x00 5060 to 0x00 5061 | Reserved area (2 bytes) | | | |
| 0x00 5062 | Flash | FLASH_PUKR | Flash program memory unprotection register | 0x00 |

| Address | Block | Register label | Register name | Reset status | |
|------------------------|--------------------------|-------------------------|---|-----------------------|------|
| 0x00 5063 | Reserved area (1 byte) | | | | |
| 0x00 5064 | Flash | FLASH_DUKR | Data EEPROM unprotection register | 0x00 | |
| 0x00 5065 to 0x00 509F | Reserved area (59 bytes) | | | | |
| 0x00 50A0 | ITC | EXTI_CR1 | External interrupt control register 1 | 0x00 | |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 | |
| 0x00 50A2 to 0x00 50B2 | Reserved area (17 bytes) | | | | |
| 0x00 50B3 | RST | RST_SR | Reset status register | 0xXX ⁽¹⁾ | |
| 0x00 50B4 to 0x00 50BF | Reserved area (12 bytes) | | | | |
| 0x00 50C0 | CLK | CLK_ICKR | Internal clock control register | 0x01 | |
| 0x00 50C1 | | CLK_ECKR | External clock control register | 0x00 | |
| 0x00 50C2 | Reserved area (1 byte) | | | | |
| 0x00 50C3 | CLK | CLK_CMSR | Clock master status register | 0xE1 | |
| 0x00 50C4 | | CLK_SWR | Clock master switch register | 0xE1 | |
| 0x00 50C5 | | CLK_SWCR | Clock switch control register | 0xXX | |
| 0x00 50C6 | | CLK_CKDIVR | Clock divider register | 0x18 | |
| 0x00 50C7 | | CLK_PCKENR1 | Peripheral clock gating register 1 | 0xFF | |
| 0x00 50C8 | | CLK_CSSR | Clock security system register | 0x00 | |
| 0x00 50C9 | | CLK_CCOR | Configurable clock control register | 0x00 | |
| 0x00 50CA | | CLK_PCKENR2 | Peripheral clock gating register 2 | 0xFF | |
| 0x00 50CB | | CLK_CANCCR | CAN clock control register | 0x00 | |
| 0x00 50CC | | CLK_HSTRIMR | HSI clock calibration trimming register | 0x00 | |
| 0x00 50CD | | CLK_SWIMCCR | SWIM clock control register | 0bXXXX XXX0 | |
| 0x00 50CE to 0x00 50D0 | | Reserved area (3 bytes) | | | |
| 0x00 50D1 | | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D2 | WWDG_WR | | WWDG window register | 0x7F | |
| 0x00 50D3 to 0x00 50DF | Reserved area (13 bytes) | | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX ⁽²⁾ | |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 | |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF | |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 bytes) | | | | |
| 0x00 50F0 | AWU | AWU_CSR1 | AWU control/ status register 1 | 0x00 | |

| Address | Block | Register label | Register name | Reset status | |
|------------------------|--------------------------|--------------------------|---|--------------|--|
| 0x00 50F1 | | AWU_APR | AWU asynchronous prescaler buffer register | 0x3F | |
| 0x00 50F2 | | AWU_TBR | AWU timebase selection register | 0x00 | |
| 0x00 50F3 | BEEP | BEEP_CSR | BEEP control/ status register | 0x1F | |
| 0x00 50F4 to 0x00 50FF | Reserved area (12 bytes) | | | | |
| 0x00 5200 | SPI | SPI_CR1 | SPI control register 1 | 0x00 | |
| 0x00 5201 | | SPI_CR2 | SPI control register 2 | 0x00 | |
| 0x00 5202 | | SPI_ICR | SPI interrupt control register | 0x00 | |
| 0x00 5203 | | SPI_SR | SPI status register | 0x02 | |
| 0x00 5204 | | SPI_DR | SPI data register | 0x00 | |
| 0x00 5205 | | SPI_CRCPR | SPI CRC polynomial register | 0x07 | |
| 0x00 5206 | | SPI_RXCR | SPI Rx CRC register | 0xFF | |
| 0x00 5207 | | SPI_TXCR | SPI Tx CRC register | 0xFF | |
| 0x00 5208 to 0x00 520F | Reserved area (8 bytes) | | | | |
| 0x00 5210 | I ² C | I2C_CR1 | I ² C control register 1 | 0x00 | |
| 0x00 5211 | | I2C_CR2 | I ² C control register 2 | 0x00 | |
| 0x00 5212 | | I2C_FREQR | I ² C frequency register | 0x00 | |
| 0x00 5213 | | I2C_OARL | I ² C Own address register low | 0x00 | |
| 0x00 5214 | | I2C_OARH | I ² C own address register high | 0x00 | |
| 0x00 5215 | | Reserved | | | |
| 0x00 5216 | | I2C_DR | I ² C data register | 0x00 | |
| 0x00 5217 | | I2C_SR1 | I ² C status register 1 | 0x00 | |
| 0x00 5218 | | I2C_SR2 | I ² C status register 2 | 0x00 | |
| 0x00 5219 | | I2C_SR3 | I ² C status register 3 | 0x00 | |
| 0x00 521A | | I2C_ITR | I ² C interrupt control register | 0x00 | |
| 0x00 521B | | I2C_CCRL | I ² C clock control register low | 0x00 | |
| 0x00 521C | | I2C_CCRH | I ² C clock control register high | 0x00 | |
| 0x00 521D | | I2C_TRISER | I ² C TRISE register | 0x02 | |
| 0x00 521E | | I2C_PECR | I ² C packet error checking register | 0x00 | |
| 0x00 521F to 0x00 522F | | Reserved area (17 bytes) | | | |
| 0x00 5230 to 0x00 523F | Reserved area (6 bytes) | | | | |
| 0x00 5240 | UART2 | UART2_SR | UART2 status register | 0xC0 | |
| 0x00 5241 | | UART2_DR | UART2 data register | 0xFF | |
| 0x00 5242 | | UART2_BRR1 | UART2 baud rate register 1 | 0x00 | |

| Address | Block | Register label | Register name | Reset status |
|------------------------|----------|----------------------------------|---|--------------|
| 0x00 5243 | | UART2_BRR2 | UART2 baud rate register 2 | 0x00 |
| 0x00 5244 | | UART2_CR1 | UART2 control register 1 | 0x00 |
| 0x00 5245 | | UART2_CR2 | UART2 control register 2 | 0x00 |
| 0x00 5246 | | UART2_CR3 | UART2 control register 3 | 0x00 |
| 0x00 5247 | | UART2_CR4 | UART2 control register 4 | 0x00 |
| 0x00 5248 | | UART2_CR5 | UART2 control register 5 | 0x00 |
| 0x00 5249 | | UART2_CR6 | UART2 control register 6 | 0x00 |
| 0x00 524A | | UART2_GTR | UART2 guard time register | 0x00 |
| 0x00 524B | | UART2_PSCR | UART2 prescaler register | 0x00 |
| 0x00 524C to 0x00 524F | | Reserved area (4 bytes) | | |
| 0x00 5250 | TIM1 | TIM1_CR1 | TIM1 control register 1 | 0x00 |
| 0x00 5251 | | TIM1_CR2 | TIM1 control register 2 | 0x00 |
| 0x00 5252 | | TIM1_SMCR | TIM1 slave mode control register | 0x00 |
| 0x00 5253 | | TIM1_ETR | TIM1 external trigger register | 0x00 |
| 0x00 5254 | | TIM1_IER | TIM1 interrupt enable register | 0x00 |
| 0x00 5255 | | TIM1_SR1 | TIM1 status register 1 | 0x00 |
| 0x00 5256 | | TIM1_SR2 | TIM1 status register 2 | 0x00 |
| 0x00 5257 | | TIM1_EGR | TIM1 event generation register | 0x00 |
| 0x00 5258 | | TIM1_CCMR1 | TIM1 capture/ compare mode register 1 | 0x00 |
| 0x00 5259 | | TIM1_CCMR2 | TIM1 capture/compare mode register 2 | 0x00 |
| 0x00 525A | | TIM1_CCMR3 | TIM1 capture/ compare mode register 3 | 0x00 |
| 0x00 525B | | TIM1_CCMR4 | TIM1 capture/compare mode register 4 | 0x00 |
| 0x00 525C | | TIM1_CCER1 | TIM1 capture/ compare enable register 1 | 0x00 |
| 0x00 525D | | TIM1_CCER2 | TIM1 capture/compare enable register 2 | 0x00 |
| 0x00 525E | | TIM1_CNTRH | TIM1 counter high | 0x00 |
| 0x00 525F | | TIM1_CNTRL | TIM1 counter low | 0x00 |
| 0x00 5260 | | TIM1_PSCRH | TIM1 prescaler register high | 0x00 |
| 0x00 5261 | | TIM1_PSCRL | TIM1 prescaler register low | 0x00 |
| 0x00 5262 | | TIM1_ARRH | TIM1 auto-reload register high | 0xFF |
| 0x00 5263 | | TIM1_ARRL | TIM1 auto-reload register low | 0xFF |
| 0x00 5264 | TIM1_RCR | TIM1 repetition counter register | 0x00 | |

| Address | Block | Register label | Register name | Reset status |
|------------------------|-----------|-------------------------------|---|--------------|
| 0x00 5265 | | TIM1_CCR1H | TIM1 capture/ compare register 1 high | 0x00 |
| 0x00 5266 | | TIM1_CCR1L | TIM1 capture/ compare register 1 low | 0x00 |
| 0x00 5267 | | TIM1_CCR2H | TIM1 capture/ compare register 2 high | 0x00 |
| 0x00 5268 | | TIM1_CCR2L | TIM1 capture/ compare register 2 low | 0x00 |
| 0x00 5269 | | TIM1_CCR3H | TIM1 capture/ compare register 3 high | 0x00 |
| 0x00 526A | | TIM1_CCR3L | TIM1 capture/ compare register 3 low | 0x00 |
| 0x00 526B | | TIM1_CCR4H | TIM1 capture/ compare register 4 high | 0x00 |
| 0x00 526C | | TIM1_CCR4L | TIM1 capture/ compare register 4 low | 0x00 |
| 0x00 526D | | TIM1_BKR | TIM1 break register | 0x00 |
| 0x00 526E | | TIM1_DTR | TIM1 dead-time register | 0x00 |
| 0x00 526F | | TIM1_OISR | TIM1 output idle state register | 0x00 |
| 0x00 5270 to 0x00 52FF | | Reserved area (147 bytes) | | |
| 0x00 5300 | TIM2 | TIM2_CR1 | TIM2 control register 1 | 0x00 |
| 0x00 5301 | | TIM2_IER | TIM2 interrupt enable register | 0x00 |
| 0x00 5302 | | TIM2_SR1 | TIM2 status register 1 | 0x00 |
| 0x00 5303 | | TIM2_SR2 | TIM2 status register 2 | 0x00 |
| 0x00 5304 | | TIM2_EGR | TIM2 event generation register | 0x00 |
| 0x00 5305 | | TIM2_CCMR1 | TIM2 capture/ compare mode register 1 | 0x00 |
| 0x00 5306 | | TIM2_CCMR2 | TIM2 capture/ compare mode register 2 | 0x00 |
| 0x00 5307 | | TIM2_CCMR3 | TIM2 capture/ compare mode register 3 | 0x00 |
| 0x00 5308 | | TIM2_CCER1 | TIM2 capture/ compare enable register 1 | 0x00 |
| 0x00 5309 | | TIM2_CCER2 | TIM2 capture/ compare enable register 2 | 0x00 |
| 0x00 530A | | TIM2_CNTRH | TIM2 counter high | 0x00 |
| 0x00 530B | | TIM2_CNTRL | TIM2 counter low | 0x00 |
| 0x00 530C | | TIM2_PSCR | TIM2 prescaler register | 0x00 |
| 0x00 530D | | TIM2_ARRH | TIM2 auto-reload register high | 0xFF |
| 0x00 530E | TIM2_ARRL | TIM2 auto-reload register low | 0xFF | |

| Address | Block | Register label | Register name | Reset status |
|------------------------|--------------------------|----------------|---|--------------|
| 0x00 530F | | TIM2_CCR1H | TIM2 capture/ compare register 1 high | 0x00 |
| 0x00 5310 | | TIM2_CCR1L | TIM2 capture/ compare register 1 low | 0x00 |
| 0x00 5311 | | TIM2_CCR2H | TIM2 capture/ compare reg. 2 high | 0x00 |
| 0x00 5312 | | TIM2_CCR2L | TIM2 capture/ compare register 2 low | 0x00 |
| 0x00 5313 | | TIM2_CCR3H | TIM2 capture/ compare register 3 high | 0x00 |
| 0x00 5314 | | TIM2_CCR3L | TIM2 capture/ compare register 3 low | 0x00 |
| 0x00 5315 to 0x00 531F | Reserved area (11 bytes) | | | |
| 0x00 5320 | TIM3 | TIM3_CR1 | TIM3 control register 1 | 0x00 |
| 0x00 5321 | | TIM3_IER | TIM3 interrupt enable register | 0x00 |
| 0x00 5322 | | TIM3_SR1 | TIM3 status register 1 | 0x00 |
| 0x00 5323 | | TIM3_SR2 | TIM3 status register 2 | 0x00 |
| 0x00 5324 | | TIM3_EGR | TIM3 event generation register | 0x00 |
| 0x00 5325 | | TIM3_CCMR1 | TIM3 capture/ compare mode register 1 | 0x00 |
| 0x00 5326 | | TIM3_CCMR2 | TIM3 capture/ compare mode register 2 | 0x00 |
| 0x00 5327 | | TIM3_CCER1 | TIM3 capture/ compare enable register 1 | 0x00 |
| 0x00 5328 | | TIM3_CNTRH | TIM3 counter high | 0x00 |
| 0x00 5329 | | TIM3_CNTRL | TIM3 counter low | 0x00 |
| 0x00 532A | | TIM3_PSCR | TIM3 prescaler register | 0x00 |
| 0x00 532B | | TIM3_ARRH | TIM3 auto-reload register high | 0xFF |
| 0x00 532C | | TIM3_ARRL | TIM3 auto-reload register low | 0xFF |
| 0x00 532D | | TIM3_CCR1H | TIM3 capture/ compare register 1 high | 0x00 |
| 0x00 532E | | TIM3_CCR1L | TIM3 capture/ compare register 1 low | 0x00 |
| 0x00 532F | | TIM3_CCR2H | TIM3 capture/ compare register 2 high | 0x00 |
| 0x00 5330 | | TIM3_CCR2L | TIM3 capture/ compare register 2 low | 0x00 |
| 0x00 5331 to 0x00 533F | Reserved area (15 bytes) | | | |
| 0x00 5340 | TIM4 | TIM4_CR1 | TIM4 control register 1 | 0x00 |
| 0x00 5341 | | TIM4_IER | TIM4 interrupt enable register | 0x00 |

| Address | Block | Register label | Register name | Reset status |
|------------------------|----------------------------|--|---|--------------|
| 0x00 5342 | | TIM4_SR | TIM4 status register | 0x00 |
| 0x00 5343 | | TIM4_EGR | TIM4 event generation register | 0x00 |
| 0x00 5344 | | TIM4_CNTR | TIM4 counter | 0x00 |
| 0x00 5345 | | TIM4_PSCR | TIM4 prescaler register | 0x00 |
| 0x00 5346 | | TIM4_ARR | TIM4 auto-reload register | 0xFF |
| 0x00 5347 to 0x00 53DF | Reserved area (153 bytes) | | | |
| 0x00 53E0 to 0x00 53F3 | ADC1 | ADC_DBxR | ADC data buffer registers | 0x00 |
| 0x00 53F4 to 0x00 53FF | Reserved area (12 bytes) | | | |
| 0x00 5400 | ADC1 | ADC_CSR | ADC control/ status register | 0x00 |
| 0x00 5401 | | ADC_CR1 | ADC configuration register 1 | 0x00 |
| 0x00 5402 | | ADC_CR2 | ADC configuration register 2 | 0x00 |
| 0x00 5403 | | ADC_CR3 | ADC configuration register 3 | 0x00 |
| 0x00 5404 | | ADC_DRH | ADC data register high | 0xFF |
| 0x00 5405 | | ADC_DRL | ADC data register low | 0xFF |
| 0x00 5406 | | ADC_TDRH | ADC Schmitt trigger disable register high | 0x00 |
| 0x00 5407 | | ADC_TDRL | ADC Schmitt trigger disable register low | 0x00 |
| 0x00 5408 | | ADC_HTRH | ADC high threshold register high | 0x03 |
| 0x00 5409 | | ADC_HTRL | ADC high threshold register low | 0xFF |
| 0x00 540A | | ADC_LTRH | ADC low threshold register high | 0x00 |
| 0x00 540B | | ADC_LTRL | ADC low threshold register low | 0x00 |
| 0x00 540C | | ADC_AWSRH | ADC analog watchdog status register high | 0x00 |
| 0x00 540D | | ADC_AWSRL | ADC analog watchdog status register low | 0x00 |
| 0x00 540E | | ADC_AWCRH | ADC analog watchdog control register high | 0x00 |
| 0x00 540F | ADC_AWCRL | ADC analog watchdog control register low | 0x00 | |
| 0x00 5410 to 0x00 57FF | Reserved area (1008 bytes) | | | |

Notes:

(1) Depends on the previous reset source.

(2) Write only register.

6.2.3 CPU/SWIM/debug module/interrupt controller registers

Table 10: CPU/SWIM/debug module/interrupt controller registers

| Address | Block | Register label | Register name | Reset status |
|------------------------|--------------------------|--------------------------|--|--------------|
| 0x00 7F00 | CPU (1) | A | Accumulator | 0x00 |
| 0x00 7F01 | | PCE | Program counter extended | 0x00 |
| 0x00 7F02 | | PCH | Program counter high | 0x00 |
| 0x00 7F03 | | PCL | Program counter low | 0x00 |
| 0x00 7F04 | | XH | X index register high | 0x00 |
| 0x00 7F05 | | XL | X index register low | 0x00 |
| 0x00 7F06 | | YH | Y index register high | 0x00 |
| 0x00 7F07 | | YL | Y index register low | 0x00 |
| 0x00 7F08 | | SPH | Stack pointer high | 0x07 |
| 0x00 7F09 | | SPL | Stack pointer low | 0xFF |
| 0x00 7F0A | | CCR | Condition code register | 0x28 |
| 0x00 7F0B to 0x00 7F5F | | Reserved area (85 bytes) | | |
| 0x00 7F60 | CPU | CFG_GCR | Global configuration register | 0x00 |
| 0x00 7F70 | ITC | ITC_SPR1 | Interrupt software priority register 1 | 0xFF |
| 0x00 7F71 | | ITC_SPR2 | Interrupt software priority register 2 | 0xFF |
| 0x00 7F72 | | ITC_SPR3 | Interrupt software priority register 3 | 0xFF |
| 0x00 7F73 | | ITC_SPR4 | Interrupt software priority register 4 | 0xFF |
| 0x00 7F74 | | ITC_SPR5 | Interrupt software priority register 5 | 0xFF |
| 0x00 7F75 | | ITC_SPR6 | Interrupt software priority register 6 | 0xFF |
| 0x00 7F76 | | ITC_SPR7 | Interrupt software priority register 7 | 0xFF |
| 0x00 7F77 | | ITC_SPR8 | Interrupt software priority register 8 | 0xFF |
| 0x00 7F78 to 0x00 7F79 | Reserved area (2 bytes) | | | |
| 0x00 7F80 | SWIM | SWIM_CSR | SWIM control status register | 0x00 |
| 0x00 7F81 to 0x00 7F8F | Reserved area (15 bytes) | | | |
| 0x00 7F90 | DM | DM_BK1RE | DM breakpoint 1 register extended byte | 0xFF |
| 0x00 7F91 | | DM_BK1RH | DM breakpoint 1 register high byte | 0xFF |
| 0x00 7F92 | | DM_BK1RL | DM breakpoint 1 register low byte | 0xFF |
| 0x00 7F93 | | DM_BK2RE | DM breakpoint 2 register extended byte | 0xFF |
| 0x00 7F94 | | DM_BK2RH | DM breakpoint 2 register high byte | 0xFF |
| 0x00 7F95 | | DM_BK2RL | DM breakpoint 2 register low byte | 0xFF |
| 0x00 7F96 | | DM_CR1 | DM debug module control | 0x00 |

| Address | Block | Register label | Register name | Reset status |
|------------------------|-------------------------|----------------|---|--------------|
| | | | register 1 | |
| 0x00 7F97 | | DM_CR2 | DM debug module control register 2 | 0x00 |
| 0x00 7F98 | | DM_CSR1 | DM debug module control/status register 1 | 0x10 |
| 0x00 7F99 | | DM_CSR2 | DM debug module control/status register 2 | 0x00 |
| 0x00 7F9A | | DM_ENFCTR | DM enable function register | 0xFF |
| 0x00 7F9B to 0x00 7F9F | Reserved area (5 bytes) | | | |

Notes:

⁽¹⁾ Accessible by debug module only

7 Interrupt vector mapping

Table 11: Interrupt mapping

| IRQ no. | Source block | Description | Wakeup from halt mode | Wakeup from active-halt mode | Vector address |
|----------|------------------|---|-----------------------|------------------------------|-----------------------|
| | RESET | Reset | Yes | Yes | 0x00 8000 |
| | TRAP | Software interrupt | - | - | 0x00 8004 |
| 0 | TLI | External top level interrupt | - | - | 0x00 8008 |
| 1 | AWU | Auto wake up from halt | - | Yes | 0x00 800C |
| 2 | CLK | Clock controller | - | - | 0x00 8010 |
| 3 | EXTI0 | Port A external interrupts | Yes ⁽¹⁾ | Yes ⁽¹⁾ | 0x00 8014 |
| 4 | EXTI1 | Port B external interrupts | Yes | Yes | 0x00 8018 |
| 5 | EXTI2 | Port C external interrupts | Yes | Yes | 0x00 801C |
| 6 | EXTI3 | Port D external interrupts | Yes | Yes | 0x00 8020 |
| 7 | EXTI4 | Port E external interrupts | Yes | Yes | 0x00 8024 |
| 8 | | | | | 0x00 8028 |
| 9 | | Reserved | - | - | 0x00 802C |
| 10 | SPI | End of transfer | Yes | Yes | 0x00 8030 |
| 11 | TIM1 | TIM1 update/ overflow/ underflow/ trigger/ break | - | - | 0x00 8034 |
| 12 | TIM1 | TIM1 capture/ compare | - | - | 0x00 8038 |
| 13 | TIM2 | TIM update/ overflow | - | - | 0x00 803C |
| 14 | TIM2 | TIM capture/ compare | - | - | 0x00 8040 |
| 15 | TIM3 | Update/ overflow | - | - | 0x00 8044 |
| 16 | TIM3 | Capture/ compare | - | - | 0x00 8048 |
| 17 | | Reserved | - | - | 0x00 804C |
| 18 | | Reserved | - | - | 0x00 8050 |
| 19 | I ² C | I ² C interrupt | Yes | Yes | 0x00 8054 |
| 20 | UART2 | Tx complete | - | - | 0x00 8058 |
| 21 | UART2 | Receive register DATA FULL | - | - | 0x00 805C |
| 22 | ADC1 | ADC1 end of conversion/ analog watchdog interrupt | - | - | 0x00 8060 |
| 23 | TIM4 | TIM update/ overflow | - | - | 0x00 8064 |
| 24 | Flash | EOP/ WR_PG_DIS | - | - | 0x00 8068 |
| Reserved | | | | | 0x00 806C to 0x00807C |

Notes: ⁽¹⁾ Except PA1

8 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in the table below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 12: Option bytes

| Addr. | Option name | Option byte no. | Option bits | | | | | | | | Factory default setting |
|---------------|------------------------------------|-----------------|---------------|-------|-------|-----------|------------|----------|----------|------------|-------------------------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x4800 | Read-out protection (ROP) | OPT0 | ROP [7:0] | | | | | | | | 00h |
| 0x4801 | User boot code(UBC) | OPT1 | UBC [7:0] | | | | | | | | 00h |
| 0x4802 | | NOPT1 | NUBC [7:0] | | | | | | | | FFh |
| 0x4803 | Alternate function remapping (AFR) | OPT2 | AFR7 | AFR6 | AFR5 | AFR4 | AFR3 | AFR2 | AFR1 | AFR0 | 00h |
| 0x4804 | | NOPT2 | NAFR7 | NAFR6 | NAFR5 | NAFR4 | NAFR3 | NAFR2 | NAFR1 | NAFR0 | FFh |
| 0x4805h | Miscell. option | OPT3 | Reserved | | | HSI TRIM | LSI_EN | IWDG_HW | WWDG_HW | WWDG_HALT | 00h |
| 0x4806 | | NOPT3 | Reserved | | | NHSI TRIM | NLSI_EN | NIWDG_HW | NWWDG_HW | NWWDG_HALT | FFh |
| 0x4807 | Clock option | OPT4 | Reserved | | | EXT CLK | CKAWU_SEL | PRS C1 | PRS C0 | 00h | |
| 0x4808 | | NOPT4 | Reserved | | | NEXT CLK | NCKA_WUSEL | NPRSC1 | NPR SC0 | FFh | |
| 0x4809 | HSE clock startup | OPT5 | HSECNT [7:0] | | | | | | | | 00h |
| 0x480A | | NOPT5 | NHSECNT [7:0] | | | | | | | | FFh |
| 0x480B | Reserved | OPT6 | Reserved | | | | | | | | 00h |
| 0x480C | | NOPT6 | Reserved | | | | | | | | FFh |
| 0x480D | Reserved | OPT7 | Reserved | | | | | | | | 00h |
| 0x480E | | NOPT7 | Reserved | | | | | | | | FFh |
| 0x480F-0x48FD | Reserved | | | | | | | | | | |
| 0x487E | Bootloader | OPTBL | BL[7:0] | | | | | | | | 00h |

| Addr. | Option name | Option byte no. | Option bits | | | | | | | | Factory default setting |
|--------|-------------|-----------------|-------------|---|---|---|---|---|---|---|-------------------------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x487F | | NOPTBL | NBL[7:0] | | | | | | | | |

Table 13: Option byte description

| Option byte no. | Description |
|-----------------|--|
| OPT0 | <p>ROP[7:0] Memory readout protection (ROP) AAh: Enable readout protection (write access via SWIM protocol) <i>Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.</i></p> |
| OPT1 | <p>UBC[7:0] User boot code area 0x00: no UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03: Page 0 to 4 defined as UBC, memory write-protected ... 0x3E: Pages 0 to 63 defined as UBC, memory write-protected Other values: Reserved <i>Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.</i></p> |
| OPT2 | <p>AFR[7:0] Refer to following table for the alternate function remapping descriptions of bits [7:2].</p> |
| OPT3 | <p>HSITRIM:High speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register</p> |
| | <p>LSI_EN:Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source</p> |
| | <p>IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware</p> |
| | <p>WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware</p> |
| | <p>WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active</p> |
| OPT4 | <p>EXTCLK: External clock selection 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN</p> |
| | <p>CKAWUSEL:Auto wake-up unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for for AWU</p> |

| Option byte no. | Description |
|-----------------|--|
| | <p>PRSC[1:0] AWU clock prescaler</p> <p>0x: 16 MHz to 128 kHz prescaler</p> <p>10: 8 MHz to 128 kHz prescaler</p> <p>11: 4 MHz to 128 kHz prescaler</p> |
| OPT5 | <p>HSECNT[7:0]:HSE crystal oscillator stabilization time</p> <p>0x00: 2048 HSE cycles</p> <p>0xB4: 128 HSE cycles</p> <p>0xD2: 8 HSE cycles</p> <p>0xE1: 0.5 HSE cycles</p> |
| OPT6 | Reserved |
| OPT7 | Reserved |
| OPTBL | <p>BL[7:0] Bootloader option byte</p> <p>For STM8S products, this option is checked by the boot ROM code after reset. Depending on the content of addresses 0x487E, 0x487F, and 0x8000 (reset vector), the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 (STM8L/S bootloader manual) for more details.</p> <p>For STM8L products, the bootloader option bytes are on addresses 0xFFFF and 0xFFFF+1 (2 bytes). These option bytes control whether the bootloader is active or not. For more details, refer to the UM0560 (STM8L/S bootloader manual) for more details.</p> |

Table 14: Description of alternate function remapping bits [7:0] of OPT2

| Option byte no. | Description ⁽¹⁾ |
|-----------------|---|
| OPT2 | <p>AFR7 Alternate function remapping option 7</p> <p>0: AFR7 remapping option inactive: Default alternate function ⁽²⁾.</p> <p>1: Port D4 alternate function = BEEP.</p> <p>AFR6 Alternate function remapping option 6</p> <p>0: AFR6 remapping option inactive: Default alternate functions ⁽²⁾.</p> <p>1: Port B5 alternate function = I²C_SDA; port B4 alternate function = I²C_SCL.</p> <p>AFR5 Alternate function remapping option 5</p> <p>0: AFR5 remapping option inactive: Default alternate functions ⁽²⁾.</p> <p>1: Port B3 alternate function = TIM1_ETR; port B2 alternate function = TIM1_NCC3; port B1 alternate function = TIM1_CH2N; port B0 alternate function = TIM1_CH1N.</p> <p>AFR4 Alternate function remapping option 4</p> <p>0: AFR4 remapping option inactive: Default alternate function ⁽²⁾.</p> <p>1: Port D7 alternate function = TIM1_CH4.</p> <p>AFR3 Alternate function remapping option 3</p> <p>0: AFR3 remapping option inactive: Default alternate function ⁽²⁾.</p> <p>1: Port D0 alternate function = TIM1_BKIN.</p> <p>AFR2 Alternate function remapping option 2</p> <p>0: AFR2 remapping option inactive: Default alternate function ⁽²⁾.</p> <p>1: Port D0 alternate function = CLK_CCO. Note: AFR2 option has priority over AFR3 if both are activated.</p> <p>AFR1 Alternate function remapping option 1</p> <p>0: AFR1 remapping option inactive: Default alternate functions ⁽²⁾.</p> |

| Option byte no. | Description ⁽¹⁾ |
|-----------------|---|
| | 1: Port A3 alternate function = TIM3_CH1; port D2 alternate function TIM2_CH3. AFR0 Alternate function remapping option 0 0: AFR0 remapping option inactive: Default alternate function ⁽²⁾ . 1: Port D3 alternate function = ADC_ETR. |

Notes:

⁽¹⁾ Do not use more than one remapping option in the same port.

⁽²⁾ Refer to pinout description.

9 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 15: Unique ID registers (96 bits)

| Address | Content description | Unique ID bits | | | | | | | |
|---------|----------------------------|----------------|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x48CD | X co-ordinate on the wafer | U_ID[7:0] | | | | | | | |
| 0x48CE | | U_ID[15:8] | | | | | | | |
| 0x48CF | Y co-ordinate on the wafer | U_ID[23:16] | | | | | | | |
| 0x48D0 | | U_ID[31:24] | | | | | | | |
| 0x48D1 | Wafer number | U_ID[39:32] | | | | | | | |
| 0x48D2 | Lot number | U_ID[47:40] | | | | | | | |
| 0x48D3 | | U_ID[55:48] | | | | | | | |
| 0x48D4 | | U_ID[63:56] | | | | | | | |
| 0x48D5 | | U_ID[71:64] | | | | | | | |
| 0x48D6 | | U_ID[79:72] | | | | | | | |
| 0x48D7 | | U_ID[87:80] | | | | | | | |
| 0x48D8 | | U_ID[95:88] | | | | | | | |

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at $T_A = 25\text{ °C}$ and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\ \Sigma$).

10.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ °C}$, $V_{DD} = 5\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\ \Sigma$).

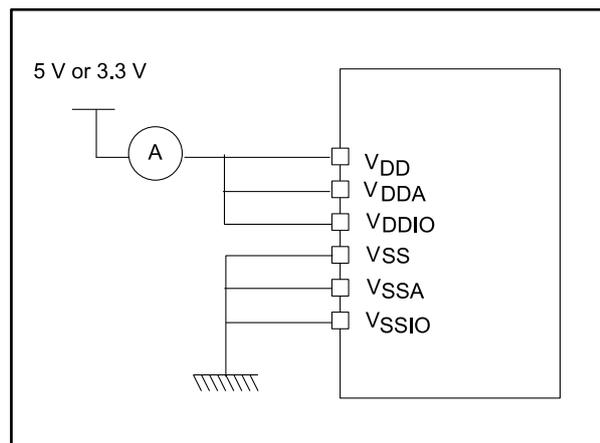
10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Typical current consumption

For typical current consumption measurements, V_{DD} , V_{DDIO} and V_{DDA} are connected together in the configuration shown in the following figure.

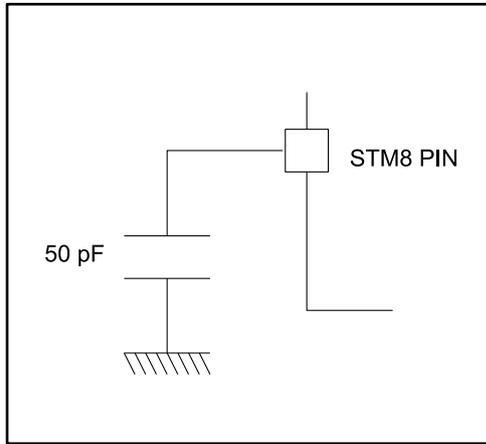
Figure 8: Supply current measurement conditions



10.1.5 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the following figure.

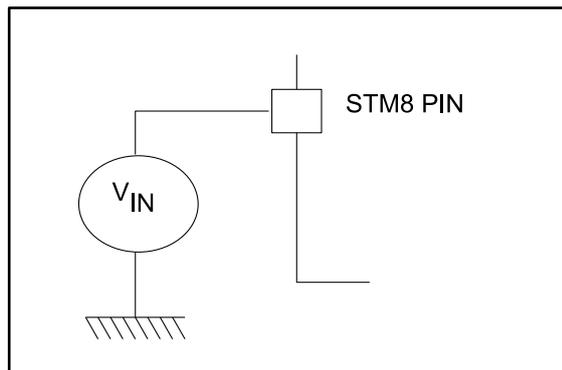
Figure 9: Pin loading conditions



10.1.6 Pin input voltage

The input voltage measurement on a pin of the device is described in the following figure.

Figure 10: Pin input voltage



10.2 Absolute maximum ratings

Stresses above those listed as ‘absolute maximum ratings’ may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 16: Voltage characteristics

| Symbol | Ratings | Min | Max | Unit |
|--------------------|---|----------------|----------------|------|
| $V_{DDx} - V_{SS}$ | Supply voltage (including V_{DDA} and V_{DDIO}) ⁽¹⁾ | -0.3 | 6.5 | V |
| V_{IN} | Input voltage on true open drain pins (PE1, PE2) ⁽²⁾ | $V_{SS} - 0.3$ | 6.5 | |
| | Input voltage on any other pin ⁽²⁾ | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | |
| $ V_{DDx} -$ | Variations between different power | | 50 | mV |

| Symbol | Ratings | Min | Max | Unit |
|----------------------|--|--|-----|------|
| V_{DD} | pins | | | |
| $ V_{SSx} - V_{SS} $ | Variations between all the different ground pins | | 50 | |
| V_{ESD} | Electrostatic discharge voltage | see Section 13.3.12.4: "Absolute maximum ratings (electrical sensitivity)" | | |

Notes:

(1) All power (V_{DD} , V_{DDIO} , V_{DDA}) and ground (V_{SS} , V_{SSIO} , V_{SSA}) pins must always be connected to the external power supply

(2) $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 17: Current characteristics

| Symbol | Ratings | Max. (1) | Unit |
|---------------------------|---|-------------|------|
| I_{VDD} | Total current into V_{DD} power lines (source) (2) | 60 | mA |
| I_{VSS} | Total current out of V_{SS} ground lines (sink) (2) | 60 | |
| I_{IO} | Output current sunk by any I/O and control pin | 20 | |
| | Output current source by any I/Os and control pin | 20 | |
| ΣI_{IO} | Total output current sourced (sum of all I/O and control pins) for devices with two V_{DDIO} pins (3) | 200 | |
| | Total output current sourced (sum of all I/O and control pins) for devices with one V_{DDIO} pin (3) | 100 | |
| | Total output current sunk (sum of all I/O and control pins) for devices with two V_{SSIO} pins (3) | 160 | |
| | Total output current sunk (sum of all I/O and control pins) for devices with one V_{SSIO} pin (3) | 80 | |
| $I_{INJ(PIN)}$ (4)(5) | Injected current on NRST pin | ± 4 | |
| | Injected current on OSCIN pin | ± 4 | |
| | Injected current on any other pin (6) | ± 4 | |
| $\Sigma I_{INJ(PIN)}$ (4) | Total injected current (sum of all I/O and control pins) (6) | ± 20 | |

Notes:

(1) Data based on characterization results, not tested in production.

(2) All power (V_{DD} , V_{DDIO} , V_{DDA}) and ground (V_{SS} , V_{SSIO} , V_{SSA}) pins must always be connected to the external supply.

(3) I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package between the V_{DDIO}/V_{SSIO} pins.

(4) $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

(5) Negative injection disturbs the analog performance of the device. See note in [Section 7.11: "TIM2, TIM3 - 16-bit general purpose timers"](#).

(6) When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the

positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ}(PIN)$ maximum current injection on four I/O port pins of the device.

Table 18: Thermal characteristics

| Symbol | Ratings | Value | Unit |
|------------------|------------------------------|------------|------|
| T _{STG} | Storage temperature range | -65 to 150 | °C |
| T _J | Maximum junction temperature | 150 | |

10.3 Operating conditions

The device must be used in operating conditions that respect the parameters in the table below. In addition, full account must be taken of all physical capacitor characteristics and tolerances.

Table 19: General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|--|------|------|------|
| f _{CPU} | Internal CPU clock frequency | | 0 | 16 | MHz |
| V _{DD} / V _{DD_IO} | Standard operating voltage | | 2.95 | 5.5 | V |
| VCAP ⁽¹⁾ | C _{EXT} : capacitance of external capacitor | | 470 | 3300 | nF |
| | ESR of external capacitor | at 1 MHz ⁽²⁾ | - | 0.3 | Ohm |
| | ESL of external capacitor | | - | 15 | nH |
| P _D ⁽³⁾ | Power dissipation at T _A = 85 °C for suffix 6or T _A = 125° C for suffix 3 | 44 and 48-pin devices, with output on eight standard ports, two high sink ports and two open drain ports simultaneously ⁽⁴⁾ | - | 443 | mW |
| | | 32-pin package, with output on eight standard ports and two high sink ports simultaneously ⁽⁴⁾ | - | 360 | |
| T _A | Ambient temperature for 6 suffix version | Maximum power dissipation | -40 | 85 | °C |
| | Ambient temperature for 3 suffix version | Maximum power dissipation | -40 | 125 | |
| T _J | Junction temperature range | 6 suffix version | -40 | 105 | |
| | | 3 suffix version | -40 | 130 | |

Notes:

(1) Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.

(2) This frequency of 1 MHz as a condition for VCAP parameters is given by design of internal regulator.

(3) To calculate P_{Dmax}(T_A), use the formula $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ (see [Section 7.7: "Watchdog timers"](#)) with the value for T_{Jmax} given in the current table and the value for θ_{JA} given in [Section 7.7: "Watchdog timers"](#).

(4) Refer to [Section 7.7: "Watchdog timers"](#)

Figure 11: f_{CPU}max versus V_{DD}

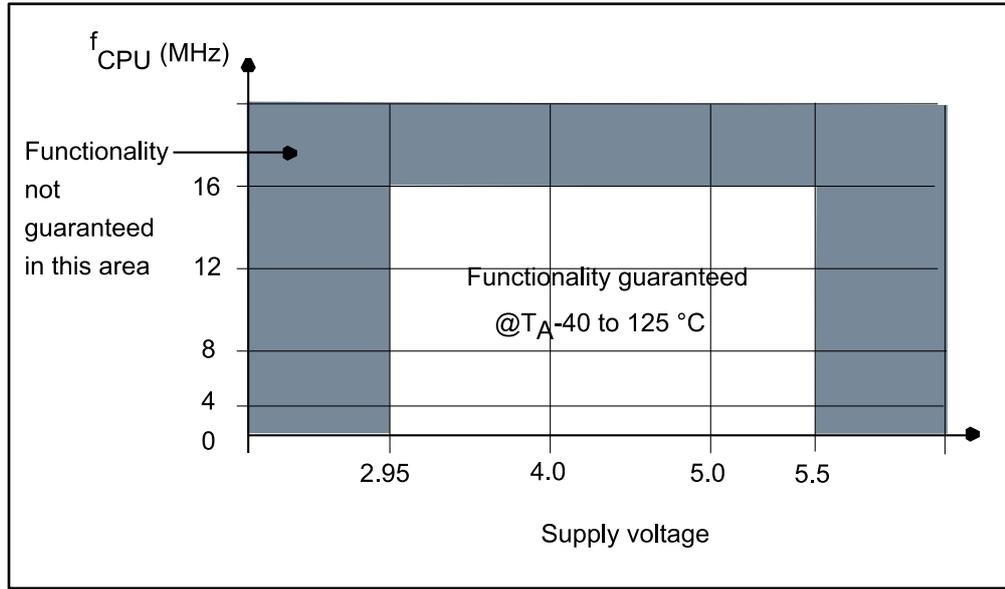


Table 20: Operating conditions at power-up/power-down

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--------------------------------|------------------------|--------------------|-----|--------------------|------|
| t _{VDD} | V _{DD} rise time rate | | 2.0 ⁽¹⁾ | | ∞ | μs/V |
| | V _{DD} fall time rate | | 2.0 ⁽¹⁾ | | ∞ | |
| t _{TEMP} | Reset releasedelay | V _{DD} rising | | | 1.7 ⁽¹⁾ | ms |
| V _{IT+} | Power-on reset threshold | | 2.65 | 2.8 | 2.95 | V |
| V _{IT-} | Brown-out reset threshold | | 2.58 | 2.7 | 2.88 | |
| V _{HYS(BOR)} | Brown-out reset hysteresis | | | 70 | | mV |

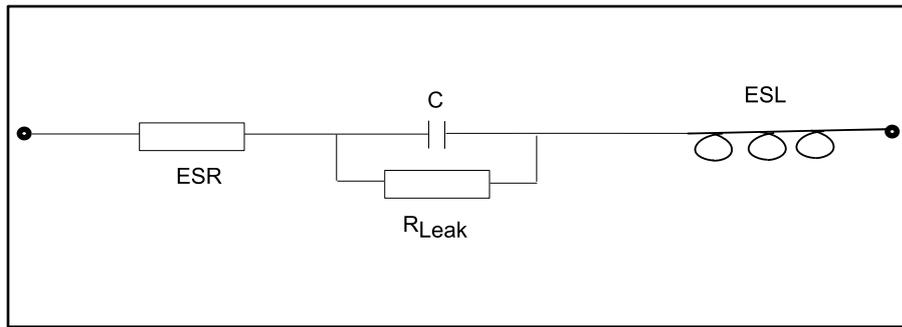
Notes:

⁽¹⁾ Guaranteed by design, not tested in production.

10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in the Operating conditions section. Care should be taken to limit the series inductance to less than 15 nH.

Figure 12: External capacitor CEXT



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as described in [Section 7.3: "Interrupt controller"](#).

10.3.2.1 Total current consumption in run mode

Table 21: Total current consumption with code execution in run mode at VDD = 5 V

| Symbol | Parameter | Conditions | | Typ | Max (1) | Unit |
|--|--|--|------------------------------|------|------------|------|
| I _{DD(RUN)} | Supply current in run mode, code executed from RAM | f _{CPU} = f _{MASTER} = 16 MHz | HSE crystal osc. (16 MHz) | 3.2 | | mA |
| | | | HSE user ext. clock (16 MHz) | 2.6 | 3.2 | |
| | | | HSI RC osc. (16 MHz) | 2.5 | 3.2 | |
| | | f _{CPU} = f _{MASTER} /128 = 125 kHz | HSE user ext. clock (16 MHz) | 1.6 | 2.2 | |
| | | | HSI RC osc. (16 MHz) | 1.3 | 2.0 | |
| | | f _{CPU} = f _{MASTER} /128 = 15.625 kHz | HSI RC osc. (16 MHz/8) | 0.75 | | |
| f _{CPU} = f _{MASTER} = 128 kHz | LSI RC osc. (128 kHz) | 0.55 | | | | |
| I _{DD(RUN)} | Supply current in run mode, code executed from Flash | f _{CPU} = f _{MASTER} = 16 MHz | HSE crystal osc. (16 MHz) | 7.7 | | |
| | | | HSE user ext. clock (16 MHz) | 7.0 | 8.0 | |
| | | | HSI RC osc. (16 MHz) | 7.0 | 8.0 | |
| | | f _{CPU} = f _{MASTER} | HSI RC osc. | 1.5 | | |

| Symbol | Parameter | Conditions | | Typ | Max ⁽¹⁾ | Unit |
|--------|-----------|---|---------------------------|------|--------------------|------|
| | | = 2 MHz | (16 MHz/8) ⁽²⁾ | | | |
| | | $f_{CPU} = f_{MASTER}/128 = 125 \text{ kHz}$ | HSI RC osc. (16 MHz) | 1.35 | 2.0 | |
| | | $f_{CPU} = f_{MASTER}/128 = 15.625 \text{ kHz}$ | HSI RC osc. (16 MHz/8) | 0.75 | | |
| | | $f_{CPU} = f_{MASTER} = 128 \text{ kHz}$ | LSI RC osc. (128 kHz) | 0.6 | | |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production.

⁽²⁾ Default clock configuration measured with all peripherals off.

Table 22: Total current consumption with code execution in run mode at VDD = 3.3 V

| Symbol | Parameter | Conditions | | Typ | Max ⁽¹⁾ | Unit |
|--|--|---|------------------------------|------|--------------------|------|
| I _{DD(RUN)} | Supply current in run mode, code executed from RAM | $f_{CPU} = f_{MASTER} = 16 \text{ MHz}$ | HSE crystal osc. (16 MHz) | 2.8 | | mA |
| | | | HSE user ext. clock (16 MHz) | 2.6 | 3.2 | |
| | | | HSI RC osc. (16 MHz) | 2.5 | 3.2 | |
| | | $f_{CPU} = f_{MASTER}/128 = 125 \text{ kHz}$ | HSE user ext. clock (16 MHz) | 1.6 | 2.2 | |
| | | | HSI RC osc. (16 MHz) | 1.3 | 2.0 | |
| | | $f_{CPU} = f_{MASTER}/128 = 15.625 \text{ kHz}$ | HSI RC osc. (16 MHz/8) | 0.75 | | |
| | $f_{CPU} = f_{MASTER} = 128 \text{ kHz}$ | LSI RC osc. (128 kHz) | 0.55 | | | |
| | Supply current in run mode, code executed from Flash | $f_{CPU} = f_{MASTER} = 16 \text{ MHz}$ | HSE crystal osc. (16 MHz) | 7.3 | | |
| | | | HSE user ext. clock (16 MHz) | 7.0 | 8.0 | |
| | | | HSI RC osc. (16 MHz) | 7.0 | 8.0 | |
| $f_{CPU} = f_{MASTER} = 2 \text{ MHz}$ | | HSI RC osc. (16 MHz/8) ⁽²⁾ | 1.5 | | | |

| Symbol | Parameter | Conditions | | Typ | Max ⁽¹⁾ | Unit |
|--------|-----------|---|------------------------|------|--------------------|------|
| | | $f_{CPU} = f_{MASTER}/128 = 125 \text{ kHz}$ | HSI RC osc. (16 MHz) | 1.35 | 2.0 | |
| | | $f_{CPU} = f_{MASTER}/128 = 15.625 \text{ kHz}$ | HSI RC osc. (16 MHz/8) | 0.75 | | |
| | | $f_{CPU} = f_{MASTER} = 128 \text{ kHz}$ | LSI RC osc. (128 kHz) | 0.6 | | |

Notes:

- (1) Data based on characterization results, not tested in production.
- (2) Default clock configuration measured with all peripherals off.

10.3.2.2 Total current consumption in wait mode

Table 23: Total current consumption in wait mode at VDD = 5 V

| Symbol | Parameter | Conditions | | Typ | Max ⁽¹⁾ | Unit |
|---------------|-----------------------------|---|---------------------------------------|------|--------------------|------|
| $I_{DD(WFI)}$ | Supply current in wait mode | $f_{CPU} = f_{MASTER} = 16 \text{ MHz}$ | HSE crystal osc. (16 MHz) | 2.15 | | mA |
| | | | HSE user ext. clock (16 MHz) | 1.55 | 2.0 | |
| | | | HSI RC osc. (16 MHz) | 1.5 | 1.9 | |
| | | $f_{CPU} = f_{MASTER}/128 = 125 \text{ kHz}$ | HSI RC osc. (16 MHz) | 1.3 | | |
| | | $f_{CPU} = f_{MASTER}/128 = 15.625 \text{ kHz}$ | HSI RC osc. (16 MHz/8) ⁽²⁾ | 0.7 | | |
| | | $f_{CPU} = f_{MASTER} = 128 \text{ kHz}$ | LSI RC osc. (128 kHz) | 0.5 | | |

Notes:

- (1) Data based on characterization results, not tested in production.
- (2) Default clock configuration measured with all peripherals off.

Table 24: Total current consumption in wait mode at VDD = 3.3 V

| Symbol | Parameter | Conditions | | Typ | Max ⁽¹⁾ | Unit |
|---------------|-----------------------------|---|---------------------------|------|--------------------|------|
| $I_{DD(WFI)}$ | Supply current in wait mode | $f_{CPU} = f_{MASTER} = 16 \text{ MHz}$ | HSE crystal osc. (16 MHz) | 1.75 | | mA |
| | | | HSE user ext. clock | 1.55 | 2.0 | |

| Symbol | Parameter | Conditions | Typ | Max (1) | Unit |
|--------|-----------|--|-----|------------|------|
| | | (16 MHz) | | | |
| | | HSI RC osc. (16 MHz) | 1.5 | 1.9 | |
| | | $f_{\text{CPU}} = f_{\text{MASTER}}/128 = 125$ kHz | 1.3 | | |
| | | HSI RC osc. (16 MHz) | 1.3 | | |
| | | $f_{\text{CPU}} = f_{\text{MASTER}}/128 =$ 15.625 kHz | 0.7 | | |
| | | HSI RC osc. (16 MHz/8) (2) | 0.7 | | |
| | | $f_{\text{CPU}} = f_{\text{MASTER}} = 128$ kHz | 0.5 | | |
| | | LSI RC osc. (128 kHz) | 0.5 | | |

Notes:

(1) Data based on characterization results, not tested in production.

(2) Default clock configuration measured with all peripherals off.

10.3.2.3 Total current consumption in active halt mode**Table 25: Total current consumption in active halt mode at VDD = 5 V**

| Symbol | Parameter | Conditions | | | Typ | Max at 85 °C (1) | Max at 125 °C (1) | Unit |
|---------------------|--|--|------------------------|---------------------------------------|------|------------------------|-------------------------|------|
| | | Main voltage regulator (MVR) (2) | Flash mode (3) | Clock source | | | | |
| I _{DD(AH)} | Supply current in active halt mode | On | Operating mode | HSE crystal osc. (16 MHz) | 1080 | | | µA |
| | | | | LSI RC osc. (128 kHz) | 200 | 320 | 400 | |
| | | | Power- down mode | HSE crystal osc. (16 MHz) | 1030 | | | |
| | | | | LSI RC osc. (128 kHz) | 140 | 270 | 350 | |
| | | Off | Operating mode | LSI RC osc. (128 kHz) | 68 | 120 | 220 | |
| | | | Power- down mode | LSI RC osc. (128 kHz) | 12 | 60 | 150 | |

Notes:

- (1) Data based on characterization results, not tested in production
 (2) Configured by the REGAH bit in the CLK_ICKR register.
 (3) Configured by the AHALT bit in the FLASH_CR1 register.

Table 26: Total current consumption in active halt mode at VDD = 3.3 V

| Symbol | Parameter | Conditions | | | Typ | Max at 85 °C ⁽¹⁾ | Max at 125 °C ⁽¹⁾ | Unit |
|---------------------|------------------------------------|---|---------------------------|---------------------------|-----|-----------------------------|------------------------------|------|
| | | Main voltage regulator (MVR) ⁽²⁾ | Flash mode ⁽³⁾ | Clock source | | | | |
| I _{DD(AH)} | Supply current in active halt mode | On | Operating mode | HSE crystal osc. (16 MHz) | 680 | | | μA |
| | | | | LSI RC osc. (128 kHz) | 200 | 320 | 400 | |
| | | | Power-down mode | HSE crystal osc. (16 MHz) | 630 | | | |
| | | | | LSI RC osc. (128 kHz) | 140 | 270 | 350 | |
| | | Off | Operating mode | LSI RC osc. (128 kHz) | 66 | 120 | 220 | |
| | | | Power-down mode | | 10 | 60 | 150 | |

Notes:

- (1) Data based on characterization results, not tested in production.
 (2) Configured by the REGAH bit in the CLK_ICKR register.
 (3) Configured by the AHALT bit in the FLASH_CR1 register.

10.3.2.4 Total current consumption in halt mode**Table 27: Total current consumption in halt mode at VDD = 5 V**

| Symbol | Parameter | Conditions | Typ | Max at 85 °C ⁽¹⁾ | Max at 125 °C ⁽¹⁾ | Unit |
|--------------------|-----------------------------|---|-----|-----------------------------|------------------------------|------|
| I _{DD(H)} | Supply current in halt mode | Flash in operating mode, HSI clock after wakeup | 62 | 90 | 150 | μA |
| | | Flash in powerdown mode, HSI clock after wakeup | 6.5 | 25 | 80 | |

Notes:

- (1) Data based on characterization results, not tested in production.

Table 28: Total current consumption in halt mode at VDD = 3.3 V

| Symbol | Parameter | Conditions | Typ | Max at 85 °C ⁽¹⁾ | Max at 125 °C ⁽¹⁾ | Unit |
|--------------------|-----------------------------|---|-----|-----------------------------|------------------------------|------|
| I _{DD(H)} | Supply current in halt mode | Flash in operating mode, HSI clock after wakeup | 60 | 90 | 150 | µA |
| | | Flash in powerdown mode, HSI clock after wakeup | 4.5 | 20 | 80 | |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production.

10.3.2.5 Low power mode wakeup times

Table 29: Wakeup times

| Symbol | Parameter | Conditions | | | Typ | Max ⁽¹⁾ | Unit |
|----------------------|---|---|---|--------------------|-------------------|-------------------------|------|
| t _{WU(WFI)} | Wakeup time from wait mode to run mode ⁽²⁾ | 0 to 16 MHz | | | | See note ⁽³⁾ | µs |
| | | f _{CPU} = f _{MASTER} = 16 MHz | | | 0.56 | | |
| t _{WU(AH)} | Wakeup time active halt mode to run mode ⁽²⁾ | MVR voltage regulator on ⁽⁴⁾ | Flash in operating mode ⁽⁵⁾ | HSI (after wakeup) | 1 ⁽⁶⁾ | 2 ⁽⁶⁾ | |
| | Wakeup time active halt mode to run mode ⁽²⁾ | MVR voltage regulator on ⁽⁴⁾ | Flash in power-down mode ⁽⁵⁾ | HSI (after wakeup) | 3 ⁽⁶⁾ | | |
| | Wakeup time active halt mode to run mode ⁽²⁾ | MVR voltage regulator off ⁽⁴⁾ | Flash in operating mode ⁽⁵⁾ | HSI (after wakeup) | 48 ⁽⁶⁾ | | |
| | Wakeup time active halt mode to run mode ⁽²⁾ | MVR voltage regulator off ⁽⁴⁾ | Flash in power-down mode ⁽⁵⁾ | HSI (after wakeup) | 50 ⁽⁶⁾ | | |
| t _{WU(H)} | Wakeup time from halt mode to run mode ⁽²⁾ | Flash in operating mode ⁽⁵⁾ | | | 52 | | |
| | | Flash in power-down mode ⁽⁵⁾ | | | 54 | | |

Notes:

⁽¹⁾ Data guaranteed by design, not tested in production.

⁽²⁾ Measured from interrupt event to interrupt vector fetch.

⁽³⁾ t_{WU(WFI)} = 2 x 1/f_{master} + 67 x 1/f_{CPU}.

⁽⁴⁾ Configured by the REGAH bit in the CLK_ICR register.

⁽⁵⁾ Configured by the AHALT bit in the FLASH_CR1 register.



⁽⁶⁾ Plus 1 LSI clock depending on synchronization.

10.3.2.6 Total current consumption and timing in forced reset state

Table 30: Total current consumption and timing in forced reset state

| Symbol | Parameter | Conditions | Typ | Max ⁽¹⁾ | Unit |
|----------------------|--|-------------------------|-----|--------------------|------|
| I _{DD(R)} | Supply current in reset state ⁽²⁾ | V _{DD} = 5 V | 500 | | μA |
| | | V _{DD} = 3.3 V | 400 | | |
| t _{RESETBL} | Reset pin release to vector fetch | | | 150 | μs |

Notes:

⁽¹⁾ Data guaranteed by design, not tested in production.

⁽²⁾ Characterized with all I/Os tied to V_{SS}.

10.3.2.7 Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz.

Table 31: Peripheral current consumption

| Symbol | Parameter | Typ. | Unit |
|---------------------------------|--|------|------|
| I _{DD(TIM1)} | TIM1 supply current ⁽¹⁾ | 230 | μA |
| I _{DD(TIM2)} | TIM2 supply current ⁽¹⁾ | 115 | |
| I _{DD(TIM3)} | TIM3 timer supply current ⁽¹⁾ | 90 | |
| I _{DD(TIM4)} | TIM4 timer supply current ⁽¹⁾ | 30 | |
| I _{DD(UART2)} | UART2 supply current ⁽²⁾ | 110 | |
| I _{DD(SPI)} | SPI supply current ⁽²⁾ | 45 | |
| I _{DD(I²C)} | I ² C supply current ⁽²⁾ | 65 | |
| I _{DD(ADC1)} | ADC1 supply current when converting ⁽³⁾ | 955 | |

Notes:

⁽¹⁾ Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.

⁽²⁾ Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.

⁽³⁾ Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

10.3.2.8 Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

Figure 13: Typ. $I_{DD}(RUN)$ vs. V_{DD} , HSE user external clock, $f_{CPU} = 16$ MHz

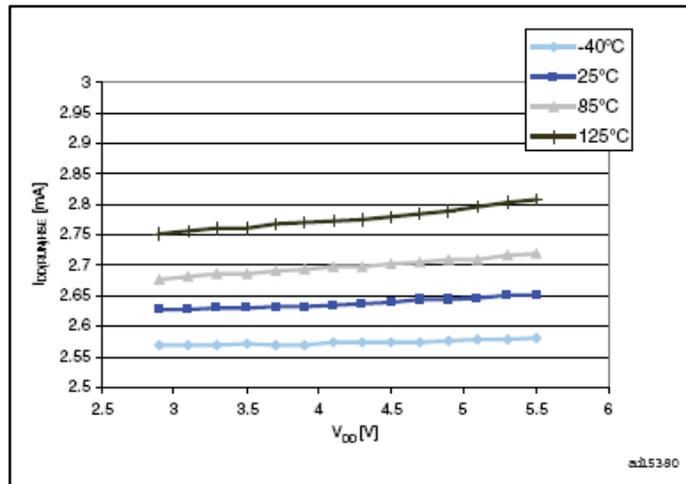


Figure 14: Typ. $I_{DD}(RUN)$ vs. f_{CPU} , HSE user external clock, $V_{DD} = 5$ V

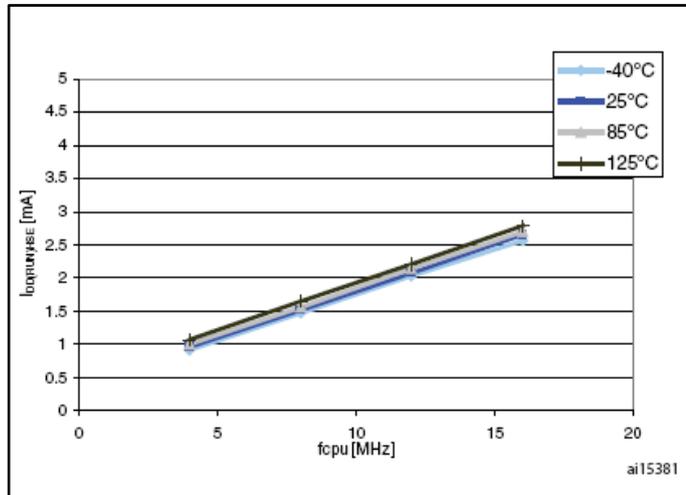


Figure 15: Typ. $I_{DD}(RUN)$ vs. V_{DD} , HSI RC osc, $f_{CPU} = 16$ MHz

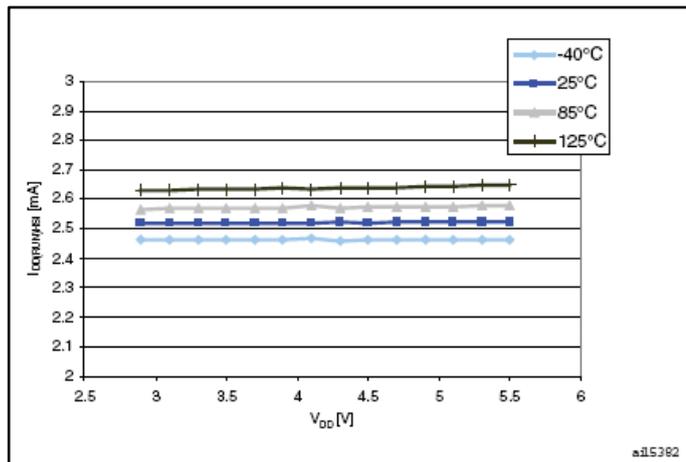


Figure 16: Typ. IDD(WFI) vs. VDD, HSE user external clock, fCPU = 16 MHz

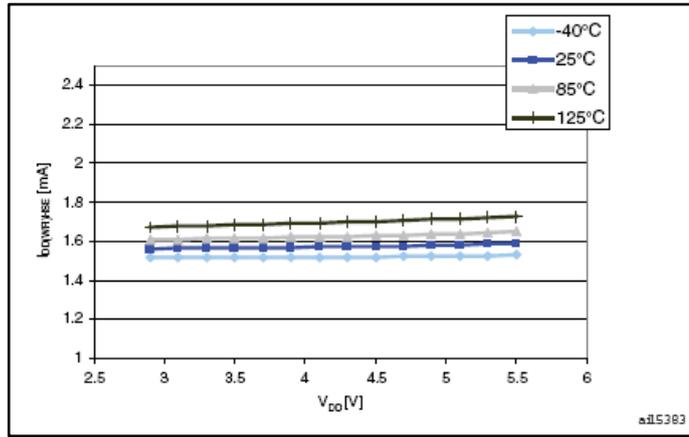


Figure 17: Typ. IDD(WFI) vs. fCPU, HSE user external clock VDD = 5 V

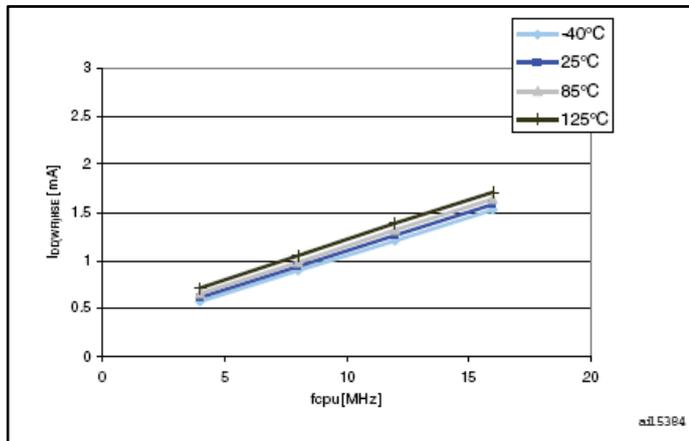
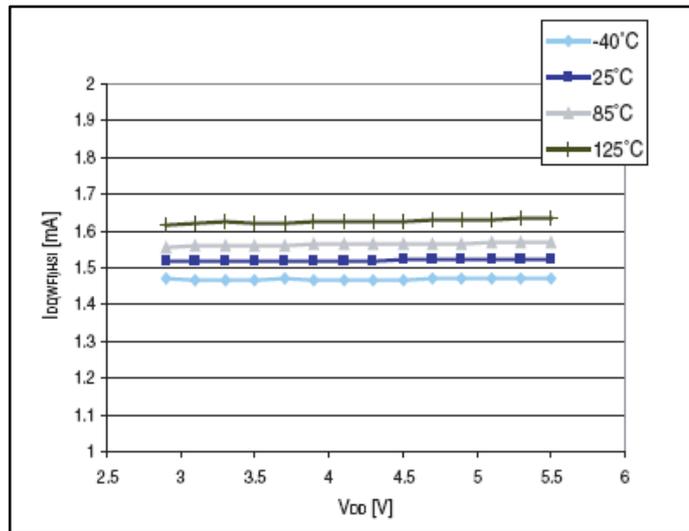


Figure 18: Typ. IDD(WFI) vs. VDD, HSI RC osc, fCPU = 16 MHz



10.3.3 External clock sources and timing characteristics

HSE user external clock

Subject to general operating conditions for V_{DD} and T_A .

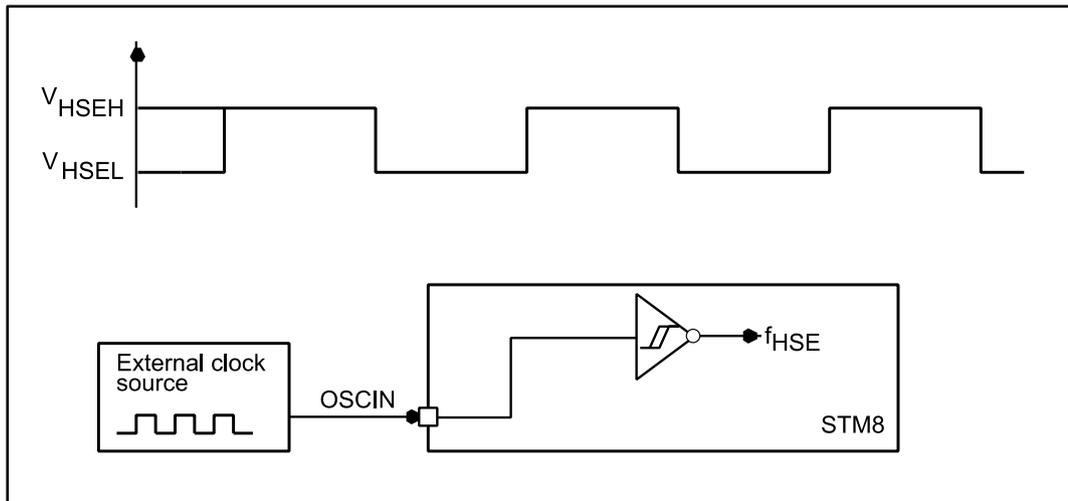
Table 32: HSE user external clock characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|--------------------------------------|----------------------------|---------------------|---------------------|---------|
| f_{HSE_ext} | User external clock source frequency | | 0 | 16 | MHz |
| $V_{HSEH}^{(1)}$ | OSCIN input pin high level voltage | | $0.7 \times V_{DD}$ | $V_{DD} + 0.3 V$ | V |
| $V_{HSEL}^{(1)}$ | OSCIN input pin low level voltage | | V_{SS} | $0.3 \times V_{DD}$ | V |
| I_{LEAK_HSE} | OSCIN input leakage current | $V_{SS} < V_{IN} < V_{DD}$ | -1 | +1 | μA |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production.

Figure 19: HSE external clocksource



HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 33: HSE oscillator characteristics

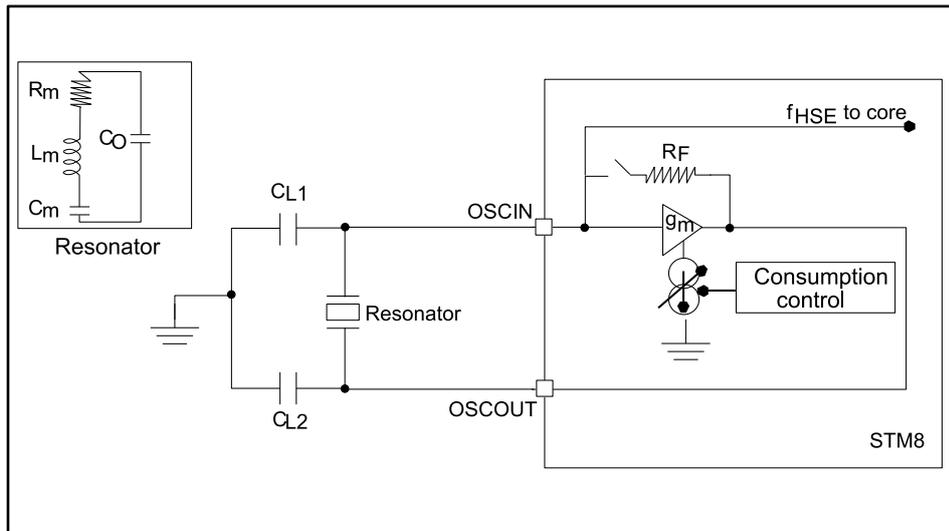
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--|------------|-----|-----|-----|------------|
| f_{HSE} | External high speed oscillator frequency | | 1 | | 16 | MHz |
| R_F | Feedback resistor | | | 220 | | k Ω |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|---|---|-----|-----|--|------|
| C ⁽¹⁾ | Recommended load capacitance ⁽²⁾ | | | | 20 | pF |
| I _{DD(HSE)} | HSE oscillator power consumption | C = 20 pF, f _{OSC} = 16 MHz | | | 6 (startup) 1.6 (stabilized) ⁽³⁾ | mA |
| | | C = 10 pF, f _{OSC} = 16 MHz | | | 6 (startup) 1.2 (stabilized) ⁽³⁾ | |
| g _m | Oscillator transconductance | | 5 | | | mA/V |
| t _{SU(HSE)} ⁽⁴⁾ | Startup time | V _{DD} is stabilized | | 1 | | ms |

Notes:

- (1) C is approximately equivalent to 2 x crystal Cload.
- (2) The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
- (3) Data based on characterization results, not tested in production.
- (4) t_{SU(HSE)} is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 20: HSE oscillator circuit diagram



HSE oscillator critical g_m equation

$$g_{m\text{crit}} = (2 \times \pi \times f_{\text{HSE}})^2 \times R_m(2C_o + C)^2$$

R_m: Notional resistance (see crystal specification)

L_m: Notional inductance (see crystal specification)

C_m: Notional capacitance (see crystal specification)

C_o: Shunt capacitance (see crystal specification)

C_{L1} = C_{L2} = C: Grounded external capacitance

g_m >> g_mcrit

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A .

High speed internal RC oscillator (HSI)

Table 34: HSI oscillator characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|---|--|---------------------|-----|--------------------|---------------|
| f_{HSI} | Frequency | | | 16 | | MHz |
| ACC_{HSI} | Accuracy of HSI oscillator | User-trimmed with CLK_HSITRIMR register for given V_{DD} and T_A conditions ⁽¹⁾ | | | 1.0 ⁽²⁾ | % |
| | Accuracy of HSI oscillator (factory calibrated) | $V_{DD} = 5\text{ V}, T_A = 25^\circ\text{C}$ ⁽³⁾ | -1.0 | | 1.0 | |
| | | $V_{DD} = 5\text{ V}, 25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | -2.0 | | 2.0 | |
| | | $2.95 \leq V_{DD} \leq 5.5\text{ V}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | -3.0 ⁽³⁾ | | 3.0 ⁽³⁾ | |
| $t_{su(HSI)}$ | HSI oscillator wake-up time including calibration | | | | 1.0 ⁽²⁾ | μs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 170 | 250 ⁽³⁾ | μA |

Notes:

- ⁽¹⁾ Refer to application note.
- ⁽²⁾ Guaranteed by design, not tested in production.
- ⁽³⁾ Data based on characterization results, not tested in production.

Figure 21: Typical HSI accuracy at $V_{DD} = 5\text{ V}$ vs 5 temperatures

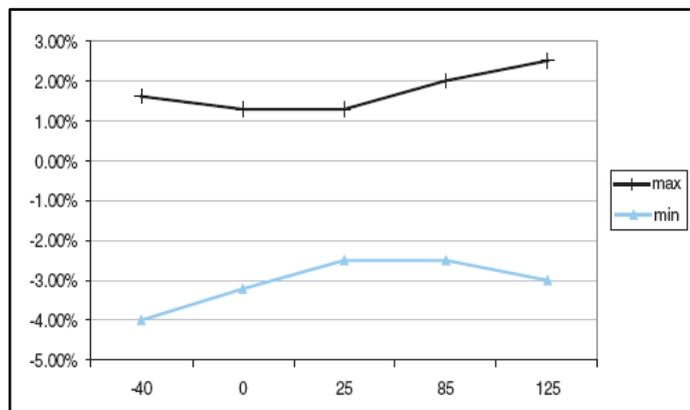
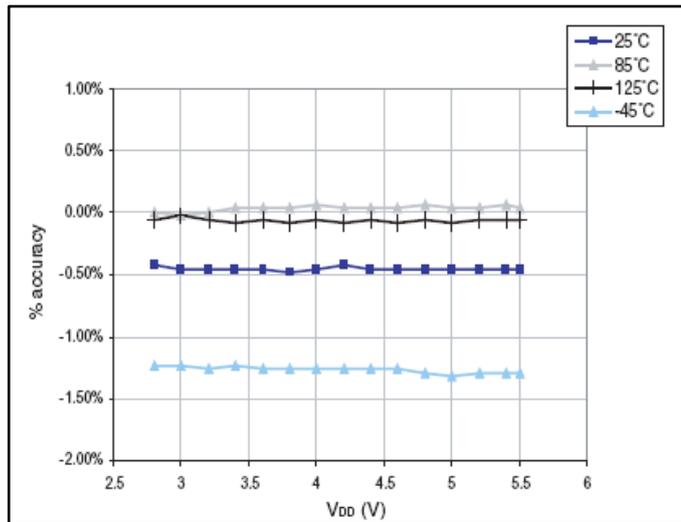


Figure 22: Typical HSI accuracy vs VDD @ 4 temperatures



Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

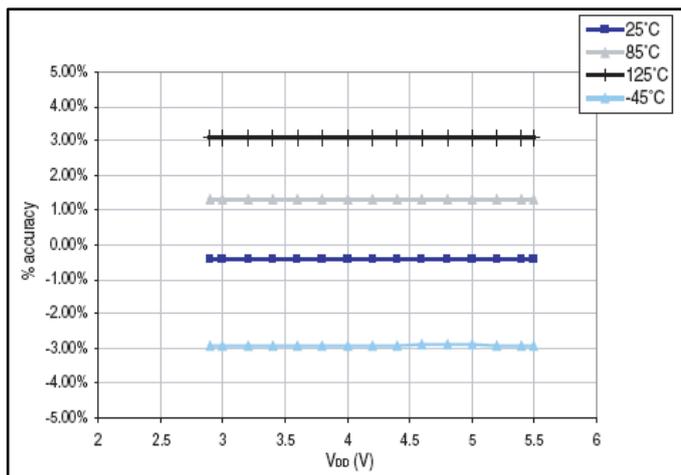
Table 35: LSI oscillator characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------------------|----------------------------------|-----|-----|------------------|------|
| f _{LSI} | Frequency | 110 | 128 | 146 | kHz |
| t _{su(LSI)} | LSI oscillator wakeup time | | | 7 ⁽¹⁾ | µs |
| I _{DD(LSI)} | LSI oscillator power consumption | | 5 | | µA |

Notes:

⁽¹⁾ Guaranteed by design, not tested in production.

Figure 23: Typical LSI accuracy vs VDD @ 4 temperatures



10.3.5 Memory characteristics

RAM and hardware registers

Table 36: RAM and hardware registers

| Symbol | Parameter | Conditions | Min | Unit |
|----------|------------------------------------|----------------------|-----------------------------|------|
| V_{RM} | Data retention mode ⁽¹⁾ | Halt mode (or reset) | V_{IT-max} ⁽²⁾ | V |

Notes:

⁽¹⁾ Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production. refer to [Section 7.10: "TIM1 - 16-bit advanced control timer"](#) for the value of V_{IT-max}

⁽²⁾ Refer to the Operating conditions section for the value of V_{IT-max}

Flash program memory/data EEPROM memory

General conditions: $T_A = -40$ to 125°C .

Table 37: Flash program memory/data EEPROM memory

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max | Unit |
|-------------|--|------------------------------|--------------------|------|-----|--------|
| V_{DD} | Operating voltage (all modes, execution/write/erase) | $f_{CPU} \leq 16$ MHz | 2.95 | | 5.5 | V |
| t_{prog} | Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes) | | | 6.0 | 6.6 | ms |
| | Fast programming time for 1 block (128 bytes) | | | 3.0 | 3.3 | ms |
| t_{erase} | Erase time for 1 block (128 bytes) | | | 3.0 | 3.3 | ms |
| N_{RW} | Erase/write cycles ⁽²⁾ (program memory) | $T_A = +85^\circ\text{C}$ | 10 k | | | cycles |
| | Erase/write cycles(data memory) ⁽²⁾ | $T_A = +125^\circ\text{C}$ | 300 k | 1.0M | | |
| t_{RET} | Data retention (program memory) after 10k erase/write cycles at $T_A = +85^\circ\text{C}$ | $T_{RET} = 55^\circ\text{C}$ | 20 | | | years |
| | Data retention (data memory) after 10k erase/write cycles at $T_A = +85^\circ\text{C}$ | $T_{RET} = 55^\circ\text{C}$ | 20 | | | |
| | Data retention (data memory) after 300 k erase/write cycles at $T_A = +125^\circ\text{C}$ | $T_{RET} = 85^\circ\text{C}$ | 1.0 | | | |
| I_{DD} | Supply current (Flash programming or erasing for 1 to 128 bytes) | | | 2.0 | | mA |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production.

⁽²⁾ The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 38: I/O static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--|--|---------------------|-----|--------------------------|---------------|
| V_{IL} | Input low level voltage | $V_{DD} = 5\text{ V}$ | -0.3 | | $0.3 \times V_{DD}$ | V |
| V_{IH} | Input high level voltage | | $0.7 \times V_{DD}$ | | $V_{DD} + 0.3\text{ V}$ | V |
| V_{hys} | Hysteresis ⁽¹⁾ | | | 700 | | mV |
| R_{pu} | Pull-up resistor | $V_{DD} = 5\text{ V}, V_{IN} = V_{SS}$ | 30 | 55 | 80 | k Ω |
| t_R, t_F | Rise and fall time(10 % - 90 %) | Fast I/Os load = 50 pF | | | 35 ⁽²⁾ | ns |
| | | Standard and high sink I/Os load = 50 pF | | | 125 ⁽²⁾ | |
| | | Fast I/Os load = 20 pF | | | 20 ⁽²⁾ | |
| | | Standard and high sink I/Os load = 20 pF | | | 50 ⁽²⁾ | |
| I_{lkg} | Input leakage current, analog and digital | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ± 1.0 ⁽³⁾ | μA |
| $I_{lkg\text{ ana}}$ | Analog input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ± 250 ⁽³⁾ | nA |
| $I_{lkg(inj)}$ | Leakage current in adjacent I/O ⁽³⁾ | Injection current $\pm 4\text{ mA}$ | | | ± 1.0 ⁽³⁾ | μA |

Notes:

⁽¹⁾ Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.

⁽²⁾ Data guaranteed by design.

⁽³⁾ Data based on characterization results, not tested in production.

Figure 24: Typical VIL and VIH vs VDD @ 4 temperatures

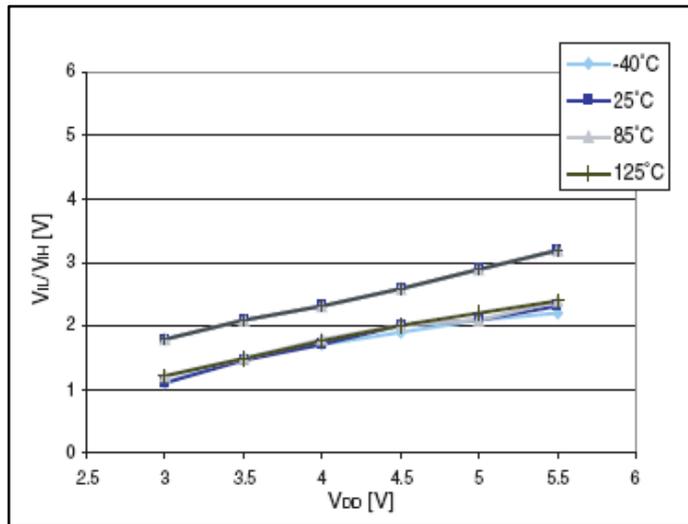


Figure 25: Typical pull-up resistance vs VDD @ 4 temperatures

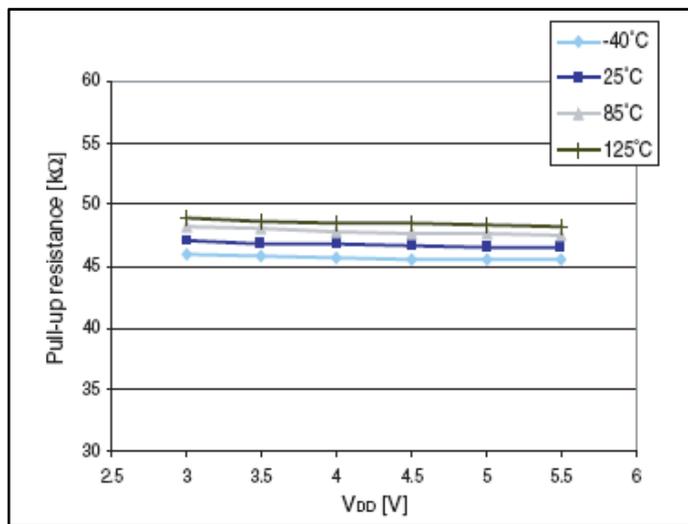
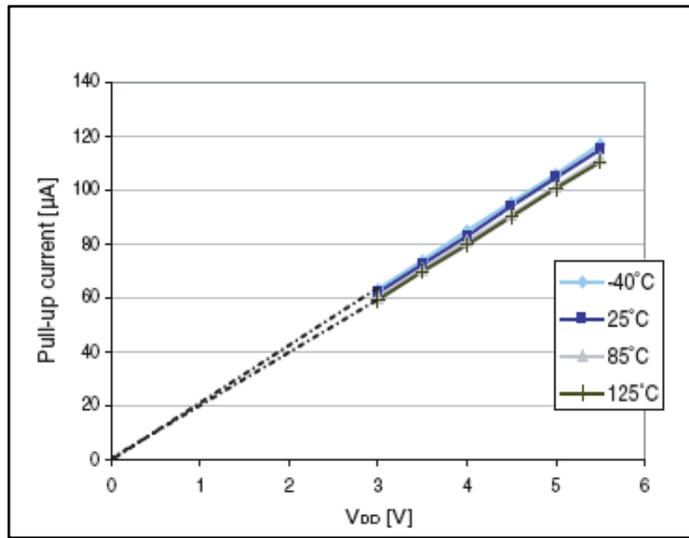


Figure 26: Typical pull-up current vs VDD @ 4 temperatures



1. The pull-up is a pure resistor (slope goes through 0).

Table 39: Output driving current (standard ports)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|---|---|--------------------|--------------------|------|
| V _{OL} | Output low level with four pins sunk | I _{IO} = 4 mA, V _{DD} = 3.3 V | | 1.0 ⁽¹⁾ | V |
| | Output low level with eight pins sunk | I _{IO} = 10 mA, V _{DD} = 5 V | | 2.0 | |
| V _{OH} | Output high level with four pins sourced | I _{IO} = 4 mA, V _{DD} = 3.3 V | 2.0 ⁽¹⁾ | | V |
| | Output high level with eight pins sourced | I _{IO} = 10 mA, V _{DD} = 5 V | 2.4 | | |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production

Table 40: Output driving current (true open drain ports)

| Symbol | Parameter | Conditions | Max | Unit |
|-----------------|-------------------------------------|--|--------------------|------|
| V _{OL} | Output low level with two pins sunk | I _{IO} = 10 mA, V _{DD} = 3.3 V | 1.5 ⁽¹⁾ | V |
| | | I _{IO} = 10 mA, V _{DD} = 5 V | 1.0 | |
| | | I _{IO} = 20 mA, V _{DD} = 5 V | 2.0 ⁽¹⁾ | |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production

Table 41: Output driving current (high sink ports)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|--------------------------------------|--------------------------|-----|--------------------|------|
| V _{OL} | Output low level with four pins sunk | I _{IO} = 10 mA, | | 1.1 ⁽¹⁾ | V |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------|---|--|--------------------|--------------------|------|
| | | $V_{DD} = 3.3\text{ V}$ | | | |
| | Output low level with eight pins sunk | $I_{IO} = 10\text{ mA}$, $V_{DD} = 5\text{ V}$ | | 0.9 | |
| | Output low level with four pins sunk | $I_{IO} = 20\text{ mA}$, $V_{DD} = 5\text{ V}$ | | 1.6 ⁽¹⁾ | |
| V_{OH} | Output high level with four pins sourced | $I_{IO} = 10\text{ mA}$, $V_{DD} = 3.3\text{ V}$ | 1.9 ⁽¹⁾ | | |
| | Output high level with eight pins sourced | $I_{IO} = 10\text{ mA}$, $V_{DD} = 5\text{ V}$ | 3.8 | | |
| | Output high level with four pins sourced | $I_{IO} = 20\text{ mA}$, $V_{DD} = 5\text{ V}$ | 2.9 ⁽¹⁾ | | |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production

10.3.7 Typical output level curves

The following figures show typical output level curves measured with output on a single pin.

Figure 27: Typ. VOL @ VDD = 5 V (standard ports)

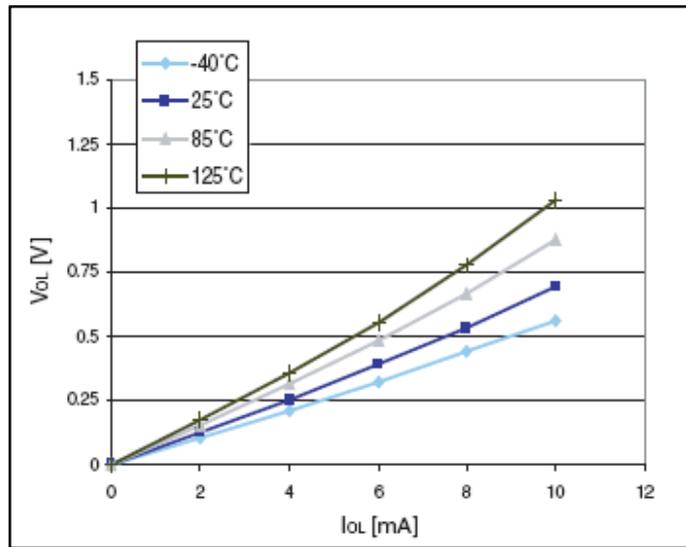


Figure 28: Typ. VOL @ VDD = 3.3 V (standard ports)

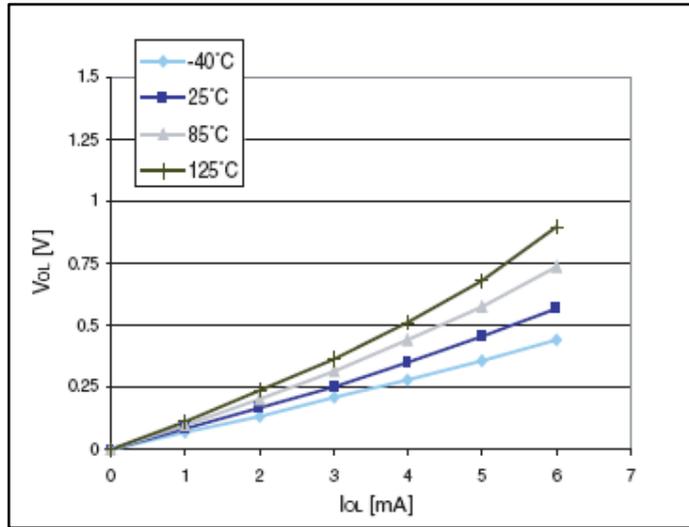


Figure 29: Typ. VOL @ VDD = 5 V (true open drain ports)

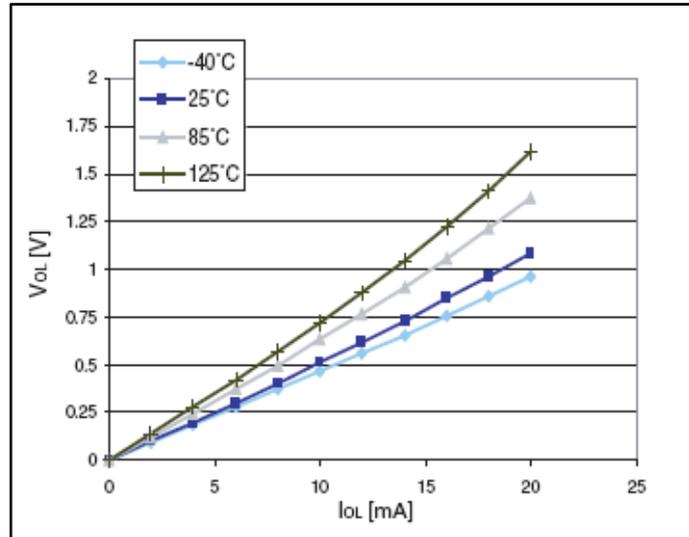


Figure 30: Typ. VOL @ VDD = 3.3 V (true open drain ports)

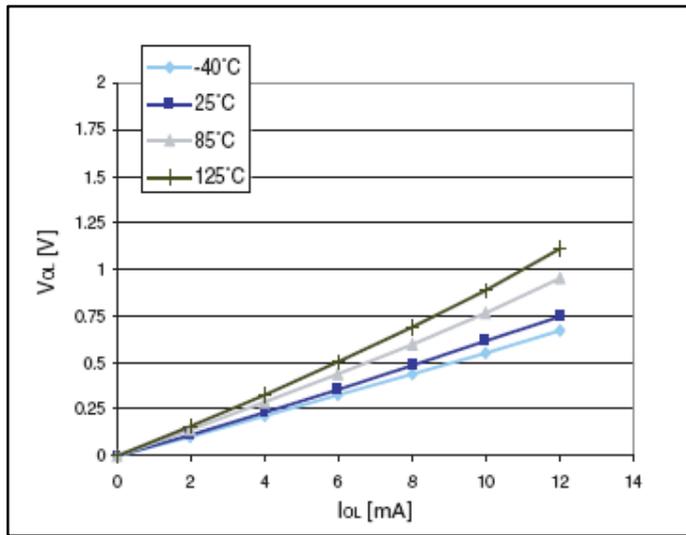


Figure 31: Typ. VOL @ VDD = 5 V (high sink ports)

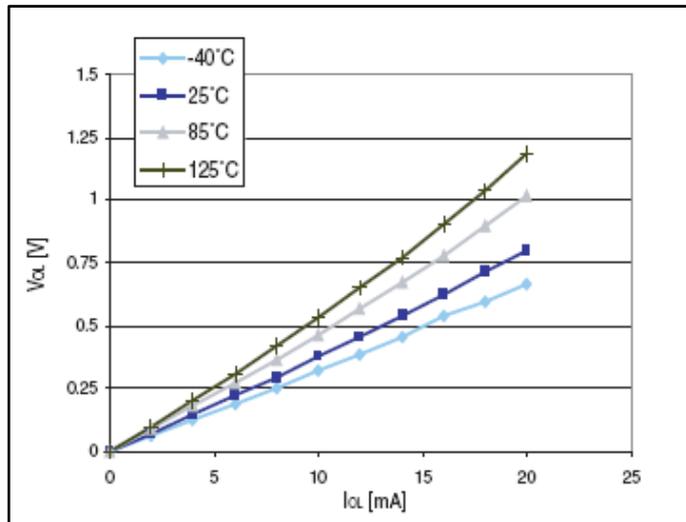


Figure 32: Typ. VOL @ VDD = 3.3 V (high sink ports)

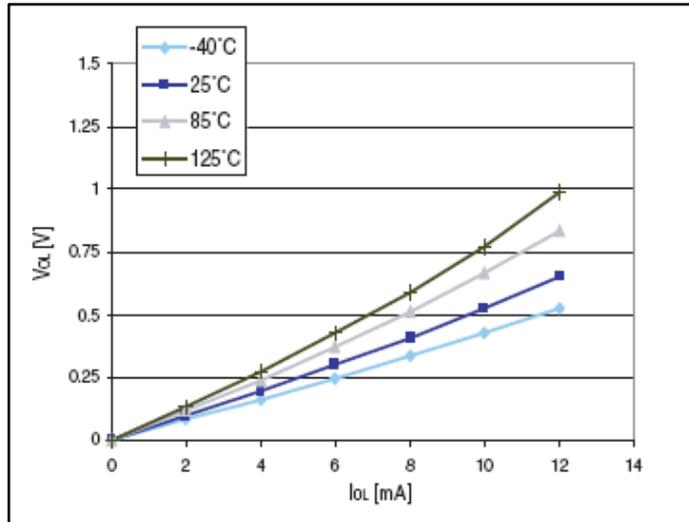


Figure 33: Typ. VDD - VOH @ VDD = 5 V (standard ports)

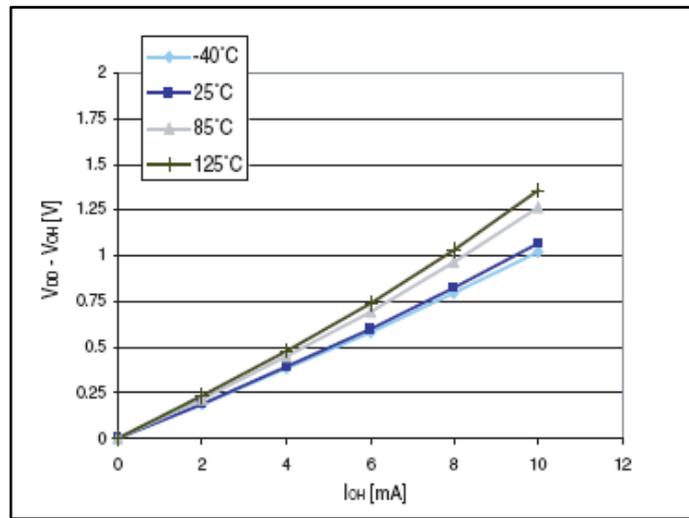


Figure 34: Typ. VDD - VOH @ VDD = 3.3 V (standard ports)

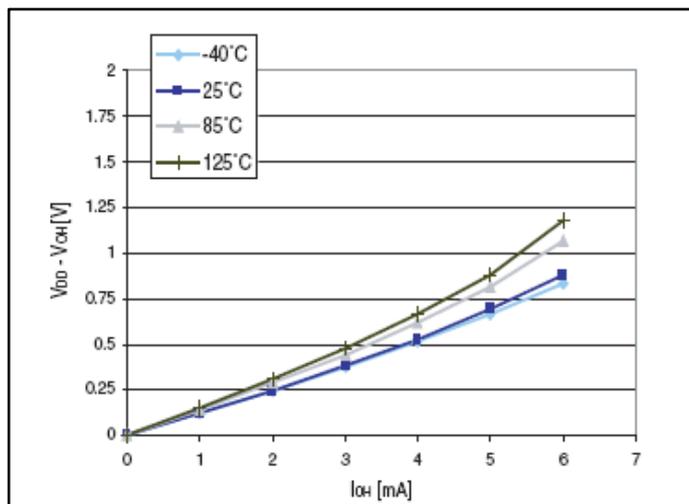


Figure 35: Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (high sink ports)

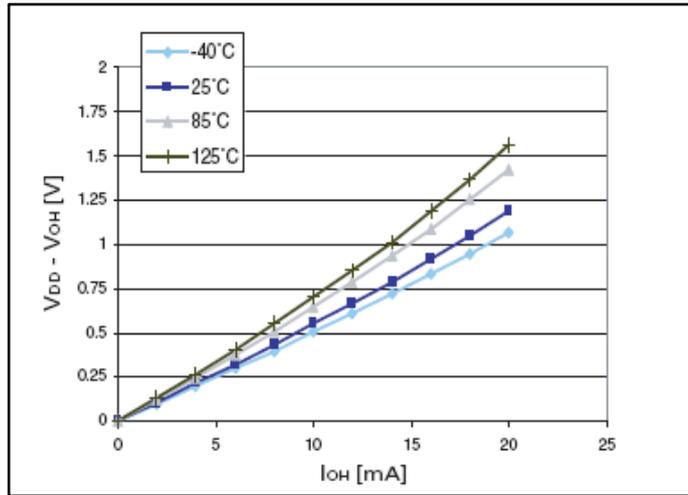
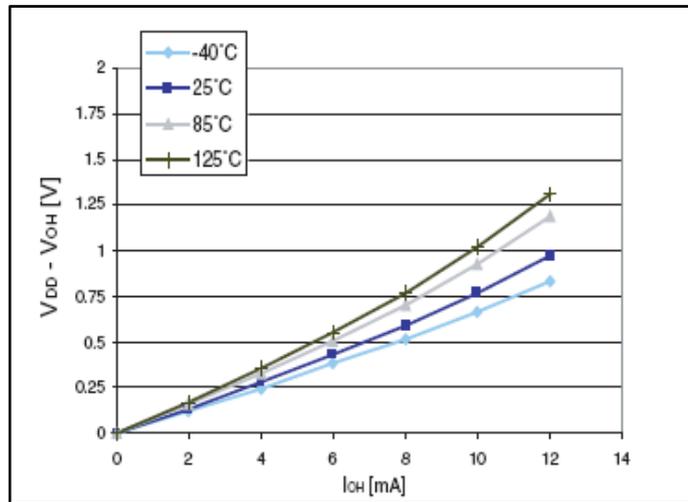


Figure 36: Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)



10.3.8 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42: NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|--|-----------------------|-----------------------|-----|-----------------------|------|
| V _{IL(NRST)} | NRST input low level voltage ⁽¹⁾ | | -0.3 | - | 0.3 x V _{DD} | V |
| V _{IH(NRST)} | NRST input high level voltage ⁽¹⁾ | I _{OL} =2 mA | 0.7 x V _{DD} | - | V _{DD} + 0.3 | |
| V _{OL(NRST)} | NRST output low level voltage ⁽¹⁾ | | - | - | 0.5 | |
| R _{PU(NRST)} | NRST pull-up resistor ⁽²⁾ | | 30 | 55 | 80 | kΩ |
| t _{IFP(NRST)} | NRST input filtered pulse ⁽³⁾ | | - | - | 75 | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--|------------|----------|-----|-----|---------|
| $t_{INFP(NRST)}$ | NRST input not filtered pulse ⁽³⁾ | | 500 | - | - | |
| $t_{OP(NRST)}$ | NRST output pulse ⁽³⁾ | | 20 15 | - | - | μs |

Notes:

- (1) Data based on characterization results, not tested in production.
- (2) The R_{PU} pull-up equivalent resistor is based on a resistive transistor
- (3) Data guaranteed by design, not tested in production.

Figure 37: Typical NRST VIL and VIH vs VDD @ 4 temperatures

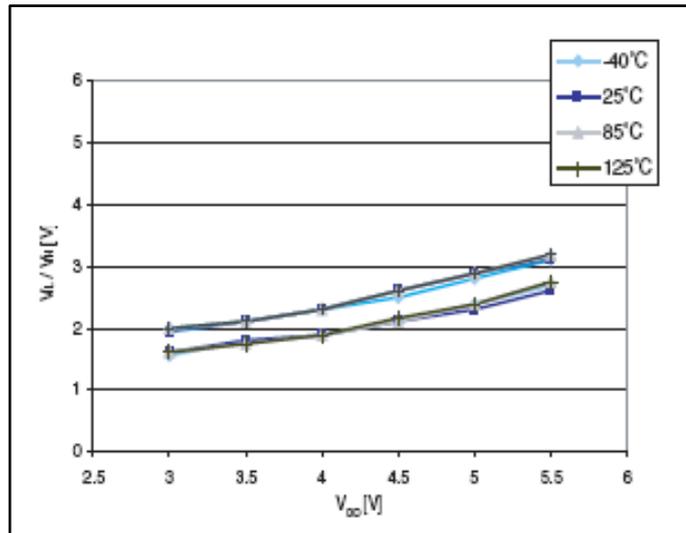


Figure 38: Typical NRST pull-up resistance vs VDD @ 4 temperatures

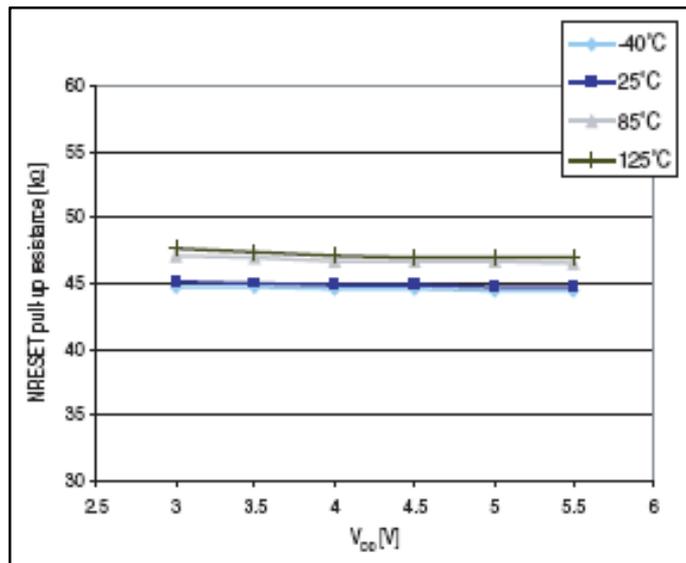
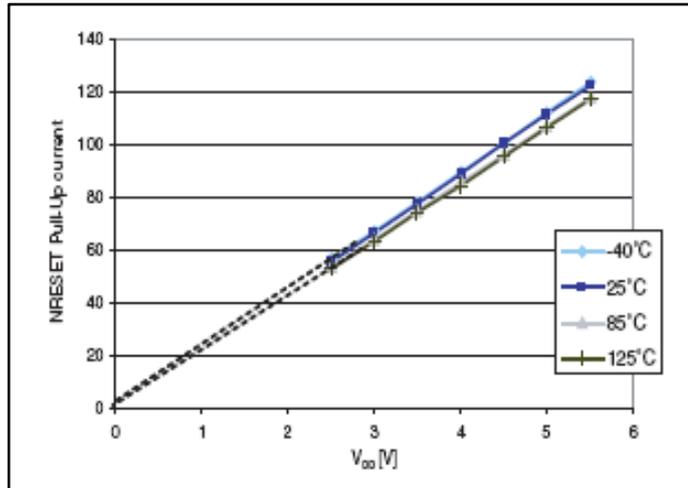


Figure 39: Typical NRST pull-up current vs VDD @ 4 temperatures



The reset network shown in the following figure protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below V_{IL(NRST)} max. (see [Table 38: "I/O static characteristics"](#)), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 100 nF.

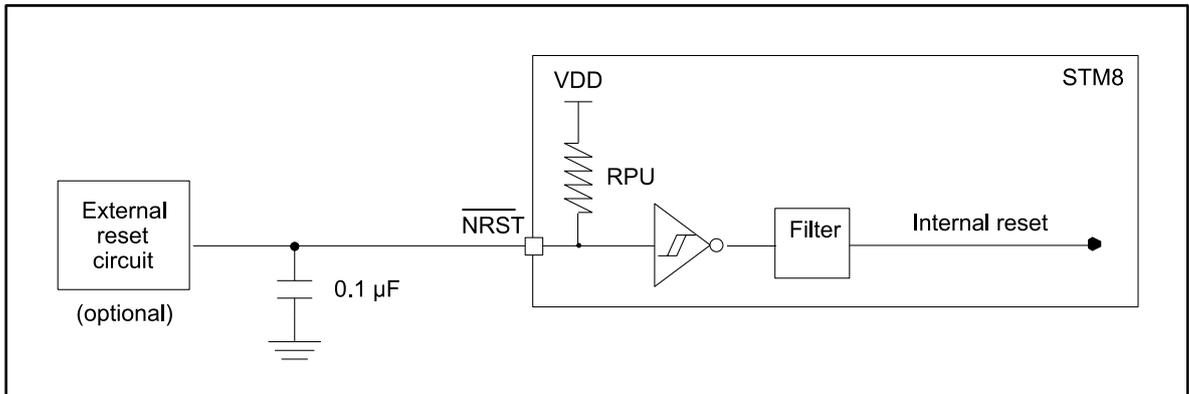


Figure 40: Recommended reset pin protection

10.3.9 SPI serial peripheral interface

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. t_{MASTER} = 1/f_{MASTER}.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 43: SPI characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|------------------------------|------------------------------------|------------------|------------------|------|
| f_{SCK1} | SPI clock frequency | Master mode | 0 | 8 | MHz |
| $t_{c(SCK)}$ | | Slave mode | 0 | 6 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | | 25 | ns |
| $t_{su(NSS)}^{(1)}$ | NSS setup time | Slave mode | 4 x t_{MASTER} | | ns |
| $t_{h(NSS)}^{(1)}$ | NSS hold time | Slave mode | 70 | | ns |
| $t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$ | SCK high and low time | Master mode | $t_{SCK}/2 - 15$ | $t_{SCK}/2 + 15$ | ns |
| $t_{su(MI)}^{(1)}$ | Data input setup time | Master mode | 5 | | ns |
| $t_{su(SI)}^{(1)}$ | Data input setup time | Slave mode | 5 | | ns |
| $t_{h(MI)}^{(1)}$ | Data input hold time | Master mode | 7 | | ns |
| $t_{h(SI)}^{(1)}$ | Data input hold time | Slave mode | 10 | | ns |
| $t_{a(SO)}^{(1)(2)}$ | Data output access time | Slave mode | | 3 x t_{MASTER} | ns |
| $t_{dis(SO)}^{(1)(3)}$ | Data output disable time | Slave mode | 25 | | ns |
| $t_{v(SO)}^{(1)}$ | Data output valid time | Slave mode (after enable edge) | | 73 | ns |
| $t_{v(MO)}^{(1)}$ | Data output valid time | Master mode (after enable edge) | | 36 | ns |
| $t_{h(SO)}^{(1)}$ | Data output hold time | Slave mode (after enable edge) | 28 | | ns |
| $t_{h(MO)}^{(1)}$ | | Master mode (after enable edge) | 12 | | ns |

Notes:

⁽¹⁾ Values based on design simulation and/or characterization results, and not tested in production.

⁽²⁾ Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

⁽³⁾ Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 41: SPI timing diagram - slave mode and CPHA = 0

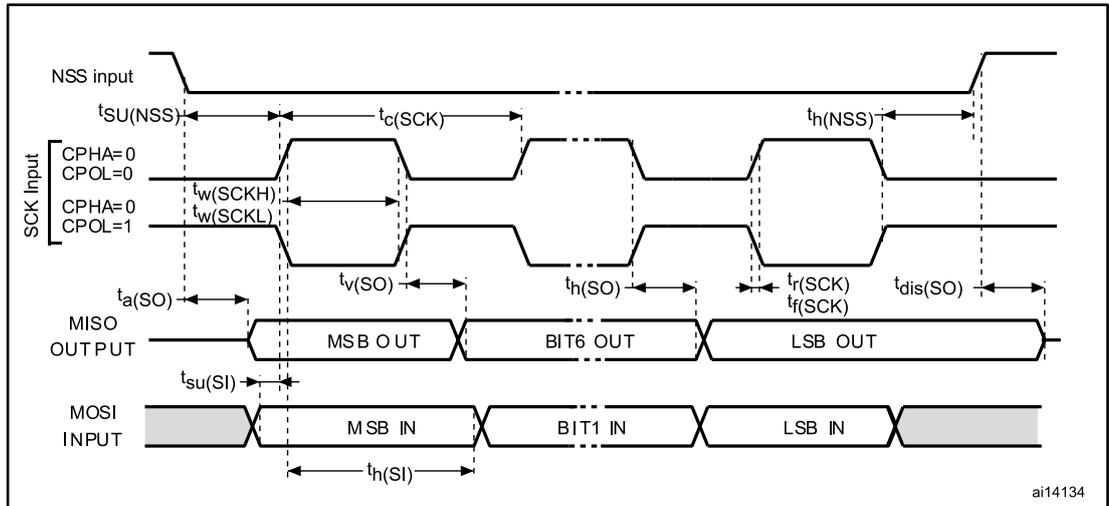
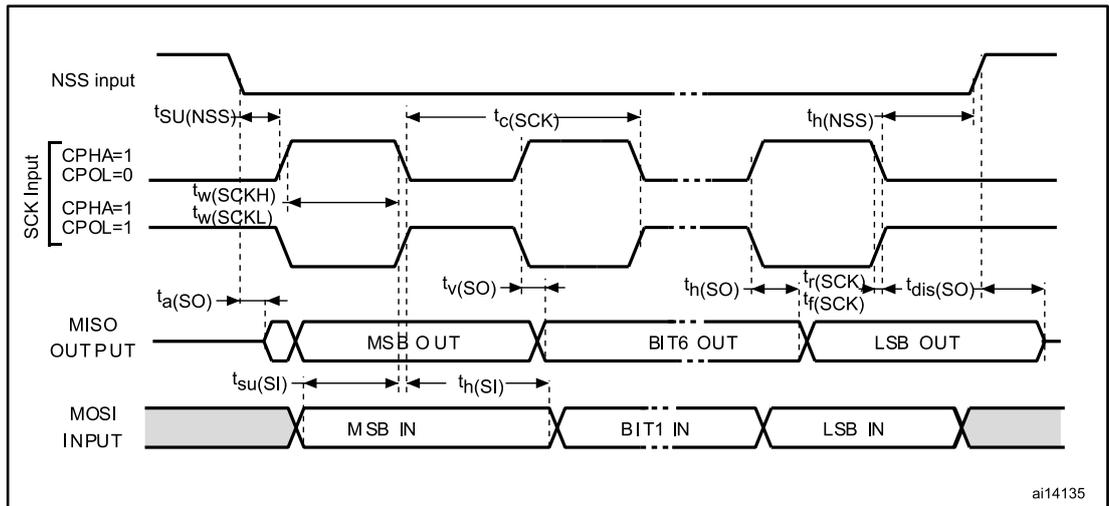
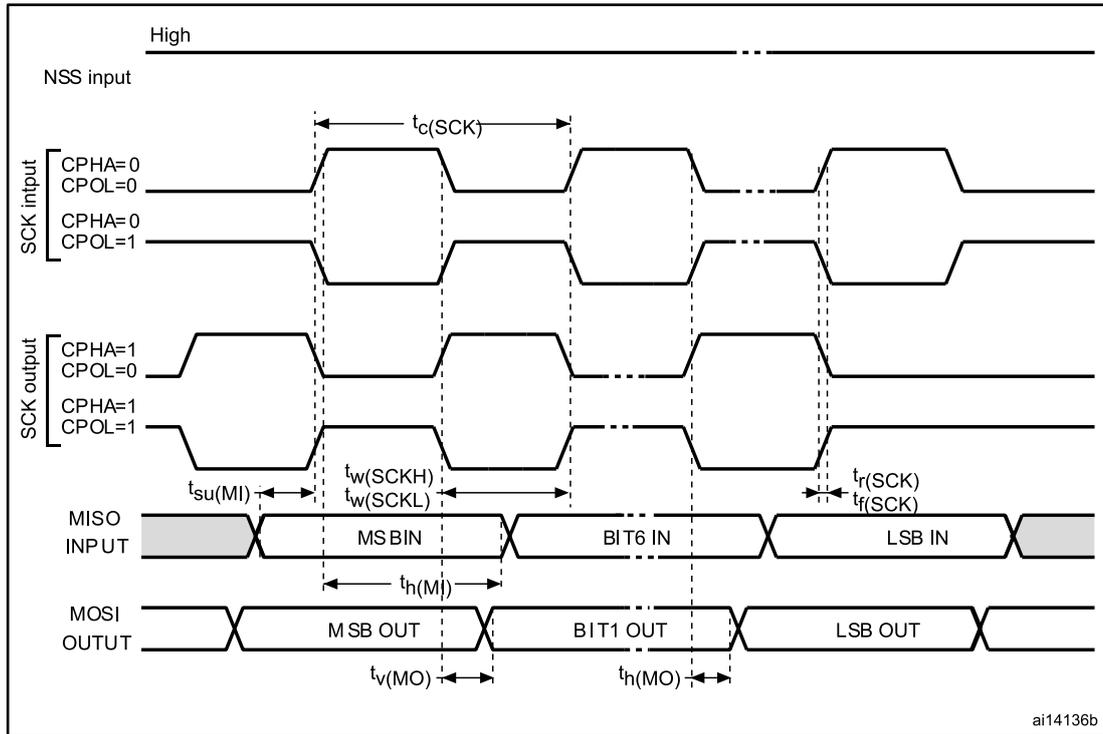


Figure 42: SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are made at CMOS levels: $0.3 V_{DD}$ and $0.7 V_{DD}$.

Figure 43: SPI timing diagram - master mode(1)



1. Measurement points are made at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

10.3.10 I2C interface characteristics

Table 44: I2C characteristics

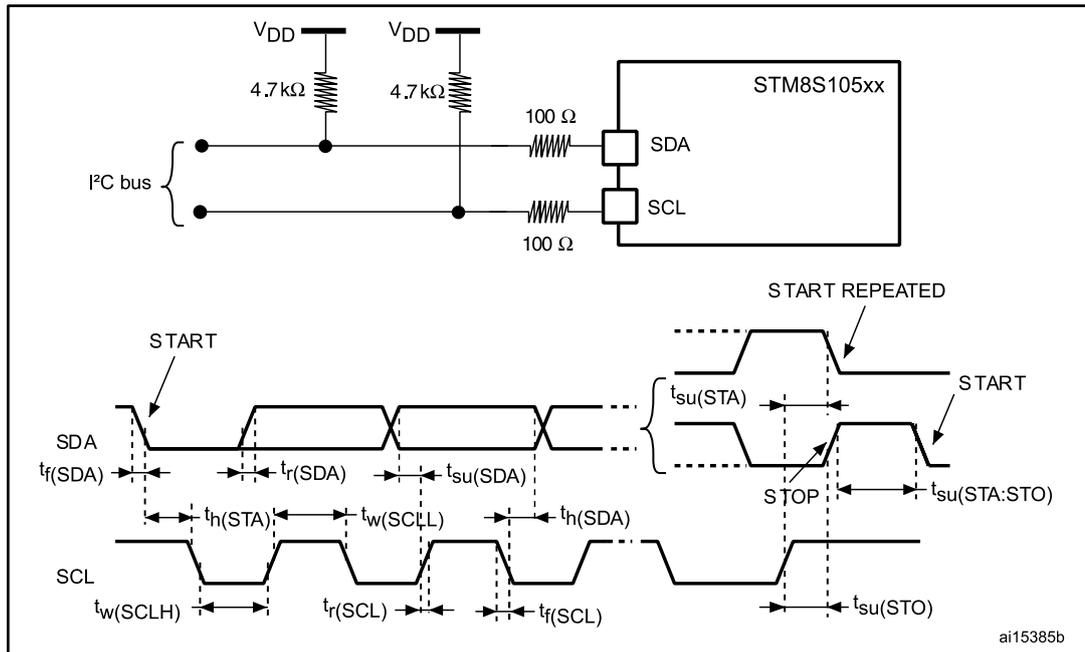
| Symbol | Parameter | Standard mode I ² C | | Fast mode I ² C ⁽¹⁾ | | Unit |
|--------------------------|---|--------------------------------|--------------------|---|--------------------|---------|
| | | Min ⁽²⁾ | Max ⁽²⁾ | Min ⁽²⁾ | Max ⁽²⁾ | |
| $t_w(SCLL)$ | SCL clock low time | 4.7 | | 1.3 | | μs |
| $t_w(SCLH)$ | SCL clock high time | 4.0 | | 0.6 | | μs |
| $t_{su}(SDA)$ | SDA setup time | 250 | | 100 | | ns |
| $t_h(SDA)$ | SDA data hold time | 0 ⁽³⁾ | | 0 ⁽⁴⁾ | 900 ⁽³⁾ | ns |
| $t_r(SDA)$ $t_r(SCL)$ | SDA and SCL rise time | | 1000 | | 300 | ns |
| $t_f(SDA)$ $t_f(SCL)$ | SDA and SCL fall time | | 300 | | 300 | ns |
| $t_h(STA)$ | START condition hold time | 4.0 | | 0.6 | | μs |
| $t_{su}(STA)$ | Repeated START condition setup time | 4.7 | | 0.6 | | μs |
| $t_{su}(STO)$ | STOP condition setup time | 4.0 | | 0.6 | | μs |
| $t_w(STO:STA)$ | STOP to START condition time (bus free) | 4.7 | | 1.3 | | μs |

| Symbol | Parameter | Standard mode I ² C | | Fast mode I ² C ⁽¹⁾ | | Unit |
|----------------|-----------------------------------|--------------------------------|--------------------|---|--------------------|------|
| | | Min ⁽²⁾ | Max ⁽²⁾ | Min ⁽²⁾ | Max ⁽²⁾ | |
| C _b | Capacitive load for each bus line | | 400 | | 400 | pF |

Notes:

- ⁽¹⁾ f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400kHz).
- ⁽²⁾ Data based on standard I²C protocol requirement, not tested in production.
- ⁽³⁾ The maximum hold time of the start condition has only to be met if the interface does not stretch the low time.
- ⁽⁴⁾ The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 44: Typical application with I2C bus and timing diagram (1)



- 1. Measurement points are made at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

10.3.11 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 45: ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|----------------------------|----------------------------------|---------------------|-----|------------------|------|
| f _{ADC} | ADC clock frequency | V _{DDA} = 2.95 to 5.5 V | 1.0 | | 4.0 | MHz |
| | | V _{DDA} = 4.5 to 5.5 V | 1.0 | | 6.0 | |
| V _{DDA} | Analog supply | | 3.0 | | 5.5 | V |
| V _{REF+} | Positive reference voltage | | 2.75 ⁽¹⁾ | | V _{DDA} | V |
| V _{REF-} | Negative reference voltage | | V _{SSA} | | 0.5 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|--|---|-------------------|-----|-------------------|--------------------|
| | | | | | (1) | |
| V _{AIN} | Conversion voltage range (2) | | V _{SSA} | | V _{DDA} | V |
| | | Devices with external V _{REF+} /V _{REF-} pins | V _{REF-} | | V _{REF+} | V |
| C _{ADC} | Internal sample and hold capacitor | | | 3.0 | | pF |
| t _S (2) | Sampling time | f _{ADC} = 4 MHz | 0.75 | | | μs |
| | | f _{ADC} = 6 MHz | 0.5 | | | |
| t _{STAB} | Wakeup time from standby | | | 7.0 | | μs |
| t _{CONV} | Total conversion time (including sampling time, 10-bit resolution) | f _{ADC} = 4 MHz | 3.5 | | | μs |
| | | f _{ADC} = 6 MHz | 2.33 | | | μs |
| | | | 14 | | | 1/f _{ADC} |

Notes:

(1) Data guaranteed by design, not tested in production..

(2) During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 46: ADC accuracy with RAIN < 10 kΩ , VDDA= 5 V

| Symbol | Parameter | Conditions | Typ | Max (1) | Unit |
|----------------|----------------------------------|--------------------------|-----|---------|------|
| E _T | Total unadjusted error (2) | f _{ADC} = 2 MHz | 1.0 | 2.5 | LSB |
| | | f _{ADC} = 4 MHz | 1.4 | 3.0 | |
| | | f _{ADC} = 6 MHz | 1.6 | 3.5 | |
| E _O | Offset error (2) | f _{ADC} = 2 MHz | 0.6 | 2.0 | |
| | | f _{ADC} = 4 MHz | 1.1 | 2.5 | |
| | | f _{ADC} = 6 MHz | 1.2 | 2.5 | |
| E _G | Gain error (2) | f _{ADC} = 2 MHz | 0.2 | 2.0 | |
| | | f _{ADC} = 4 MHz | 0.6 | 2.5 | |
| | | f _{ADC} = 6 MHz | 0.8 | 2.5 | |
| E _D | Differential linearity error (2) | f _{ADC} = 2 MHz | 0.7 | 1.5 | |
| | | f _{ADC} = 4 MHz | 0.7 | 1.5 | |
| | | f _{ADC} = 6 MHz | 0.8 | 1.5 | |
| E _L | Integral linearity error (2) | f _{ADC} = 2 MHz | 0.6 | 1.5 | |
| | | f _{ADC} = 4 MHz | 0.6 | 1.5 | |
| | | f _{ADC} = 6 MHz | 0.6 | 1.5 | |

Notes:

(1) Data based on characterization results, not tested in production.

(2) ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input.

It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.

Table 47: ADC accuracy with RAIN < 10 kΩ RAIN, VDDA = 3.3 V

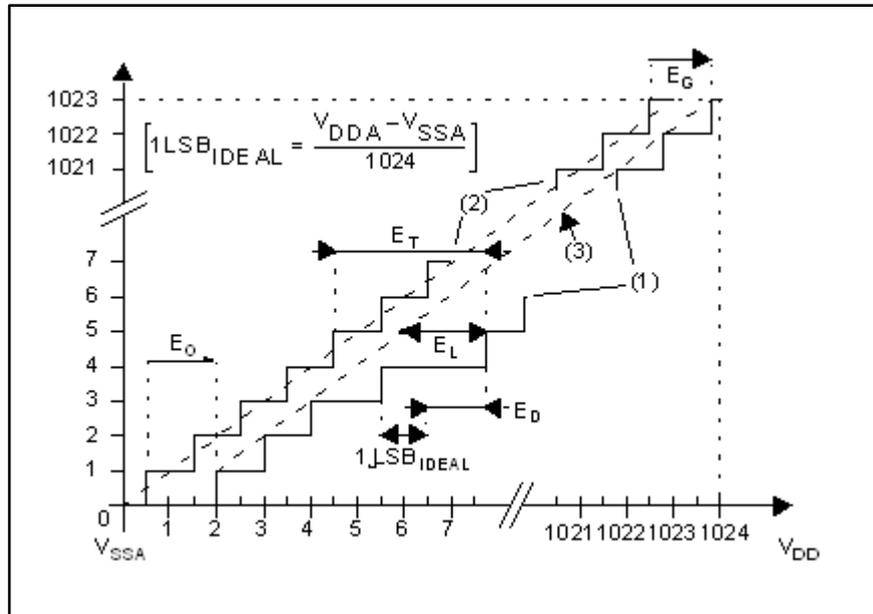
| Symbol | Parameter | Conditions | Typ | Max ⁽¹⁾ | Unit |
|----------------|---|--------------------------|-----|--------------------|------|
| E _T | Total unadjusted error ⁽²⁾ | f _{ADC} = 2 MHz | 1.1 | 2.0 | LSB |
| | | f _{ADC} = 4 MHz | 1.6 | 2.5 | |
| E _O | Offset error ⁽²⁾ | f _{ADC} = 2 MHz | 0.7 | 1.5 | |
| | | f _{ADC} = 4 MHz | 1.3 | 2.0 | |
| E _G | Gain error ⁽²⁾ | f _{ADC} = 2 MHz | 0.2 | 1.5 | |
| | | f _{ADC} = 4 MHz | 0.5 | 2.0 | |
| E _D | Differential linearity error ⁽²⁾ | f _{ADC} = 2 MHz | 0.7 | 1.0 | |
| | | f _{ADC} = 4 MHz | 0.7 | 1.0 | |
| E _L | Integral linearity error ⁽²⁾ | f _{ADC} = 2 MHz | 0.6 | 1.5 | |
| | | f _{ADC} = 4 MHz | 0.6 | 1.5 | |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production.

⁽²⁾ ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 13.3.6: "I/O port pin characteristics"](#) does not affect the ADC accuracy.

Figure 45: ADC accuracy characteristics



1. Example of an actual transfer curve.
2. The ideal transfer curve

3. End point correlation line

E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.

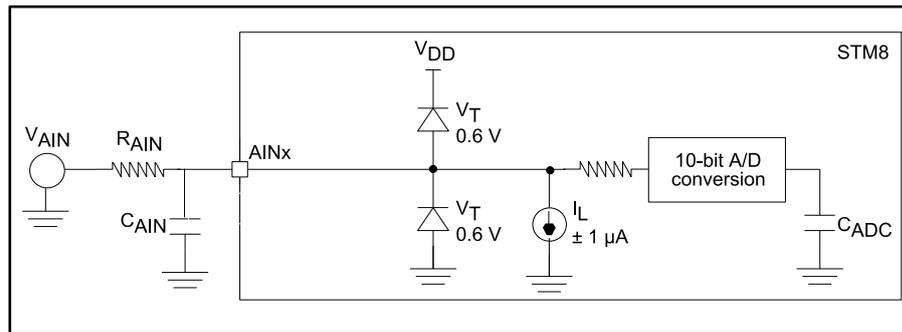
E_O = Offset error: deviation between the first actual transition and the first ideal one.

E_G = Gain error: deviation between the last ideal transition and the last actual one.

E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.

E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 46: Typical application with ADC



10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

10.3.12.1 Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- FESD: Functional electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- FTB: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms to IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. Test results are given in table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for ST Microcontrollers).

10.3.12.2 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 48: EMS data

| Symbol | Parameter | Conditions | Level/class |
|-------------------|---|---|--------------------|
| V _{FESD} | Voltage limits to be applied on any I/O pin to induce a functional disturbance | V _{DD} = 3.3 V, T _A = 25 °C, f _{MASTER} = 16 MHz (HSI clock), conforming to IEC 61000-4-2 V _{DD} = 5 V, T _A = 25 °C, f _{MASTER} = 16 MHz, conforming to IEC 1000-4-2 | 2/B ⁽¹⁾ |
| V _{EFTB} | Fast transient voltage burst limits to be applied through 100 pF on V _{DD} and V _{SS} pins to induce a functional disturbance | V _{DD} = 3.3 V, T _A = 25 °C, f _{MASTER} = 16 MHz (HSI clock), conforming to IEC 61000-4-4 V _{DD} = 5 V, T _A = 25 °C, f _{MASTER} = 16 MHz, conforming to IEC 1000-4-4 | 4/A ⁽¹⁾ |

Notes:

⁽¹⁾ Data obtained with HSI clock configuration, after applying HW recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

10.3.12.3 Electromagnetic interference (EMI)

Emission tests conform to the IEC61967-2 standard for test software, board layout and pin loading.

Table 49: EMI data

| Symbol | Parameter | Conditions | | | | Unit |
|------------------|---------------|---|--------------------------|---|--------------|------|
| | | General conditions | Monitored frequency band | Max f _{HSE} /f _{CPU} ⁽¹⁾ | | |
| | | | | 8 MHz/8 MHz | 8 MHz/16 MHz | |
| S _{EMI} | Peak level | V _{DD} = 5 V, T _A = +25 °C, LQFP48 package conforming to IEC61967-2 | 0.1 MHz to 30 MHz | 13 | 14 | dBμV |
| | | | 30 MHz to 130 MHz | 23 | 19 | |
| | | | 130 MHz to 1 GHz | -4.0 | -4.0 | |
| | SAE EMI level | | 2.0 | 1.5 | — | |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production.

10.3.12.4 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

10.3.12.5 Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 50: ESD absolute maximum ratings

| Symbol | Ratings | Conditions | Class | Maximum value ⁽¹⁾ | Unit |
|-----------------------|---|---|-------|------------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (Human body model) | T _A = +25°C, conforming to JESD22-A114 | A | 2000 | V |
| V _{ESD(CDM)} | Electrostatic discharge voltage (Charge device model) | T _A = +25°C, conforming to JESD22-C101 | IV | 1000 | V |

Notes:

⁽¹⁾ Data based on characterization results, not tested in production

10.3.12.6 Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) is performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 51: Electrical sensitivities

| Symbol | Parameter | Conditions | Class ⁽¹⁾ |
|--------|-----------------------|--------------------------|----------------------|
| LU | Static latch-up class | T _A = +25 °C | A |
| | | T _A = +85 °C | A |
| | | T _A = +125 °C | A |

Notes:

⁽¹⁾ Class description: A Class is a STMicroelectronics internal specification. All limits are higher than JEDEC specifications, that means when a device belongs to class A it exceeds JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

11.1 48-pin LQFP package mechanical data

Figure 47: 48-pin low profile quad flat package (7 x 7)

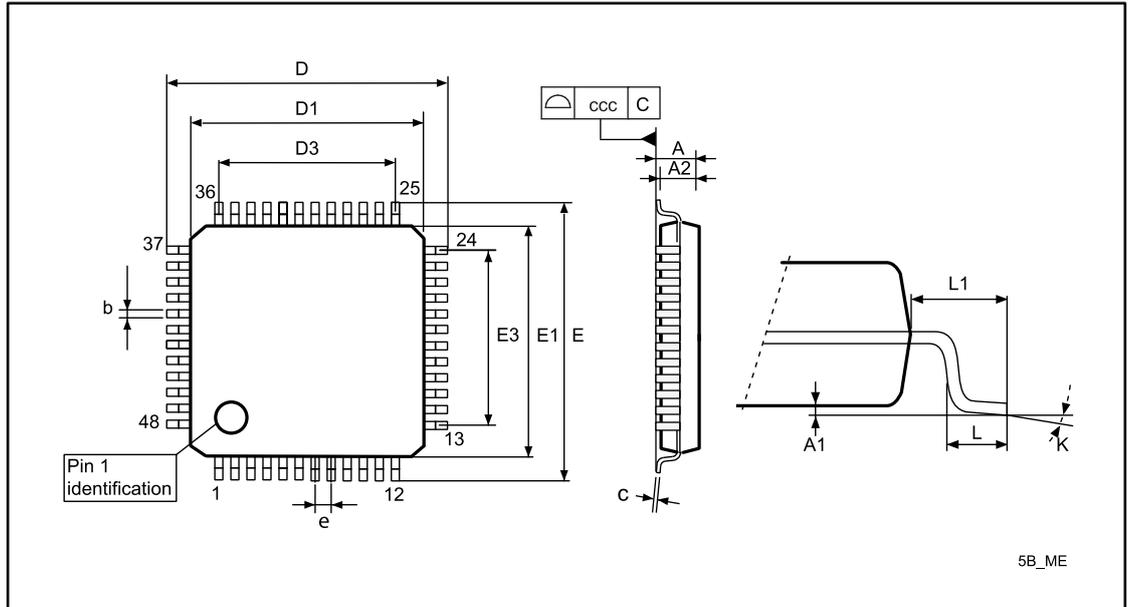


Table 52: 48-pin low profile quad flat package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|-------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | | 5.500 | | | 0.2165 | |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | | 5.500 | | | 0.2165 | |
| e | | 0.500 | | | 0.0197 | |

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|-------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0° | 3.5° | 7.0° | 0° | 3.5° | 7.0° |
| ccc | | | 0.080 | | | 0.0031 |

Notes:

⁽¹⁾ Values in inches are converted from mm and rounded to 4 decimal digits

11.2 44-pin LQFP package mechanical data

Figure 48: 44-pin low profile quad flat package

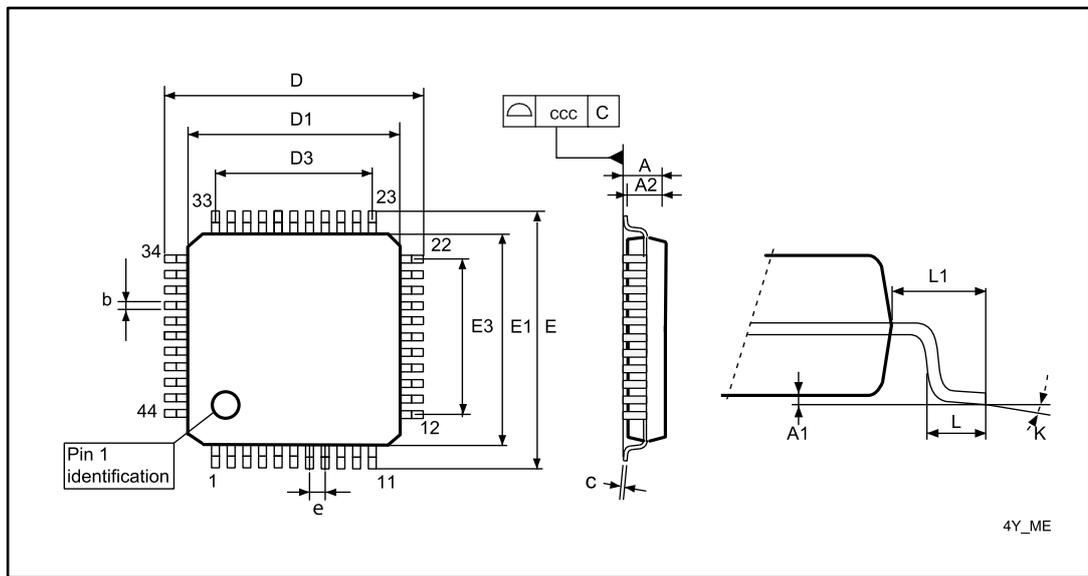


Table 53: 44-pin low profile quad flat package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|--------|--------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.300 | 0.370 | 0.450 | 0.0118 | 0.0146 | 0.0177 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 11.800 | 12.000 | 12.200 | 0.4646 | 0.4724 | 0.4803 |
| D1 | 9.800 | 10.000 | 10.200 | 0.3858 | 0.3937 | 0.4016 |
| D3 | | 8.000 | | | 0.3150 | |
| E | 11.800 | 12.000 | 12.200 | 0.4646 | 0.4724 | 0.4803 |
| E1 | 9.800 | 10.000 | 10.200 | 0.3858 | 0.3937 | 0.4016 |

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|-------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | | 8.000 | | | 0.3150 | |
| e | | 0.800 | | | 0.0315 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | | | 0.100 | | | 0.0039 |

Notes:

⁽¹⁾ Values in inches are converted from mm and rounded to 4 decimal digits

11.3 32-pin LQFP package mechanical data

Figure 49: 32-pin low profile quad flat package (7 x 7)

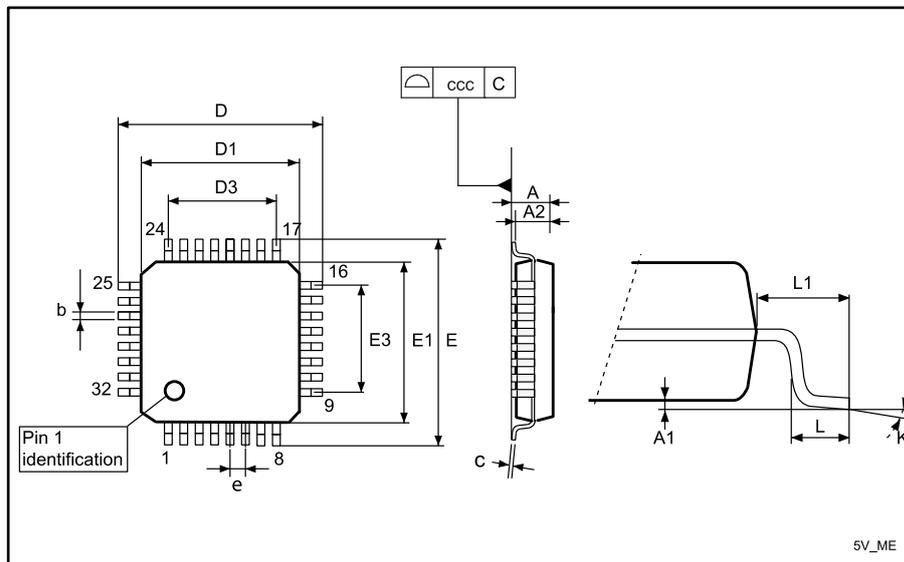


Table 54: 32-pin low profile quad flat package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|-------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.300 | 0.370 | 0.450 | 0.0118 | 0.0146 | 0.0177 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | | 5.600 | | | 0.2205 | |

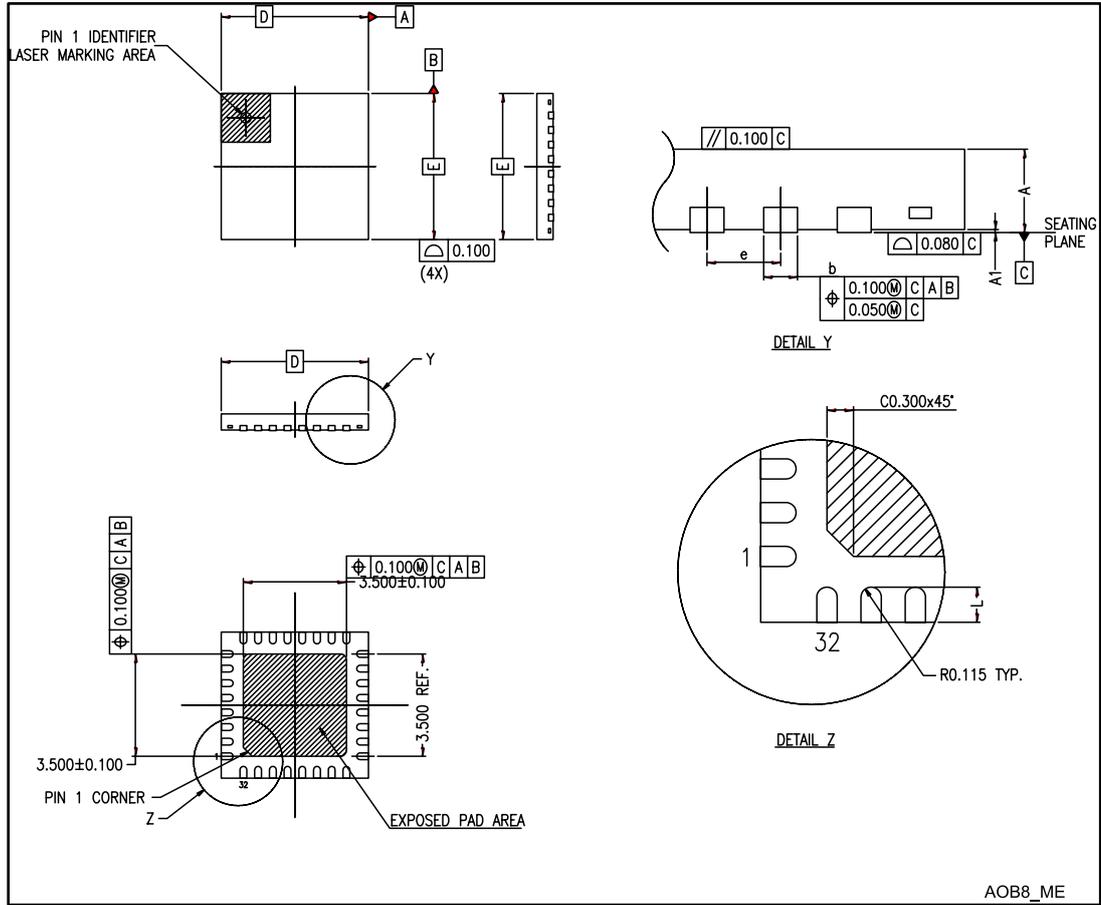
| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|-------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | | 5.600 | | | 0.2205 | |
| e | | 0.800 | | | 0.0315 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0° | 3.5° | 7.0° | 0° | 3.5° | 7.0° |
| ccc | | | 0.100 | | | 0.0039 |

Notes:

(1) Values in inches are converted from mm and rounded to 4 decimal digits

11.4 32-lead UFQFPN package mechanical data

Figure 50: 32-lead, ultra-thin, fine pitch quad flat no-lead package (5 x 5)



1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.
4. Dimensions are in millimeters.

Table 55: 32-lead ultra-thin fine pitch quad flat no-lead package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|-------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0 | 0.020 | 0.050 | | 0.0008 | 0.0020 |
| A3 | | 0.200 | | | 0.0079 | |
| b | 0.180 | 0.250 | 0.300 | 0.0071 | 0.0098 | 0.0118 |
| D | 4.900 | 5.000 | 5.100 | 0.1909 | 0.1969 | 0.2028 |
| D2 | 3.200 | 3.450 | 3.700 | 0.1260 | | 0.1457 |
| E | 4.900 | 5.000 | 5.100 | 0.1909 | 0.1969 | 0.2028 |

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|-------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| E2 | 3.200 | 3.450 | 3.700 | 0.1260 | 0.1358 | 0.1457 |
| e | | 0.500 | | | 0.0197 | |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | | | 0.080 | | | 0.0031 |

Notes:

⁽¹⁾ Values in inches are converted from mm and rounded to 4 decimal digits.

11.5 SDIP32 package mechanical data

Figure 51: 32-lead shrink plastic DIP (400 ml) package

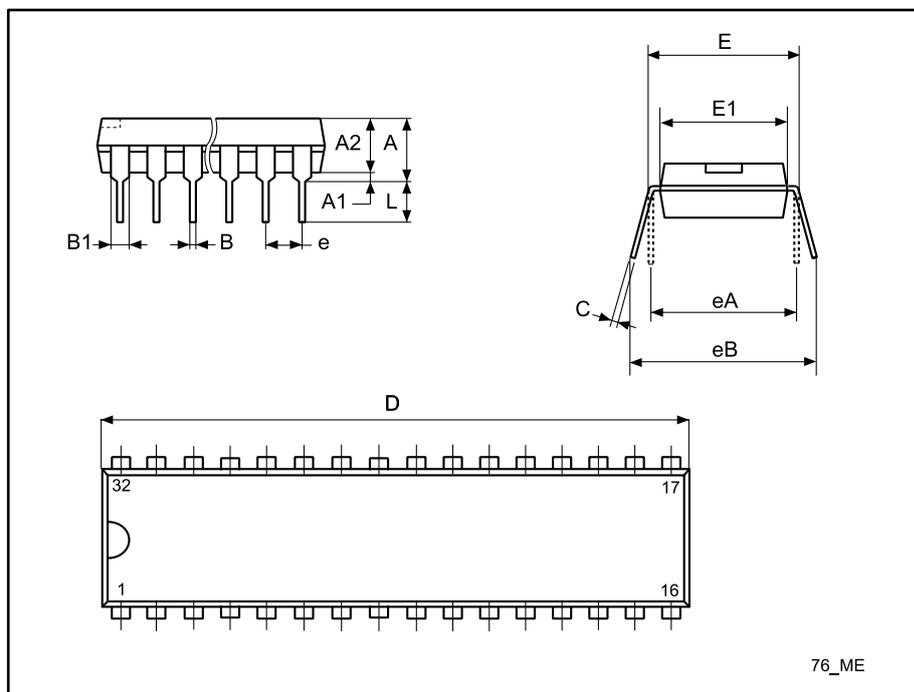


Table 56: 32-lead shrink plastic DIP (400 ml) package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|--------|--------|--------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 3.556 | 3.759 | 5.080 | 0.1400 | 0.1480 | 0.2000 |
| A1 | 0.508 | | | 0.0200 | | |
| A2 | 3.048 | 3.556 | 4.572 | 0.1200 | 0.1400 | 0.1800 |
| B | 0.356 | 0.457 | 0.584 | 0.0140 | 0.0180 | 0.0230 |
| B1 | 0.762 | 1.016 | 1.397 | 0.0300 | 0.0400 | 0.0550 |
| C | 0.203 | 0.254 | 0.356 | 0.0079 | 0.0100 | 0.0140 |
| D | 27.430 | 27.940 | 28.450 | 1.0799 | 1.1000 | 1.1201 |
| E | 9.906 | 10.410 | 11.050 | 0.3900 | 0.4098 | 0.4350 |
| E1 | 7.620 | 8.890 | 9.398 | 0.3000 | 0.3500 | 0.3700 |
| e | | 1.778 | | | 0.0700 | |
| eA | | 10.160 | | | 0.4000 | |
| eB | | | 12.700 | | | 0.5000 |
| L | 2.540 | 3.048 | 3.810 | 0.1000 | 0.1200 | 0.1500 |

Notes:

⁽¹⁾ Values in inches are converted from mm and rounded to 4 decimal digits

12 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Section 7.10: "TIM1 - 16-bit advanced control timer"](#)

The maximum chip-junction temperature, T_{Jmax} , in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins Where: $P_{I/Omax} = \Sigma (V_{OL} \cdot I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \cdot I_{OH})$, taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 57: Thermal characteristics (1)

| Symbol | Parameter | Value | Unit |
|---------------|---|-------|------|
| Θ_{JA} | Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm | 57 | °C/W |
| Θ_{JA} | Thermal resistance junction-ambient LQFP 44 - 10 x 10 mm | 54 | °C/W |
| Θ_{JA} | Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm | 60 | °C/W |
| Θ_{JA} | Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm | 38 | °C/W |
| Θ_{JA} | Thermal resistance junction-ambient SDIP 32 - 400 mils | 60 | °C/W |

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

12.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

12.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code.

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature $T_{Amax} = 82$ °C (measured according to JESD51-2)
- $I_{DDmax} = 15$ mA, $V_{DD} = 5.5$ V

- Maximum 8 standard I/Os used at the same time in output at low level with $I_{OL} = 10$ mA, $V_{OL} = 2$ V
- Maximum 4 high sink I/Os used at the same time in output at low level with $I_{OL} = 20$ mA, $V_{OL} = 1.5$ V
- Maximum 2 true open drain I/Os used at the same time in output at low level with $I_{OL} = 20$ mA, $V_{OL} = 2$ V

$$P_{INTmax} = 15 \text{ mA} \times 5.5 \text{ V} = 82.5 \text{ mW}$$

$$P_{IOmax} = (10 \text{ mA} \times 2 \text{ V} \times 8) + (20 \text{ mA} \times 2 \text{ V} \times 2) + (20 \text{ mA} \times 1.5 \text{ V} \times 4) = 360 \text{ mW}$$

This gives: $P_{INTmax} = 82.5 \text{ mW}$ and $P_{IOmax} = 360 \text{ mW}$:

$$P_{Dmax} = 82.5 \text{ mW} + 360 \text{ mW}$$

$$\text{Thus: } P_{Dmax} = 443 \text{ mW}$$

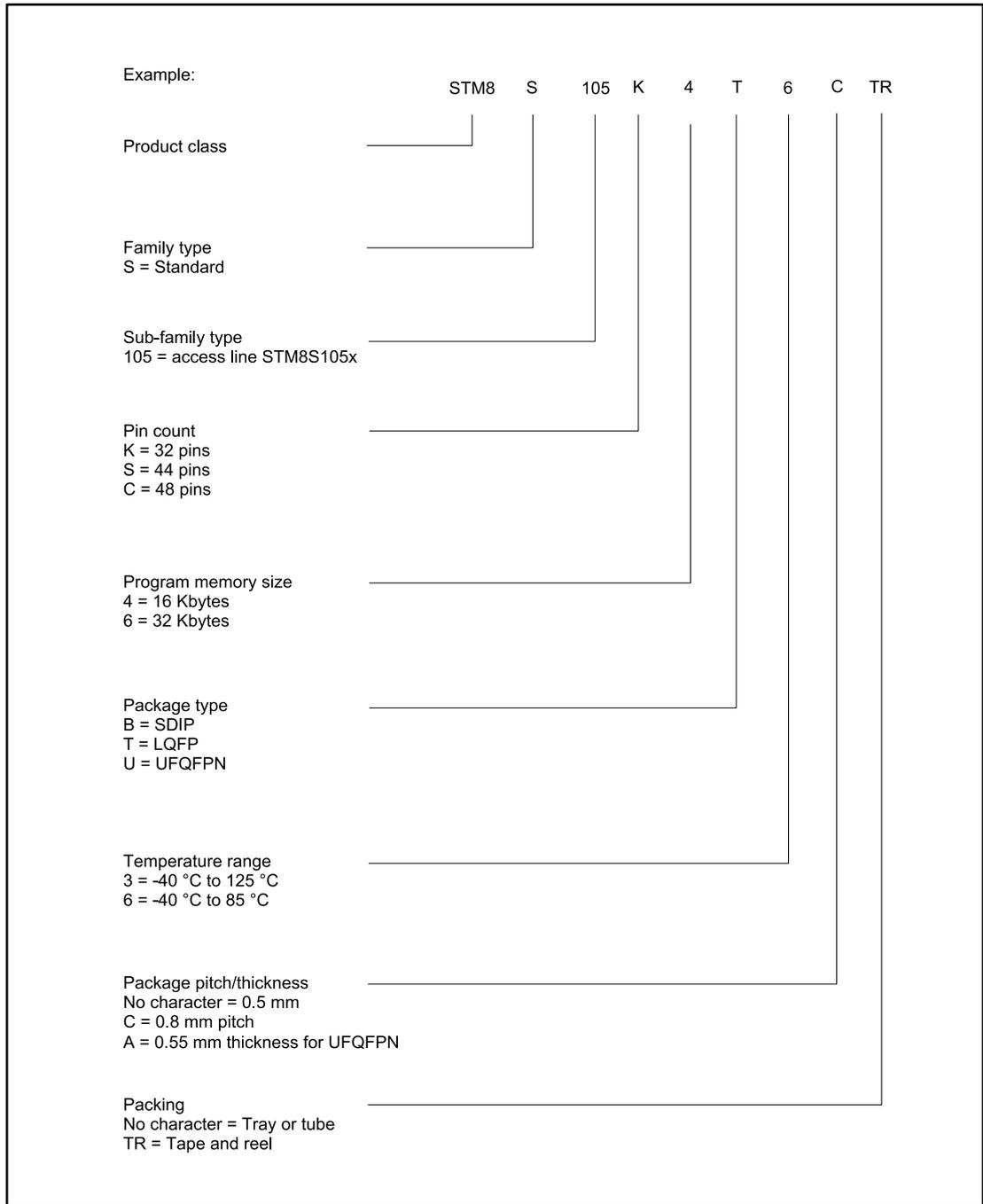
T_{Jmax} for LQFP32 can be calculated as follows, using the thermal resistance Θ_{JA} :

$$T_{Jmax} = 82^\circ \text{ C} + (60^\circ \text{ C/W} \times 443 \text{ mW}) = 82^\circ \text{ C} + 27^\circ \text{ C} = 109^\circ \text{ C}$$

This is within the range of the suffix 3 version parts ($-40 < T_J < 131^\circ \text{ C}$). In this case, parts must be ordered at least with the temperature range suffix 3.

13 Ordering information

Figure 52: STM8S105xx access line ordering information scheme



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to www.st.com or contact the ST sales office nearest to you.

14 STM8S105 FASTROM microcontroller option list

(last update: September 2010)

| | |
|---------------------------------------|-------|
| Customer | |
| Address | |
| Contact | |
| Phone no. | |
| Reference FASTROM code ⁽¹⁾ | |

Notes:

⁽¹⁾FASTROM code name is assigned by STMicroelectronics.

Preferable format for programing code is .Hex (.s19 is accepted)

If data EEPROM programing is required, a separate file must be sent with the requested data.



See the option byte section in the datasheet for authorized option byte combinations and a detailed explanation.

Device type/memory size/package (check only one option)

| FASTROM device | 16 Kbyte | 32 Kbyte |
|----------------|-------------------------------------|-------------------------------------|
| LQFP32 | <input type="checkbox"/> STM8S105K4 | <input type="checkbox"/> STM8S105K6 |
| LQFP44 | <input type="checkbox"/> STM8S105S4 | <input type="checkbox"/> STM8S105S6 |
| LQFP48 | <input type="checkbox"/> STM8S105C4 | <input type="checkbox"/> STM8S105C6 |

Conditioning (check only one option)

Tape & reel or Tray

Special marking (check only one option)

No Yes

Authorized characters are letters, digits, '.', '-', '/' and spaces only. Maximum character counts are:

LQFP32: 2 lines of 7 characters max: "_____" and "_____"

LQFP44: 2 lines of 7 characters max: "_____" and "_____"

LQFP48: 2 lines of 8 characters max: "_____" and "_____"

Temperature range

-40°C to +85°C or -40°C to +125°C

Padding value for unused program memory (check only one option)

| | |
|-------------------------------|---|
| <input type="checkbox"/> 0xFF | Fixed value |
| <input type="checkbox"/> 0x83 | TRAP instruction opcode |
| <input type="checkbox"/> 0x75 | Illegal opcode (causes a reset when executed) |

OPT0 memory readout protection (check only one option)

Disable or Enable

OPT1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below.

| | |
|-----------|--|
| UBC, bit0 | <input type="checkbox"/> 0: Reset <input type="checkbox"/> 1: Set |
| UBC bit1 | <input type="checkbox"/> 0: Reset <input type="checkbox"/> 1: Set |
| UBC bit2 | <input type="checkbox"/> 0: Reset <input type="checkbox"/> 1: Set |
| UBC bit3 | <input type="checkbox"/> 0: Reset <input type="checkbox"/> 1: Set |
| UBC bit4 | <input type="checkbox"/> 0: Reset <input type="checkbox"/> 1: Set |
| UBC bit5 | <input type="checkbox"/> 0: Reset <input type="checkbox"/> 1: Set |

OPT2 alternate function remapping

| | |
|---------------------------------|--|
| AFR0 (check only one option) | <input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. <input type="checkbox"/> 1: Port D3 alternate function = ADC_ETR |
| AFR1 (check only one option) | <input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. <input type="checkbox"/> 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function = TIM2_CH3. |
| AFR2 (check only one option) | <input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. <input type="checkbox"/> 1: Port D0 alternate function = CLK_CCO.  If both AFR2 and AFR3 are activated, AFR2 option has priority over AFR3. |
| AFR3 (check only one option) | <input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. <input type="checkbox"/> 1: Port D0 alternate function = TIM1_BKIN. |

| | |
|---------------------------------|---|
| AFR4 (check only one option) | <input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. <input type="checkbox"/> 1: Port D7 alternate function = TIM1_CH4. |
| AFR5 (check only one option) | <input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. <input type="checkbox"/> 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_NCC3, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N. |
| AFR6 (check only one option) | <input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description <input type="checkbox"/> 1: Port B5 alternate function = I2C_SDA, port B4 alternate function = I2C_SCL. |
| AFR7 (check only one option) | <input type="checkbox"/> 0: Remapping option inactive. Default alternate functions used. Refer to pinout description. <input type="checkbox"/> 1: Port D4 alternate function = BEEP. |

OPT3 watchdog

| | |
|--------------------------------------|--|
| WWDG_HALT (check only one option) | <input type="checkbox"/> 0: No reset generated on halt if WWDG active. <input type="checkbox"/> 1: Reset generated on halt if WWDG active. |
| WWDG_HW (check only one option) | <input type="checkbox"/> 0: WWDG activated by software. <input type="checkbox"/> 1: WWDG activated by hardware. |
| IWDG_HW (check only one option) | <input type="checkbox"/> 0: IWDG activated by software. <input type="checkbox"/> 1: IWDG activated by hardware. |
| LSI_EN (check only one option) | <input type="checkbox"/> 0: LSI clock is not available as CPU clock source. <input type="checkbox"/> 1: LSI clock is available as CPU clock source. |
| HSITRIM (check only one option) | <input type="checkbox"/> 0: 3-bit trimming supported in CLK_HSITRIMR register. <input type="checkbox"/> 1: 4-bit trimming supported in CLK_HSITRIMR register. |

OPT4 wakeup

| | |
|-------------------------------------|---|
| PRSC (check only one option) | <input type="checkbox"/> for 16 MHz to 128 kHz prescaler. <input type="checkbox"/> for 8 MHz to 128 kHz prescaler. <input type="checkbox"/> for 4 MHz to 128 kHz prescaler. |
| CKAWUSEL (check only one option) | <input type="checkbox"/> 0: LSI clock source selected for AWU. <input type="checkbox"/> 1: HSE clock with prescaler selected as clock source for AWU. |
| EXTCLK (check only one option) | <input type="checkbox"/> 0: External crystal connected to OSCIN/OSCOU. <input type="checkbox"/> 1: External clock signal on OSCIN. |

OPT5 crystal oscillator stabilization HSECNT (check only one option)

- 2048 HSE cycles
- 128 HSE cycles
- 8 HSE cycles
- 0.5 HSE cycles

OPT6 is reserved

OPT7 is reserved

OPTBL bootloader option byte (check only one option)

Refer to the UM0560 (STM8L/S bootloader manual) for more details.

Disable (00h)

Enable (55h)

| | |
|---|-------|
| Comments: | |
| Supply operating range in the application | |
| Notes: | |
| Date: | |
| Signature: | |

15 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STIce emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

15.1 Emulation and in-circuit debugging tools

The STIce emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STIce is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STIce offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STIce is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

STIce key features

- Occurrence and time profiling and code coverage (new features)
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

15.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8, which are available in a free version that outputs up to 16 Kbytes of code.

15.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com/mcu. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of your STM8 microcontroller's Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

15.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of your application directly from an easy-to-use graphical interface.

Available toolchains include:

- **Cosmic C compiler for STM8** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.
- **Raisonance C compiler for STM8** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.raisonance.com.
- **STM8 assembler linker** – Free assembly toolchain included in the STVD toolset, which allows you to assemble and link your application source code.

15.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on your application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming your STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

16 Revision history

Table 58: Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 05-Jun-2008 | 1 | Initial release. |
| 23-Jun-2008 | 2 | Corrected number of high sink outputs to 9 in I/Os on Section 3: "Features" . Updated part numbers in Table 2: "STM8S105xx access line features" . |
| 12-Aug-2008 | 3 | Updated part numbers in Table 2: "STM8S105xx access line features" . USART renamed UART1, LINUART renamed UART2. Added Table 7: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices. |
| 17-Sep-2008 | 4 | Removed STM8S102xx and STM8S104xx root part numbers corresponding to devices without data EEPROM. Updated STM8S103 pinout in Section 5.2 on page 29. Added low and medium density Flash memory categories. Added Note 1 in Table 17: "Current characteristics" . Updated Table 12: "Option bytes" . |
| 05-Feb-2009 | 5 | Updated STM8S103 pinout in Section 5.2 on page 29 Updated number of High Sink I/Os in pinout. TSSOP20 pinout modified (PD4 moved to pin 1 etc.) Added WFQFN20 package Updated Section 11: "Option bytes" . Added Section 4: "Introduction" . |
| 27-Feb-2009 | 6 | Removed STM8S103x products (separate STM8S103 datasheet created) Updated Section 4: "Introduction" . |
| 12-May-2009 | 7 | Added SDIP32 silhouette and package to Section 3: "Features" and Section 14.5: "SDIP32 package mechanical data" ; updated Section 8: "Pinout and pin description" . Updated V _{DD} range (2.95 V to 5.5 V) on Section 3: "Features" . Amended name of package VQFPN32 Added Table 5 on page 22 . Updated Section 7.8: "Auto wakeup counter" . Updated pins 25, 30, and 31 in Section 8: "Pinout and pin description" . Removed Table 7: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices. Added Table 14: "Description of alternate function remapping bits [7:0] of OPT2" . Section 4: "Introduction" : Updated VCAP specifications; updated Table 15, Table 18, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 29, Table 35, and Table 42; added current consumption curves ; removed Figure 20: typical HSE frequency vs fcpu @ 4 temperatures; updated Figure 13, Figure 14, Figure 15, Figure 16 and Figure 17 ; modified HSI accuracy in Table 33 ; added Figure 44 ; modified fSCK, tV(SO) and tV(MO) in Table 42 ; updated figures and tables of High speed internal RC oscillator (HSI) ; replaced Figure 23, Figure 24, Figure 26, and Figure 39 . Section 14: "Package information" : Updated Table 57: "Thermal |

| Date | Revision | Changes |
|-------------|----------|--|
| | | <i>characteristics(1)</i> " and removed Table 57: Junction temperature range. Updated <i>Figure 52: "STM8S105xx access line ordering information scheme"</i> . |
| 10-Jun-2009 | 8 | Document status changed from "preliminary data" to "datasheet". Standardized name of the VFQFPN package. Removed 'wpu' from I2C pins in <i>Section 8: "Pinout and pin description"</i> |
| 21-Apr-2010 | 9 | Added UFQFPN32 package silhouette to the title page. <i>Section 3: "Features"</i> : added unique ID. <i>Section 7.4: "Flash program and data EEPROM memory"</i> : updated bit positions for TIM2 and TIM3. <i>Section 7.9: "Beeper"</i> : added information about availability of the beeper output port through option bit AFR7. <i>Section 7.13: "Analog-to-digital converter (ADC1)"</i> : added a note concerning additional AIN12 analog input. <i>Section 8.1: "STM8S105 pinouts and pin description"</i> : added UFQFPN32 package details; updated default alternate function of PB2/AIN2[TIM1_CH3N] pin in the "Pin description for STM8S105 microcontrollers" table. <i>Section 11: "Option bytes"</i> : added description of STM8L bootloader option bytes to the option byte description table. Added <i>Section 4: "Introduction"</i> <i>Section 7.10: "TIM1 - 16-bit advanced control timer"</i> : added introductory text; removed low power dissipation condition for T _A , replaced "C _{EXT} " by "VCAP", and added ESR and ESL data in table "general operating conditions". <i>Section 13.3.2.4: "Total current consumption in halt mode"</i> : replaced max value of I _{DD(H)} at 85 °C from 20 µA to 25 µA for the condition "Flash in powerdown mode, HSI clock after wakeup in the table "total current consumption in halt mode at V _{DD} = 5 V". <i>Section 13.3.2.5: "Low power mode wakeup times"</i> : added first condition (0 to 16 MHz) for the t _{WU(WFI)} parameter in the table "wakeup times". <i>Section 13.3.4: "Internal clock sources and timing characteristics"</i> : In the table "HSI oscillator characteristics", replaced min and max values of "ACC _{HSI} factory calibrated parameter" and removed footnote 4 concerning further characterization of results. <i>Section 13.3.12.1: "Functional EMS (electromagnetic susceptibility)"</i> : IEC 1000 replaced with IEC 61000. <i>Section 13.3.12.2: "Designing hardened software to avoid noise problems"</i> : IEC 1000 replaced with IEC 61000. <i>Section 13.3.12.3: "Electromagnetic interference (EMI)"</i> : SAE J 1752/3 replaced with IEC61967-2. <i>Section 7.7: "Watchdog timers"</i> : Replaced the thermal resistance junction ambient temperature of LQFP32 7X7 mm from 59 °C to 60 °C in the thermal characteristics table. Added <i>Section 6: "Block diagram"</i> . Added <i>Section 17: "STM8S105 FASTROM microcontroller option list"</i> . |
| 21-Sep-2010 | 10 | <i>Table 5: "Legend/abbreviations for pinout tables "</i> : updated "reset state"; removed "HS", (T), and "[]". <i>Table 6: "Pin description for STM8S105 microcontrollers"</i> : added footnotes to the PF4 and PD1 pins. <i>Table 8: "I/O port hardware register map"</i> : changed reset status of Px_IDR from 0x00 to 0xXX. <i>Table 9: "General hardware register map"</i> : Standardized all address and reset state values; updated the reset state values of the RST_SR, CLK_SWCR, CLK_HSTRIMR, CLK_SWIMCCR, IWDG_KR, UART2_DR, and ADC_DRx |

| Date | Revision | Changes |
|-------------|----------|--|
| | | registers; replaced reserved address "0x00 5248" with the UART2_CR5. <i>Figure 40: "Recommended reset pin protection"</i> : replaced 0.01 μF with 0.1 μF Updated <i>Figure 44: "Typical application with I2C bus and timing diagram (1)"</i> . Updated footnote 1 in <i>Table 46: ADC accuracy with RAIN < 10 kΩ, VDDA= 5V</i> and <i>Table 47: ADC accuracy with RAIN < 10 kΩ RAIN, VDDA=3.3V</i> . <i>Section 17: "STM8S105 FASTROM microcontroller option list"</i> : removed bits 6 and 7 from OPT1 user boot code area (UBC); added "disable" to 00h and "enable" to 55h of OPTBL bootloader option byte. VFQFPN Package Mechanical datas : replaced note 1 and added note 2. |
| 04-Apr-2012 | 11 | Removed VFQFPN32 package. Modified <i>Section 5: "Description"</i> . Remove weak pull-up input for PE1 and PE2 in <i>Table 6: "Pin description for STM8S105 microcontrollers"</i> Updated <i>Table 11: "Interrupt mapping"</i> for TIM2 and TIM4. Updated notes related to V_{CAP} in <i>Table 19: "General operating conditions"</i> . Added values of $t_{\text{R}}/t_{\text{F}}$ for 50 pF load capacitance, and updated note in <i>Table 38: "I/O static characteristics"</i> . Updated typical and maximum values of R_{PU} in <i>Table 38: "I/O static characteristics"</i> and <i>Table 42: "NRST pin characteristics"</i> . Changed SCK input to SCK output in <i>Section 13.3.9: "SPI serial peripheral interface"</i> Added Θ_{JA} for UFQFPN32 and SDIP32 in <i>Table 57: "Thermal characteristics(1)"</i> , and updated <i>Section 7.9: "Beeper"</i> |
| 28-Jun-2012 | 12 | Added UFQFPN package thickness in <i>Figure 52: "STM8S105xx access line ordering information scheme"</i> . |
| 7-Feb-2014 | 13 | UART2_CK mapped to correct pin (pin 24) in <i>Figure 4: "LQFP 44-pin pinout"</i> . Reserved area updated in <i>Table 12: "Option bytes "</i> . Package Information updated in <i>Table 55: "32-lead ultra-thin fine pitch quad flat no-lead package mechanical data"</i> . |

17 Disclaimer

Please Read Carefully

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype [ameyasales1](#) [ameyasales2](#)

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com