

# AS1153, AS1157

## Dual LVDS Receiver

### 1 General Description

The AS1153, AS1157 are dual flow-through LVDS (low-voltage differential signaling) receivers which accept LVDS differential inputs and convert them to LVCMOS outputs. The receivers are perfect for low-power low-noise applications requiring high signaling rates and reduced EMI emissions.

The devices are guaranteed to receive data at speeds up to 260Mbps (130MHz) over controlled impedance media of approximately 100Ω. Supported transmission media are PCB traces, backplanes, and cables.

The AS1153, AS1157 features integrated parallel termination resistors (nominally 107Ω), which eliminate the requirement for discrete termination resistors, and reduce stub lengths. The AS1153, AS1157 uses high impedance inputs and requires an external termination resistor when used in a point-to-point connection.

The integrated Failsafe feature sets the output high if the inputs are open, undriven and terminated, or undriven and shorted.

All inputs conform to the *ANSI TIA/EIA-644* LVDS standards. Flow-through pinout simplifies PC board layout and reduces crosstalk by separating the LVDS inputs and LVCMOS outputs.

The devices are available in a 8-pin SOIC package.

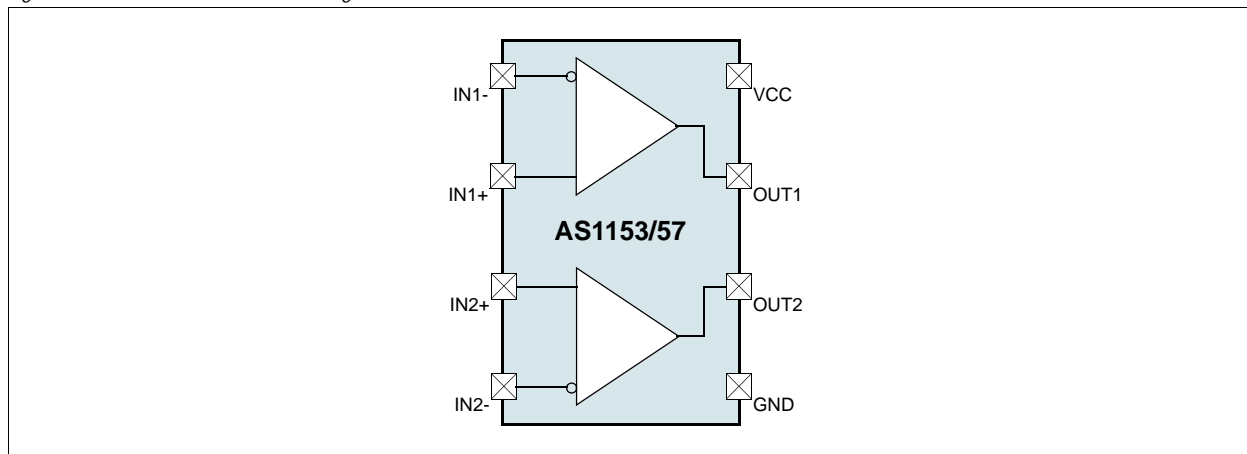
### 2 Key Features

- Flow-Through Pinout
- Guaranteed 260Mbps Data Rate
- 300ps Pulse Skew (Max)
- Conform to *ANSI TIA/EIA-644* LVDS Standards
- Single +3.3V Supply
- Operating Temperature Range: -40°C to +85°C
- Failsafe Circuit
- Integrated Termination (AS1157)
- 8-pin SOIC Package

### 3 Applications

Digital Copiers, Laser Printers, Cellular Phone Base Stations, Add/Drop Muxes, Digital Cross-Connects, DSLAMs, Network Switches/Routers, Backplane Interconnect, Clock Distribution Computers, Intelligent Instruments, Controllers, Critical Microprocessors and Microcontrollers, Power Monitoring, and Portable/Battery-Powered Equipment.

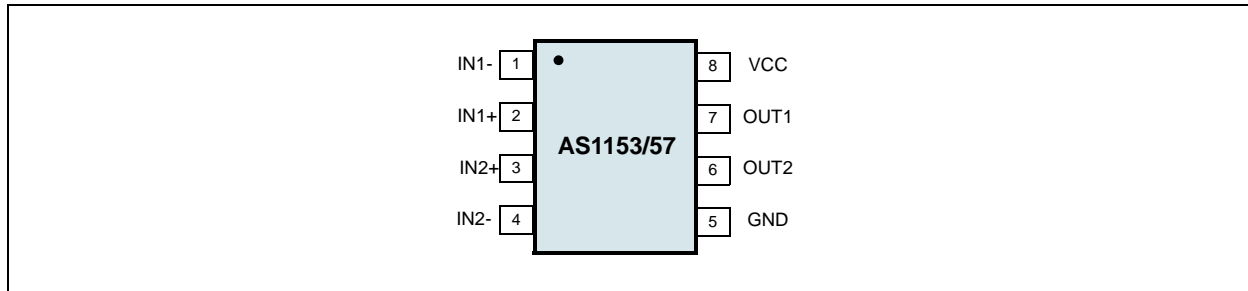
Figure 1. AS1153, AS1157 - Block Diagram



## 4 Pinout and Packaging

### Pin Assignments

Figure 2. Pin Assignments (Top View)



### Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	IN1-	Inverting Differential Receiver Input
2	IN1+	Noninverting Differential Receiver Input
3	IN2+	Noninverting Differential Receiver Input
4	IN2-	Inverting Differential Receiver Input
5	GND	Ground
6	OUT2	LVC MOS/LVTTL Receiver Output
7	OUT1	LVC MOS/LVTTL Receiver Output
8	VCC	Power-Supply Input. Bypass VCC to GND with 0.1 $\mu$ F and 0.001 $\mu$ F ceramic capacitors.

## 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
VCC to GND	-0.3	5.0	V	
INx+, INx- to GND	-0.3	5.0	V	
OUTx+, OUTx- to GND	-0.3	Vcc + 0.3	V	
Electrostatic Discharge				
Electrostatic Discharge HBM	+/- 4		kV	Norm: MIL 883 E method 3015, INx+, INx-
Temperature Ranges and Storage Conditions				
Thermal Resistance $\Theta_{JA}$		128	°C/W	Typical 4-layer application
Junction Temperature		+150	°C	
Storage Temperature Range	-55	+125	°C	
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> . The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	1			Represents a max. floor life time of unlimited

## 6 Electrical Characteristics

### DC Electrical Characteristics

$V_{CC} = +3.0$  to  $+3.6V$ , Differential Input Voltage  $|V_{ID}| = +0.1$  to  $+1.0V$ , Common-Mode Voltage  $V_{CM} = |V_{ID}|/2$  to  $2.4V - |V_{ID}|/2$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$ . Typical values are at  $V_{CC} = +3.3V$ ,  $T_{AMB} = +25^{\circ}C$  (unless otherwise specified).

Table 3. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Temperature Range	$T_{AMB}$		-40		+85	$^{\circ}C$
<b>LVDS Inputs (IN<sub>x+</sub>, IN<sub>x-</sub>)</b>						
Differential Input High Threshold	$V_{TH}$				100	mV
Differential Input Low Threshold	$V_{TL}$		-100			mV
Input Current <sup>1</sup> (AS1153)	$I_{INx+}, I_{INx-}$	$0.1V \leq  V_{ID}  \leq 0.6V$	-20		20	$\mu A$
		$0.6V \leq  V_{ID}  \leq 1.0V$	-25		25	$\mu A$
Differential Input Resistance (AS1157)	$R_{DIFF}$	$V_{CC} = 3.6V$ or 0, Figure 18 on page 9	90	107	132	$\Omega$
Differential Input Resistance (AS1153)	$R_{DIFF}$ <sup>2</sup>	$V_{CC} = 3.6V$ or 0, Figure 18 on page 9	40	100		$k\Omega$
<b>LVC MOS/LVTTL Outputs (OUT<sub>x</sub>)</b>						
Output High Voltage (Table 5)	$V_{OH}$	$I_{OH} = -4.0mA$ (AS1153)	Open, undriven short, or undriven $100\Omega$ parallel termination	2.7	3.2	V
			$V_{ID} = +100mV$	2.7	3.2	
		$I_{OH} = -4.0mA$ (AS1157)	Open or undriven short	2.7	3.2	
			$V_{ID} = +100mV$	2.7	3.2	
Output Low Voltage	$V_{OL}$	$I_{OL} = +4.0mA$ , $V_{ID} = -100mV$		0.1	0.25	V
Output Short-Circuit Current <sup>3</sup>	$I_{OS}$	$V_{ID} = 100mV$ , $V_{OUTx} = 0$	15			mA
<b>Supply</b>						
Supply Current	$I_{CC}$	Inputs open		0.6	2	mA
		$ V_{ID}  = 200mV$		4.5	8	mA

1. Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except  $V_{TH}$ ,  $V_{TL}$ , and  $V_{ID}$ .

2.  $2xR_{IN} = R_{DIFF}$

3. Short only one output at a time. Do not exceed the absolute maximum junction temperature specification.

**Note:** All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

## AC Electrical Characteristics

$V_{CC} = +3.0$  to  $+3.6V$ ,  $C_{LOAD} = 10pF$ , Differential Input Voltage  $|V_{ID}| = 0.2$  to  $1.0V$ , Common-Mode Voltage  $V_{CM} = |V_{ID}|/2$  to  $2.4V - |V_{ID}|/2$ , Input Rise and Fall Time =  $1ns$  (20 to 80%), Input Frequency =  $100MHz$ ,  $T_{AMB} = -40$  to  $+85^{\circ}C$ . Typical values are at  $V_{CC} = +3.3V$ ,  $V_{CM} = 1.2V$ ,  $|V_{ID}| = 0.2V$ ,  $T_{AMB} = +25^{\circ}C$  (unless otherwise specified).<sup>1, 2</sup>

Table 4. AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Propagation Delay High-to-Low	t <sub>PHLD</sub>	Figure 20 on page 11 and Figure 21 on page 12	1	1.8	3.1	ns
Differential Propagation Delay Low-to-High	t <sub>PLHD</sub>	Figure 20 on page 11 and Figure 21 on page 12	1	1.8	3.1	ns
Differential Pulse Skew (t <sub>PHLD</sub> - t <sub>PLHD</sub> ) <sup>3</sup>	tskD1	Figure 20 on page 11 and Figure 21 on page 12		250	600	ps
Differential Channel-to-Channel Skew <sup>4</sup>	tskD2	Figure 20 on page 11 and Figure 21 on page 12			600	ps
Differential Part-to-Part Skew <sup>5</sup>	tskD3	Figure 20 on page 11 and Figure 21 on page 12			0.8	ns
Differential Part-to-Part Skew <sup>6</sup>	tskD4	Figure 20 on page 11 and Figure 21 on page 12			1.5	ns
Rise Time	t <sub>TLH</sub>	Figure 20 on page 11 and Figure 21 on page 12		0.4	1.0	ns
Fall Time	t <sub>THL</sub>	Figure 20 on page 11 and Figure 21 on page 12		0.4	1.0	ns
Maximum Operating Frequency <sup>7, 8</sup>	f <sub>MAX</sub>	All Channels Switching	130	160		MHz

### Notes:

1. AC parameters are guaranteed by design and characterization.
2. CL includes scope probe and test jig capacitance.
3. tskD1 is the magnitude difference of differential propagation delays in a channel.  $tskD1 = |t_{PHLD} - t_{PLHD}|$ .
4. tskD2 is the magnitude difference of the t<sub>PLHD</sub> or t<sub>PHLD</sub> of one channel and the t<sub>PLHD</sub> or t<sub>PHLD</sub> of any other channel on the same device.
5. tskD3 is the magnitude difference of any differential propagation delays between devices operating over rated conditions at the same  $V_{CC}$  and within  $5^{\circ}C$  of each other.
6. tskD4 is the magnitude difference of any differential propagation delays between devices operating over rated conditions.
7. f<sub>MAX</sub> generator output conditions:
  - a. Rise time = fall time =  $1ns$  (0 to 100%)
  - b. 50% duty cycle
  - c.  $V_{OH} = +1.3V$
  - d.  $V_{OL} = +1.1V$
8. Output criteria:
  - a. Duty cycle = 60% to 40%
  - b.  $V_{OL} = 0.4V$  (max)
  - c.  $V_{OH} = 2.7V$  (min)
  - d. Load =  $10pF$

## 7 Typical Operating Characteristics

$V_{CC} = +3.3V$ ,  $V_{CM} = +1.2V$ ,  $|V_{ID}| = 0.2V$ ,  $C_{LOAD} = 10pF$ ,  $T_{AMB} = +25^{\circ}C$ , unless otherwise noted.

Figure 3. Supply Current vs. Frequency

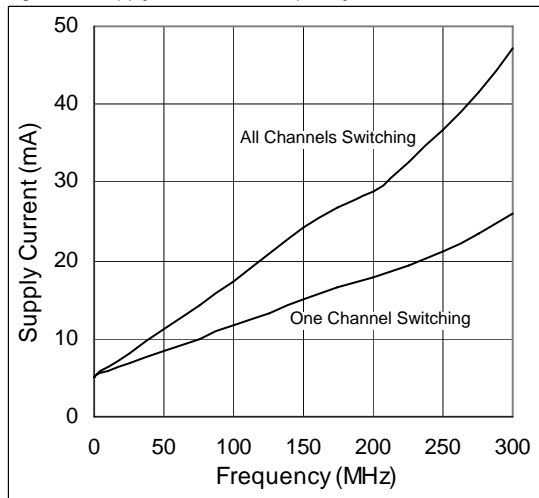


Figure 4. Supply Current vs. Temperature

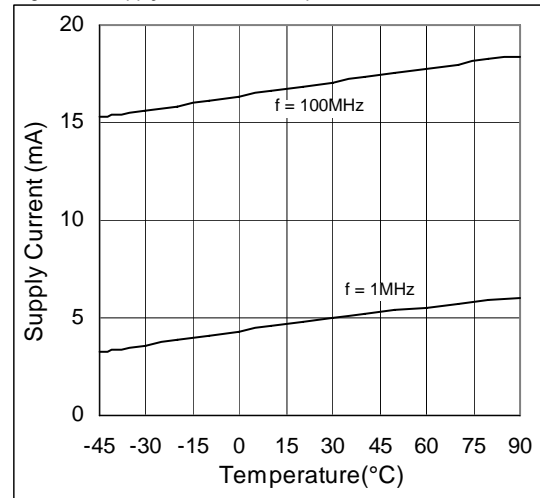


Figure 5. Diff. Threshold Voltage vs.  $V_{CC}$

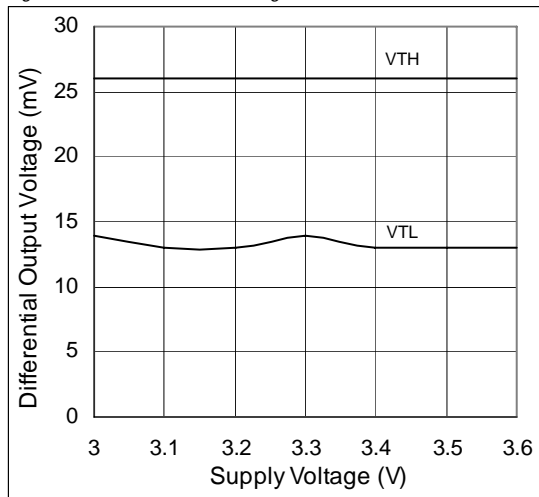


Figure 6. Output Short-Circuit Current vs.  $V_{CC}$

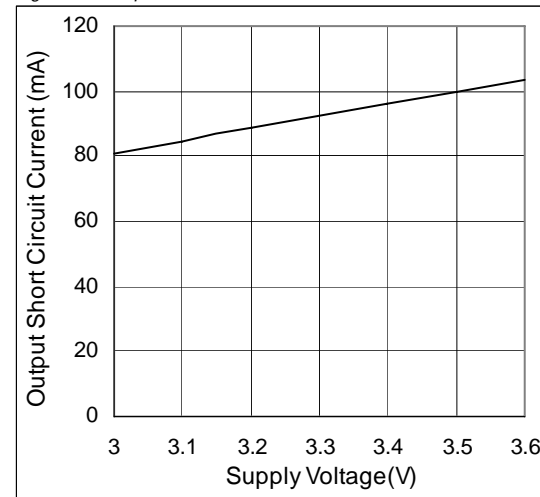


Figure 7. Output Low Voltage vs.  $V_{CC}$

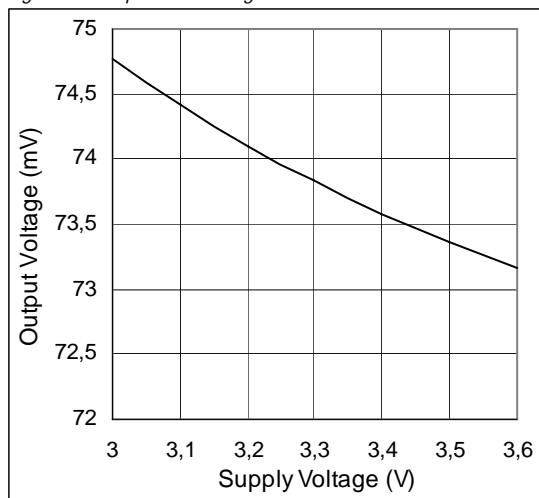


Figure 8. Output High Voltage vs.  $V_{CC}$

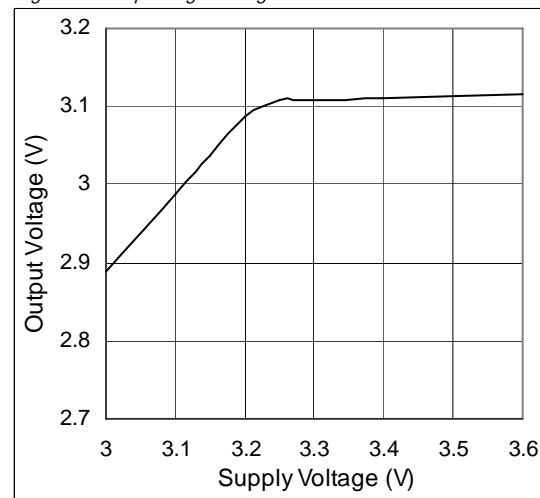


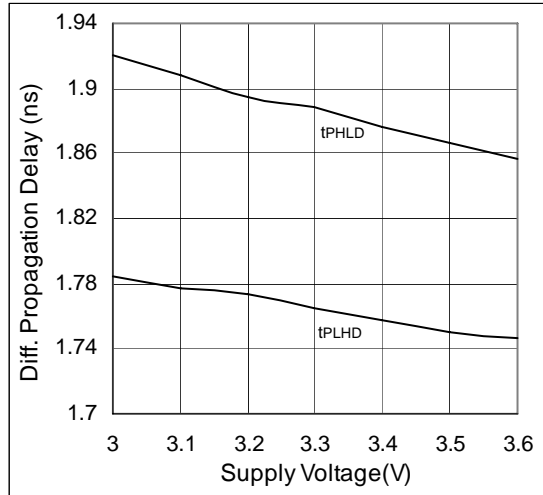
Figure 9. Differential Propagation Delay vs.  $V_{CC}$ 

Figure 10. Differential Propagation Delay vs. Temp.

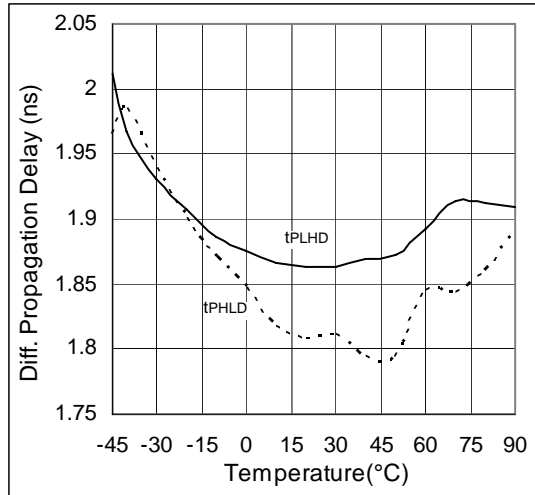
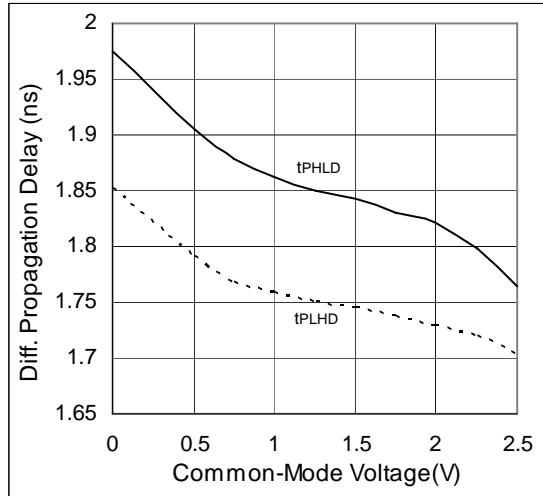
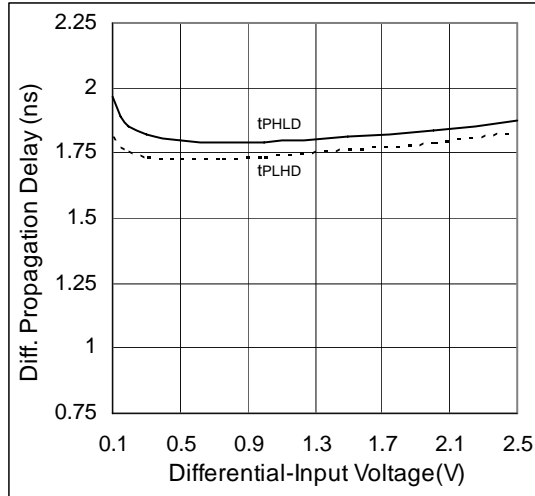
Figure 11. Differential Propagation Delay vs.  $V_{CM}$ Figure 12. Differential Propagation Delay vs.  $V_{ID}$ 

Figure 13. Differential Propagation Delay vs. Load

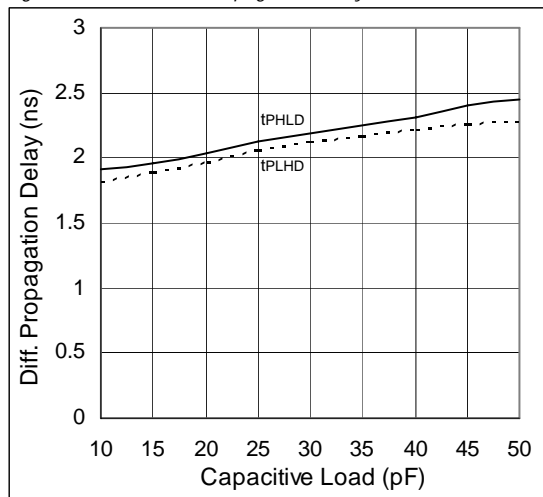


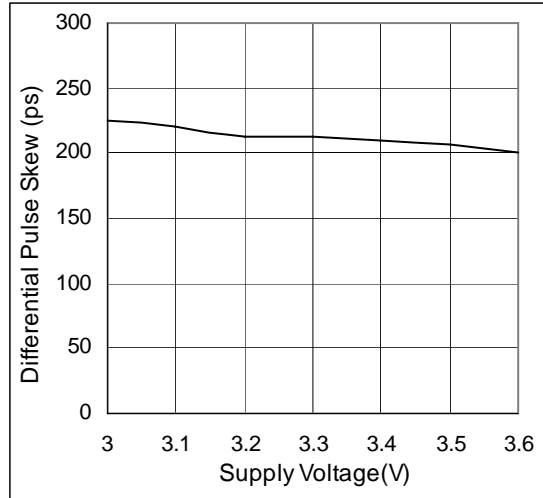
Figure 14. Differential Pulse Skew vs.  $V_{CC}$ 

Figure 15. Transition Time vs. Capacitive Load

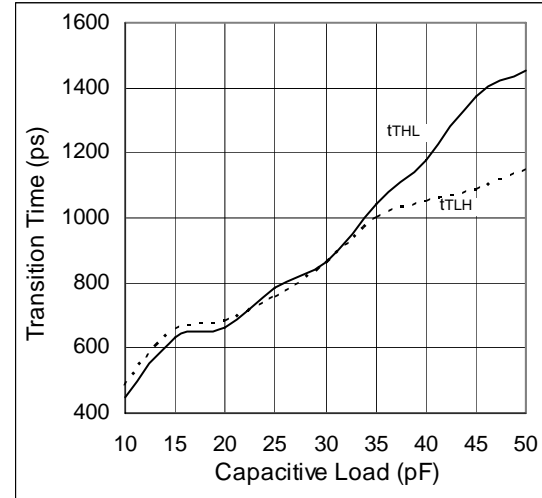
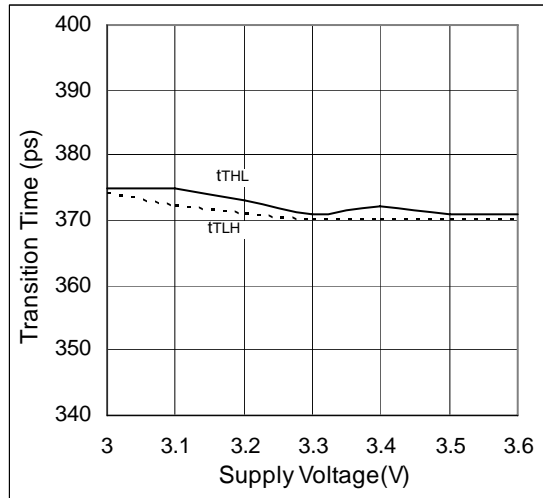
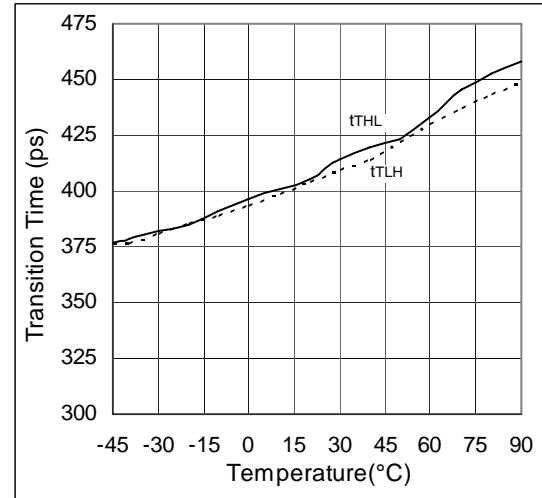
Figure 16. Transition Time vs.  $V_{CC}$ 

Figure 17. Transition Time vs. Temperature





## 8 Detailed Description

The AS1153, AS1157 are 260Mbps, dual-channel LVDS receivers intended for high-speed, point-to-point, low-power applications. Each independent channel accepts and converts an LVDS input to an LVTTTL/LVCMOS output. The devices are capable of detecting differential signals from 100mV to 1V within an input voltage range of 0 to 2.4V.

The 250 to 450mV differential output of an LVDS driver is nominally centered around 1.25V. Due to the receiver input voltage range, a  $\pm 1V$  voltage shift in the signal relative to the receiver is allowed. Thus, a difference in ground references of the transmitter and the receiver, as well as the common mode effect of coupled noise, can be tolerated.

### LVDS Interface

The LVDS Interface Standard is a signaling method defined for point-to-point communication over a controlled-impedance medium as defined by the *ANSI TIA/EIA-644* and *IEEE 1596.3* standards. The LVDS standard uses a lower voltage swing than other common communication standards, resulting in higher data rates, reduced power consumption and EMI emissions, and less susceptibility to noise.

The devices fully comply with the LVDS standard input voltage range of 0 to +2.4V referenced to receiver ground.

The AS1157 has an integrated termination resistors connected internally across each receiver input. This internal termination saves board space, eases layout, and reduces stub length compared to an external termination resistor. In other words, the transmission line is terminated on the IC.

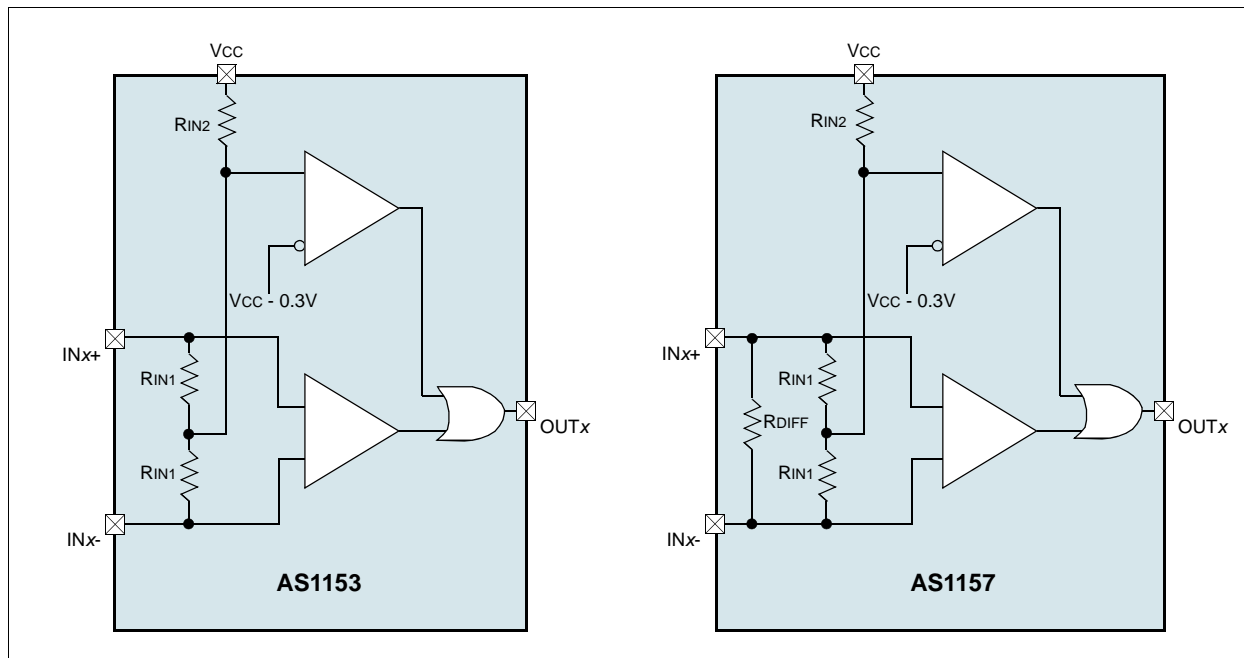
### Failsafe Circuit

The devices contain an integrated Failsafe circuit to prevent noise at inputs that are open, undriven and terminated, or undriven and shorted.

Open or undriven terminated input conditions can occur if there is a cable failure or when the LVDS driver outputs are high impedance. A short condition also can occur because of a cable failure. The Failsafe circuit of the AS1153, AS1157 automatically sets the output high if any of these conditions are true.

The Failsafe input circuit (see Figure 18) samples the input common-mode voltage and compares it to  $V_{CC} - 0.3V$  (nominal). If the input is driven to levels specified in the LVDS standards, the input common-mode voltage is less than  $V_{CC} - 0.3V$  and the Failsafe circuit is not activated. If the inputs are open, undriven and shorted, or undriven and parallel terminated, there is no input current. In this case, a pullup resistor in the Failsafe circuit pulls both inputs above  $V_{CC} - 0.3V$ , activating the Failsafe circuit and thus forcing the device output high.

Figure 18. Failsafe Input Circuit

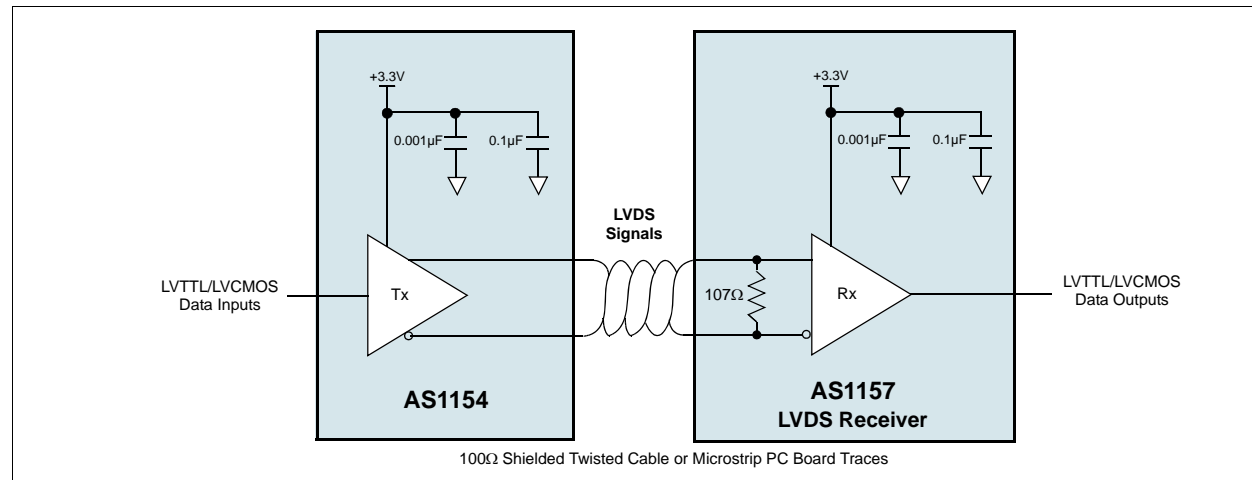


## 9 Applications

Table 5. Function Table

Input		Output
IN <sub>x</sub> +	IN <sub>x</sub> -	OUT <sub>x</sub>
V <sub>ID</sub> ≥ +100mV		H
V <sub>ID</sub> ≤ +100mV		L
AS1153 – Open, undriven short, or undriven 100Ω parallel termination		H
AS1157 – Open or undriven short		

Figure 19. Typical Application Circuit



### Power-Supply Bypassing

To bypass V<sub>CC</sub>, use high-frequency surface-mount ceramic 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to pin V<sub>CC</sub>.

### Differential Traces

Input trace characteristics can adversely affect the performance of the AS1153, AS1157.

- Use controlled-impedance PC board traces to match the cable characteristic impedance. The termination resistor must also be matched to this characteristic impedance.
- Eliminate reflections and ensure that noise couples as common mode by running differential traces close together.
- Reduce skew by using matched trace lengths. Tight skew control is required to minimize emissions and proper data recovery of the devices.
- Route each channel's differential signals very close to each other for optimal cancellation of their respective external magnetic fields. Use a constant distance between the differential traces to avoid irregularities in differential impedance.
- Avoid 90° turns (use two 45° turns).
- Minimize the number of vias to further prevent impedance irregularities.

## Cables and Connectors

Supported transmission media include printed circuit board traces, backplanes, and cables.

- Use cables and connectors with matched differential impedance (typically  $100\Omega$ ) to minimize impedance mismatches.
- Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.
- Avoid the use of unbalanced cables such as ribbon cable or simple coaxial cable.

## Termination

Due to the high data rates of LVDS drivers, matched termination will prevent the generation of any signal reflections, and reduce EMI.

- The AS1157 has integrated termination resistors connected across the inputs of each receiver. The value of the integrated resistor is specified in Table 3.
- The AS1153 requires an external termination resistor. The termination resistor should match the differential impedance of the transmission line and be placed as close to the receiver inputs as possible. Termination resistance values may range between  $90$  to  $132\Omega$  depending on the characteristic impedance of the transmission medium. Use 1% surface-mount resistors.

## Board Layout

The device should be placed as close to the interface connector as possible to minimize LVDS trace length.

- Keep the LVDS and any other digital signals separated from each other to reduce crosstalk.
- Use a four-layer PC board that provides separate power, ground, LVDS signals, and input signals.
- Isolate the input LVDS signals from each other and the output LVCMOS/LVTTL signals from each other to prevent coupling.
- Separate the input LVDS signals from the output signals planes with the power and ground planes for best results.

Figure 20. Propagation Delay and Transition Time Test Circuit

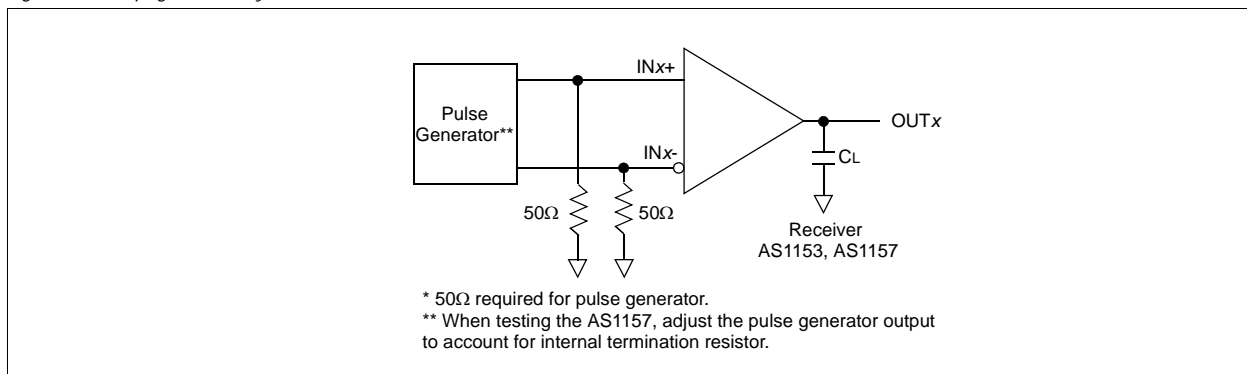
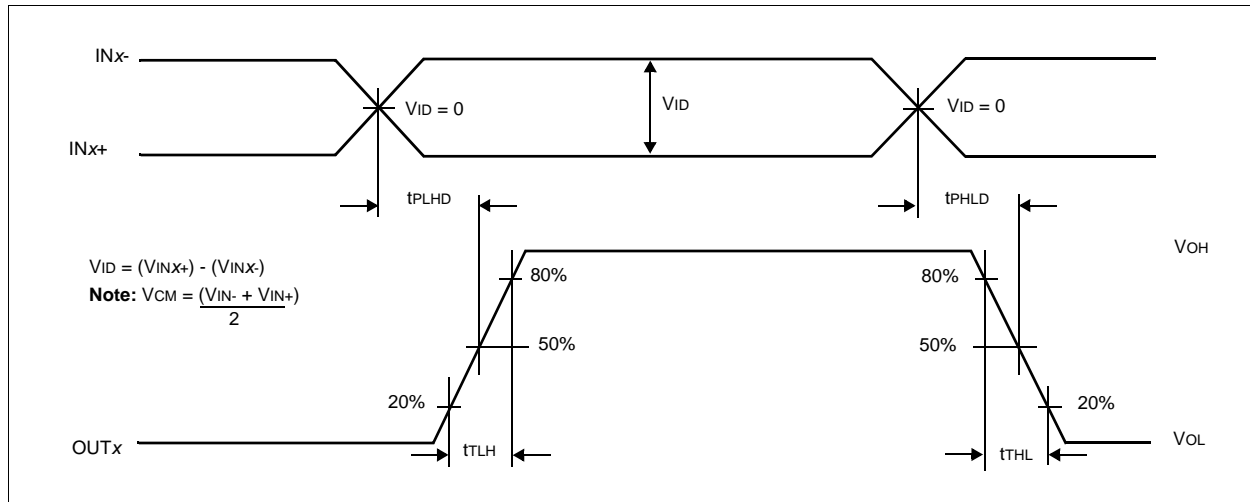


Figure 21. Propagation Delay and Transition Time Waveforms



## 10 Package Drawings and Markings

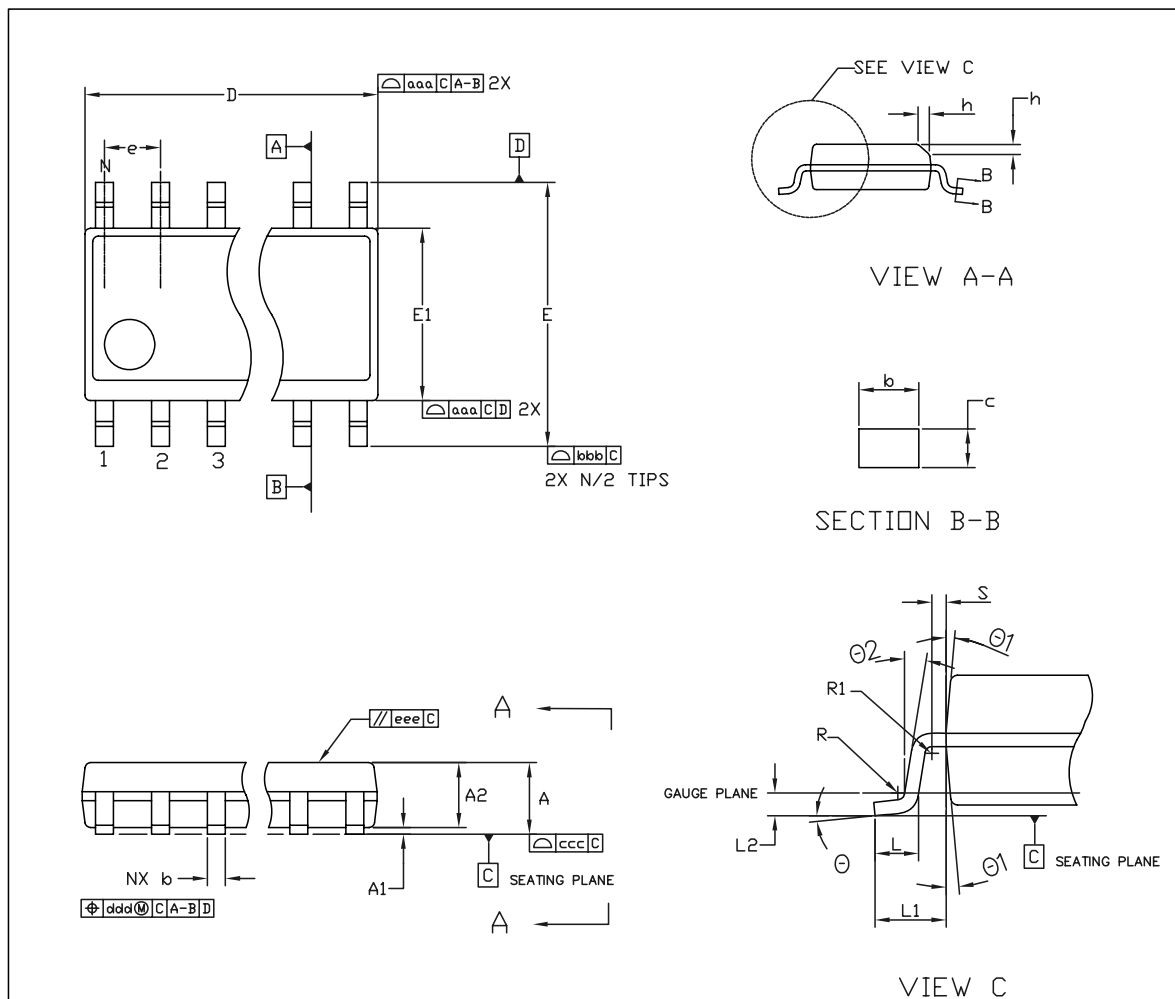
Figure 22. 8-pin SOIC Marking



Table 6. Packaging Code xxxx

xxxx
encoded Datecode

Figure 23. 8-pin SOIC Package Diagram



REF.	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.17	—	0.25
D	—	4.90 BSC	—
E	—	6.00 BSC	—
E1	—	3.90 BSC	—
e	—	1.27 BSC	—
L	0.40	—	1.27
L1	—	1.40 REF	—
L2	—	0.25 BSC	—
R	0.07	—	—
R1	0.07	—	—
h	0.25	—	0.50
theta	0°	—	8°
theta1	5°	—	15°
theta2	0°	—	—
aaa	—	0.10	—
bbb	—	0.20	—
ccc	—	0.10	—
ddd	—	0.25	—
eee	—	0.10	—
fff	—	0.15	—
ggg	—	0.15	—
N	—	8	—

## NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.



 austriamicrosystems  
*a leap ahead in analog*

ASSEMBLY ENGINEERING

TITLE  
SOIC mm, 8 LEAD, 150MILREFERENCE DOCUMENT  
JEDEC MS - 012  
latest revisionDRAWN  
RH8DATE  
2010.09.21REV.  
N/CCHECKED  
GBODATE  
2010.09.21DRAWING NO.  
JLC

UNIT

APPROVED  
MKRDATE  
2010.09.21SHEET  
1 OF 1

DIMENSION AND TOLERANCE

SCALE  
NOT IN SCALE

## 11 Ordering Information

The devices are available as the standard products shown in Table 7.

Table 7. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1153	AS1153	Dual LVDS Receiver	Tubes	8-pin SOIC
AS1153-T	AS1153	Dual LVDS Receiver	Tape and Reel	8-pin SOIC
AS1157	AS1157	Dual LVDS Receiver, with termination	Tubes	8-pin SOIC
AS1157-T	AS1157	Dual LVDS Receiver, with termination	Tape and Reel	8-pin SOIC

**Note:** All products are RoHS compliant.

Buy our products or get free samples online at ICdirect: <http://www.austriamicrosystems.com/ICdirect>

Technical Support is found at <http://www.austriamicrosystems.com/Technical-Support>

For further information and requests, please contact us <mailto:sales@austriamicrosystems.com>  
or find your local distributor at <http://www.austriamicrosystems.com/distributor>

## Copyrights

Copyright © 1997-2010, austriamicrosystems AG, Tobelbaderstrasse 30, 8141 Unterpremstaetten, Austria-Europe. Trademarks Registered ®. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

All products and companies mentioned are trademarks or registered trademarks of their respective companies.

## Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.



## Contact Information

Headquarters

austriamicrosystems AG  
Tobelbaderstrasse 30  
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0  
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

<http://www.austriamicrosystems.com/contact>



# AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit [www.ameya360.com](http://www.ameya360.com)

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct     +86 (21) 6401-6692  
  
Email       amall@ameya360.com  
  
QQ         800077892  
  
Skype      ameyasales1 ameyasales2

➤ Customer Service :

Email       service@ameya360.com

➤ Partnership :

Tel         +86 (21) 64016692-8333  
  
Email      mkt@ameya360.com