

**8-BIT SHIFT REGISTER WITH 8-BIT OUTPUT REGISTER**

**Description**

The 74HCT594 is a high speed CMOS device that is designed to be pin compatible with 74LS low power Schottky types.

An eight bit shift register accepts data from the serial input (DS) on each positive transition of the shift register clock (SHCP). When asserted low the shift register reset function ( $\overline{\text{SHR}}$ ) sets all shift register values to zero and is independent of all clocks. Also when asserted low the storage register reset function ( $\overline{\text{STR}}$ ) sets all shift register values to zero and is independent of all clocks

Data from the input serial shift register is placed in the output register with a rising pulse on the storage register clock (STCP). The storage register includes output Q7S which is used for cascading information between devices. As the information moves into the storage register, it is asserted on the push-pull outputs Q0-Q7.

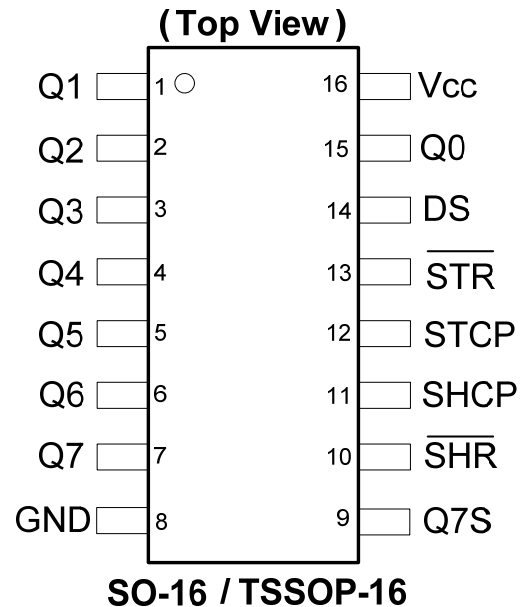
All registers capture data on rising edge and change output on the falling edge. If both clocks are connected together, the input shift register is always one clock cycle ahead of the output register.

**Features**

- Wide Supply Voltage Range from 4.5V to 5.5V
- Sinks or sources 8mA at  $V_{CC} = 4.5V$
- CMOS low power consumption
- Schmitt Trigger Action at All Inputs
- Inputs accept up to 6.0V
- ESD Protection Tested per JESD 22
  - Exceeds 200-V Machine Model (A115-A)
  - Exceeds 2000-V Human Body Model (A114-A)
  - Exceeds 1000-V Charged Device Model (C101C)
- Latch-Up Exceeds 250mA per JESD 78, Class II
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.  
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.  
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and < 1000 ppm antimony compounds.

**Pin Assignments**



**Applications**

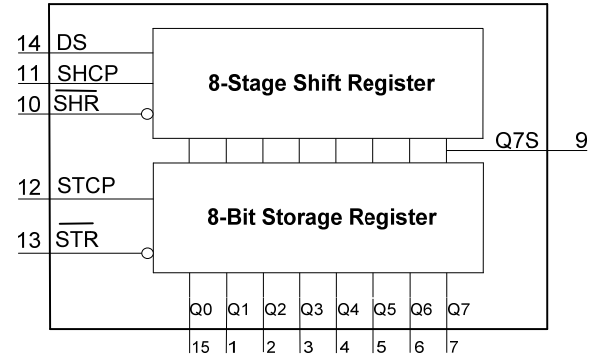
- General Purpose Logic
- Serial to Parallel Data conversion
- Capture and hold data for extended periods of time.
- Allow simple serial bit streams from a microcontroller to control as many peripheral lines as needed.
- Wide array of products such as:
  - Computer peripherals
  - Appliances
  - Industrial control

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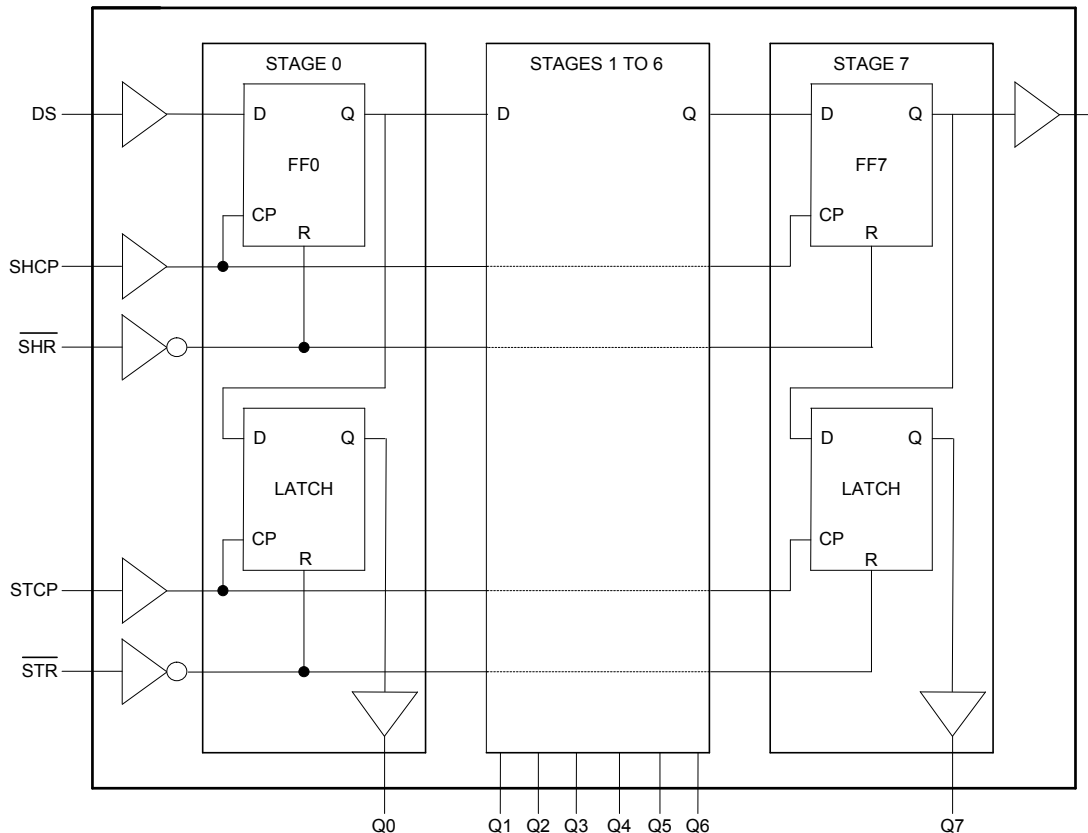
**Pin Descriptions**

Pin Number	Pin Name	Description
1	Q1	Parallel Data Output 1
2	Q2	Parallel Data Output 2
3	Q3	Parallel Data Output 3
4	Q4	Parallel Data Output 4
5	Q5	Parallel Data Output 5
6	Q6	Parallel Data Output 6
7	Q7	Parallel Data Output 7
8	GND	Ground
9	Q7S	Serial Data Output
10	$\overline{\text{SHR}}$	Shift Register Reset active low
11	SHCP	Shift Register Clock Input
12	STCP	Storage Register Clock Input
13	$\overline{\text{STR}}$	Storage Register Reset active low
14	DS	Serial Data Input
15	Q0	Parallel Data Output 0
16	Vcc	Supply Voltage

**Functional Diagram**



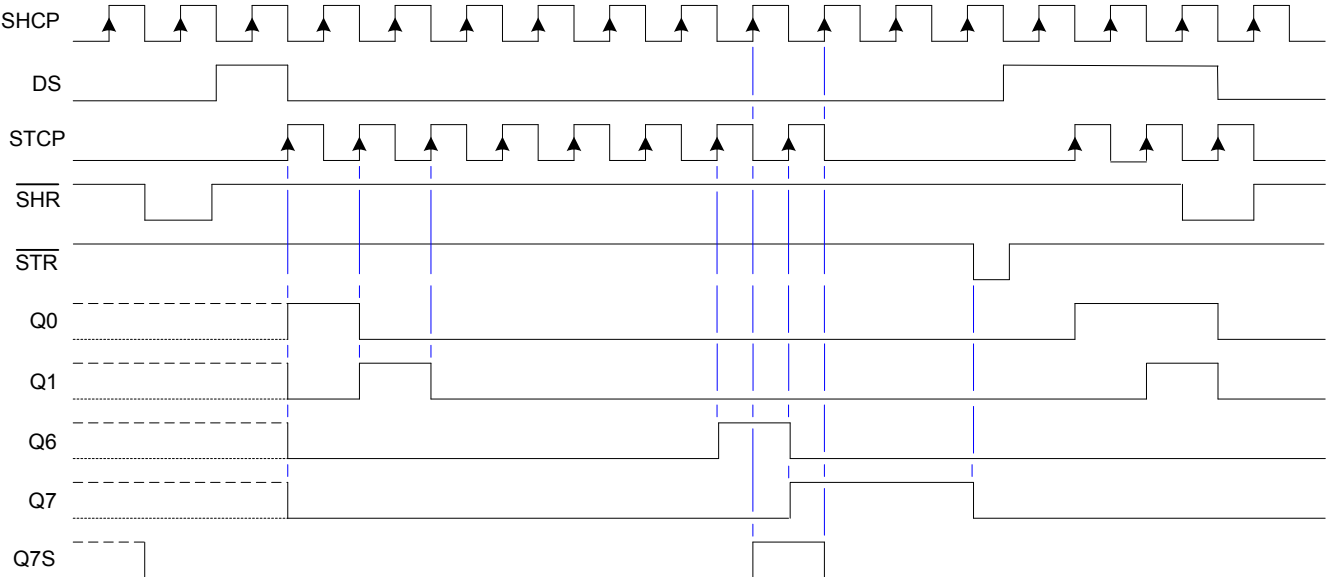
**Logic Diagram**



**Functional Description and Timing Diagram**

Control				Input	Output		Function
$\overline{\text{SHR}}$	$\overline{\text{STR}}$	SHCP	STCP	DS	Q7S	Qn	
L	X	X	X	X	L	NC	Clear Shift Register
X	L	X	X	X	NC	L	Clear Storage Register
H	X	↑	L	H or L	Q6S	NC	Loads DS into shift register stage 0. All Q <sub>S</sub> shifted
H	H	X	↑	X	NC	Q <sub>S</sub>	Contents of shift register moved to starge register all Q <sub>S</sub> -> Q <sub>N</sub>
H	H	↑	↑	H or L	Q6S	QnS	Shift Register one pulse count ahead of storage register.

H=HIGH voltage state  
 L=LOW voltage state  
 ↑=LOW to HIGH transition  
 X= don't care – high or low (not floating)  
 NC= No change



**Absolute Maximum Ratings** (Note 4) (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Description	Rating	Unit	
ESD HBM	Human Body Model ESD Protection	2	KV	
ESD CDM	Charged Device Model ESD Protection	1	KV	
ESD MM	Machine Model ESD Protection	200	V	
$V_{CC}$	Supply Voltage Range	-0.5 to 7.0	V	
$V_I$	Input Voltage Range	-0.5 to 7.0	V	
$V_O$	Voltage applied to output in high or low state	-0.3 to $V_{CC} + 0.5$	V	
$I_{IK}$	Input Clamp Current $V_I < -0.5V$	-20	mA	
$I_{IK}$	Input Clamp Current $V_I > V_{CC} + 0.5V$	20	mA	
$I_{OK}$	Output Clamp Current $V_O < -0.5V$	-20	mA	
$I_{OK}$	Output Clamp Current $V_O > V_{CC} + 0.5V$	20	mA	
$I_O$	Continuous output current	Q7 standard output	+/- 25	mA
		Qn bus driver outputs	+/- 35	mA
$I_{CC}$	Continuous current through $V_{CC}$	70	mA	
$I_{GND}$	Continuous current through GND	-70	mA	
$T_J$	Operating Junction Temperature	-40 to +150	$^\circ\text{C}$	
$T_{STG}$	Storage Temperature	-65 to +150	$^\circ\text{C}$	
$P_{TOT}$	Total Power Dissipation	500	mW	

Notes: 4. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

**Recommended Operating Conditions** (Note 5) (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply Voltage	–	4.5	5.5	V
$V_I$	Input Voltage	–	0	5.5	V
$V_O$	Output Voltage	Active Mode	0	$V_{CC}$	V
$\Delta t/\Delta V$	Input transition rise or fall rate	$V_{CC} = 4.5V$ to $5.5V$	–	500	ns/V
$T_A$	Operating free-air temperature	–	-40	+125	$^\circ\text{C}$

Notes: 5. Unused inputs should be held at  $V_{CC}$  or Ground.

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	V <sub>CC</sub>	T <sub>A</sub> = +25°C			-40°C to +85°C		-40°C to +125°C		Unit	
				Min	Typ	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High-level Input Voltage	–	4.5 V to 5.5 V	2.0	1.6	–	2.0	–	2.0	–	V	
V <sub>IL</sub>	Low-level input voltage	–	4.5 V to 5.5 V	–	–	0.8	–	0.8	–	0.8	V	
V <sub>OH</sub>	High Level Output Voltage	I <sub>OH</sub> = -20μA All outputs	4.5 V	4.4	4.5	–	4.4	–	4.4	–	V	
	Q7S output	I <sub>OH</sub> = -4.0mA	4.5 V	3.98	4.32	–	3.85	–	3.7	–		
	Qn Bus Outputs	I <sub>OH</sub> = -6.0 mA	4.5 V	3.98	4.32	–	3.85	–	3.7	–	–	
V <sub>OL</sub>	Low-level Output Voltage	I <sub>OL</sub> = 20μA All outputs	4.5 V	–	0	0.1	–	0.1	–	0.1	V	
	Q7S output	I <sub>OL</sub> = 4.0mA	4.5 V	–	0.15	0.26	–	0.33	–	0.4		
	Qn Bus Outputs	I <sub>OL</sub> = 6.0mA	4.5 V	–	0.16	0.26	–	0.33	–	0.4	–	
I <sub>I</sub>	Input Current	V <sub>I</sub> = GND to 5.5 V	5.5 V	–	–	±0.1	–	± 1	–	± 1	μA	
I <sub>CC</sub>	Supply Current	V <sub>I</sub> = GND or V <sub>CC</sub> I <sub>O</sub> = 0	5.5 V	–	–	8.0	–	80	–	160	μA	
ΔI <sub>CC</sub>	Additional Supply Current	Test Per Pin	PINS SHCP SHST $\overline{\text{SHR}}$ $\overline{\text{STR}}$	4.5V to 5.5 V	–	100	240	–	300	–	300	μA
		Other										
C <sub>i</sub>	Input Capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	–	3.5	10	–	–	10	–	10	pF

**Operating Characteristics**

Parameter		Test Conditions	V <sub>CC</sub> = 5V	Unit
			TYP	
C <sub>pd</sub>	Power dissipation capacitance	f = 1 MHz all outputs switching-no load V <sub>I</sub> = GND TO V <sub>CC</sub> – 1.5V	51	pF

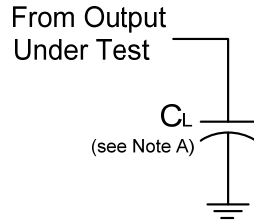
**Switching Characteristics**

Symbol / Parameter	Pins	Test Conditions	V <sub>cc</sub>	T <sub>A</sub> = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ.	Max	Min	Max	Min	Max	
f <sub>MAX</sub> Maximum Frequency	SHCP or STCP	Figure 2 C <sub>L</sub> =15pF	5.0 V	30	92	–	24	–	20	–	MHz
t <sub>w</sub> Pulse Width	SHCP HIGH or LOW	Figure 2 C <sub>L</sub> =50pF	4.5 V	16	4	–	20	–	24	–	ns
	STCP HIGH or LOW	Figure 2 C <sub>L</sub> =50pF	4.5 V	16	4	–	20	–	24	–	
	SHR and STR HIGH or LOW	Figure 2 C <sub>L</sub> =50pF	4.5 V	16	6	–	20	–	24	–	
t <sub>su</sub> Set-up Time	DS to SHCP	Figure 2 C <sub>L</sub> =50pF	4.5 V	20	4	–	25	–	30	–	ns
	SHR to STCP	Figure 2 C <sub>L</sub> =50pF 2	4.5 V	20	6	–	25	–	30	–	
	SHCP to STCP	Figure 2 C <sub>L</sub> =50pF	4.5 V	20	7	–	25	–	30	–	
t <sub>PD</sub> Propagation Delay	SHCP to Q7S	Figure 2 C <sub>L</sub> =50p	4.5 V	–	18	32	–	40	–	48	ns
		Figure 2 C <sub>L</sub> =15pF	5.0 V	–	15	–	–	–	–	–	
	STCP to Qn	Figure 2 C <sub>L</sub> =50p	4.5 V	–	18	32	–	40	–	48	
		Figure 2 C <sub>L</sub> =15p	5.0 V	–	15	–	–	–	–	–	
t <sub>H</sub> Hold Time	DS to SHCP	Figure 2	4.5 V	5	-3	–	6	–	7	–	ns
t <sub>REC</sub> Recovery Time	SHR to SHCP and STR to STCP	Figure 2	4.5 V	10	-5	–	13	–	15	–	ns

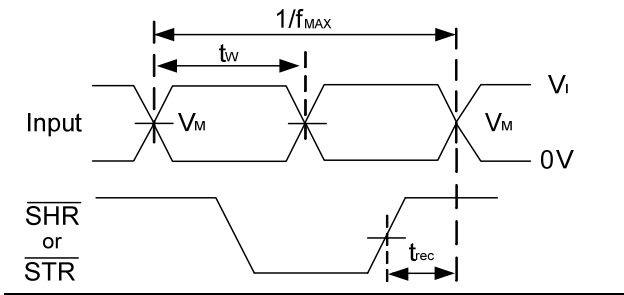
**Switching Characteristics** (cont.)

Symbol / Parameter	Pins	Test Conditions	V <sub>CC</sub>	T <sub>A</sub> = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ.	Max	Min	Max	Min	Max	
t <sub>PHL</sub> Propagation Delay	SHR to Q7S	Figure 2 C <sub>L</sub> =50pF	4.5 V	–	17	30	–	38	–	45	ns
		Figure 2 C <sub>L</sub> =15pF	5.0 V	–	14	–	–	–	–	–	
	STR to Qn	Figure 2 C <sub>L</sub> =50pF	4.5 V	–	17	30	–	38	–	45	ns
		Figure 2 C <sub>L</sub> =15pF	5.0 V	–	14	–	–	–	–	–	
t <sub>THL</sub> t <sub>TLH</sub> Transition Times	Serial data output Q7S	Figure 2 C <sub>L</sub> =50pF	4.5 V	–	7	15	–	19	–	22	ns
	Parallel Data Outputs Q <sub>N</sub>	Figure 2 C <sub>L</sub> =50pF	4.5 V	–	5	12	–	15	–	18	ns

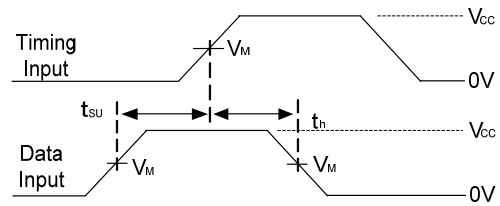
**Parameter Measurement Information**



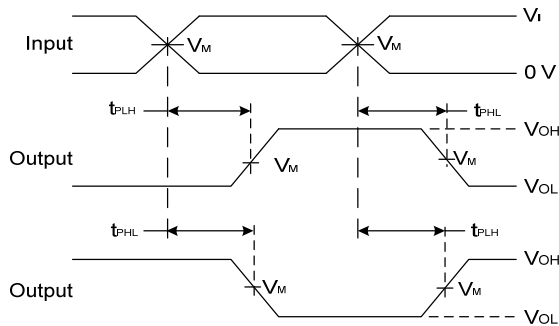
$V_{CC}$	Inputs		$V_M$
	$V_I$	$t_r/t_f$	
4.5V	$V_{CC}$	6ns	$V_{CC}/2$
5.0V	$V_{CC}$	6ns	$V_{CC}/2$



**Voltage Waveform  
Pulse Duration and Recovery Time**



**Voltage Waveform  
Set-up and Hold Times**



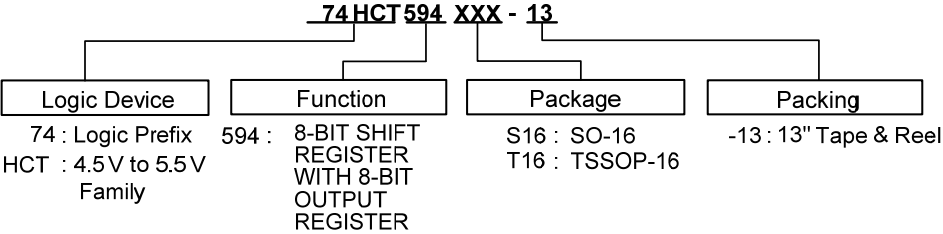
**Voltage Waveform  
Propagation Delay Times  
Inverting and Non Inverting Outputs**

- Notes: A . Includes test lead and test apparatus capacitance.  
 B. All pulses are supplied at pulse repetition rate  $\leq 10$  MHz  
 C. Inputs are measured separately one transition per measurement  
 D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$

**Figure 2. Load Circuit and Voltage Waveforms**



**Ordering Information**

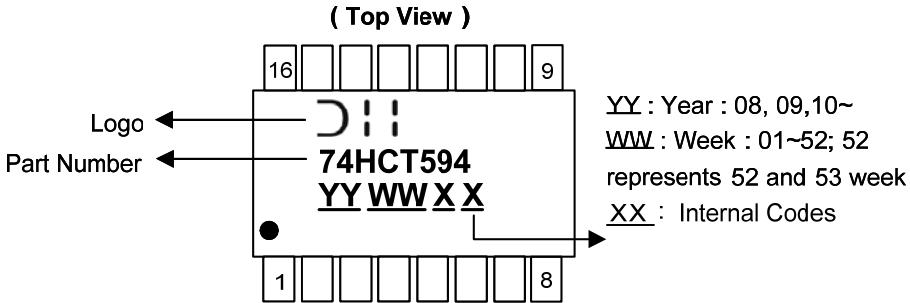


Device	Package Code	Packaging	7" Tape and Reel (Note 6)	
			Quantity	Part Number Suffix
74HCT594S16-13	S16	SO-16	2500/Tape & Reel	-13
74HCT594T16-13	T16	TSSOP-16	2500/Tape & Reel	-13

Notes: 6. The taping orientation is located on our website at <http://www.diodes.com/datasheets/ap02007.pdf>

**Marking Information**

**(1) SO-16, TSSOP-16**

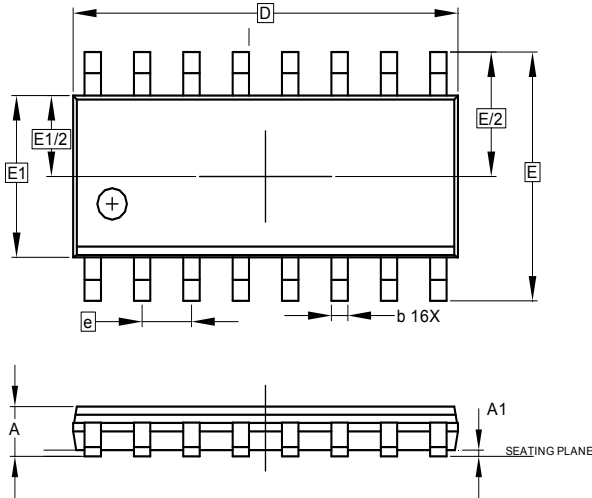


Part Number	Package
74HCT594S16	SO-16
74HCT594T16	TSSOP-16

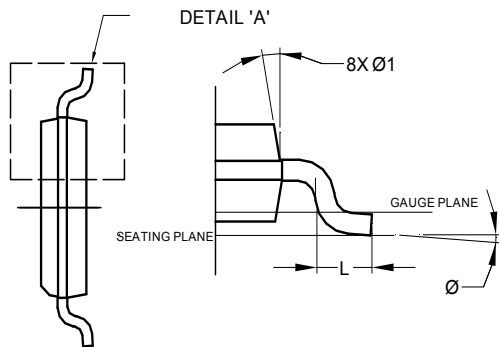
**Package Outline Dimensions** (All Dimensions in mm.)

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

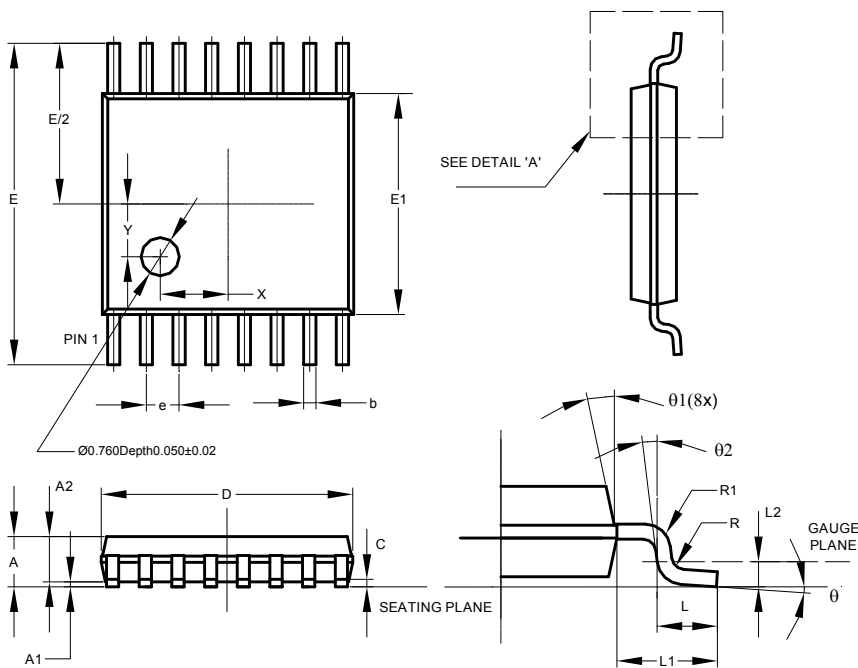
**(1) Package Type: SO-16**



SOIC-16			
Dim	Min	Max	Typ
A	—	1.75	—
A1	0.10	0.25	—
b	0.31	0.51	—
c	0.10	0.25	—
D	9.80	10.00	—
E	5.80	6.20	—
E1	3.80	4.00	—
e	—	—	1.27
L	0.40	1.27	—
Ø	0°	8°	—
Ø1	5°	15°	—
All Dimensions in mm			



**(2) Package Type: TSSOP-16**

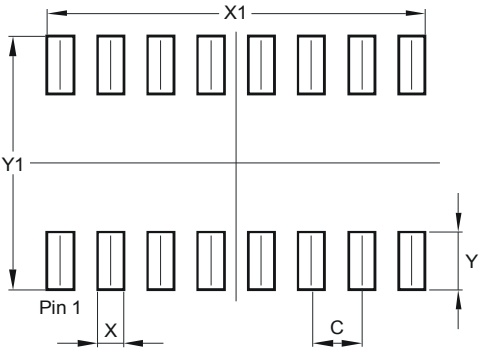


TSSOP-16			
Dim	Min	Max	Typ
A	—	1.08	—
A1	0.05	0.15	—
A2	0.80	0.93	—
b	0.19	0.30	—
c	0.09	0.20	—
D	4.90	5.10	—
E	6.40 BSC		
E1	4.30	4.50	—
e	0.65 BSC		
L	0.45	0.75	—
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	—	—
R1	0.09	—	—
X	—	—	1.350
Y	—	—	1.050
Ø	0°	8°	—
Ø1	5°	15°	—
Ø2	0°	—	—
All Dimensions in mm			

**Suggested Pad Layout**

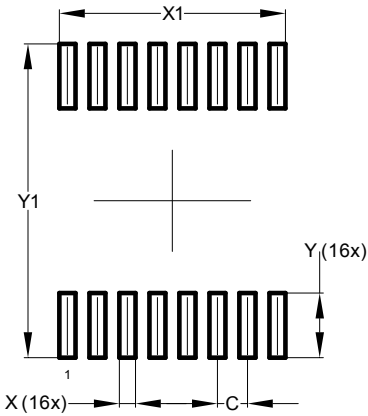
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

**Package Type: SO-16**



Dimensions	Value (in mm)
C	1.270
X	0.670
X1	9.560
Y	1.450
Y1	6.400

**Package Type: TSSOP-16**



Dimensions	Value (in mm)
C	0.650
X	0.350
X1	4.900
Y	1.400
Y1	6.800

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