Data Sheet August 2004 FN9117.2

Highly Integrated Battery Charger for Notebook Computers

The ISL6253 is a highly integrated battery charger controller for Li-Ion/Li-Polymer batteries. High Efficiency is achieved by a synchronous buck topology and the use of a MOSFET, instead of a diode, for selecting power from the adapter or battery. The low side MOSFET emulates a diode at light loads to improve the light load efficiency and prevent system bus boosting.

The constant output voltage can be selected for 2, 3 or 4 series Li-Ion cells with 0.5% accuracy over temperature. It can also be programmed between 4.2V +5% per cell and 4.2V -5% per cell to optimize battery capacity. When supplying the load and battery charger simultaneously, the input current limit for the AC adapter is programmable to within 3% accuracy to avoid overloading the AC adapter, and to allow the system to make efficient use of available adapter power for charging. It also has programmable charging current with 4% accuracy. The ISL6253 provides outputs that are used to monitor the current drawn from the AC adapter, and to monitor for the presence of an AC adapter. The ISL6253 automatically transitions from regulating current to regulating voltage. A conditioning charge feature provides approximately 10% of full scale charge current to safely charge deeply discharged lithium-ion (LI+) battery packs when the battery voltage is below 3.0V/cell.

ISL6253 has a feature of automatic power source selection by switching to the battery when the AC adapter is removed or switching to the AC adapter when the AC adapter is available. It also supports aircraft power applications while powering the system and not charging the battery.

Ordering Information

PART #	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6253HRZ (Note 1)	-10 to 100	28 Ld 5x5 QFN (Pb-free)	L28.5x5
ISL6253HAZ (Note 1)	-10 to 100	28 Ld QSOP (Pb-free)	M28.15

NOTES:

1. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.
2. Add “-T” for Tape and Reel.

Features

- ±0.5% Voltage Accuracy
- ±3% Input Current Limit Accuracy
- ±4% Accurate Battery Charge Current Limit
- Programmable Charge Limit Current, Adaptor Current Limit and Charge Voltage
- Fixed 300kHz PWM Synchronous Buck Controller with Diode Emulation at Light Load
- Output for Current Drawn from the AC Adapter
- AC Adapter Present Indicator
- Fast Input Current Limit Response
- Input Voltage Range 7V to 25V
- Up to 17.6V Battery-Voltage Set Point
- Trickle Charge Mode When Battery Voltage is below 3.0V/Cell
- Supports 2, 3 and 4 Cell Battery Packs
- Control Adapter Power Source Select MOSFET
- Thermal Shutdown
- Aircraft Power Capable
- DC Adapter Present Indicator
- Battery Discharge MOSFET Control
- Less than 10µA Battery Leakage Current
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-free Available

Applications

- Notebook, Desknote and Sub-notebook Computers
- Personal Digital Assistants

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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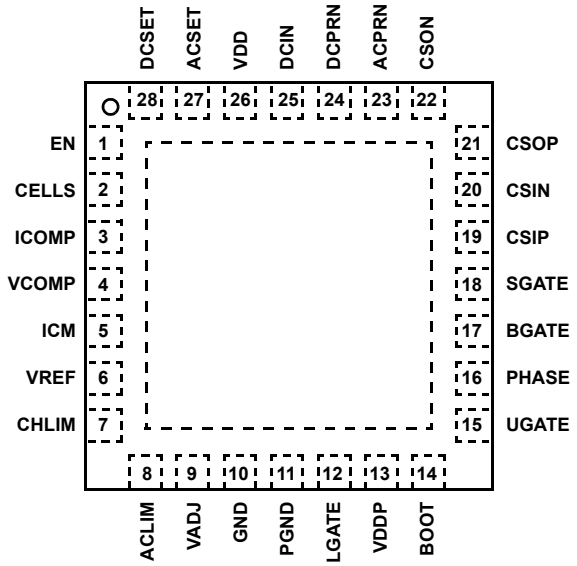
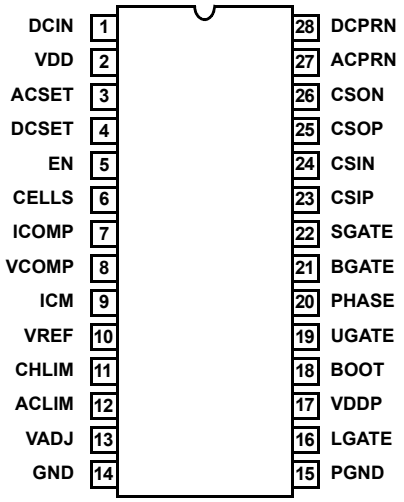
Pinouts

ISL6253 (28 LD QFN)
TOP VIEW



ISL6253 (28 LD QSOP)
TOP VIEW



Absolute Maximum Ratings

DCIN, CSIP, DCPRN, ACPRN, CSON to GND . . . . . -0.3V to +28V
CSIP-CSIN, CSOP-CSON . . . . . -0.3V to +0.3V
CSIP-SGATE, CSIP-BGATE . . . . . -0.3V to 16V
PHASE to GND . . . . . -7V to 28V
BOOT to GND . . . . . -0.3V to +35V
BOOT-PHASE, VDD-GND, VDDP-PGND . . . . . -0.3V to 7V
ICM, ICOMP, VCOMP . . . . . -0.3V to VDD+0.3V
ACSET and DCSET to GND (Note 3) . . . . . -0.8V to VDD+0.3V
VDDP, ACLIM, CHLIM, VREF, CELLS. . . . . -0.3V to VDD+0.3V
EN, VADJ, PGND to GND . . . . . -0.3V to VDD+0.3V
UGATE. . . . . PHASE-0.3V to BOOT+0.3V
LGATE . . . . . PGND-0.3V to VDDP+0.3V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 6).	39	9.5
QSOP Package (Note 5)	80	NA

ESD Classification . . . . . Level 1
Junction Temperature Range. . . . . -10°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature. . . . . -65°C to +150°C
Lead Temperature (soldering, 10s).. . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress ratings only and operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

NOTES:

3. When the voltage across ACSET and DCSET is below 0V, the current through ACSET and DCSET should be limited less than 1mA.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = DCSET = 1.5V, VREF = ACLIM = CHLIM, VADJ = Floating, EN = VDD = 5V, BOOT-PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq$ 125°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND BIAS REGULATOR					
DCIN Input Voltage Range		7		25	V
DCIN Quiescent Current	EN = VDD, 7V $\leq$ DCIN $\leq$ 25V		1.6	4	mA
DCIN Quiescent Current in Shutdown mode	EN = 0, 7V $\leq$ DCIN $\leq$ 25V		1.3	3	mA
Battery Leakage Current (Note 5)	DCIN = 0, no load		2	10	µA
VDD Output Voltage/Regulation	7V $\leq$ DCIN $\leq$ 25 V, 0 $\leq$ I_{VDD} $\leq$ 30mA	4.925	5.075	5.225	V
VDD Undervoltage Lockout Trip Point	Rising	4.2	4.4	4.6	V
	Hysteresis	100	250	400	mV
Reference Output Voltage VREF	O $\leq$ I_{VREF} $\leq$ 300µA	2.365	2.390	2.415	V
Battery Charge Voltage Accuracy	CSON = 16.8V, CELLS = VDD, VADJ = Float	-0.5	0	0.5	%
	CSON = 12.6V, CELLS = GND, VADJ = Float	-0.55	0	0.55	
	CSON = 8.4V, CELLS = FLOAT, VADJ = Float	-0.55	0	0.55	
	CSON = 17.64V, CELLS = VDD, VADJ = VREF	-0.6	0	0.6	
	CSON = 13.23V, CELLS = GND, VADJ = VREF	-0.6	0	0.6	
	CSON = 8.82V, CELLS = FLOAT, VADJ = VREF	-0.6	0	0.6	
	CSON = 15.96V, CELLS = VDD, VADJ = GND	-0.6	0	0.6	
	CSON = 11.97V, CELLS = GND, VADJ = GND	-0.6	0	0.6	
	CSON = 7.98V, CELLS = FLOAT, VADJ = GND	-0.6	0	0.6	
TRIP POINTS					
ACSET Threshold		1.235	1.26	1.285	V
ACSET Input Bias Current Hysteresis		2	3.4	4.8	µA
ACSET Input Bias Current	ACSET $\geq$ 1.26V	2	3.4	4.8	µA
ACSET Input Bias Current	ACSET < 1.26V	-1	0	1	µA
DCSET Threshold		1.235	1.26	1.285	V

Electrical Specifications DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = DCSET = 1.5V, VREF = ACLIM = CHLIM, VADJ = Floating, EN = VDD = 5V, BOOT-PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq$ 125°C, unless otherwise noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DCSET Input Bias Current Hysteresis		2	3.4	4.8	µA
DCSET Input Bias Current	DCSET ≥ 1.26V	2	3.4	4.8	µA
DCSET Input Bias Current	DCSET < 1.26V	-1	0	1	µA
OSCILLATOR					
Frequency		240	300	360	kHz
PWM Ramp Voltage (peak-peak)	CSIP = 18V	1.4	1.55	1.7	V
	CSIP = 11V	0.8	0.9	1.0	V
SYNCHRONOUS BUCK REGULATOR					
Maximum Duty Cycle	300kHz	97	99	99.6	%
UGATE Pull-up Resistance	BOOT-PHASE = 5V, 500mA source current		1.8	3.0	Ω
UGATE Source Current	BOOT-PHASE = 5V, BOOT-UGATE = 2.5V		1.0		A
UGATE Pull-down Resistance	BOOT-PHASE = 5V, 500mA sink current		0.9	1.8	Ω
UGATE Sink Current	BOOT-PHASE = 5V, UGATE-PHASE = 2.5V		1.8		A
LGATE Pull-up Resistance	VDDP-PGND = 5V, 500mA source current		1.8	3.0	Ω
LGATE Source Current	VDDP-PGND = 5V, VDDP-LGATE = 2.5V		1.0		A
LGATE Pull-down Resistance	VDDP-PGND = 5V, 500mA sink current		0.9	1.8	Ω
LGATE Sink Current	VDDP-PGND = 5V, LGATE = 2.5V		1.8		A
CHARGING CURRENT SENSING AMPLIFIER					
Input Common Mode Range		0		18	V
Input Offset Voltage	Guarantee by design	-3	0	3	mV
Input Bias Current at CSOP	0 < CSOP < 18V		10	20	µA
Input Bias Current at CSON	0 < CSON < 18V		300	425	µA
CSOP to CSON Input Full Scale Sense Voltage	CHLIM = 3.3V	123	127	131	mV
	CHLIM = VREF	96	100	104	mV
	CHLIM = FLOAT	61	65	69	mV
	CHLIM = GND	26	30	34	mV
CSOP to CSON Input Full Scale Sense Voltage in Trickle Charge Mode	CHLIM = 3.3V	6	8.9	12.0	mV
	CHLIM = VREF	4.0	7.5	11.0	mV
	CHLIM = FLOAT	2.5	5.6	9.0	mV
	CHLIM = GND	1.5	3.7	7.0	mV
Trickle Charge Threshold Voltage	CSON Rising	3.0	3.1	3.2	V/CELL
	Hysteresis	20	100	180	mV/CELL
CHLIM Input Bias Current	CHLIM = GND or VREF	-25		25	µA
ADAPTER CURRENT SENSING AMPLIFIER					
Input Common Mode Range		7		25	V
Input Offset Voltage	Guarantee by design	-2		2	mV
Input Bias Current at CSIP	0 < CSIP < DCIN		325	475	µA
Input Bias Current at CSIN	0 < CSIN < DCIN		1	10	µA
ADAPTER CURRENT LIMIT THRESHOLD					
CSIP to CSIN Input Full Scale Sense Voltage	ACLIM = VREF	100	103	106	mV
	ACLIM = Float	75	78	81	mV
	ACLIM = GND	50	53	56	mV

Electrical Specifications DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = DCSET = 1.5V, VREF = ACLIM = CHLIM, VADJ = Floating, EN = VDD = 5V, BOOT-PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq$ 125°C, unless otherwise noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACLIM Input Bias Current	ACLIM = GND, or VREF	-25		25	µA
VOLTAGE REGULATION ERROR AMPLIFIER					
Error Amplifier Trans-conductance from CSON to VCOMP	CELLS = VDD	20	30	40	µA/V
VCOMP Voltage Range		0.3		4	V
CURRENT REGULATION ERROR AMPLIFIER					
Charging Current Error Amplifier Trans conductance			50		µA/V
Adapter Current Error Amplifier Trans conductance			50		µA/V
ICOMP Voltage Range		0.3		4	V
BATTERY CELL SELECTOR					
CELLS Input Low Voltage				0.5	V
CELLS Input Float Voltage	CELLS = Float	VREF -0.3	VREF	VREF + 0.3	V
CELLS Input High Current		VDD-0.5			V
MOSFET DRIVER					
BGATE Pull-up Current	CSIP-BGATE = 3V	1	1.4	2	mA
BGATE Pull-down Current	CSIP-BGATE = 5V	3.25	5.0	7	mA
CSIP-BGATE Voltage High		8.0	10	12	V
CSIP-BGATE Voltage Low			0	0.1	V
DCIN-CSON Threshold for CSIP-BGATE Going High	DCIN = 12V, CSON Rising	-200	0	200	mV
DCIN-CSON Threshold for CSIP-BGATE Going Low	DCIN = 12V, CSON Falling	0	300	500	mV
DCIN-CSON Threshold Hysteresis		250	300	400	mV
SGATE Pull-up Current	CSIP-SGATE = 3V	1.0	1.4	2.0	mA
SGATE Pull-down Current	CSIP-SGATE = 2.5V	40	150	350	µA
CSIP-SGATE Voltage High		5	8.5	15	V
CSIP-SGATE Voltage Low			0	0.1	V
CSIP-CSIN Threshold for CSIP-SGATE Going High		3	8.5	15	mV
CSIP-CSIN Threshold Hysteresis		1	2	6	mV
LOGIC INTERFACE					
EN Low Level Input Voltage				0.8	V
EN High Level Input Voltage		2.0			V
ACPRN Sink Current	ACPRN = 0.4V	3	8	13	mA
ACPRN Leakage Current	ACPRN = 20V	-1		1	µA
DCPRN Sink Current	DCPRN = 0.4V	3	8	13	mA
DCPRN Leakage Current	DCPRN = 20V	-1		1	µA
ICM Output Voltage	Iload = 0 to 100µA, CSIP-CSIN = 103mV	1.885	1.980	2.085	V
Thermal Shutdown Temperature	Rising		150		°C
Thermal Shutdown Temperature Hysteresis			20		°C

NOTE:

7. This is sum of currents in these pins (CSIP, CSIN, BOOT, UGATE, PHASE, CSOP and CSON) tied together to 18V. EN, ACSET, DCSET, VADJ, CELLS, ACLIM, CHLIM, VDD, DCIN = 0.

Typical Operating Performance

Circuit of Figure 18, VDCIN = 20V, 4S2P Li-Ion Battery, T_A = 25°C, unless otherwise noted.

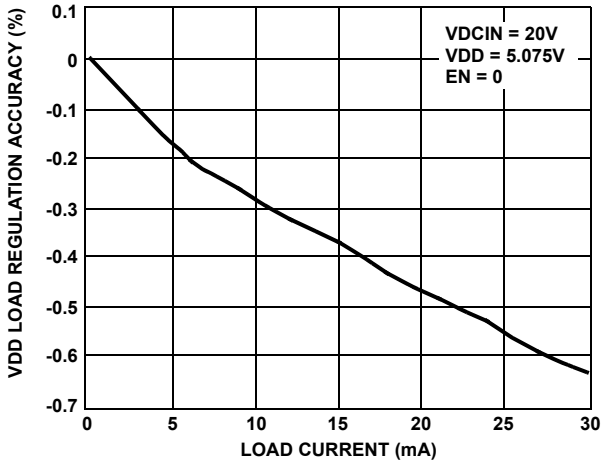


FIGURE 1. VDD LOAD REGULATION

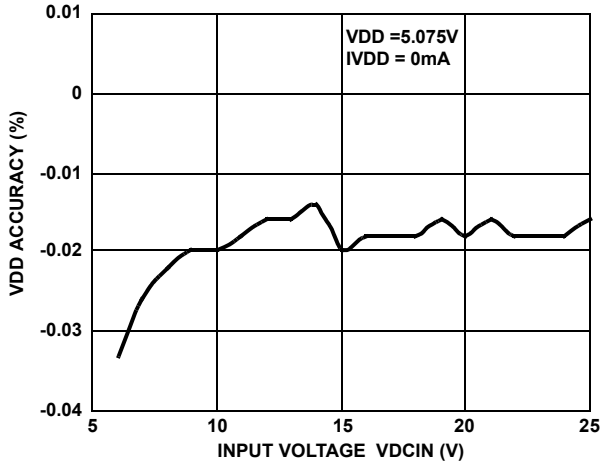


FIGURE 2. VDD LINE REGULATION

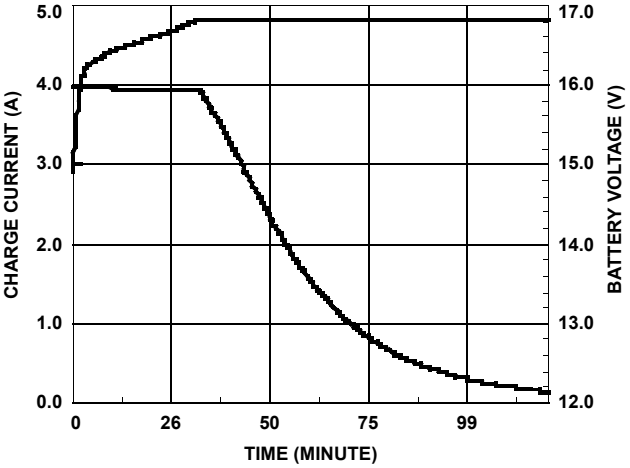


FIGURE 3. BATTERY CHARGE V-I CHARACTERISTICS

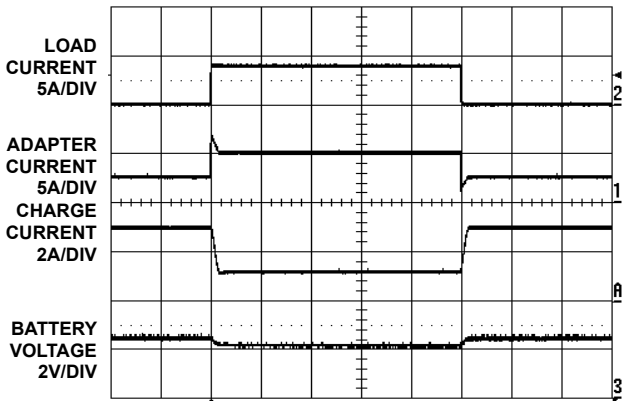


FIGURE 4. LOAD TRANSIENT RESPONSE

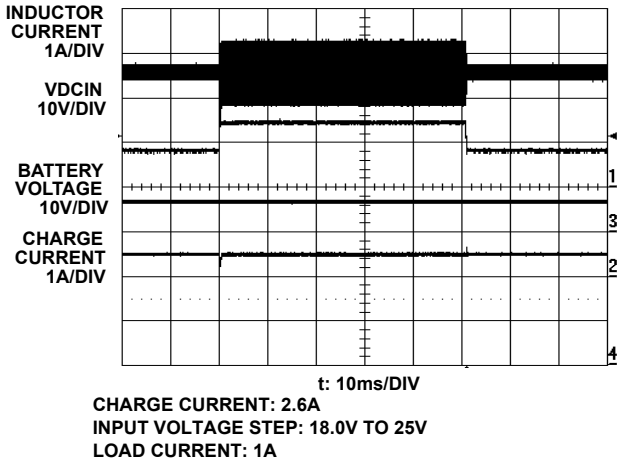


FIGURE 5. LINE TRANSIENT RESPONSE

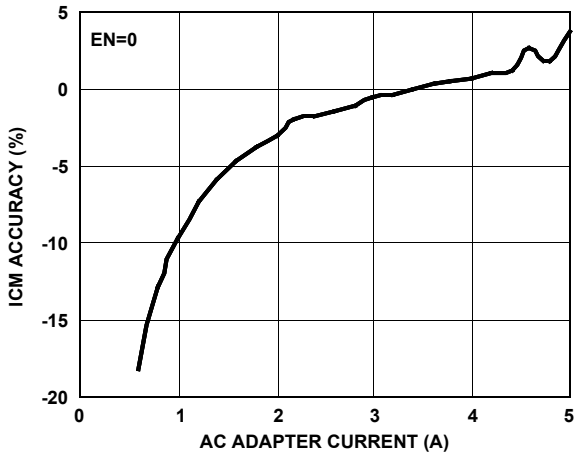


FIGURE 6. ICM ACCURACY vs AC ADAPTER CURRENT

Typical Operating Performance (Continued)

Circuit of Figure 18, VDCIN = 20V, 4S2P Li-Ion Battery, T_A = 25°C, unless otherwise noted.

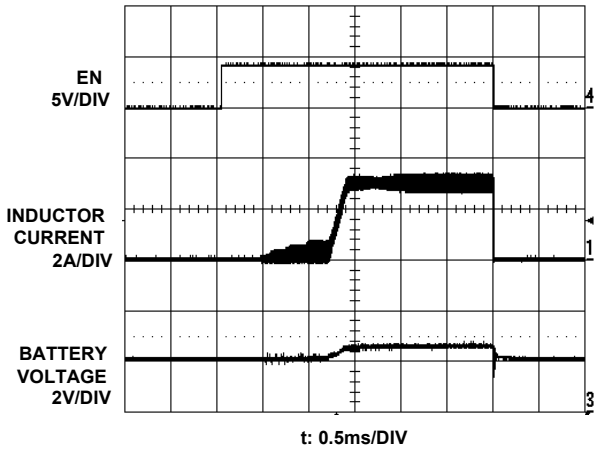


FIGURE 7. CHARGE ENABLE AND SHUTDOWN

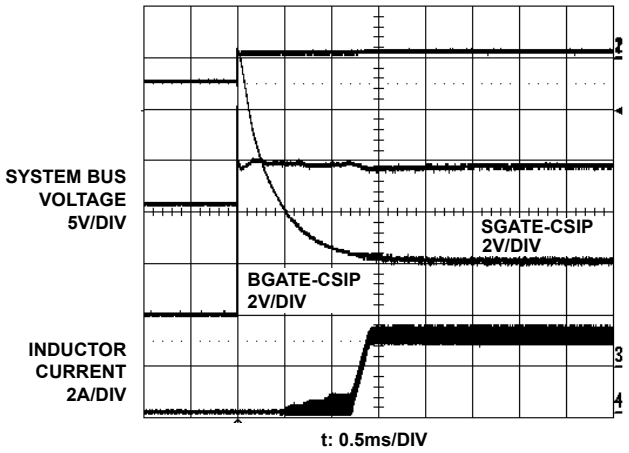


FIGURE 8. AC ADAPTER INSERTION

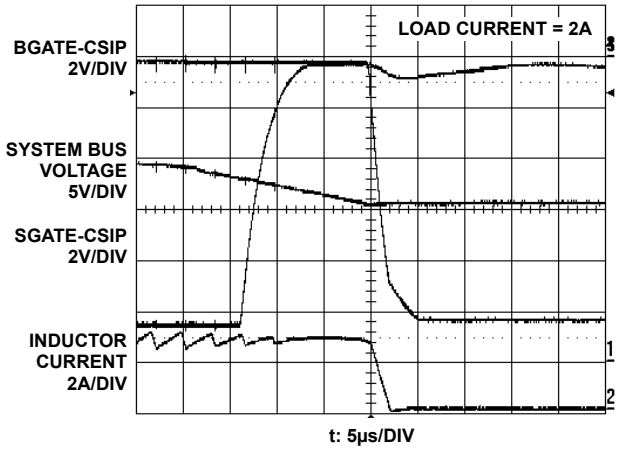


FIGURE 9. AC ADAPTER REMOVAL

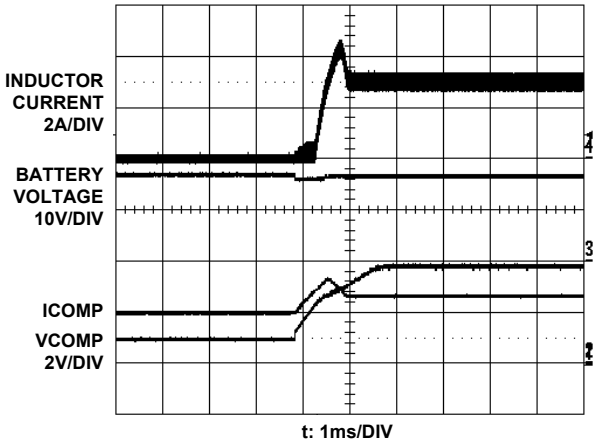


FIGURE 10. BATTERY INSERTION

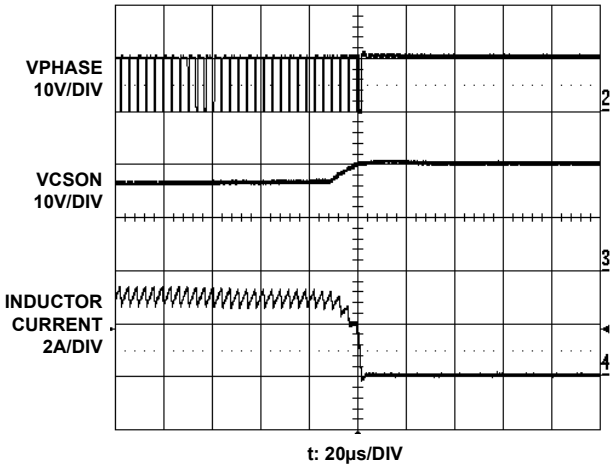


FIGURE 11. BATTERY REMOVAL

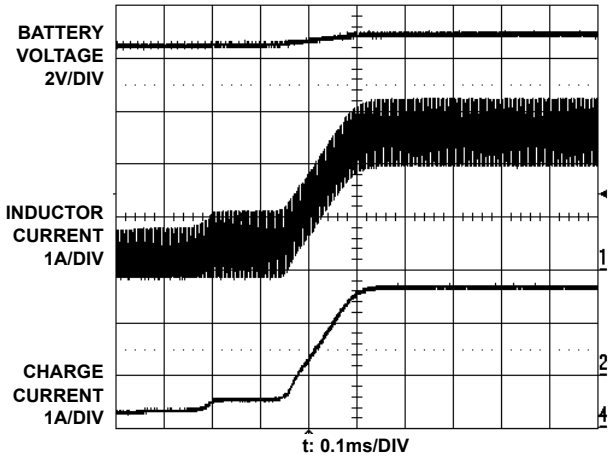


FIGURE 12. CHARGE MODE TRANSITION FROM TRICKLE MODE TO CONSTANT CURRENT MODE

Typical Operating Performance (Continued)

Circuit of Figure 18, VDCIN = 20V, 4S2P Li-Ion Battery, T_A = 25°C, unless otherwise noted.

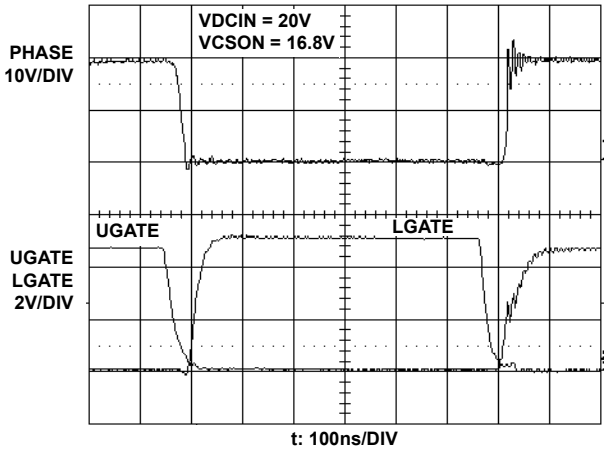


FIGURE 13. SWITCHING WAVEFORMS AT CONSTANT CHARGE CURRENT MODE

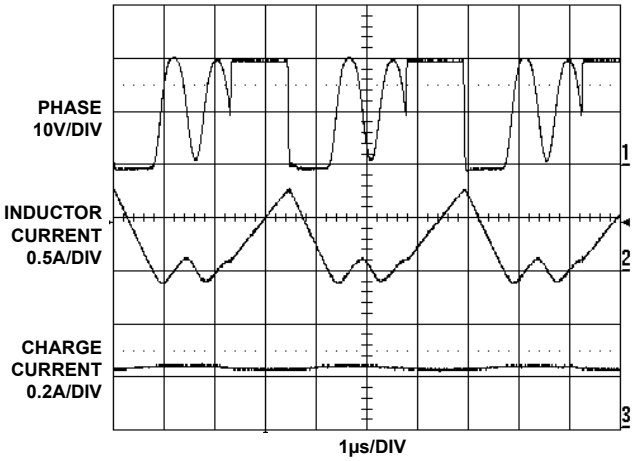


FIGURE 14. SWITCHING WAVEFORMS AT TRICKLE CHARGE MODE

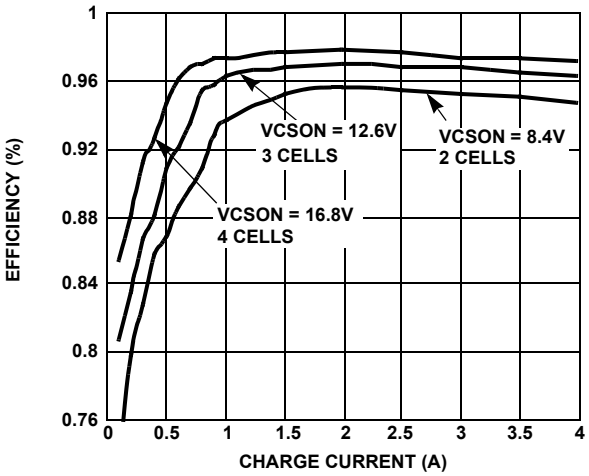


FIGURE 15. EFFICIENCY vs CHARGE CURRENT

Functional Pin Descriptions

BOOT

Connect BOOT to a 0.1µF ceramic capacitor to the PHASE pin and connect to the cathode of the bootstrap Schottky diode.

UGATE

UGATE is the high side MOSFET gate drive output.

SGATE

SGATE is the AC adapter power source select output. The SGATE pin drives an external P-MOSFET used to switch to AC adapter as the system power source.

BGATE

BGATE power source select output. This pin drives an external P-channel MOSFET used to switch the battery as the system power source. When the voltage at the CSON pin is higher than the AC adapter output voltage at DCIN, BGATE is driven to low and selects the battery as the power source.

LGATE

LGATE is the low side MOSFET gate drive output; swing between PGND and VDDP.

PHASE

The Phase connection pin connects to the high side MOSFET source, output inductor, and low side MOSFET drain.

CSOP/CSON

CSOP/CSON are the battery charging current sensing positive/negative inputs. The differential voltage across CSOP and CSON is used to sense the battery charging current, and is compared with the charging current limit threshold to regulate the charging current. The CSON pin is also used as the battery feedback voltage to perform voltage regulation.

CSIP/CSIN

CSIP/CSIN are the AC adapter current sensing positive/negative inputs. The differential voltage across CSIP and CSIN is used to sense the AC adapter current, and is compared with the AC adapter current limit to regulate the AC adapter current.

GND

GND is an analog ground.

DCIN

The DCIN pin is the input of the internal 5V LDO. Connect it to the AC adapter output. Connect DCIN to a 0.1μF ceramic capacitor.

ACSET

ACSET is an AC adapter detection input. Connect a resistor divider to an AC adapter.

ACPRN

ACPRN is an AC adapter present open drain output. ACPRN is active low when ACSET is higher than 1.26V; and active high when ACSET is lower than 1.26V.

DCSET

DCSET is a lower voltage adapter detection input (like aircraft power 15V). This allows power to the system, but power is not used to charge the battery.

DCPRN

DCPRN is a DC adapter present open drain output. DCPRN is active low when DCSET is higher than 1.26V; and active high when DCSET is lower than 1.26V.

EN

EN is the Charge Enable input. Connecting EN to high enables the charge control function, connecting EN to low disables charging functions.

ICM

ICM is the adapter current output. The output of this pin produces a voltage proportional to the adapter current.

PGND

PGND is the power ground. Connect PGND to the source of the low side MOSFET for the low side MOSFET gate driver.

VDD

VDD is an internal LDO output to supply the IC analog circuit. Connect a 1μF ceramic capacitor to ground.

VDDP

VDDP is the supply voltage for the MOSFET gate driver. Connect a 4.7Ω resistor to VDD and a 1μF ceramic capacitor to power ground.

ICOMP

ICOMP is a current loop error amplifier output. Connect a ceramic capacitor to ground.

VCOMP

VCOMP is a voltage loop amplifier output. Connect a ceramic capacitor in series with a resistor to ground.

CELLS

This pin is used to select the battery voltage. CELLS = VDD for a 4S battery, CELLS = GND for a 3S battery pack, and CELLS = Float for a 2S battery pack.

VADJ

VADJ adjusts battery regulation voltage. VADJ = VREF for 4.2V +5%/cell; VADJ = Floating for 4.2V/cell; VADJ = GND for 4.2V -5%/cell. Connect to a resistor divider from VREF to program the desired battery cell voltage between 4.2V -5% and 4.2V +5%.

CHLIM

CHLIM is the battery charge current limit set pin. CHLIM = VREF for 100mV, CHLIM = Floating for 65mV; CHLIM = GND for 30mV. Connect 3.3V for 127mV. Connect a resistor divider to program the charge current limit threshold between 30mV and 127mV.

ACLIM

ACLIM is the adapter current limit set pin. ACLIM = VREF for 103mV, ACLIM = Floating for 78mV, and ACLIM = GND for 53mV. Connect a resistor divider from VREF to program the adapter current limit threshold between 53mV and 103mV.

VREF

VREF is a reference output pin. Do not connect a decoupling capacitor.

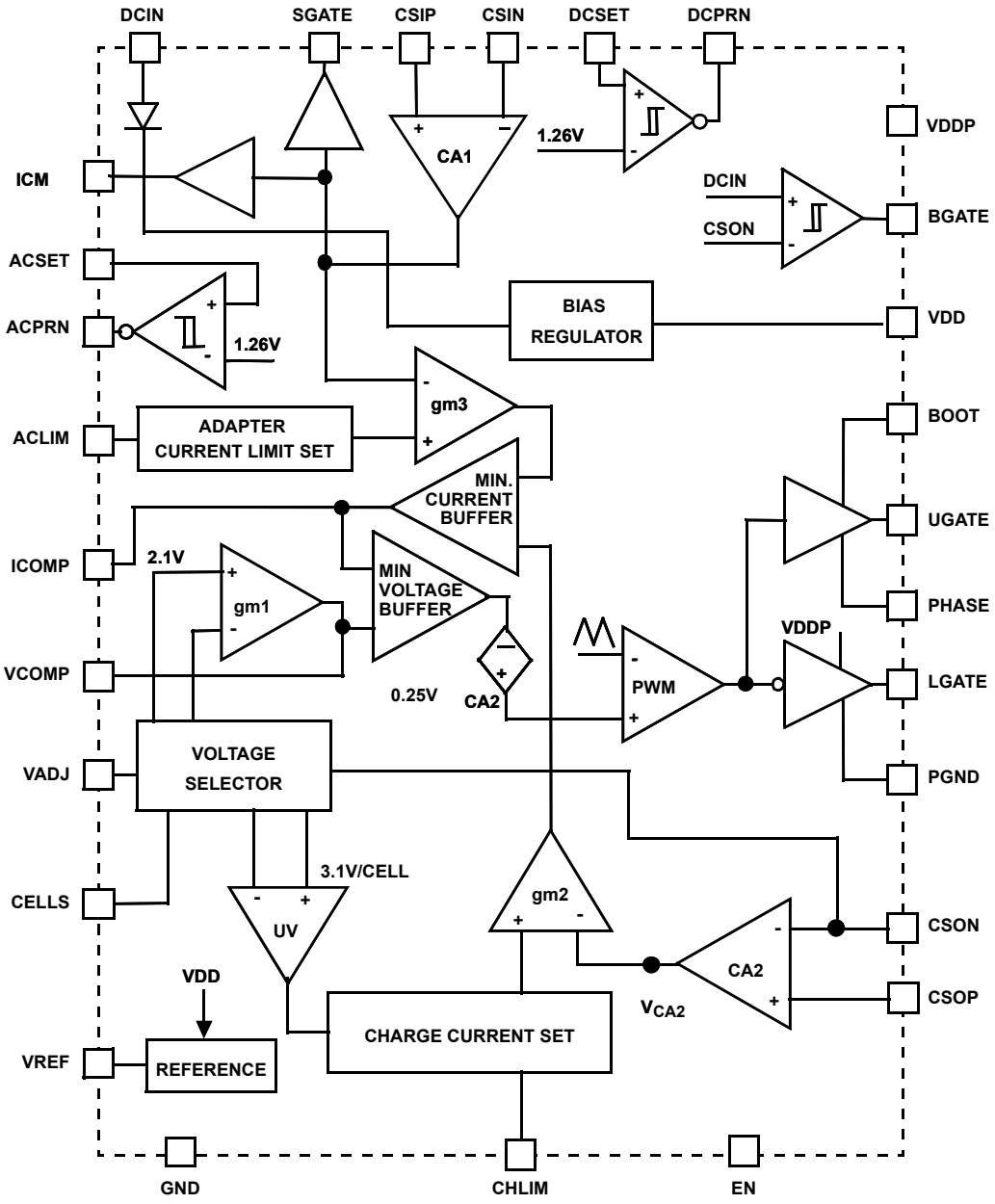


FIGURE 16. BLOCK DIAGRAM

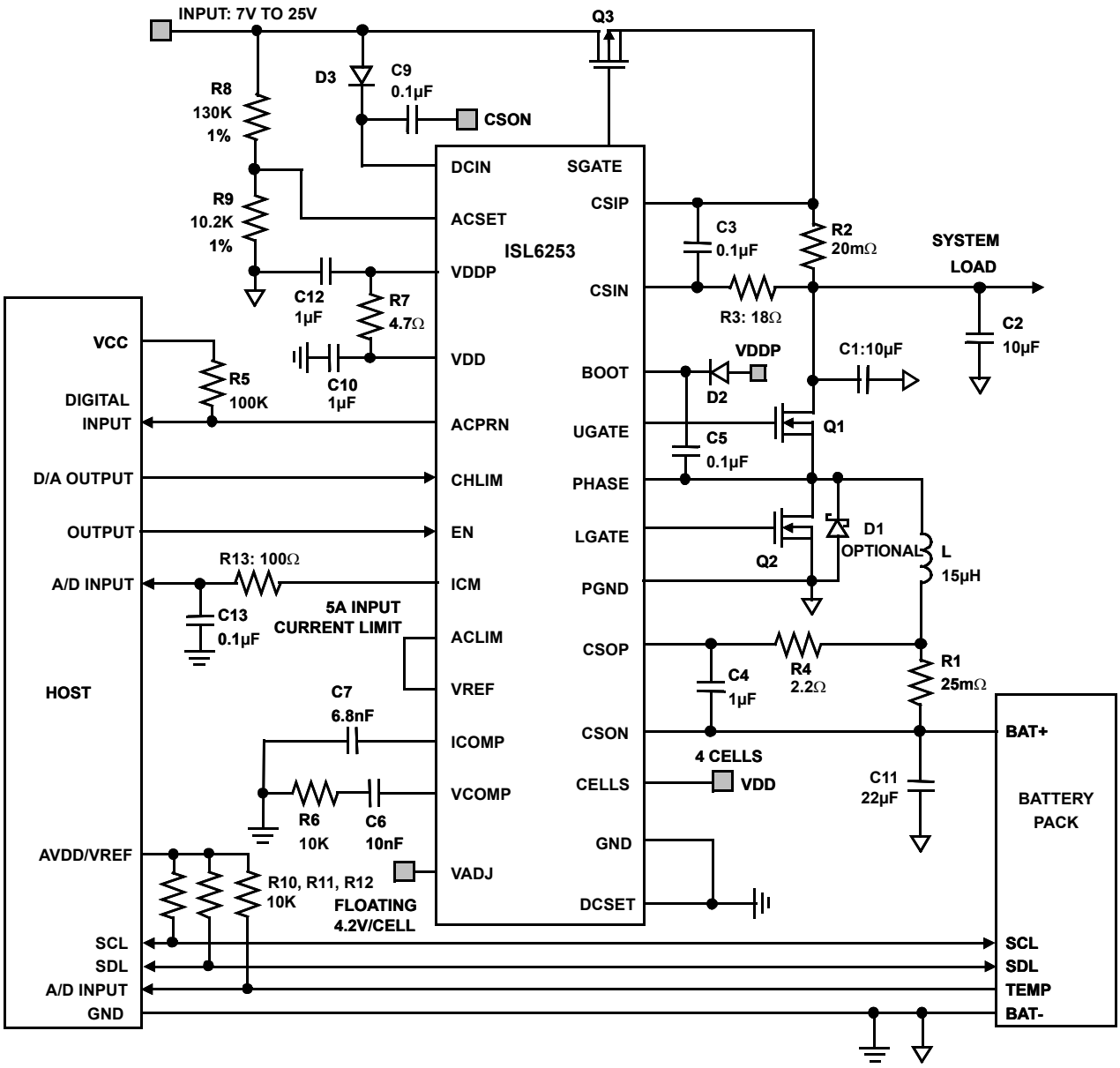


FIGURE 17. TYPICAL APPLICATION CIRCUIT 1

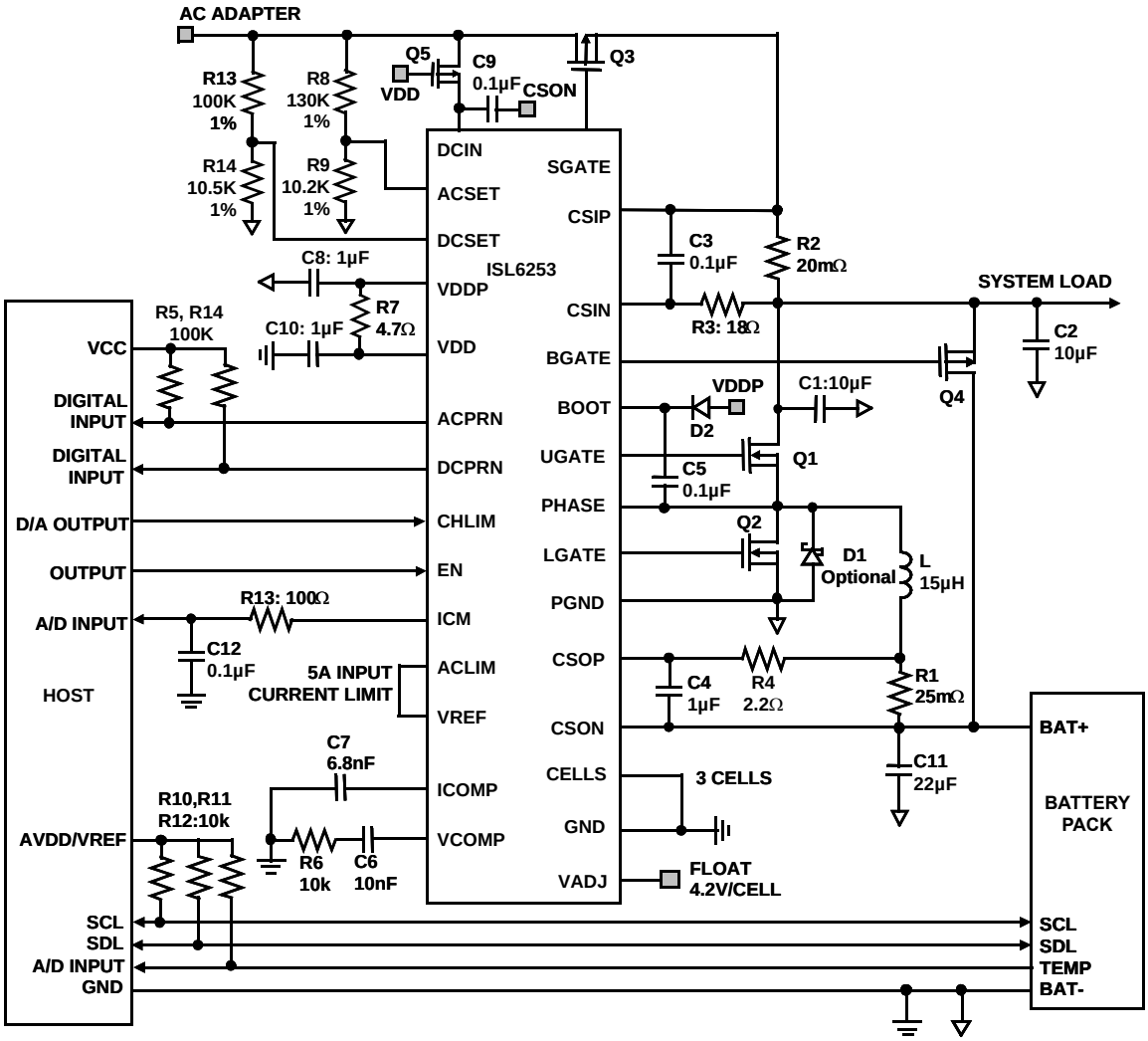


FIGURE 18. ISL6253 CONTROLLED TYPICAL APPLICATION 2

Theory of Operation

Introduction

The ISL6253 includes all of the functions necessary to charge 2 to 4 cell Li-Ion and Li-polymer batteries. A high efficiency synchronous buck converter is used to control the charging voltage and charging current up to 10 amps. The ISL6253 has input current limiting and analog inputs for setting the charge current and charge voltage; CHLIM inputs are used to control charge current and VADJ inputs are used to control charge voltage.

The ISL6253 safely conditions over-discharged battery cells with a percentage of full charge current until the battery voltage exceeds 3.1V × number of series connected cells. When the battery voltage exceeds 3.1V × number of series connected cells, the ISL6253 charges the battery with constant charge current, set by CHLIM input, until the battery voltage rises to a programmed charge voltage set by VADJ input; then the charger begins to operate at constant voltage charge mode. The charger drives an adapter isolation p-channel MOSFET to efficiently switch in the adapter supply.

ISL6253 is a complete power source selection controller for single battery systems and also aircraft power applications. ISL6253 drives a battery selector p-channel MOSFET to efficiently select between a single battery and the adapter. It controls the battery discharging MOSFET and switches to the battery when the AC adapter is removed, or, switches to the AC adapter when the AC adapter is inserted for a single battery system. The EN input allows shutdown of the charger from a micro-controller. The amount of adapter current is reported on the ICM output. Figure 16 shows the IC functional block diagram.

The synchronous buck converter uses external N-channel MOSFETs to convert the input voltage to the required charging current and charging voltage. Figure 17 shows the ISL6253 typical application circuit 1 without power source selection function. The typical application circuit 2 shown in Figure 18 has automatic power source selection functionality and supports aircraft power applications. The voltage at CHLIM and the value of R1 sets the charging current. The DC-DC converter generates the control signals to drive two external N-channel MOSFETs to regulate the voltage and current set by the ACLIM, CHLIM, VADJ and CELLS inputs.

The ISL6253 features a voltage regulation loop (VCOMP) and two current regulation loops (ICOMP). The VCOMP voltage regulation loop monitors CSON to ensure that its voltage never exceeds the voltage set by VADJ. The ICOMP current regulation loops regulate the battery charging current delivered to the battery to ensure that it never exceeds the charging current limit set by CHLIM; and the ICOMP current regulation loops regulate the input current drawn from the AC adapter to ensure that it never exceeds the input current limit set by ACLIM, and to prevent a system crash and AC adapter overload.

PWM Control

The ISL6253 employs a fixed frequency PWM current mode control architecture with a feed forward function. The feed-forward function maintains a constant modulator gain of 11 to achieve fast line regulation as the buck input voltage changes. When the battery charge voltage approaches the input voltage, the DC-DC converter operates in dropout mode, where there is a timer to prevent the frequency from dropping into the audible frequency range. It can achieve a maximum duty cycle of up to 99.6%.

An adaptive gate drive scheme is used to control the dead time between two switches. The dead time control circuit monitors the LGATE output and prevents the upper side MOSFET from turning on until LGATE is fully off, preventing cross-conduction and shoot-through. In order for the dead time circuit to work properly, there must be a low resistance, low inductance path from the LGATE driver to MOSFET gate, and from the source of MOSFET to PGND. The external Schottky diode is between the VDDP pin and BOOT pin to keep the bootstrap capacitor charged.

The PWM controller is disabled when EN = GND, but the rest of the circuitry, including the AC or DC adapter detecting circuit and AC adapter current monitoring circuits, is still alive.

Setting the Battery Regulation Voltage

The ISL6253 uses a high-accuracy trimmed band-gap voltage reference to regulate the battery charging voltage. The VADJ input adjusts the charger output voltage, and the VADJ control voltage can vary from 0 to VREF (2.39V), providing a 10% adjustment range (from 4.2V -5% to 4.2V +5%) on CSON regulation voltage. An overall voltage accuracy of better than 0.5% is achieved.

The per-cell battery termination voltage is a function of the battery chemistry. Consult the battery manufacturers to determine this voltage.

Float VADJ to set the battery voltage V_{CSON} = 4.2V × number of the cells,

- Connect VADJ to VREF to set 4.41V × number of cells,
- Connect VADJ to ground to set 3.99V × number of cells.

Note that other battery charge voltages can be set by connecting a resistor divider from VREF to ground. The resistor divider should be sized to draw no more than 100µA from VREF; or connect a low impedance voltage source like the D/A converter in the micro-controller. The programmed battery voltage per cell can be determined by the following equation:

$$V_{CELL} = 0.175V_{VADJ} + 3.99V \quad \text{(EQ. 1)}$$

Connect CELLS as shown in Table 1 to charge 2, 3, or 4 Li+ cells. When charging other cell chemistries, use CELLS to select an output voltage range for the charger. The internal error amplifier gm1 maintains voltage regulation. The voltage error amplifier is compensated at VCOMP. The component values shown in Figure 18 provide suitable performance for most applications. Individual compensation of the voltage regulation and current-regulation loops allows for optimal compensation.

TABLE 1. CELL NUMBER PROGRAMMING

CELLS	CELL NUMBER
VCC	4
GND	3
Float	2

Setting the Battery Charge Current Limit

The CHLIM input sets the maximum charging current. The current set by the current sense-resistor connects between CSOP and CSON. There are three default battery charge current-sense threshold voltages: 127mV for CHLIM = 3.3V, 100mV for CHLIM = VREF, 65mV for Float, and 30mV for ground. The full-scale differential voltage between CSOP and CSON is 100mV for CHLIM = VREF, so the maximum charging current is 4.0A for a 25mΩ sensing resistor. Other battery charge current-sense threshold values can be set by connecting a resistor divider from VREF or VDD to ground, or by connecting a low impedance voltage source like a D/A converter in the microcontroller. The charge current limit threshold is given by:

$$I_{CHG} = \frac{1}{R_1}\left(\frac{0.07}{VREF}V_{CHLIM} + 0.03\right) \quad \text{(EQ. 2)}$$

If the battery voltage is less than 3.0V/cell and the battery charging voltage is a percentage of the charging current in constant current charge mode, the trickle charge current limit threshold is given by:

$$I_{TR,CHG} = \frac{1}{R_1}(0.00157 \times V_{CHLIM} + 0.0037) \quad \text{(EQ. 3)}$$

When choosing the current sensing resistor, note that the voltage drop across the sensing resistor causes further power dissipation, reducing efficiency. However, adjusting CHLIM voltage to reduce the voltage across the current sense resistor R1 will degrade accuracy due to the smaller signal to the input of the current sense amplifier. There is a trade-off between accuracy and power dissipation. A low pass filter is recommended to eliminate switching noise. Connect the resistor to the CSOP pin instead of the CSON pin, as the CSOP pin has lower bias current and less influence on current-sense accuracy.

Setting the Input Current Limit

The total input current from an AC adapter, or other DC source, is a function of the system supply current and the battery-charging current. The input current regulator limits the input current by reducing the charging current, when the input current exceeds the input current–limit set point. System current normally fluctuates as portions of the system are powered up or down. Without input current regulation, the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using the input current limiter, the current capability of the AC adapter can be lowered, reducing system cost.

The ISL6253 limits the battery charge current when the input current-limit threshold is exceeded, ensuring the battery charger does not load down the AC adapter voltage. An internal amplifier gm3 compares the voltage between CSIP and CSIN to the input current limit threshold voltage set by ACLIM. Connect ACLIM to REF, Float and GND for the full-scale input current limit threshold voltage of 103mV, 78mV, and 53mV, respectively, or use a resistor divider from VREF to ground to set the input current limit as the following equation:

$$I_{INPUT} = \frac{1}{R_2}\left(\frac{0.05}{VREF}V_{ACLIM} + 0.053\right) \quad \text{(EQ. 4)}$$

When choosing the current sense resistor, note that the voltage drop across this resistor causes further power dissipation, reducing efficiency. The AC adapter current sense accuracy is very important. Use a 1% tolerance current-sense resistor. The highest accuracy of ± 3% is achieved with 103mV current-sense threshold voltage for ACLIM = VREF, but it has the highest power dissipation. For example, it has 400mW power dissipation for rated 4A AC adapter, and a 1W sensing resistor may have to be used. ± 4% and ± 6% accuracy can be achieved with 78mV and 53mV current-sense threshold voltage for ACLIM = Floating and ACLIM = GND, respectively.

A low pass filter is recommended to eliminate the switching noise. Connect the resistor to the CSIN pin instead of the CSIP pin because the CSIN pin has lower bias current and less influence on the current-sense accuracy.

AC Adapter Detection

Connect the AC adapter voltage through a resistor divider to ACSET to detect when AC power is available, as shown in Figure 17. ACPRN is an open-drain output and is high impedance when ACSET is less than $V_{th,rise}$ and active low impedance when ACSET is above $V_{th,fall}$. $V_{th,rise}$ and $V_{th,fall}$ are given by:

$$V_{th,\,rise} = \left(\frac{R_8}{R_9} + 1\right) \bullet V_{ACSET} \quad \text{(EQ. 5)}$$

$$V_{th,\,fall} = \left(\frac{R_8}{R_9} + 1\right) \bullet V_{ACSET} - I_{hys}R_8$$

Where I_{hys} is the ACSET input bias current hysteresis and V_{ACSET} = 1.235V (min), 1.26V (typ.) and 1.285V (max.). The hysteresis is I_{hys} R_8, where I_{hys} = 2µA (min.), 3.4µA (typ.) and 4.8µA (max.)

DC Adapter Detection

Connect the DC adapter voltage like aircraft power through a resistor divider to DCSET to detect when DC power is available, as shown in Figure 18. DCPRN is an open-drain output and is high impedance when DCSET is less than $V_{th,rise}$, and active low impedance when DCSET is above $V_{th,fall}$. $V_{th,rise}$ and $V_{th,fall}$ are given by:

$$V_{th,rise} = \left(\frac{R_{13}}{R_{14}} + 1\right) \bullet V_{DCSET} \quad \text{(EQ. 6)}$$

$$V_{th,fall} = \left(\frac{R_{13}}{R_{14}} + 1\right) \bullet V_{DCSET} - I_{hys}R_{13}$$

Where I_{hys} is the DCSET input bias current hysteresis and V_{ACSET} = 1.235V (min), 1.26V (typ.) and 1.285V (max.). The hysteresis is $I_{hys}R_{13}$, where I_{hys} = 2µA (min.), 3.4µA (typ.) and 4.8µA (max.)

Current Measurement

Use ICM to monitor the input current being sensed across CSIP and CSIN. The output voltage range is 0 to 2.5V. The voltage of ICM is proportional to the voltage drop across CSIP and CSIN, and is given by the following equation:

$$ICM = 19.22 \bullet I_{INPUT} \bullet R_2 \quad \text{(EQ. 7)}$$

where I_{INPUT} is the DC current drawn from the AC adapter. ICM has ±5% accuracy. Connect a low pass filter to ICM to bypass the switching frequency noise.

LDO Regulator

VDD provides a 5.0V supply voltage from the internal LDO regulator from DCIN and can deliver up to 30mA of current. This 30mA current is only used to supply the analog and logic circuits for the IC and power the gate drivers. The MOSFET drivers are powered by VDDP, and VDDP connects to VDD through an external low pass filter. Bypass VDDP and VDD with a 1µF capacitor.

Supply Isolation

If the voltage across the adapter sense resistor R2 is typically greater than 8.5mV, the p-channel MOSFET controlled by SGATE is turned on reducing the power dissipation. If the voltage across the adapter sense resistor R2 is less than 2mV, SGATE turns off the p-channel MOSFET isolating the adapter from the system bus.

Battery Power Source Selection and Aircraft Power Application

The battery voltage is monitored by CSON. If the battery voltage measured on CSON is less than the adapter voltage measured on DCIN, then the p-channel MOSFET controlled by BGATE turns off. If it is greater, then BGATE turns on the battery discharge p-channel MOSFET to minimize the power loss. In the meantime, it also disables charging function and turns off the AC adapter isolation p-channel MOSFET controlled by SGATE. If designing for airplane power, DCSET is tied to a resistor divider sensing the adapter voltage. When a user is plugged into the 15V airplane supply and their battery is lower than 15V, the MOSFET driven by BGATE (see Figure 18) is turned off and keeps the battery from supplying the system bus. The comparator looking at CSON and DCIN has 300mV of hysteresis to avoid chattering. For aircraft power applications the ISL6253 is only able to support 2S and 3S battery packs when disabling the charging function based on DCPRN and ACPRN signals. For 4S battery packs, DCSET = 0 and the DCPRN signal is not available to support aircraft power applications.

Short Circuit Protection and 0V Battery Charging

Since the battery charger will regulate the charge current to be trickle charge current, as long as the battery voltage is below 3.0V/cell, it automatically has short circuit protection and is able to provide the trickle charge current and “wake-up” an extremely discharged battery.

Over Temperature Protection

If the die temp exceeds 150°C, it stops charging. Once the die temp drops below 130°C, charging will start up again.

Application Information

The following battery charger design refers to the typical application circuit in Figure 17, where a typical battery configuration of 4S2P is used. This section describes how to select the external components including the inductor, input and output capacitors, switching MOSFETs, and current sensing resistors.

Inductor Selection

The inductor selection has trade-offs between cost, size and efficiency. For example, the lower the inductance, the smaller the size, but ripple current is higher. This also results in higher ac losses in the magnetic core and the windings, which decrease the system efficiency. On the other hand, the higher inductance results in lower ripple current and smaller output filter capacitors, but it has higher DCR (dc resistance of the inductor) loss, and has slower transient response. So, the practical inductor design is based on the inductor ripple current being ±(15-20)% of the maximum operating dc current at maximum input voltage. The required inductance can be calculated from:

$$L = \frac{V_{IN,MAX} - V_{BAT}}{\Delta I_L} \frac{V_{BAT}}{V_{IN,MAX} f_s} \quad \text{(EQ. 8)}$$

where $V_{IN,MAX}$, V_{BAT}, and f_s are the maximum input voltage, battery voltage and switching frequency, respectively. The inductor ripple current ΔI_L is found from:

$$\Delta I_L = 30\% \cdot I_{BAT,MAX} \quad \text{(EQ. 9)}$$

where the maximum peak-to-peak ripple current is 30% of the maximum charge current used.

For $V_{IN,MAX}$ = 20V, V_{BAT} = 16.8V, $I_{BAT,MAX}$ = 4A, and f_s = 300kHz, the calculated inductance is 12.8µH. Choosing the closest standard value gives L = 15µH. Ferrite cores are often the best choice since they are optimized at 300kHz to 600kHz operation with low core loss. The core must be large enough not to saturate at the peak inductor current I_{Peak}:

$$I_{Peak} = I_{BAT,MAX} + \frac{1}{2}\Delta I_L \quad \text{(EQ. 10)}$$

Output Capacitor Selection

The output capacitor in parallel with the battery is used to absorb the high frequency switching ripple current and smooth the output voltage. The RMS value of the output ripple current I_{rms} is given by:

$$I_{RMS} = \frac{V_{IN,MAX}}{\sqrt{12}\, L f_s} D(1-D) \quad \text{(EQ. 11)}$$

where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for continuous conduction mode, which is typical operation for a battery charger. During the battery charge period, the output voltage varies from its initial battery voltage to the rated battery voltage; therefore, the duty cycle change can be in the range of between 0.375 and 0.63 for the minimum battery voltage of 7.5V (2.5V/Cell) and the maximum battery voltage of 12.8V. The maximum RMS value of the output ripple current occurs at the duty cycle of 0.5 and is expressed as:

$$I_{RMS} = \frac{V_{IN,MAX}}{4\sqrt{12}\, L f_s} \quad \text{(EQ. 12)}$$

For $V_{IN,MAX}$ = 20V, L = 15µH, and f_s = 300kHz, the maximum RMS current is 0.32A. A typical 10µF or 22µF ceramic capacitor is a good choice to absorb this current, and also has very small size. The tantalum capacitor has a known failure mechanism when subjected to high surge current.

EMI considerations usually make it desirable to minimize ripple current in the battery leads. Beads may be added in series with the battery pack to increase the battery impedance at 300kHz switching frequency. Switching ripple current splits itself between the battery and the output capacitor, depending on the ESR of the output capacitor and the battery impedance. If the ESR of the output capacitor is 20mΩ and the battery impedance is raised to 2Ω with a bead, then only 1% of the ripple current will flow in the battery.

MOSFET Selection

The notebook battery charger synchronous buck converter has input voltage from the AC adapter output. The maximum AC adapter output voltage does not exceed 25V; therefore, a 30V logic MOSFET should be used.

The high side MOSFET must be able to dissipate the conduction losses plus the switching losses. For the battery charger application, the input voltage of the synchronous buck converter is equal to the AC adapter output voltage, which is relatively constant. The maximum efficiency is achieved by selecting a high side MOSFET that has the conduction losses equal to the switching losses. Ensure that the ISL6253 LGATE gate driver can supply sufficient gate current to prevent it from conduction, which is due to the injected current into the drain-to-source parasitic capacitor (Miller capacitor C_{gd}), and caused by the voltage rising rate at the phase node at the moment of the high-side MOSFET turning on; otherwise, cross-conduction problems may occur. Reasonably slowing the turn-on speed of the high-side MOSFET, by connecting a resistor between the BOOT pin and gate drive supply source, and the high sink current capability of the low-side MOSFET gate driver, helps reduce the possibility of cross-conduction.

For the high-side MOSFET, the worst-case conduction losses occur at the minimum input voltage:

$$P_{Q1,Conduction} = \frac{V_{OUT}}{V_{IN}} I_{BAT}^2 R_{DSON} \quad \text{(EQ. 13)}$$

The optimum efficiency occurs when the switching losses equal the conduction losses. However, it is difficult to calculate the switching losses in the high-side MOSFET since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include: the MOSFET internal gate resistance, gate charge, threshold voltage, stray inductance, and pull-up and pull-down resistance of the gate driver. The following switching loss calculation provides a rough estimate:

$$P_{Q1,Switching} = \frac{1}{2} V_{IN} I_{LV} f_s \frac{Q_{gd}}{I_{g,source}} + \frac{1}{2} V_{IN} I_{LP} f_s \frac{Q_{gd}}{I_{g,sink}} + Q_{rr} V_{IN} f_s \quad \text{(EQ. 14)}$$

where Q_{gd} is drain-to-gate charge; Q_{rr} is total reverse recovery charge of the body-diode in low side MOSFET; I_{LV} is inductor valley current; I_{LP} is Inductor peak current; and $I_{g,sink}$ and $I_{g,source}$ are the peak gate-drive source/sink current of Q1, respectively.

Achievement of low switching losses requires low drain-to-gate charge, Q_{gd}. Generally, the lower the drain-to-gate charge, the higher the on-resistance; therefore, there is a trade-off between the on-resistance and drain-to-gate charge. Good MOSFET selection is based on the Figure of Merit (FOM), which is the product of the total gate charge and on-resistance. Usually, the smaller the value of FOM, the higher the efficiency for the same application.

For the low-side MOSFET, the worst-case power dissipation occurs at minimum battery voltage and maximum input voltage:

$$P_{Q2} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) I_{BAT}^2 R_{DSON} \quad \text{(EQ. 15)}$$

Choose a low-side MOSFET that has the lowest possible on-resistance, has a moderate-sized package like SO-8 and is reasonably priced. The switching losses are not an issue for the low side MOSFET because it operates at zero-voltage-switching.

Choose a Schottky diode in parallel with low-side MOSFET Q2 with a forward voltage drop low enough to prevent the low-side MOSFET Q2 body-diode from turning on during the dead time. This also reduces the power loss in the high-side MOSFET associated with the reverse recovery of the low-side MOSFET Q2 body diode.

As a general rule, select a diode with a DC current rating equal to one-third of the load current. One option is to choose a combined MOSFET and Schottky diode in a single package. The integrated packages may work better in practice because there is less stray inductance due to a short connection. This Schottky diode is optional and may be removed if efficiency loss can be tolerated. In addition, ensure that the required total gate drive current for the selected MOSFETs is less than 26mA. The total gate charge for the high-side and low-side MOSFETs is limited by the following equation:

$$Q_{GATE} \leq \frac{I_{GATE}}{f_s} \quad \text{(EQ. 16)}$$

where I_{GATE} is the total gate drive current and should be less than 26mA. Substituting I_{GATE} = 26mA and f_s = 300kHz into the above equation yields a total gate charge which should be less than 86nC; therefore, the ISL6253 easily drives the battery charge current up to 10A.

Input Capacitor Selection

The input capacitor absorbs the ripple current from the synchronous buck converter, which is given by:

$$I_{rms} = I_{BAT}\sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}} \quad \text{(EQ. 17)}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor data sheet. Non-tantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents when the AC adapter is plugged into the battery charger. For Notebook battery charger applications, a ceramic capacitor or a polymer capacitor from Sanyo is recommended due to its small size and reasonable cost.

Table 2 shows the component lists for the typical application circuit in Figure 18.

TABLE 2. COMPONENT LIST

PARTS	PART NUMBERS AND MANUFACTURER
C1, C2	10µF/25V ceramic capacitor, TDK, C4532X7R1E106M
C3, C5, C9, C12	0.1µF/50V ceramic capacitor
C4, C8, C10	1µF/10V ceramic capacitor, Taiyo Yuden LMK212BJ105MG
C6	10nF ceramic capacitor
C7	6.8nF ceramic capacitor
C11	10µF or 22µF/25V/10mΩ ceramic capacitor TDK, C5750X7R1E226M
D1	30V/3A Schottky Diode, EC31QS03L, Nihon (optional)
D2, D3	100mA/30V Schottky Diode, Central Semiconductor
L	15µH/4.5A/20mΩ, Sumida, CDRH127-150
Q1	30V/14mΩ, IRF7811AV, International Rectifier
Q2	30V/30mΩ, FDS6612A, Fairchild
Q3	-30V/9.5mΩ, Si4413DY, Siliconix
R1	25mΩ, ±1%, LRC-LR2010-01-R025-F, IRC
R2	20mΩ, ±1%, LRC-LR2010-01-R020-F, IRC
R3	18Ω, ±5%, (0805)
R4	2.2Ω, ±5%, (0805)
R5	100kΩ, ±5%, (0805)
R6	10k, ±5%, (0805)
R7	4.7Ω, ±5%, (0805)
R8	130kΩ, ±1%, (0805)
R9	10.2kΩ, ±1%, (0805)
R10, R11, R12	10kΩ, ±5%, (0805)
R13	100Ω, ±5%, (0805)
R14	100kΩ, ±5%, (0805)

Loop Compensation Design

ISL6253 uses constant frequency current mode control architecture to achieve fast loop transient response. Accurate current sensing resistors in series with the output inductor is used to regulate the charge current, and the sensed current signal is injected into the voltage loop to achieve current mode control to simplify the loop compensation design. The inductor is not considered as a state variable for current mode control, and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the voltage loop than voltage mode control.

Figure 19 shows the small signal model of the synchronous buck regulator.

PWM Comparator Gain F_m

The PWM comparator gain Fm for peak current mode control is given by:

$$F_m = \frac{\hat{d}}{\hat{v}_{comp}} = \frac{1}{V_{PWM}} \quad \text{(EQ. 18)}$$

where V_{PWM} is the peak-peak voltage of the PWM ramp signal.

Current Sampling Transfer Function $H_e(S)$

In current loop, the current signal is sampled every switching cycle. It has the following transfer function:

$$H_e(S) = \frac{S^2}{\omega_n^2} + \frac{S}{\omega_n Q_n} + 1 \quad \text{(EQ. 19)}$$

where Q_n and ω_n are given by $Q_n = \frac{2}{\pi}, \omega_n = \pi f_s$, respectively.

Power Stage Transfer Functions

Transfer function $F_1(S)$ from control to output voltage is:

$$F_1(S) = \frac{\hat{v}_o}{\hat{d}} = V_{in}\frac{1 + \frac{S}{\omega_{esr}}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \quad \text{(EQ. 20)}$$

Where $\omega_{esr} = \frac{1}{R_c C_o}, Q_p \approx R_o\sqrt{\frac{C_o}{L}}, \omega_o = \frac{1}{\sqrt{LC_o}}$

Transfer function $F_2(S)$ from control to inductor current is,

$$F_2(S) = \frac{\hat{i}_o}{\hat{d}} = \frac{V_{in}}{R_o + R_L}\frac{1 + \frac{S}{\omega_z}}{\frac{S^2}{\omega_o^2} + \frac{S}{\omega_o Q_p} + 1} \text{ where } \omega_z \approx \frac{1}{R_o C_o} \quad \text{(EQ. 21)}$$

Current loop gain $T_i(S)$ is expressed as the following equation:

$$T_i(S) = R_T F_m F_2(S) H_e(S) \quad \text{(EQ. 22)}$$

where R_T is the trans-resistance in current loop. R_T is usually equal to the product of the current sensing resistance of the current amplifier. For ISL6253, $R_T = 24R_1$.

The voltage gain with open current loop is:

$$T_v(S) = KF_m F_1(S) A_v(S) \quad \text{(EQ. 23)}$$

where $K = \frac{V_{FB}}{V_o}$, V_{FB} is the feedback voltage of the voltage error amplifier.

The Voltage loop gain with current loop closed is given by:

$$L_v(S) = \frac{T_v(S)}{1 + T_i(S)} \quad \text{(EQ. 24)}$$

If $T_i(S)$>>1, then the above equation can be simplified as follows:

$$L_v(S) = \frac{V_{FB}}{V_o}\frac{R_o + R_L}{R_{TV}}\frac{1 + \frac{S}{\omega_{esr}}}{1 + \frac{S}{\omega_p}}A_v(S), \quad \omega_p \approx \frac{1}{R_o C_o} \quad \text{(EQ. 25)}$$

Where RTV is the trans-resistance due to the current information fed into the voltage loop. From the above equation, it is shown that the system is a single order system, which has a single pole located at ω_p before the half switching frequency. Therefore, a simple type II compensator can be easily used to stabilize the system.

Figure 20 shows the type II compensator, and its transfer function is expressed as follows:

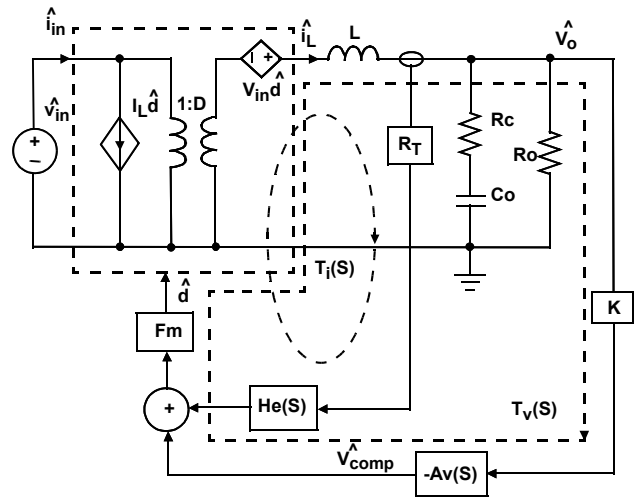


FIGURE 19. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

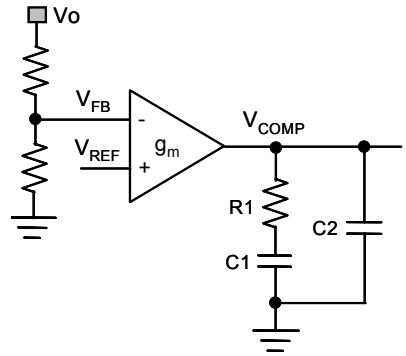


FIGURE 20. TYPE II COMPENSATOR

Figure 20 shows the type II compensator and its transfer function is expressed as follows:

$$A_v(S) = \frac{\hat{v}_{comp}}{\hat{v}_{FB}} = \frac{g_m}{C_1 + C_2} \frac{1 + \frac{S}{\omega_{cz}}}{S\left(1 + \frac{S}{\omega_{cp}}\right)} \quad \text{(EQ. 26)}$$

where $\omega_{cz} = \frac{1}{R_1 C_1}$, $\omega_{cp} = \frac{C_1 + C_2}{R_1 C_1 C_2}$

Compensator design goal:

- High DC gain
- Loop bandwidth f_c: $\left(\frac{1}{5} - \frac{1}{30}\right) f_s$
- Gain margin: >10dB
- Phase margin: 40°

The compensator design procedure is as follows:

1. Put compensator zero at $\omega_{cz} = (1 - 3)\frac{1}{R_o C_o}$
2. Put one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either esr zero frequency or half switching frequency, whichever is lower.

The loop gain $T_v(S)$ at cross over frequency of f_c has unity gain. Therefore, the compensator resistance R_1 is determined by:

$$R_1 = \frac{2\pi f_c V_o C_o R_T}{g_m V_{FB}} \quad \text{(EQ. 27)}$$

where g_m is the trans-conductance of the voltage error amplifier. Compensator capacitor C1 is then given by:

$$C_1 = \frac{1}{R_1 \omega_{cz}}, C_2 = \frac{C_1}{2\pi R_1 C_1 f_{esr} - 1} \quad \text{(EQ. 28)}$$

Example: V_{in} = 20V, V_o = 16.8V, I_o = 4A, f_s = 300kHz, C_o = 22µF/10mΩ, L = 15µH, g_m = 250µs, R_T = 0.15Ω (R_{cs} = 25mΩ, A_c = 6), V_{FB} = 2.1V, $V_{PWM} = V_{IN}/11$, f_c = 15kHz, then compensator resistance R_1 = 10kΩ.

Put the compensator zero at 1.7kHz, and put the compensator pole at esr zero which is 725kHz. The compensator capacitors are:

C_1 = 10nF, C_2 = 22pF

Such small C_2 may not be necessary since it does not affect the phase and gain at such high frequency.

PCB Layout Considerations

Power and Signal Layer Placement on the PCB

As a general rule, power layers should be close together, either on the top or bottom of the board, with signal layers on the opposite side of the board. For example, layer arrangement on a 4 layer board is shown below:

Layer 1: Small signal external components

Layer 2: Signal Ground

Layer 3: Power Ground

Layer 4: Bottom Layer: Power MOSFET, Inductors and other Power traces

Separate the power voltage and current flowing path from the control and logic level signal path. The controller IC will stay on the signal layer, which is isolated by the signal ground to the power signal traces.

Component Placement

The power MOSFET should be close to the IC so that the gate drive signal, the LGATE, UGATE, PHASE, and BOOT traces can be short.

Place the components in such a way that the area under the IC has fewer noise traces with high dv/dt and di/dt, such as gate signals and phase node signals.

SIGNAL GROUND AND POWER GROUND CONNECTION

At minimum, a reasonably large area of copper, which will shield other noise couplings through the IC, should be used as signal ground beneath the IC. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each side, where there is little noise; a noisy trace beneath the IC is not recommended.

GND AND VDD PIN

At least one high quality ceramic decoupling cap should be used to cross the GND and VDD pins. The decoupling cap can be put close to the IC.

LGATE PIN

This is the gate drive signal for the bottom MOSFET of the buck converter. The signal going through this trace has both high dv/dt and high di/dt, and the peak charging and discharging current is very high. These two traces should be short, wide, and away from other traces. There should be no other traces in parallel with these traces on any layer.

PGND PIN

The PGND pin should be laid out to the negative side of the relevant output cap with separate traces. The negative side of the output capacitor must be close to the source node of the bottom MOSFET.

PHASE PIN

This trace should be short, and positioned away from other weak signal traces. This node has a very high dv/dt with a voltage swing from the input voltage to ground. No trace should be in parallel with it. This trace is also the return path for UGATE. Connect this pin to the high-side MOSFET source.

UGATE PIN

This pin has a square shape waveform with high dv/dt. It provides the gate drive current to charge and discharges the top MOSFET with high di/dt. This trace should be wide, short, and away from other traces similar to the LGATE.

BOOT PIN

The BOOT pins di/dt is as high as the UGATE; therefore, this trace should be as short as possible.

CSOP, CSON PINS

The current sense resistor connects to the CSON and the CSOP pins through a low pass filter. The CSON pin is also used as the battery voltage feedback. The traces should be away from the high dv/dt and di/di pins like the PHASE and BOOT pins. In general, the current sense resistor should be close to the IC. Other layout arrangements should be adjusted accordingly.

EN PIN

This pin stays high at enable mode and low at idle mode, and is relatively robust. Enable signals should refer to the signal ground.

DCIN PIN

This pin connects to AC adapter output voltage, and should be less noise sensitive.

Copper Size for the Phase Node

The capacitance of PHASE should be kept very low to minimize ringing. It would be best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application.

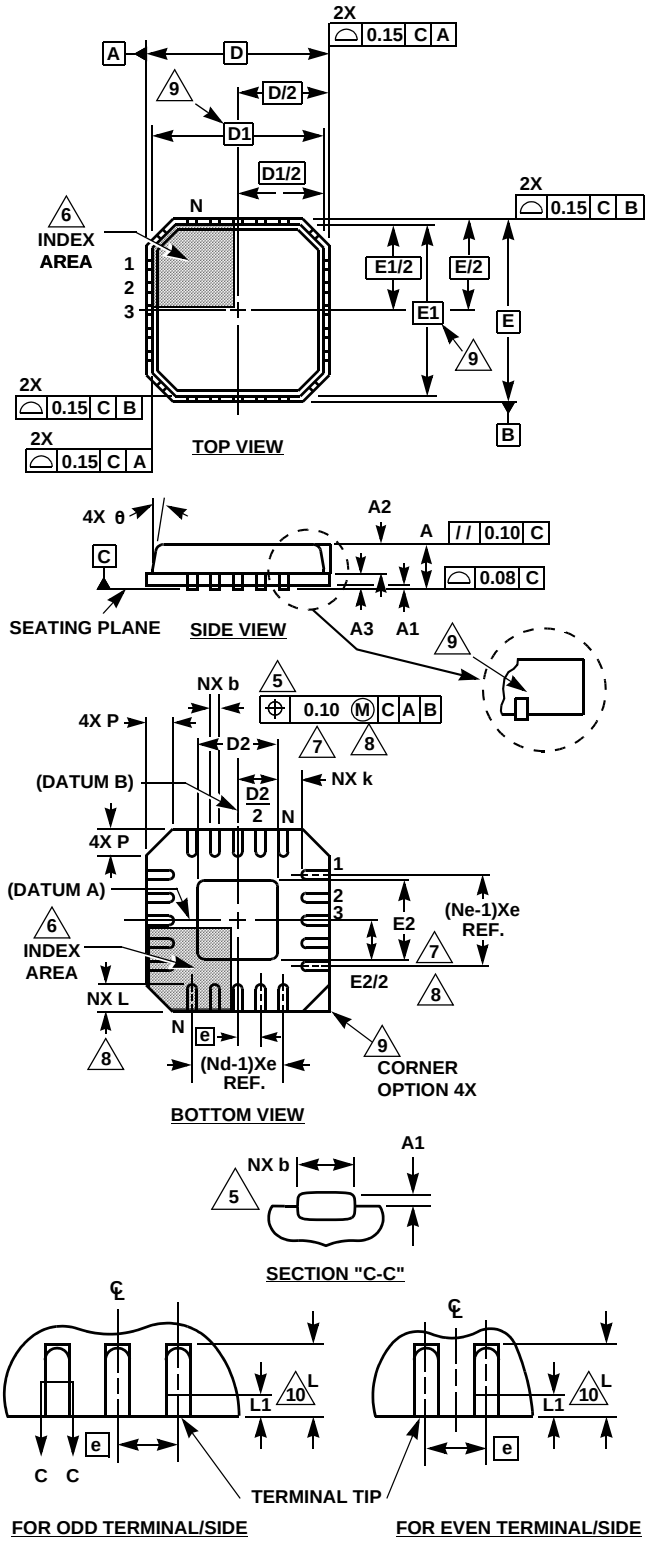
Identify the Power and Signal Ground

The input and output capacitors of the converters, and the source terminal of the bottom switching MOSFET PGND should connect to the power ground. The other components should connect to signal ground. Signal and power ground are tied together at one point.

Clamping Capacitor for Switching MOSFET

It is recommended that ceramic caps be used closely connected to the drain of the high-side MOSFET and the source of the low-side MOSFET. This capacitor reduces the noise and the power loss of the MOSFET.

Quad Flat No-Lead Plastic Package (QFN) Micro Lead Frame Plastic Package (MLFP)



L28.5x5

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-1 ISSUE C)

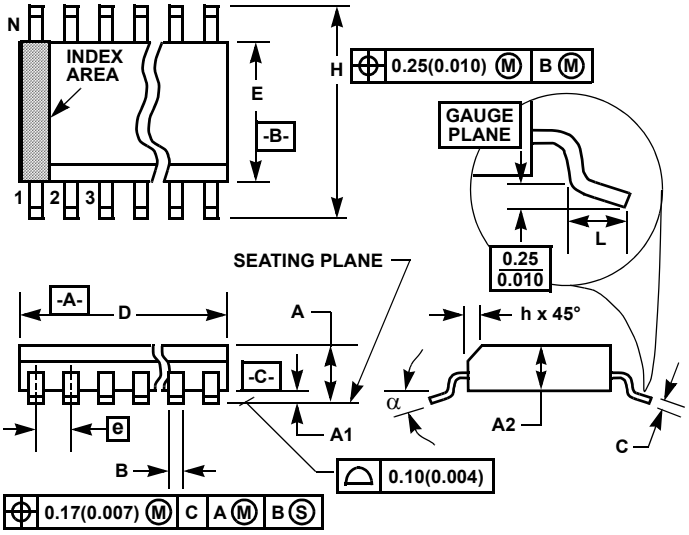
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.18	0.23	0.30	5,8
D	5.00 BSC			-
D1	4.75 BSC			9
D2	2.95	3.10	3.25	7,8
E	5.00 BSC			-
E1	4.75 BSC			9
E2	2.95	3.10	3.25	7,8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N	28			2
Nd	7			3
Ne	8	7		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 0 02/03

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Shrink Small Outline Plastic Packages (SSOP) Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M28.15

28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

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- ## Sales :

Direct +86 (21) 6401-6692

Email amall@ameya360.com

QQ 800077892

Skype ameyasales1 ameyasales2

- ## Customer Service :

Email service@ameya360.com

- ## Partnership :

Tel +86 (21) 64016692-8333

Email mkt@ameya360.com