SEVEN CHANNEL E1 LINE INTERFACE UNIT WITH CLOCK RECOVERY

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GENERAL DESCRIPTION

The XRT81L27 is an optimized seven-channel, analog, 3.3V, line interface unit, fabricated using low power CMOS technology. The device contains seven independent E1 channels, including data and clock recovery circuits. It is primarily targeted towards the SDH multiplexers that accommodate TU12 Tributary Unit Frames. Line cards in these units multiplex 21 E1 channels into higher SDH rates. Devices with seven E1 interfaces such as the XRT81L27 provide the most efficient method of implementing 21-channel line cards. Each channel performs the driver and receiver functions necessary to convert bipolar signals to logical levels and vice versa.

The receiver input accepts transformer or capacitor coupled signals, while the transmitter is coupled to the line using a 1:2 step-up transformer. The same transformer configuration can be used for both balanced 120 Ω and unbalanced 75 Ω interfaces. The Receiver Loss of Original Detection is compliant to G.775 and in Host Mode, the number of zeros received before RLOS is declared can be increased to 4096 bits. This feature provides the user with the flexibility to implement RLOS specifications that require greater than G.775 requirements

FEATURES

- Seven (7) Independent E1 (CEPT) Line Interface Units (Transmitter, Receiver, and Recovery)
- Transmit Output Pulses that are Compliant with the ITU-T G.703 Pulse Template Requirement for 2.048Mbps (E1) Rates
- On-Chip Pulse Shaping for both 75Ω and 120Ω line drivers
- Receiver Can Either Be Transformer or Capacitive-Coupled to the Line
- Detects and Clears LOS (Loss of Signal) Per ITU-T G.775 and ETS 300 233 (programmable from Host)
- Compliant with the ITU-T G.823 Jitter Tolerance Requirements
- 3.3V operation with 5V Input compatibility
- Low power consumption

APPLICATIONS

- SDH and lPDH Multiplexers
- E1 Digital Cross-Connect Systems
- DECT (Digital European Cordless Telephone) Base Stations
- CSU/DSU Equipment

FIGURE 1. BLOCK DIAGRAM

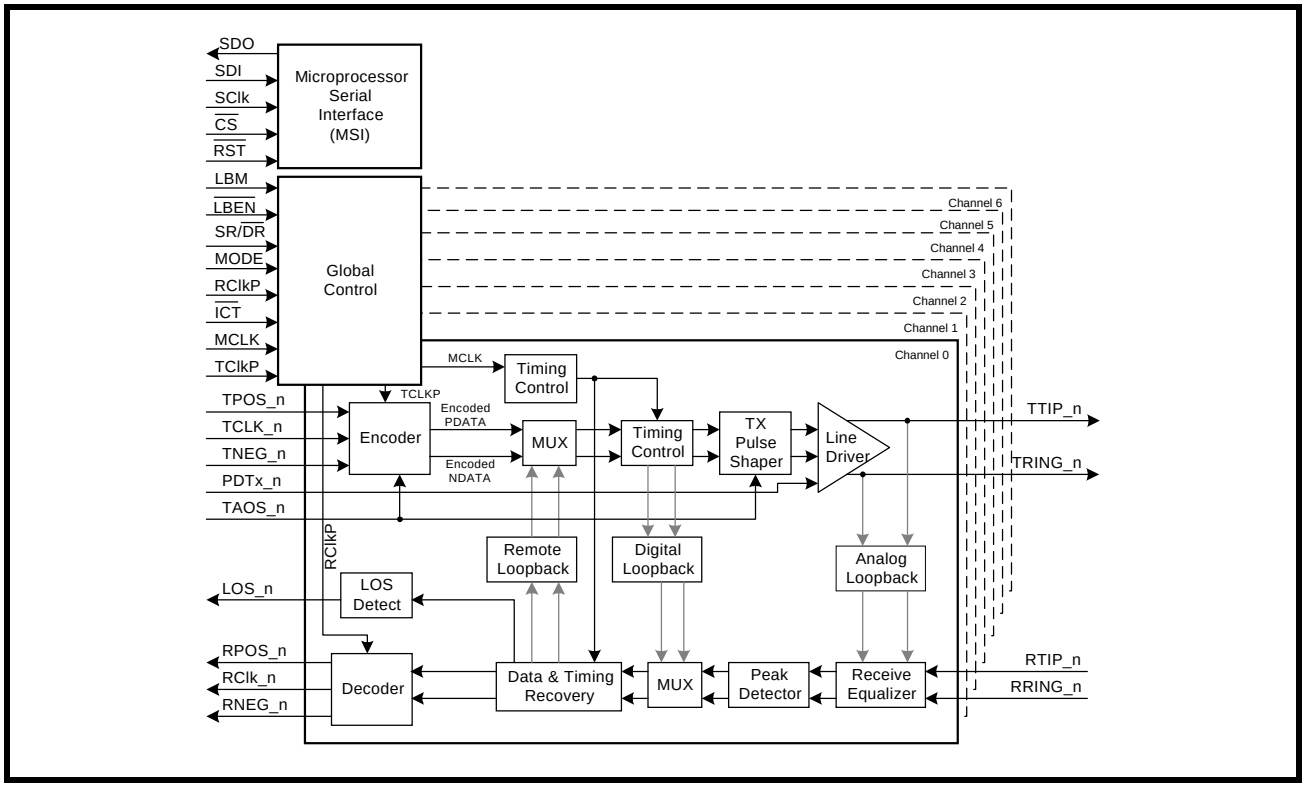
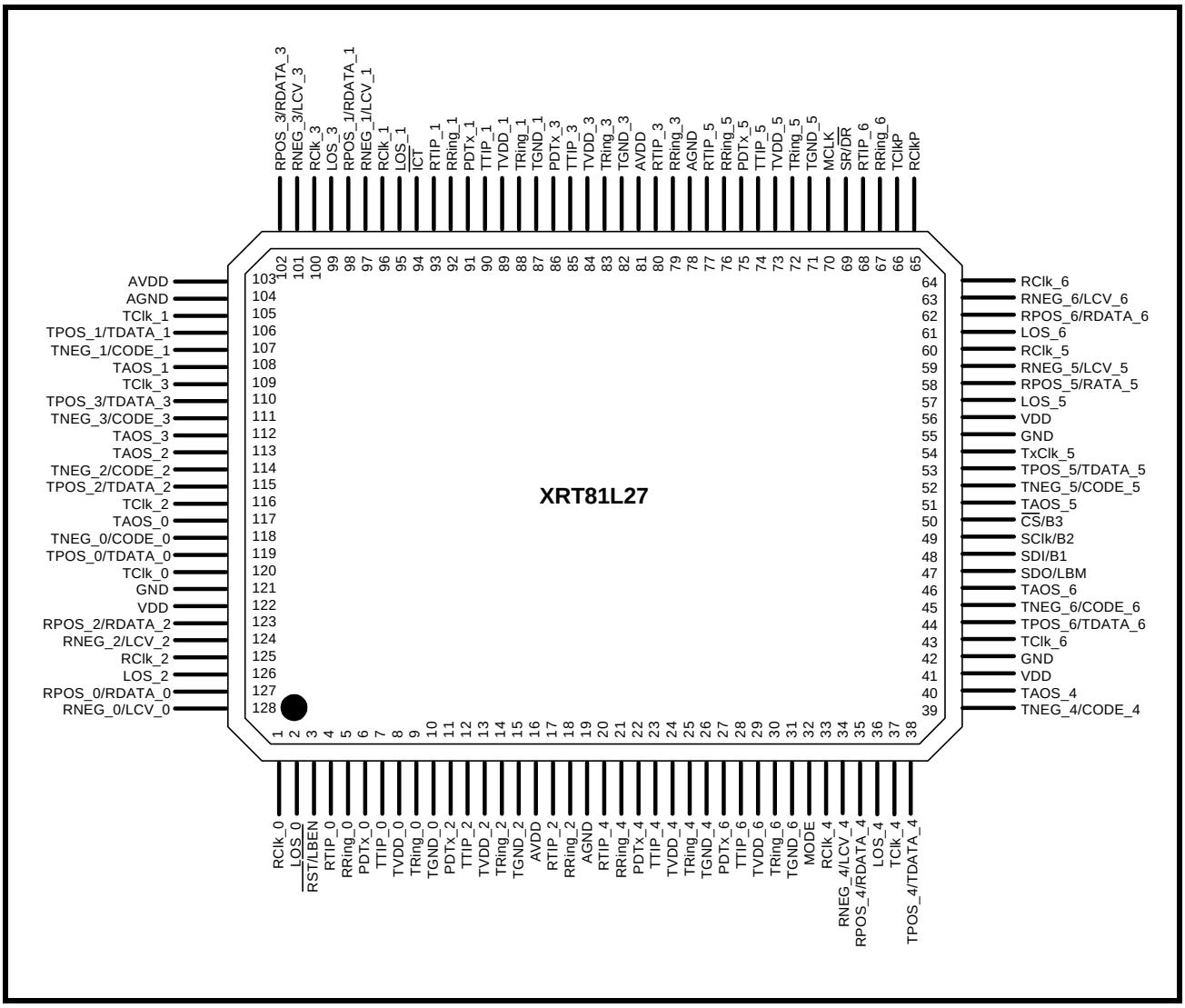


FIGURE 2. PIN OUT OF THE XRT81L27



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT81L27IV	128 Lead TQFP	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTIONS

*NOTE: **I -H** indicates an input pin with a 50kΩ pull-up Resistor, I-L indicates an input pin with a 50kΩ pull-down resistor.*

PIN #	NAME	TYPE	DESCRIPTION
1	RClk_0	O	**Receiver 0 Clock Output**
2	LOS_0	O	**Receiver 0 Loss of Signal:** This signal is asserted "High" to indicate loss of signal at the receive input.
3	$\overline{RST}$ $\overline{LBEN}$	I-H	**Reset (Active-low): (Host Mode)** "Low" Resets the register contents to zero. **Loop-back Enable (Active-low): (Hardware Mode)** "Low" for Loop-back mode enable.
4	RTIP_0	I	**Receiver 0 Bipolar Positive Input:**
5	RRING_0	I	**Receiver 0 Bipolar Negative Input:**
6	PDTx_0	I-H	**Power-down Transmitter 0:** This pin is operational for both **Host** or **Hardware Mode**. This pin MUST be pulled "Low" to enable TTIP_0 and TRING_0 output buffers. Pull this pin "High" to power-down channel 0 transmitter and set TTIP_0 and TRING_0 outputs to high impedance.
7	TTIP_0	O	**Transmitter 0 Tip Output:** Positive bipolar data output to the line
8	TVDD_0	Vdd	**Transmitter 0 Positive Supply (3.3V± 5%)**
9	TRING_0	O	**Transmitter 0 Ring Output:** Negative bipolar data output to the line.
10	TGND_0	Gnd	**Transmitter 0 Supply Ground**
11	PDTx_2	I-H	**Power-down Transmitter 2:** (see pin 6)
12	TTIP_2	O	**Transmitter 2 Tip Output:** Positive bipolar data output to the line.
13	TVDD_2	Vdd	**Transmitter 2 Positive Supply(3.3V± 5%)**
14	TRING_2	O	**Transmitter 2 Ring Output:** Negative bipolar data output to the line.
15	TGND_2	Gnd	**Transmitter 2 Supply Ground.**
16	AVDD	AVdd	**Analog Positive Supply(3.3V± 5%)**
17	RTIP_2	I	**Receiver 2 Bipolar Positive Input:**
18	RRING_2	I	**Receiver 2 Bipolar Negative Input:**
19	AGND	Gnd	**Analog Supply Ground.**
20	RTIP_4	I	**Receiver 4 Bipolar Positive Input:**
21	RRING_4	I	**Receiver 4 Bipolar Negative Input:**
22	PDTx_4	I-H	**Power-down Transmitter 4:** (see pin 6)
23	TTIP_4	O	**Transmitter 4 Tip Output:** Positive bipolar data output to the line.
24	TVDD_4	Vdd	**Transmitter 4 Positive Supply(3.3V± 5%)**
25	TRING_4	O	**Transmitter 4 Ring Output:** Negative bipolar data output to the line.

PIN DESCRIPTIONS

*NOTE: **I -H** indicates an input pin with a 50kΩ pull-up Resistor, I-L indicates an input pin with a 50kΩ pull-down resistor.*

PIN #	NAME	TYPE	DESCRIPTION
26	TGND_4	Gnd	**Transmitter 4 Supply Ground**
27	PDTx_6	I-H	**Power-down Transmitter 6:** (see pin 6)
28	TTIP_6	O	**Transmitter 6 Tip Output:** Positive bipolar data output to the line.
29	TVDD_6	Vdd	**Transmitter 6 Positive Supply(3.3V± 5%)**
30	TRING_6	O	**Transmitter 6 Ring Output:** Negative bipolar data output to the line.
31	TGND_6	Gnd	**Transmitter 6 Supply Ground**
32	MODE	I-L	**Mode Control Input:** This pin is used to select Hardware or Host Mode control of the device. Tie “Low” to select **Host Mode** "High" to select **Hardware Mode**.
33	RClk_4	O	**Receiver 4 Clock Output:**
34	RNEG_4 LCV_4	O	**Receiver 4 Negative Data Output:** In **Dual-Rail mode**, this signal is the receive n-rail output data. **Line Code Violation Output:** In **Single-Rail mode**, this signal outputs a "High" for one clock cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go "High".
35	RPOS_4 RDATA_4	O	**Receiver 4 Positive Data Output:** In **Dual-Rail mode**, this signal is the receive p-rail output data. **Receiver 4 NRZ Data Output:** In **Single-Rail mode**, this signal is the receive output data
36	LOS_4	O	**Receiver 4 Loss of Signal:** (see pin 2)
37	TClk_4	I	**Transmitter 4 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
38	TPOS_4 TDATA_4	I	**Transmitter 4 Positive Data Input:** In **Dual-Rail mode**, this signal is the p-rail input data for transmitter 4. **Transmitter 4 NRZ Data Input:** In **Single-Rail mode**, this signal is used as the NRZ input data
39	TNEG_4 CODE_4	I-L	**Transmitter 4 Negative Data Input:** In **Dual-Rail mode**, this signal is the n-rail data input for transmitter 4. In **Single-Rail mode** (pin 69=1) and with this pin tied "High", input data at the transmit input is encoded in **HDB3** format and the substitution code in the corresponding receive channel will be removed. Tie this pin "Low" to enable **AMI** encoding and decoding.
40	TAOS_4	I-L	**Transmit All Ones Channel_4:** This pin is set to insert AMI all ones data to the line using MCLK as reference. In **Host Mode**, this pin can be left unconnected.
41	VDD	Vdd	**Digital Positive Supply(3.3V± 5%).**
42	GND	Gnd	**Digital Supply Ground.**

PIN DESCRIPTIONS

*NOTE: **I -H** indicates an input pin with a 50kΩ pull-up Resistor, I-L indicates an input pin with a 50kΩ pull-down resistor.*

PIN #	NAME	TYPE	DESCRIPTION
43	TClk_6	I	**Transmitter 6 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
44	TPOS_6/ TDATA_6	I	**Transmitter 6 Positive Data/ NRZ Input:** (see pin 38)
45	TNEG_6/ CODE_6	I-L	**Transmitter 6 Negative Data Input:** (see pin 39)
46	TAOS_6	I-L	**Transmit All Ones Channel_6:** (see pin 40)
47	SDO LBM	O I	**Serial Data Output: (Host Mode**) This pin is the Serial Data Output port for the Microprocessor Serial Interface access. **Loop-back Mode:** (**Hardware Mode**) When this pin is tied "High", Analog Local loop-back is selected. Connect this pin "Low" to select remote loop-back. Digital Local loop-back is not supported in **Hardware Mode**.
48	SDI B1	I	**Serial Data Input Port:** **Host Mode, this pin is the serial data input port (see Figure 5).** **Hardware Mode**, B1, together with B2 (pin 49) and B3 (pin 50) are control bits used to select which one of the seven channels to be placed in Loop-back mode. Analog or Remote Loop-back is determined by LBM (pin 47).
49	SClk B2	I	**Microprocessor Serial Interface Clock:** **Host Mode**, this clock signal is used to clock SDI/SDO for the Serial Interface. **Hardware Mode**, B2, together with B1 and B3 are control bits to select which of the seven channels to be placed in Loop-back mode.(see pin 48 description)
50	$\overline{CS}$ B3	I	**Chip Select Input:** **Host Mode**, this pin must be asserted "Low" in order to enable communication with the device via the Serial Interface. **Hardware Mode**, B3, together with B1 and B2 are control bits to select which of the seven channels to be placed in Loop-back mode. (see pin 48 description)
51	TAOS_5	I-L	**Transmit All Ones Channel_5:** (see pin 40)

Loop-back Channel Control

B1	B2	B3	Chan. #
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	All

PIN DESCRIPTIONS

*NOTE: **I -H** indicates an input pin with a 50kΩ pull-up Resistor, I-L indicates an input pin with a 50kΩ pull-down resistor.*

PIN #	NAME	TYPE	DESCRIPTION
52	TNEG_5/ CODE_5	I-L	**Transmitter 5 Negative Data Input:** (see pin 39)**I**
53	TPOS_5/ TDATA_5	I	**Transmitter 5 Positive/ NRZ Data Input:** (see pin 38)
54	TClk_5	I	**Transmitter 5 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
55	GND	Gnd	**Digital Supply Ground**
56	VDD	Vdd	**Digital Positive Supply(3.3V± 5%)**
57	LOS_5	O	**Receiver 5 Loss of Signal:** (see pin 2)
58	RPOS_5/ RDATA_5	O	**Receiver 5 Positive/NRZ Data Output:** (see pin 35**)**
59	RNEG_5/ LCV_5	O	**Receiver 5 Negative Data Output:** (see pin 34)
60	RClk_5	O	**Receiver 5 Clock Output.**
61	LOS_6	O	**Receiver 6 Loss of Signal:** (see pin 2)
62	RPOS_6/ RDATA_6	O	**Receiver 6 Positive /NRZ Data Output:** (see pin 35**)**
63	RNEG_6/ LCV_6	O	**Receiver 6 Negative Data Output:** (see pin 34)
64	RClk_6	O	**Receiver 6 Clock Output.**
65	RClkP	I-L	**Receiver Clock Output Polarity: (Hardware Mode**) "Low", All channel RPOS /RDATA and RNEG/LCV output data are updated on the falling edge of RClk. "High" to select data update on rising edge of RClk.
66	TClkP	I-L	**Transmit Clock Polarity: (Hardware Mode**) "Low", transmit input data is sampled using the falling edge of TClk. "High" to select rising edge of TClk for data sampling.
67	RRING_6	I	**Receiver 6 Bipolar Negative Input:**
68	RTIP_6	I	**Receiver 6 Bipolar Positive Input:**
69	SR/$\overline{DR}$	I-L	**Single-rail/Dual-rail Select:** In **Hardware Mode** and with this pin tied to "High", input transmit data and receive output data is selected for **Single-Rail mode** operation. "Low" to select **Dual-Rail mode**.
70	MClk	I	**Master Clock Input:** This signal is an independent 2.048MHz clock with accuracy better than ±50ppm and duty cycle within 40% to 60%. The function of MCLK is to provide timing source for the PLL clock recovery circuit, reference clock to insert All Ones data in the transmit as well as the receive paths.
71	TGND_5	Gnd	**Transmitter 5 Supply Ground**
72	TRING_5	O	**Transmitter 5 Ring Output:** Negative bipolar data output to the line

PIN DESCRIPTIONS

*NOTE: **I -H** indicates an input pin with a 50kΩ pull-up Resistor, I-L indicates an input pin with a 50kΩ pull-down resistor.*

PIN #	NAME	TYPE	DESCRIPTION
73	TVDD_5	Vdd	**Transmitter 5 Positive Supply (3.3V± 5%)**
74	TTIP_5	O	**Transmitter 5 Tip Output:** Positive bipolar data output to the line.
75	PDTx_5	I-H	**Power-down Transmitter 5:** (see pin 6)
76	RRING_5	I	**Receiver 5 Bipolar Negative Input:**
77	RTIP_5	I	**Receiver 5 Bipolar Positive Input:**
78	AGND	Gnd	**Analog Supply Ground**
79	RRING_3	I	**Receiver 3 Bipolar Negative Input:**
80	RTIP_3	I	**Receiver 3 Bipolar Positive Input:**
81	AVDD	AVdd	**Analog Positive Supply(3.3V± 5%)**
82	TGND_3	Gnd	**Transmitter 3 Supply Ground**
83	TRING_3	O	**Transmitter 3 Ring Output:** Negative bipolar data output to the line.
84	TVDD_3	Vdd	**Transmitter 3 Positive Supply(3.3V± 5%)**
85	TTIP_3	O	**Transmitter 3 Tip Output:** Positive bipolar data output to the line.
86	PDTx_3	I-H	**Power-down Transmitter 3:** (see pin 6)
87	TGND_1	Gnd	**Transmitter 1 Supply Ground.**
88	TRING_1	O	**Transmitter 1 Ring Output:** Negative bipolar data output to the line.
89	TVDD_1	Vdd	**Transmitter 1 Positive Supply(3.3V± 5%)**
90	TTIP_1	O	**Transmitter 1 Tip Output:** Positive bipolar data output to the line.
91	PDTx_1	I-H	**Power-down Transmitter 1:** (see pin 6)
92	RRING_1	I	**Receiver 1 Bipolar Negative Input:**
93	RTIP_1	I	**Receiver 1 Bipolar Positive Input:**
94	$\overline{\text{ICT}}$	I-H	**In-Circuit Testing (Active Low):** When this pin is tied to "Low", all output pins are forced to high impedance state for in-circuit testing.
95	LOS_1	O	**Receiver 1 Loss of Signal:** (see pin 2)
96	RClk_1	O	**Receiver 1 Clock Output:**
97	RNEG_1/ LCV_1	O	**Receiver 1 Negative Data Output:** (see pin 34)
98	RPO_1S/ RDATA_1	O	**Receiver 1 Positive/NRZ Data Output:** (see pin 35**)**
99	LOS_3	O	**Receiver 3 Loss of Signal:** (see pin 2)
100	RClk_3	O	**Receiver 3 Clock Output:**
101	RNEG_3/ LCV_3	O	**Receiver 3 Negative Data Output:** (see pin 34)

PIN DESCRIPTIONS

NOTE: I -H *indicates an input pin with a 50kΩ pull-up Resistor, I-L indicates an input pin with a 50kΩ pull-down resistor.*

PIN #	NAME	TYPE	DESCRIPTION
102	RPOS_3/ RDATA_3	O	**Receiver 3 Positive/NRZ Data Output:** (see pin 35**)**
103	AVDD	AVdd	**Analog Positive Supply(3.3V± 5%)**
104	AGND	Gnd	**Analog Supply Ground**
105	TClk_1	I	**Transmitter 1 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
106	TPOS_1/ TDATA_1	I	**Transmitter 1 Positive/ NRZ Data Input:** (see pin 38)
107	TNEG_1/ CODE_1	I-L	**Transmitter 1 Negative Data Input:** (see pin 39)
108	TAOS_1	I-L	**Transmit All Ones Channel_1:** (see pin 40)
109	TClk_3	I	**Transmitter 3 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
110	TPOS_3/ TDATA_3	I	**Transmitter 3 Positive/ NRZ Data Input:** (see pin 38)
111	TNEG_3/ CODE_3	I-L	**Transmitter 3 Negative Data Input:** (see pin 39)
112	TAOS_3	I-L	**Transmit All Ones Channel_4:** (see pin 40)
113	TAOS_2	I-L	**Transmit All Ones Channel_ 2:** (see pin 40)
114	TNEG_2/ CODE_2	I-L	**Transmitter 2 Negative Data Input:** (see pin 39)
115	TPOS_2/ TDATA_2	I	**Transmitter 2 Positive/ NRZ Data Input:** (see pin 38)
116	TClk_2	I	**Transmitter 2 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
117	TAOS_0	I-L	**Transmit All Ones Channel_ 0:** (see pin 40)
118	TNEG_0/ CODE_0	I-L	**Transmitter 0 Negative Data Input:** (see pin 39)
119	TPOS_0/ TDATA_0	I	**Transmitter 0 Positive/ NRZ Data Input:** (see pin 38)
120	TClk_0	I	**Transmitter 0 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
121	GND	Gnd	**Digital Supply Ground**
122	VDD	Vdd	**Digital Positive Supply(3.3V± 5%)**
123	RPOS_2/ RDATA_2	O	**Receiver 2 Positive/NRZ Data Output:** (see pin 35**)**
124	RNEG_2/ LCV_2	O	**Receiver 2 Negative Data Output:** (see pin 34)
125	RClk_2	O	**Receiver 2 Clock Output:**
126	LOS_2	O	**Receiver 2 Loss of Signal:** (see pin 2)

PIN DESCRIPTIONS

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PIN #	NAME	TYPE	DESCRIPTION
127	RPOS_0/ RDATA_0	O	**Receiver 0 Positive /NRZ Data Output:** (see pin 35**)**
128	RNEG_0/ LCV_0	O	**Receiver 0 Negative Data Output:** (see pin 34)

TABLE 1: PIN NUMBER BY PIN NAME

CHANNEL	RTIP	RRING	TTIP	TRING	RCLK	RPOS	RNEG	LOS	TCLK	TPOS	TNEG	PDT	TAOS	TVDD	TGND
0	4	5	7	9	1	127	128	2	120	119	118	6	117	8	10
1	93	92	90	88	96	98	97	95	105	106	107	91	108	89	87
2	17	18	12	14	125	123	124	126	116	115	114	11	113	13	15
3	80	79	85	83	100	102	101	99	109	110	111	86	112	84	82
4	20	21	23	25	33	35	34	36	37	38	39	22	40	24	26
5	77	76	74	72	60	58	59	57	54	53	52	75	51	73	71
6	68	67	28	30	64	62	63	61	43	44	45	27	46	29	31
GLOBAL SIGNALS															
$\overline{RST}$	3			RClkP	65										
MODE	32			MClk	70										
SR/$\overline{DR}$	69			TClkP	66										
				ICT	94										
CONTROLLER INTERFACE															
SDO	47			SDI	48			SClk	49			$\overline{CS}$	50		
POWER PINS															
VDD	41	56	122												
GND	42	55	121												
AVDD	16	81	103												
AGND	19	78	104												

ELECTRICAL CHARACTERISTICS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

STORAGE TEMPERATURE	***-65°C to +150°C***
OPERATING TEMPERATURE	***-40°C to +85°C***
ESD RATING	***2000V on all pins[a]***
SUPPLY VOLTAGE	***-0.5 to 6.0V***
THETA-JA	***43 °C/W[b] | 32 Degrees,C/W[c]***
THETA-JC	***6 °C/W | 5 Degrees, C/W***

a. Human Body Model
b. *mounted on 4 (or more) layer board*
c. mounted on 3 (or less) layer board

TABLE 3: DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input High Voltage	V_{IH}	2.0	5.0	V
Input Low Voltage	V_{IL}	-0.5	0.8	V
Output High Voltage @ IOH = 5mA	V_{OH}	2.4	3.5	V
Output Low Voltage @ IOL = 5mA	V_{OL}	-0.5	0.4	V
Input Leakage Current (except input pins with pull-up or pull-down resistors)	I_L	----	$\pm$ 10	µA
Output Load Capacitance	C_L	----	25	pF

TABLE 4: TRANSMITTER ELECTRICAL CHARACTERISTICS

(VDD=3.3V $\pm$ 5%, T_A= -40°C to +85°C Unless Otherwise Specified)

PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
AMI Output Pulse Amplitude: 75Ω Application 120Ω Application	 2.13 2.70	 2.60 3.30	 V V	Use transformer with 1:2 ratio and 9.1Ω resistor in series with each end of primary.
Output Pulse Width	224	264	ns	
Output Pulse Width Ratio	0.95	1.05	----	ITU-G.703
Output Pulse Amplitude Ratio	0.95	1.05	----	ITU-G.703
Output Return Loss: 51KHz --102KHz 102KHz--2048KHz 2048KHz--3072KHz	 8 14 10	 ---- ---- ----	 dB dB dB	ETSI 300 166, CHPTT

TABLE 5: PER CHANNEL POWER CONSUMPTION INCLUDING LINE POWER DISSIPATION, TRANSMISSION AND RECEIVE PATHS ALL ACTIVE

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
Power Consumption	PC	-	107	mW	75Ω load, operating at 50% Mark Density
Power Consumption	PC	-	92	mW	120Ω load, operating at 50% Mark Density.
Power Consumption	PC	-	180	mW	75Ω load, operating at 100% Mark Density.
Power Consumption	PC	-	155	mW	120Ω load, operating at 100% Mark Density.

TABLE 6: RECEIVER ELECTRICAL CHARACTERISTICS

(VDD=3.3V ± 5%, T_A= -40°C to +85°C Unless Otherwise Specified)

PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
Receiver loss of signal: Number of consecutive zeros before **LOS** is set Number of consecutive Zeros before **EXLOS** is set	 10 ----	 255 4096	 bit	
Input signal level at **LOS**	12	---	dB	Cable attenuation @1024KHz
LOS Delay		255	bit	ITU-G.775, ETSI 300 233
Hysteresis		2	dB	
Receiver Sensitivity	11	----	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Interference Margin	-18	----	dB	With 6dB cable loss.
Input Impedance	10	----	KΩ	Between RTIP or RRING to ground
Jitter Tolerance: 20 Hz 700Hz 10KHz ¾100KHz	 10 5 0.3	----	UIpp	ITU G.823
Recovered Clock Jitter Transfer Peaking Amplitude	----	0.5	dB	Corner Frequency = 36KHz ITU G.736
Return Loss: 51KHz -- 102KHz 102KHz -- 2048KHz 2048KHz -- 3072KHz	 14 20 16	 ---- ---- ----	 dB dB dB	ITU-G.703

FIGURE 3. RECEIVE OUTPUT TIMING

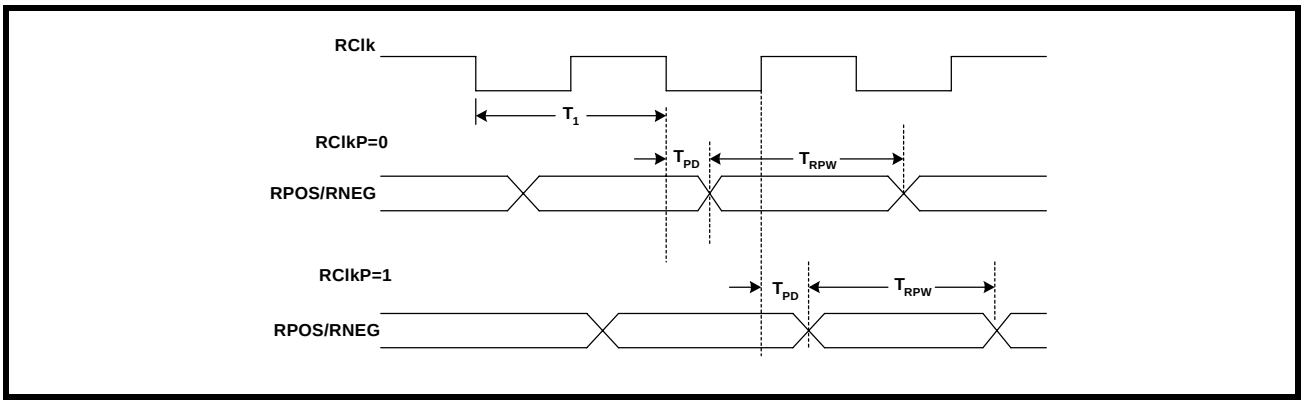


FIGURE 4. TRANSMIT INPUT TIMING

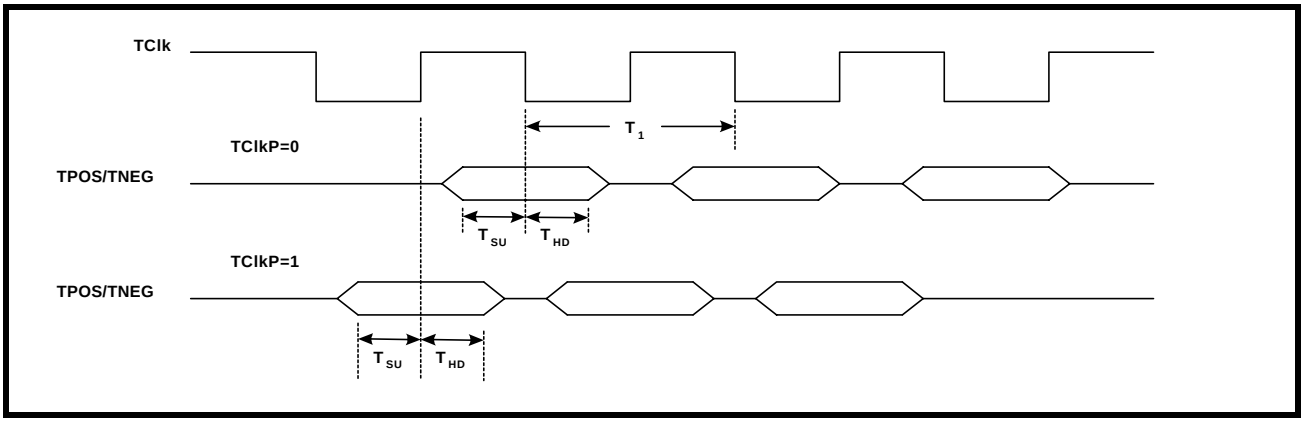


TABLE 7: AC ELECTRICAL CHARACTERISTICS

(VDD=3.3V ± 5%, T_A= -40°C to +85°C Unless Otherwise Specified)

PARAMETER	SYMBOL	MIN	MAX	UNIT
TCLK Clock Period	T_1	488.25	488.30	ns
TCLK Duty Cycle	T_{DC}	30	70	%
Transmit Data Setup Time	T_{SU}	50	-	ns
Transmit Data Hold Time	T_{HO}	50	-	ns
TCLK Rise Time(10%/90%)	T_R	-	40	ns
TCLK Fall Time(90%/10%)	T_F	-	40	ns
Receive Data Rise Time	T_R	-	40	ns
Receive Data Fall Time	T_F	-	40	ns
Receive Data Prop. Delay	T_{PD}	20	-	ns
Receive Data Pulse Width	T_{RPW}	450	-	ns

FUNCTIONAL DESCRIPTION

The XRT81L27 operates in two modes; Hardware or Host. As described below, Hardware mode allows the chip to be controlled by digital signals to put it into various configurations. The Host mode allows a Micro to control these configurations through a serial interface.

THE HARDWARE MODE

The XRT81L27 is placed into the Hardware mode by connecting the Mode pin (pin 32) to VDD ("High"). When the chip is in the Hardware mode the following control pins are active: RST/LBEN (pin 3), SDO/LBM (pin 47), SDI/B1 (pin 48), SClk/B2 (pin 49), CS/B3 (pin 50), SR/DR (pin 69), RClkP (pin 65), TClkP (pin 66). The TAOSx pins (40, 46, 51, 108, 112, 113, 117) are used to insert "all ones" data into the individual channels. In addition, the PDTx pins (6, 11, 22, 27, 75, 86, 91) are active in both Hardware and Host modes to control the individual Transmit line buffers.

The RST/LBEN pin (3) is used to enable Loopback mode. When pulled "Low" Loopback is active. SDO/LBM (pin 47) selects the type of Loopback. With LBM (pin 47) "High", Analog Loopback is active (Terminal Equipment Transmit through the channel(s) selected and back to the Receive out pins). If LBM is "Low", Remote Loopback is selected (Receive line through the channel and back out onto the Transmit TIP/RING buffer onto the Transmit line. Digital Local Loopback is not supported in Hardware mode.

Pins B1, B2, and B3 are used to select the desired Loopback channel as shown on page 5. This allows the selection of any one of the seven channels or all seven. SR/$\overline{DR}$ (pin 69) is used to select between Single Rail or Dual Rail mode for data to and from the Terminal equipment. With pin 69 tied "High", Single Rail is selected. Dual Rail will be active if the pin is pulled "Low". An internal pull-down will accomplish that if the if the pin is left open.

With RClkP "Low" or open, all RPOS & RNEG lines are updated on the falling edge of RClk. When RClkP is "High", RPOS & RNEG are updated on the rising edge of RClk. In Host mode the update edge is controlled by the RClkP bit in the Global control latch (R0, bit 1).

When TClkP is "Low" or open, all TPOS & TNEG lines are sampled on the falling edge of TCLK. When TClkP is "High", TPOS & TNEG are sampled on the rising edge of TClk. In Host mode the sampling edge is controlled by the TClkP bit in the Global control register (R0, bit 0).

If the TAOSX pin of a channel is pulled "High", the channel will Transmit all ones using the MClk signal for a timing reference. If "Low", "normal" data will be transmitted using the TClk.

THE HOST MODE

To configure the XRT81L27 to operate in the HOST Mode, connect the MODE input pin (pin 32) to Ground or leave unconnected.

When the XRT81L27 is operating in the HOST Mode, the Microprocessor Serial Interface block is enabled. Configuration selections are made by writing the appropriate data into the on-chip Command Registers via the Microprocessor Serial Interface.

1.0 THE MICROPROCESSOR SERIAL INTERFACE (MSI)

The on-chip Command Registers of the XRT81L27 E1 Line Interface Unit IC are accessed to configure the XRT81L27 into a variety of modes. This section describes how to use the Microprocessor Serial Interface and the Command Registers.

1.1 MICROPROCESSOR SERIAL INTERFACE DESCRIPTION.

The XRT81L27 MSI uses a simple four wire interface that is compatible with most microcontrollers. Either hardware blocks in the micro can supply the data or “bit-banging” can be used. This interface consists of the following signals:

$\overline{CS}$	(pin 50)	Chip Select (Active Low)
SCLK	(pin 49)	Serial Clock
SDI	(pin 48)	Serial Data Input
SDO	(pin 47)	Serial Data Output

USING THE MICROPROCESSOR SERIAL INTERFACE (MSI)

The user performs Read and Write operations to the on-chip Command Registers (via the MSI) in two distinct phases:

The “Selection Phase”, and

The “Data Phase”

The procedure for performing each of these phases is presented below.The following descriptions for using the Microprocessor Serial Interface are best understood by referring to the diagram in Figure 6.

1.1.1 Selection Phase

In order to use the Microprocessor Serial Interface, a chip select $\overline{CS}$ signal must be supplied to the $\overline{CS}$ input pin. It is important to assert the $\overline{CS}$ pin (“Low”) at least 50ns prior to the first rising edge of the clock signal.

Once the $\overline{CS}$ input pin has been asserted, the type of operation and the target register address must be specified. This information is supplied to the MSI by writing eight serial bits of information into the SDI input. Each of these bits is clocked into the MSI from the SDI input on the rising edge of SCLK. These eight bits are identified and described next.

Bit 1 - R/W (Read/Write) Bit

This bit is clocked into the SDI input on the first rising edge of SCLK after $\overline{CS}$ has been asserted. This bit indicates whether the current operation is a Read or Write operation. A "1" in this bit specifies a Read from the XRT81L27, a "0" in this bit specifies a Write to the device.

Bits 2 through 5: The four (4) bit Address Values (labeled A0, A1, A2 and A3)

The next four rising edges of the SCLK provide the 4-bit address value for this operation. The address selects the appropriate Command/Control Register in the XRT81L27. The address bits must be supplied to the SDI input pin in ascending order with the LSB (least significant bit) first.

Bits 6 and 7:

The next two bits, (A4 and A5) must be set to "0" as shown in Figure 6.

Bit 8:

The value of A6 is a "don't care" but must be clocked.

1.1.2 Data phase of the (MSI) operation

The Microprocessor Serial Interface (MSI) must next be supplied with 8 additional clocks with the relative timing of Figure 5. Table 10 provides essential values for both the selection and data phases of the MSI operation. If the operation specified is a Read, the XRT81L27 will output data on the SDO pin from the addressed register. Data is output in ascending order with the LSB first

If a Write operation has been activated, the external hardware/Micro must supply the first seven (7) bits to be written into the selected register. The eighth bit is a "Don't care" as only seven bits are used in each of the registers. These bits are input LSB first.

At the end of the serial shift phase the data is loaded in parallel into the addressed register. If any register bit was already set, that bit must be included in the input bit stream. Therefore one must either keep an image of the register status in the micro or do a "read-modify-write" operation to maintain the state of each bit that isn't changing.

FIGURE 5. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

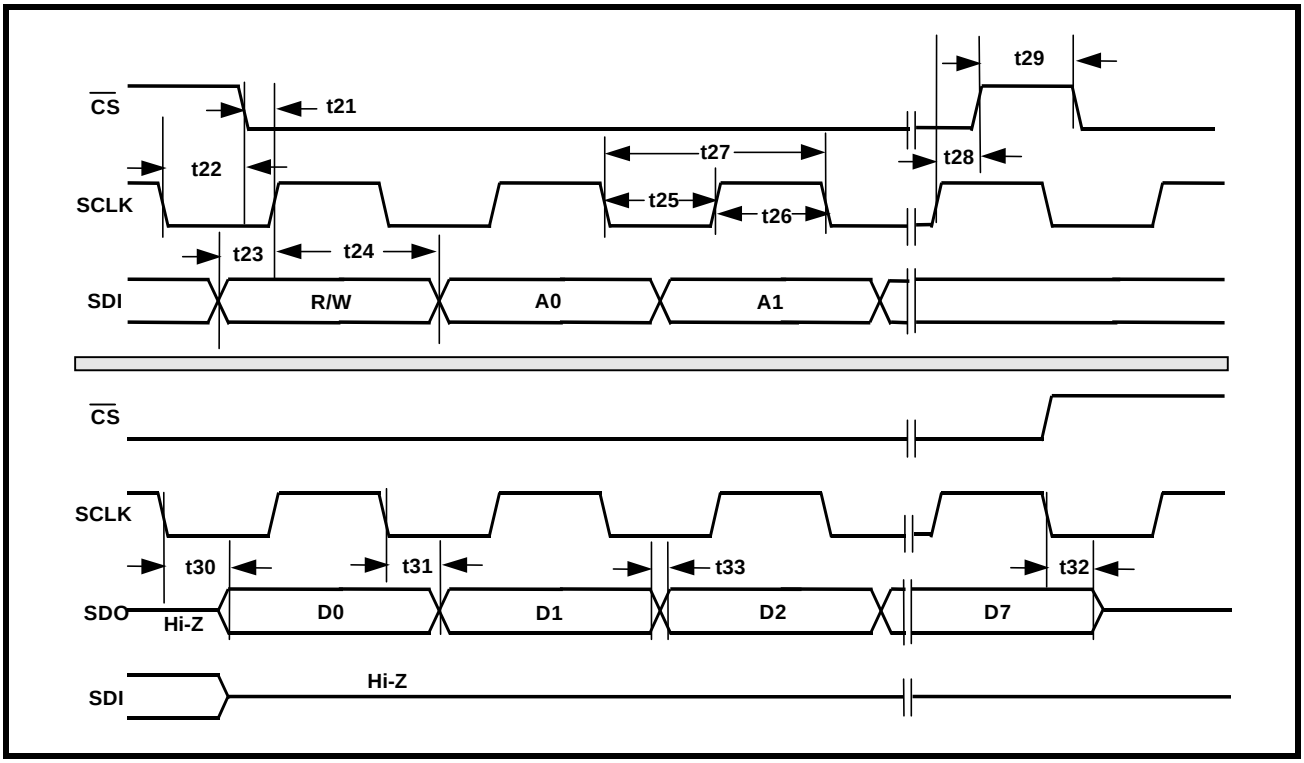
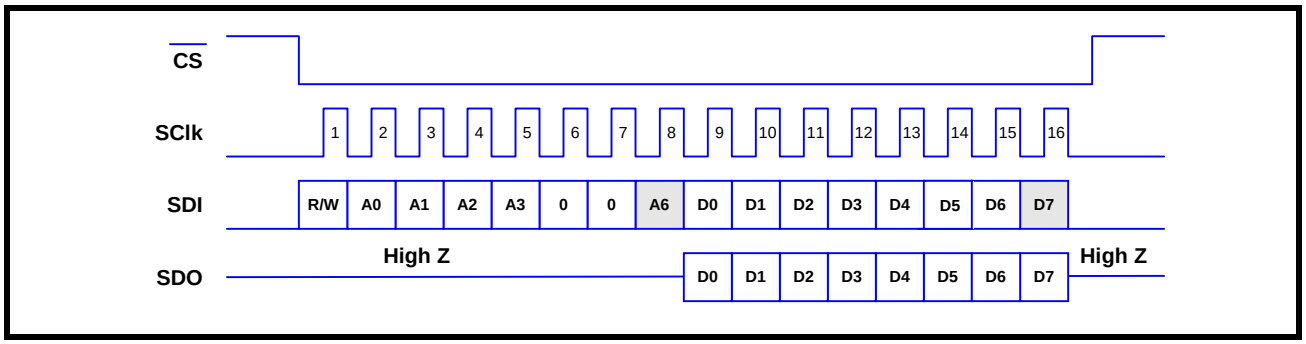


TABLE 8: MICROPROCESSOR SERIAL INTERFACE TIMING (SEE FIGURE 5)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
t_{21}	$\overline{CS}$ "Low" to Rising Edge of SCLK Setup Time	50		ns
t_{22}	$\overline{CS}$ "High" to Rising Edge of SCLK Hold Time	20		ns
t_{23}	SDI to Rising Edge of SCLK Setup Time	50		ns
t_{24}	Rising Edge of SCLK to SDI Hold Time	50		ns
t_{25}	SCLK “Low” Time	240		ns
t_{26}	SCLK “High” Time	240		ns
t_{27}	SCLK Period	500		ns
t_{28}	Rising Edge of SCLK to Rising Edge of $\overline{CS}$ Hold Time	50		ns
t_{29}	$\overline{CS}$ Inactive Time	250		ns
t_{30}	Falling Edge of SCLK to SDO Valid Time		200	ns
t_{31}	Falling Edge of SCLK to SDO Invalid Time		100	ns
t_{32}	Falling Edge of SCLK or Rising Edge of $\overline{CS}$ to high Z		100	ns
t_{33}	Rise/Fall time of SDO Output		40	ns

FIGURE 6. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



Notes:

- Denotes a “don’t care” value

A4 and A5 are always “0”.
R/W = “1” for “Read” Operations
R/W = “0” for “Write” Operations

1.2 Description of the Command Registers

A listing of these Command Registers, their binary/hex Addresses and their Bit-Formats are in Table 9. All bits are reset to zero by activation of the Reset signal (RST, pin 3). All other registers (0111 through 1111) (0x07 through 0x0F) in the address range are reserved.

TABLE 9: MICROPROCESSOR REGISTER ADDRESS AND CONTROL

REGISTER ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GLOBAL COMMAND CONTROL REGISTER (READ/WRITE)								
0000/0x00	reserved	ARAOS	EXLOS	MUTE	SR/DR	CODE	RClkP	TClkP
CHANNEL CONTROL REGISTERS (READ/WRITE)								
0001/0x01	reserved	LLB6	LLB5	LLB4	LLB3	LLB2	LLB1	LLB0
0010/0x02	reserved	RLB6	RLB5	RLB4	RLB3	RLB2	RLB1	RLB0
0011/0x03	reserved	ALB6	ALB5	ALB4	ALB3	ALB2	ALB1	ALB0
0100/0x04	reserved	TAOS6	TAOS5	TAOS4	TAOS3	TAOS2	TAOS1	TAOS0
0101/0x05	reserved	RAOS6	RAOS5	RAOS4	RAOS3	RAOS2	RAOS1	RAOS0
0110/0x06	reserved	PDTx6	PDTx5	PDTx4	PDTx3	PDTx2	PDTx1	PDTx0

TABLE 10: COMMAND CONTROL REGISTER - ADDRESS 0000 - HEX 0X00

(COMMON TO ALL SEVEN CHANNELS)

BIT #	NAME	FUNCTION	REGISTER TYPE
6	ARAOS	**Automatic Receive All Ones:** Writing a "1" to this bit globally enables receive “all one data” insertion at RPOS/RNEG upon receive LOS condition.	R/W
5	EXLOS	**Extended LOS:** Writing a "1" to this bit extends the number of zeros at the receive input to 4096 bits before LOS is declared.	R/W
4	MUTE	**Receive Output Muting:** Writing a "1" to this bit mutes the receive data output at RPOS/RNEG to a “Low” state upon LOS detection EXCEPT when AROAS is set.	R/W
3	SR/$\overline{DR}$	**Single-rail/Dual-rail:** Writing a "1" to this bit selects **single-rail** mode operation. Writing a "0" to select **dual-rail** mode operation.	R/W
2	CODE	**Coding and Decoding:** In **Single-Rail mode** ONLY, selects HDB3 encoding and decoding when set. Under all other conditions, AMI encoding and decoding is selected.	R/W
1	RClkP	**Receive Clock Polarity:** Writing a "1" to this bit selects, receive output data to be updated on the rising edge of RCLK and a "0" to update on the falling edge of RClk.	R/W
0	TClkP	**Transmit Clock Polarity:** Writing a "1" to this bit selects, input data to be sampled on the rising edge of TClk and a "0" to sample on the falling edge of TClk.	R/W

TABLE 11: LOCAL LOOP-BACK REGISTERS - ADDRESS: 0001, HEX 0X01

BIT #.	NAME	FUNCTION	REGISTER TYPE
0-6	LLB0-LLB6	**Local Loop-Back:** Writing a "1" to this bit enables Local Loop-back for the channel(s) selected. During Local loop-back, transmit input data continues to be sent to the line unless overridden by TAOS control.	R/W

TABLE 12: REMOTE LOOP-BACK REGISTERS - ADDRESS: 0010, HEX 0X02

BIT #.	NAME	FUNCTION	REGISTER TYPE
0-6	RLB0-RLB6	**Remote Loop-back:** Wring a "1" to this bit enables Remote Loop-back for the channel(s) selected. During Remote Loop-back, receive output data is available at RPOS/RNEG unless overridden by RAOS request	R/W

TABLE 13: ANALOG LOOP-BACK REGISTERS - ADDRESS: 0011, HEX 0X03

BIT #.	NAME	FUNCTION	REGISTER TYPE
0-6	ALB0-ALB6	**Analog Loop-back:** Writing a “1” to this bit enables Analog Local Loop-back for the channel(s) selected. Analog Loop-back ignores input data on RTIP and RRING and internally routes data at TTIP and TRING back to the receive input. This loop-back mode exercises most of the functional blocks of the channel. Analog Loop-back has priority over other Loop-back, TAOS and RAOS requests.	R/W

TABLE 14: TAOS REGISTERS - ADDRESS: 0100, HEX 0X04

BIT #.	NAME	FUNCTION	REGISTER TYPE
0-6	TAOS0-TAOS6	**Transmit All Ones** Writing a "1" to this bit enables an AMI encoded all ones data to be transmitted to the line for the channel(s) selected. Transmit input data is ignored when TAOS bit is set. Remote Loop-Back has priority over TAOS request.	R/W

TABLE 15: RAOS REGISTERS - ADDRESS: 0101, HEX 0X05

BIT NO.	NAME	FUNCTION	REGISTER TYPE
0-6	RAOS0-RAOS6	**Receive All Ones:** Writing a "1" to this bit enables all ones data to be inserted on the receive side for the channel(s) selected. In **Single-Rail mode**, all ones data is a continuous "High" signal at RPOS output and in **Dual-Rail mode**, a "1010" pattern is sent to RPOS and RNEG while the receive input signal at RRTIP and RRING is ignored. Local Loop-Back has priority over RAOS and ARAOS request.	R/W

TABLE 16: PDTX REGISTERS - ADDRESS: 0110, HEX 0X06

BIT NO.	NAME	FUNCTION	REGISTER TYPE
0-6	PDTx0-PDTx6	**Power-down Transmitter:** Writing a "1" to this bit shut down the transmitter channel selected and places the TTIP/TRing driver in high impedance mode. Individual pin control is also available to switch off the transmitter for fast redundancy application both in **Host** and **Hardware** mode.	R/W

1.3 OPERATION OF THE COMMAND CONTROL REGISTER BITS (ADDRESS: 0000, HEX 0X00)

TCLKP (BIT 0)

Set to a “1”, all 7 channels will sample TPOS/TNEG data on the rising edge of TClk. It will default to a “0”, sampling on the falling edge.

RCLKP (BIT 1)

Set to a “1”, all channels will output RPOS/RNEG receive data on the rising edge of RClk. The default value is “0” where it will output on the falling edge.

CODE (BIT 2)

If set and if the SR/DR bit is set, will select HDB3 encoding for Transmit and decoding for Receive on all channels. If CODE or SR/DR bits are “0”, AMI encoding/decoding is specified.

SR/DR (BIT 3)

If set, single rail mode for the DTE side TPOS in and RPOS out signals. RNEG is used for Line Code Violation (LCV) status. Default state is “0”, selecting dual-rail operation.

MUTE (BIT 4)

If set, will mute the receive outputs of a channel when the LOS condition is detected and ARAOS is not asserted.

EXLOS (BIT 5)

When set, will extend the number of contiguous received zeros to 4096 before the LOS condition is declared.

ARAOS (BIT 6)

When set this bit enables insertion of “all ones data” at RPOS/RNEG when LOS is detected on that channel.

1.4 CHANNEL CONTROL REGISTERS

These registers provide a channel by channel control of the operation and diagnostic mode of the chip. An individual or combination of the channels can be controlled. Certain combinations of modes can not be set as pointed out in the descriptions.

LLB[6:0] (ADDRESS 0001)

Setting a bit in this register causes that channel’s transmit input data to be sent back out of the RPOS/RNEG receive port. The transmit data will continue to be sent to the line unless the TAOS control is enabled.

RLB[6:0] (ADDRESS 0010)

Setting a bit in this register causes that channel’s receive data to be sent back out of the TTIP/TRING on the line to the Remote end. The receive data will continue to be sent to the DTE unless the RAOS control is enabled.

ALBX (ADDRESS 0011)

Setting a bit in this register will cause the analog signal at the output to be sent back through the receive section to the DTE equipment. This will effectively exercise most of the internal functions of that channel. The Analog loopback has priority over the other loopback modes.

TAOS[6:0] (ADDRESS 0100)

Setting this bit enables transmitting all ones data. A Remote loopback (RLB) on the channel has priority over this function.

RAOS[6:0] (ADDRESS 0101)

Setting this bit inserts all ones into the receive data stream. Local loopback has priority over RAOS and the ARAOS signal.

PDTX[6:0] (ADDRESS 0110)

Setting this bit places the Transmit driver into a high impedance state. Individual pin control is also available in both the Host and Hardware modes. Care should be taken in the usage of this feature. While the default (reset) state of this register is zero, hence enabling the outputs of the channel, the “PDT” pin has

priority. This priority allows fast switching of channels using “external hardware”. However, if software control is to be used, the PDTx pin must be tied low as there is an internal pull-up resistor.

2.0 THE TRANSMIT SECTION

The Transmit section of the XRT81L27 consists of the following blocks:

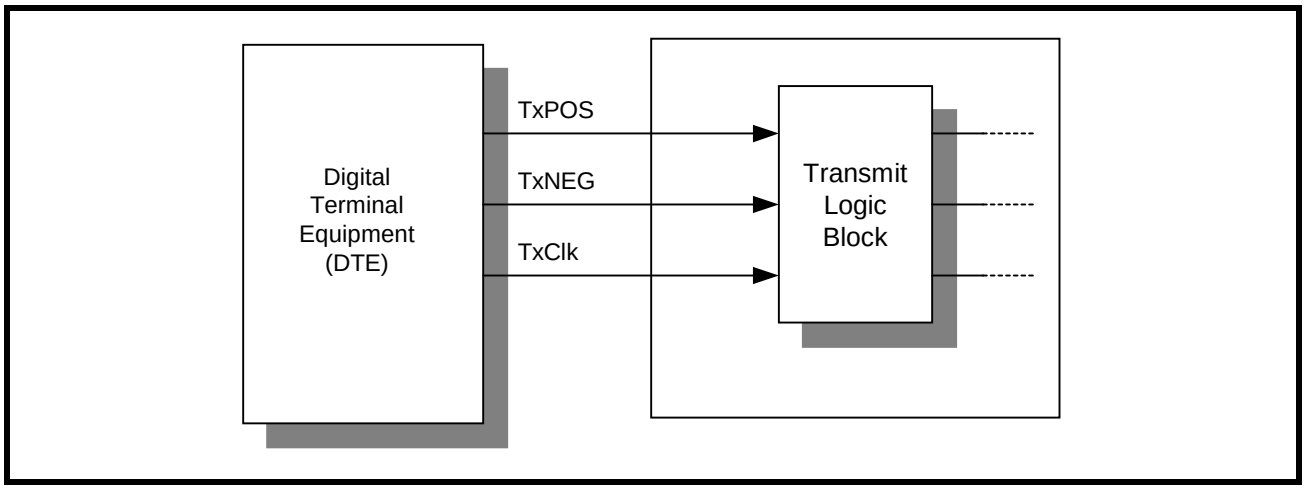
- THE TRANSMIT LOGIC BLOCK
- The Encoder block
- The MUX block
- The Timing Control block
- The TX Pulse Shaper block
- The Line Driver block

2.1 THE TRANSMIT LOGIC BLOCK.

The purpose of the Transmit Logic Block is to accept either Dual-Rail or Single-Rail TTL/CMOS level data and timing information from the Terminal Equipment.

Figure 7 illustrates the typical interface for the transmission of data between the Terminal Equipment and the Transmit Section of the XRT81L27.

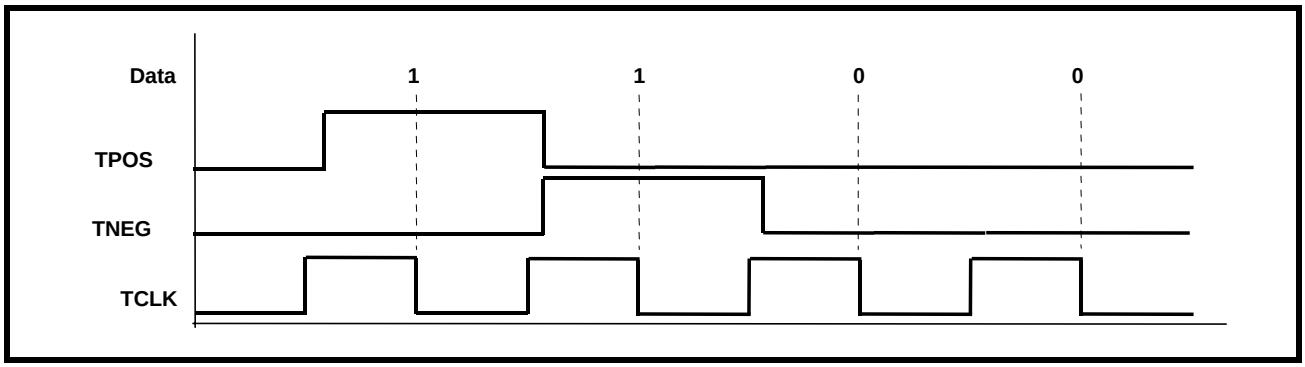
FIGURE 7. THE INTERFACE FOR THE TRANSMISSION OF DATA FROM THE TRANSMITTING TERMINAL EQUIPMENT TO THE TRANSMIT SECTION OF THE XRT81L27



2.1.1 Dual-rail input mode

The manner that the LIU handles Dual-Rail data is described below and illustrated in Figure 8. The XRT81L27samples the data on the TPOS and TNEG input pins on the falling edge of TCLK. If the XRT81L27 samples a “1” on the TPOS input pin, the Transmit Section of the device ultimately generates a positive polarity pulse via the TTIP and TRING output pins. If the XRT81L27 samples a “1” on the TNEG input pin, the Transmit Section of the device generates a negative polarity pulse via the TTIP and TRING output pins. HDB3 Encoding will already have been done on this data.

FIGURE 8. DUAL RAIL DATA FROM THE TERMINAL



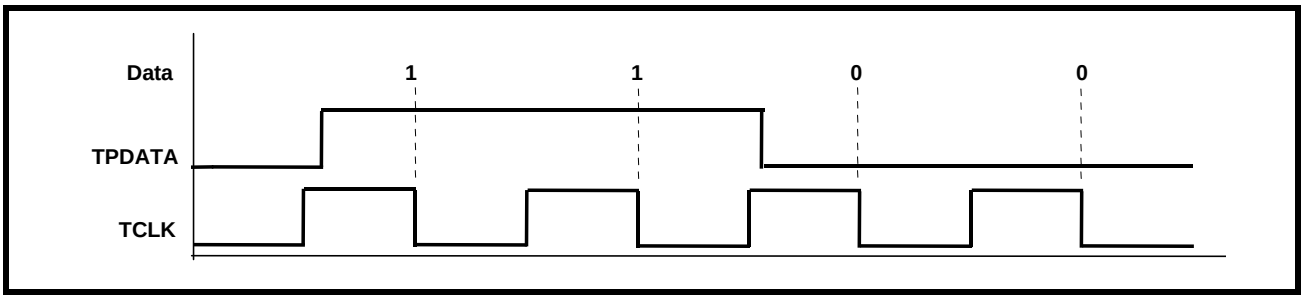
2.1.2 Single-rail input mode

Used if data is to be transmitted from the Terminal Equipment to the XRT81L27 in Single-Rail format (a binary data stream) without having to convert it into a Dual-Rail format. The Transmit Logic Block accepts Single-Rail data via the TPOS input pin. The TClk sig-

nal samples this input pin on the falling edge of the TCLK clock signal and encodes it into the appropriate bipolar line signal across the TTIP and TRING output pins.In this mode the Transmit Logic Block ignores the TNEG input pin.

Figure 9 illustrates the behavior of the TPOS and TCLK signals when the Transmit Logic Block has been configured to accept Single-Rail data from the Terminal Equipment.

FIGURE 9. SINGLE-RAIL DATA FROM THE TERMINAL



2.1.3 TClk input

TCLK is a clock input signal of 2.048 MHz. The global signal TClkP can be used to invert the polarity of the sampling clock relative to the TClk input pin for both SD and DR modes.

2.2 THE ENCODER BLOCK

The purpose of the Encoder Block is to aid in the Clock Recovery process at the Remote Terminal Equipment by ensuring an upper limit on the number of consecutive zeros that can exist in the line signal.

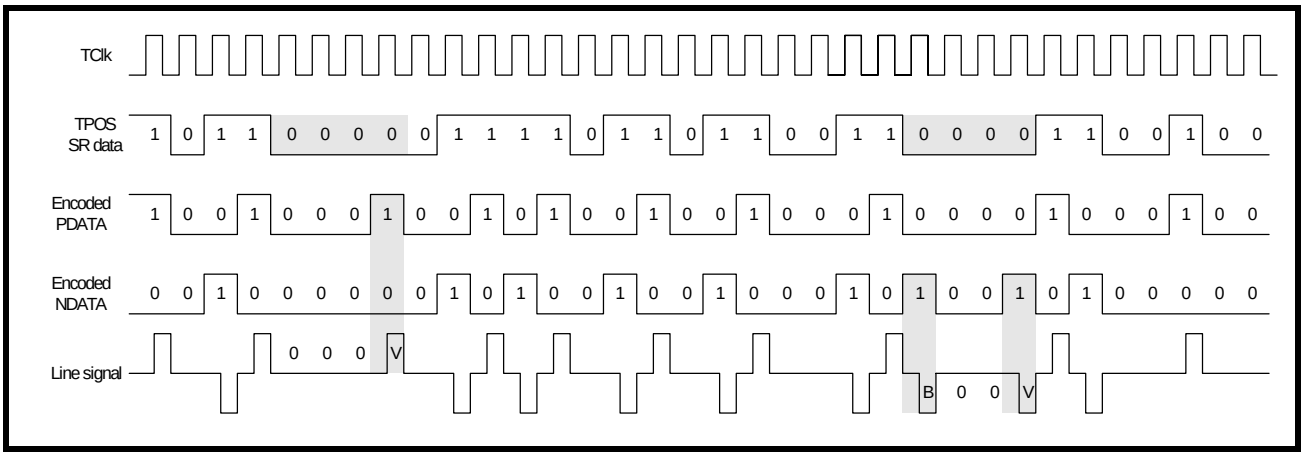
2.2.1 HDB3 Encoding

When the Encoder is enabled (by the global CODE bit set and **Single-Rail mode** selected), it parses through and searches the Transmit Data Stream from the Transmit Logic Block for the occurrence of four (4) consecutive zeros (“0000”). If the HDB3 Encoder finds an occurrence of four consecutive zeros, it then substitutes these four “0’s” with either a “000V” or a “B00V” pattern to insure that an odd number of bipolar pulses exist between any two consecutive violation pulses.

“B” represents a Bipolar pulse that is compliant with the Alternating Polarity requirements of the AMI (Alternate Mark Inversion) line code and “V” represents a bipolar Violation (e.g., a bipolar pulse that violates the Alternating Polarity requirements of the AMI line code).

Figure 10 illustrates the HDB3 Encoder at work with two separate strings of four (or more) consecutive zeros showing a “000V and a “B00V” usage

FIGURE 10. HDB3 ENCODING



2.3 THE MUX BLOCK

The MUX block accepts data inputs from the Encoder block and the Remote loopback. Under control of the channel control bits it will select the desired bit stream and send it to the timing control block. Remote loopback provides a path for the XRT81L27 to send received data back over the Transmit line (TTIP - TRING) to the “other” end of the Timing Control block

2.3.1 Timing Control Block

The Timing Control block contains several sub-blocks. These functions are used to control the timing on the input data stream such that the output meets all system timing specifications.

2.3.2 The Transmit Clock Duty Cycle Adjust Circuit

The on-chip Pulse-Shaping circuitry in the Transmit Section of the XRT81L27 has the responsibility for generating pulses of the shape and width to comply with the applicable pulse template requirement. The widths of these output pulses are defined by the width of the half-period pulses in the TCLK signal.

Allowing the widths of the pulses in the TCLK clock signal to vary significantly could jeopardize the chip's ability to generate Transmit Output pulses of the appropriate width, thereby failing the applicable Pulse Template Requirement Specification. The chips ability to generate compliant pulses could depend upon the duty cycle of the clock signal applied to the TCLK input pin.

In order to combat this phenomenon, the Transmit Clock Duty Cycle Adjust circuit was designed into the XRT81L27. The Transmit Clock Duty Cycle Adjust Circuitry is a PLL that was designed to accept clock pulses via the TCLK input pin at duty cycles ranging from 30% to 70% and to regenerate these signals with a 50% duty cycle.

The XRT81L27 Transmit Clock Duty Cycle Adjust circuit alleviates the need to supply a signal with a 50% duty cycle to the TCLK input pin.

2.3.3 Transmit All Ones

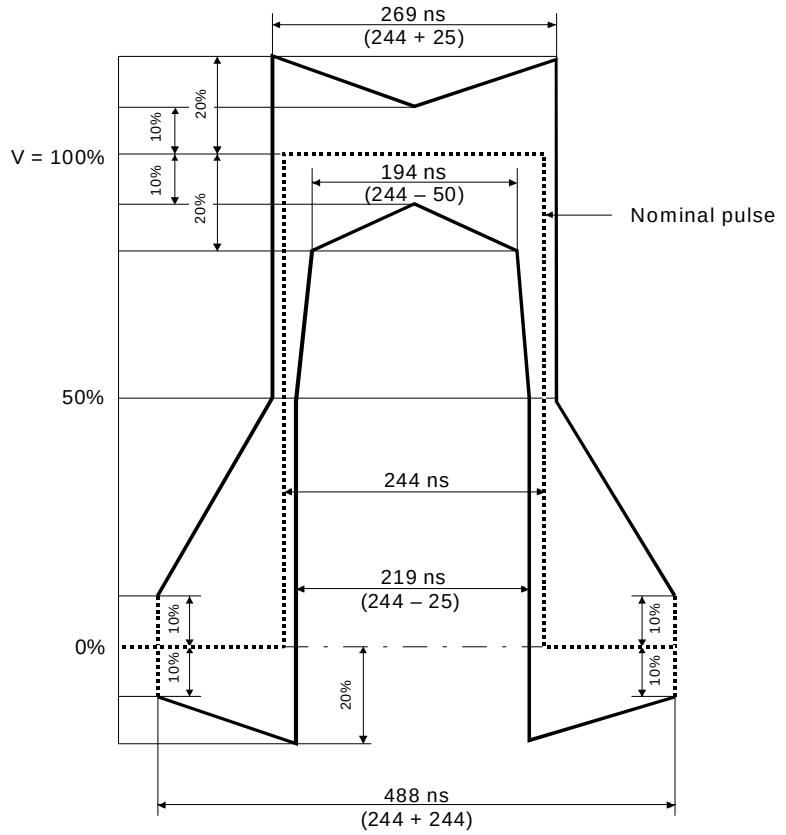
In some conditions the system will control the chip such that it will transmit “all ones” data onto the line. It is possible that a valid TClk is not available and so the MClk signal will be used to provide the timing. It should be noted that the Local feedback will NOT include the “all ones” bit stream so this data is diverted before going into the pulse shaper circuit.

2.4 The Pulse Shaping Circuit

The purpose of the "Transmit Pulse Shaping" Circuit is to generate Transmit Output pulses that comply with the ITU-T G.703 Pulse Template Requirements for E1 applications, even with TClk duty cycle between 30 and 70%.

As a consequence, each channel (within the XRT81L27) will take each mark which is provided to it via the Transmit Input Interface block, and will generate a pulse that complies with the pulse template, presented in Figure 11, (when measured on the secondary-side of the Transmit Output Transformer).

FIGURE 11. ITU-T G.703 PULSE TEMPLATE



Note – V corresponds to the nominal peak value.

2.5 THE LINE DRIVER BLOCK

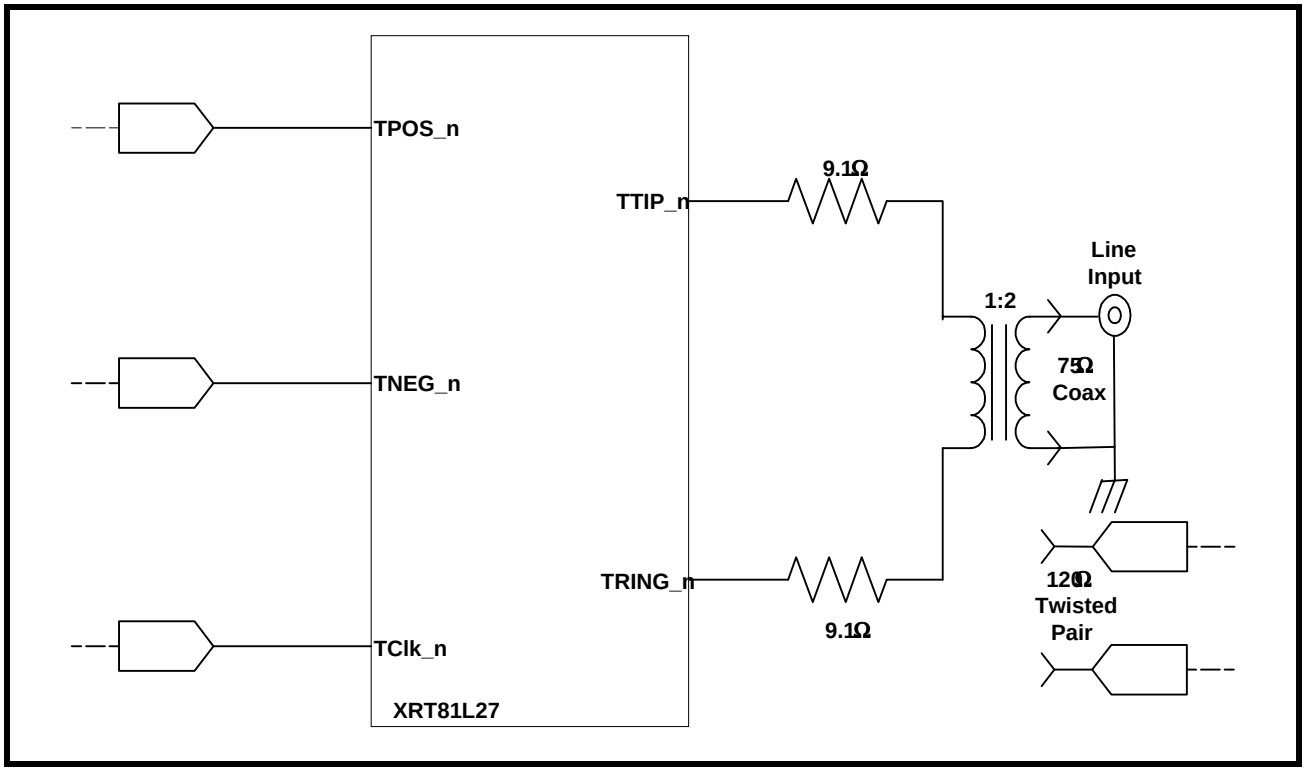
The driver block will take the TP and TN pulses out of the Pulse Shaping circuit and apply these to the TTIP and TRING pins. Output drive control is available from either a dedicated signal or (in Host mode) from one of register control bits to turn the channel “off” by placing the drivers in a high impedance state.

2.6 INTERFACING THE TRANSMIT SECTIONS OF THE XRT81L27 TO THE LINE

In both (75Ω or 120Ω) applications, the user is advised to interface the Transmitter to the Line, using the termination as shown in Figure 12. This includes 1:2 transformer with the intrinsic impedance of the line used as a termination resistance.

The configuration differs only in the type of line connects, The internal circuit adjusts to the load impedance

FIGURE 12. ILLUSTRATION OF HOW TO INTERFACE THE TRANSMIT SECTIONS OF THE XRT81L27 TO THE LINE (FOR 75 OR 120Ω APPLICATIONS)



3.0 THE RECEIVE SECTION

The Receive Sections of the XRT81L27 consists of the following blocks:

- The Receive Equalizer block
- The Peak Detector and Slicer block
- The LOS Detector block
- The Receive Output Interface block

3.1 INTERFACING THE RECEIVE SECTIONS TO THE LINE

The design of each channel (within the XRT81L27) permits the user to transformer-couple or capacitive-couple the Receive Section to the line. Additionally, as mentioned earlier, the specification documents for E1 specify 75Ω termination loads, when transmitting over coaxial cable, and 120Ω loads, when transmitting over twisted-pair. Figure 13, Figure 14 and Figure 15 present the various methods that can be employ to interface the Receivers (of the XRT81L27) to the line. The receive circuits of Figure 13, Figure 14 and Figure 15 differ in the impedance at the inputs and the line connections.

FIGURE 13. SCHEMATIC FOR INTERFACING THE RECEIVE SECTIONS OF THE XRT81L27 TO THE LINE FOR 75Ω (TRANSFORMER-COUPLED) APPLICATIONS

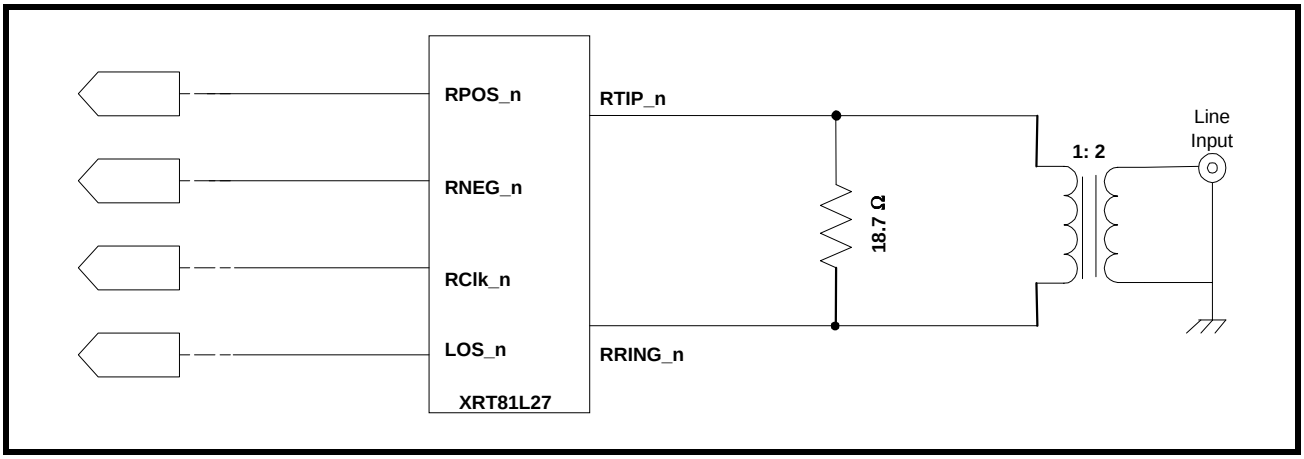
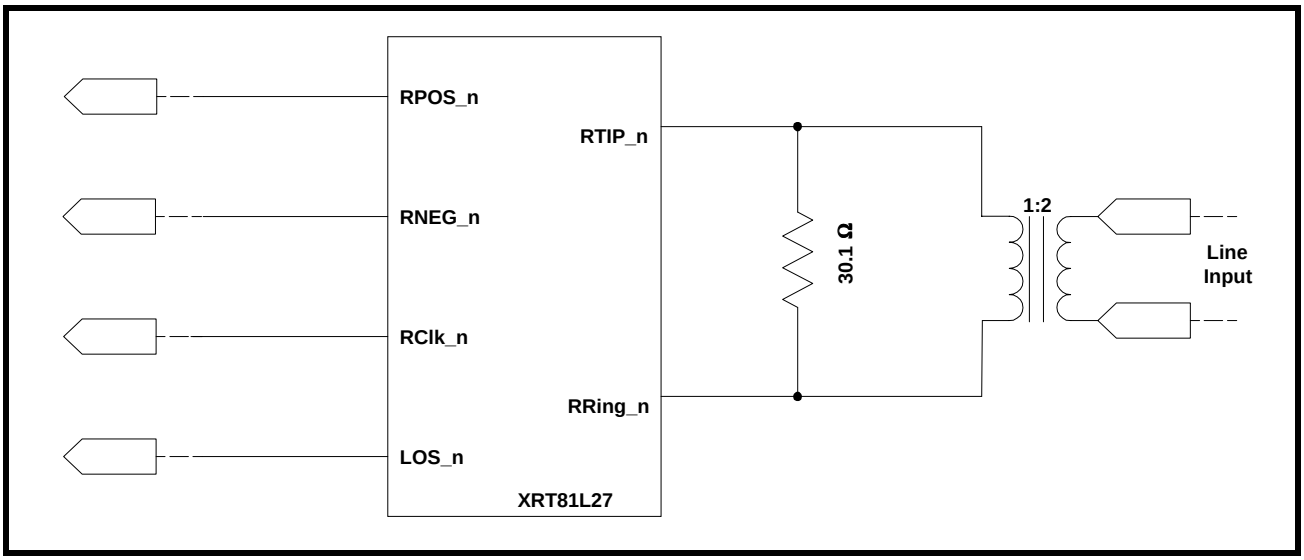


FIGURE 14. SCHEMATIC FOR INTERFACING THE RECEIVE SECTIONS OF THE XRT81L27 TO THE LINE FOR 120Ω (TRANSFORMER-COUPLED) APPLICATIONS

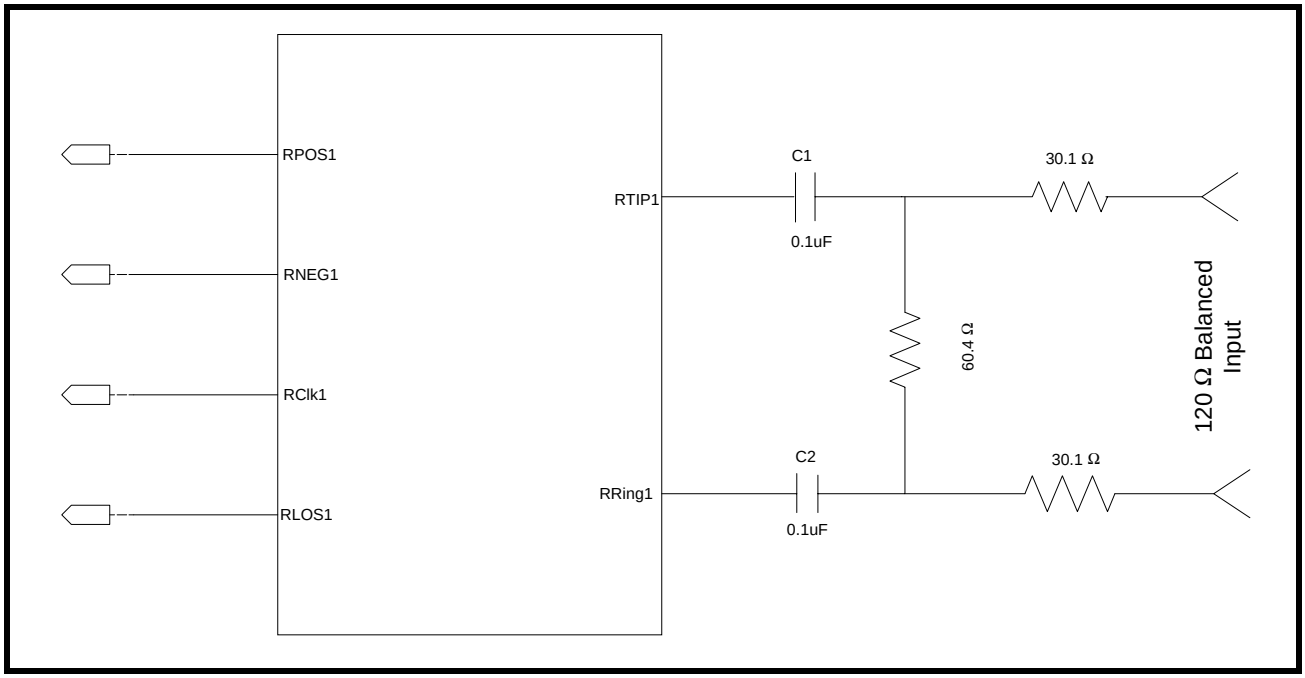


The Transformer used should be 1:2 step up for Transmit direction and 2:1 step down for the Receive direction. The following transformers are recommended: Pulse PE-65681, Pulse T1090, and HALO TG08-1505N1.

3.2 CAPACITIVE-COUPLING THE RECEIVER TO THE LINE

Figure 15 presents a recommended method to use when capacitive-coupling the Receive Section to the line.

FIGURE 15. CAPACITIVE - COUPLED RECEIVE SECTIONS OF THE XRT81L27 TO THE LINE (FOR BALANCED 120Ω APPLICATIONS)



3.3 THE RECEIVE EQUALIZER BOCK

After a given Channel (within the XRT81L27) has received the incoming line signal, via the RTIP_n (where _n is the channel number) and RRING_n input pins, the first block that this signal will pass through is the Receive Equalizer block.

As the line signal is transmitted from a given Transmitting terminal, the pulse shapes (at that location) are basically square. Hence, these pulses consist of a combination of low and high frequency Fourier components. As this line signal travels from the transmitting terminal (via the coaxial cable or twisted pair) to the receiving terminal, it will be subjected to frequency-dependent loss. The higher frequency components of the signal will be subjected to a greater amount of attenuation than the lower frequency components. If this line signal travels over reasonably long cable lengths, then the original square shape of the pulses will be distorted and with inter-symbol interference increases.

The purpose of this block is to equalize the incoming distorted signal, due to cable loss. In essence, the Receive Equalizer block accomplishes this by subjecting the received line signal to frequency-dependent amplification (which attempts to counter the frequency-dependent loss that the line signal has experienced). By doing this, the Receive Equalizer is attempting to restore the shape of the line signal so that the received data can be recovered reliably.

3.4 The Peak Detector and Slicer Block

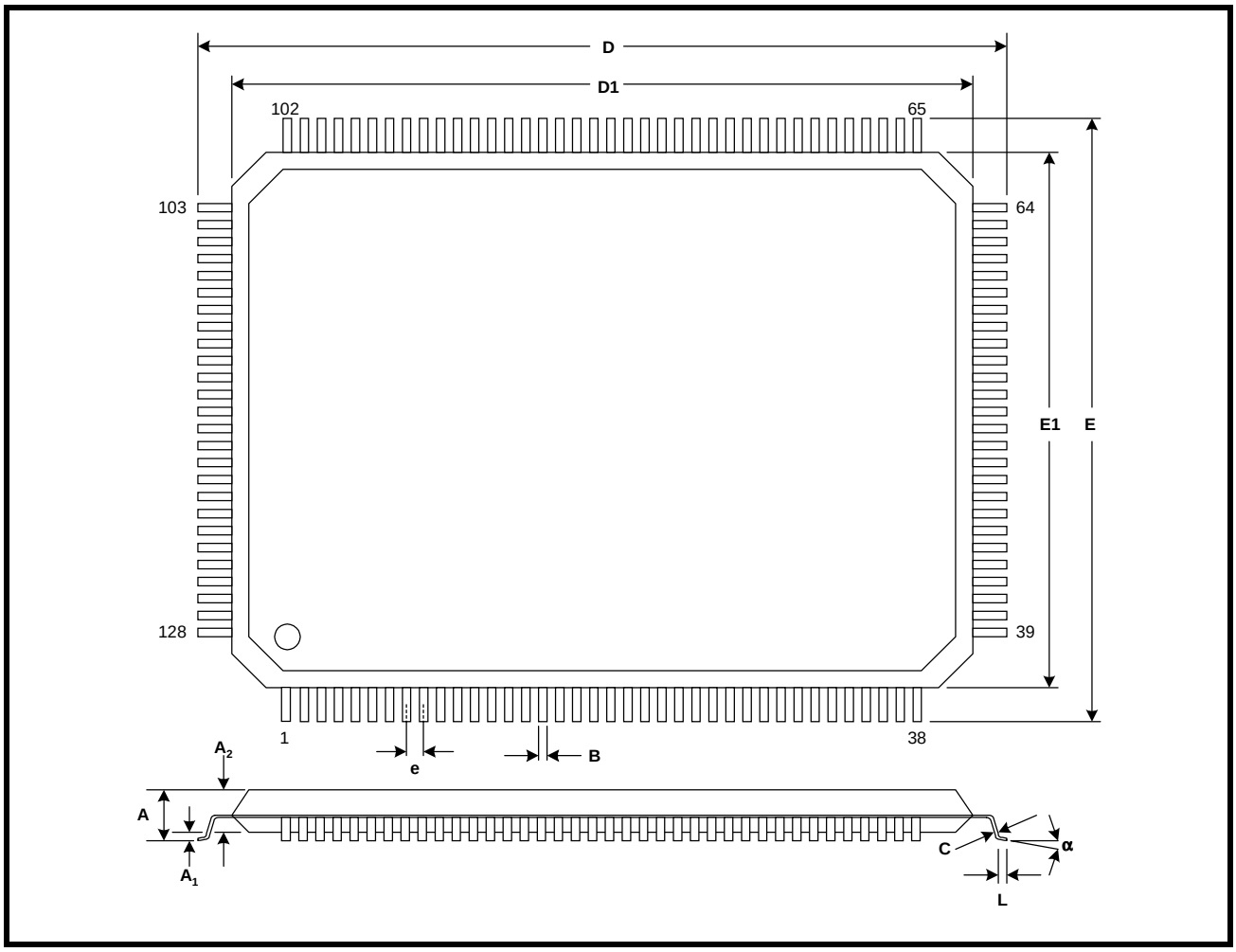
After the incoming line signal has passed through the Receive Equalizer block, it will next be routed to the Slicer block. The purpose of the Slicer block is to quantify a given bit-period (or symbol) within the incoming line signal as either a “1” or a “0”.

3.5 The LOS Detector block

The LOS Detector block, within each channel (of the XRT81L27) was specifically designed to comply with the LOS Declaration/Clearance requirements per ITU-T G.775. As a consequence, the channel will declare an LOS Condition, (by driving the LOS output pin “High”) if the received line signal amplitude drops to –20dB or below. Further, the channel will clear the LOS Condition if the signal amplitude rises back up to –15dB typically, or above. The XRT81L27 was designed to meet the ITU-T G.775 specification timing requirements for declaring and clearing the LOS indicator. In particular, the XRT81L27 will declare an LOS between 10 and 255 UI (or E1 bit periods) after the actual time the LOS condition occurred. Further, the XRT81L27 will clear the LOS indicator within 10 to 255 UI after restoration of the incoming line signal.

When operating in the Host mode, the LOS time can be extended to 4096 zeros by the activation of the EXLOS bit in the Command Control Register. This will provide for those cases where the G.775 specification value is not long enough,

FIGURE 16. PACKAGE OUTLINE DRAWING



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.858	0.874	21.80	22.20
D_1	0.783	0.791	19.90	20.10
E	0.622	0.638	15.80	16.20
E_1	0.547	0.555	13.90	14.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

REVISIONS

Rev. 1.0.1 changed package from 14x14mm 128 pins to 14x20mm 128 pins.

Rev. 1.0.2 Added info on serial processor interface. Corrected pin out for pins 33, 34, 35, 36, 37, 38, 97, 98, 101 and 102.

Rev. 1.0.3 Corrected typos in pin list (pin 29, 51, 64 and 118) and Pin out diagram (pins 47, 48 and 69).

Rev 1.0.4 “Jack Irwin” 10/19/01

Rev 1.0.5 John edits.

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