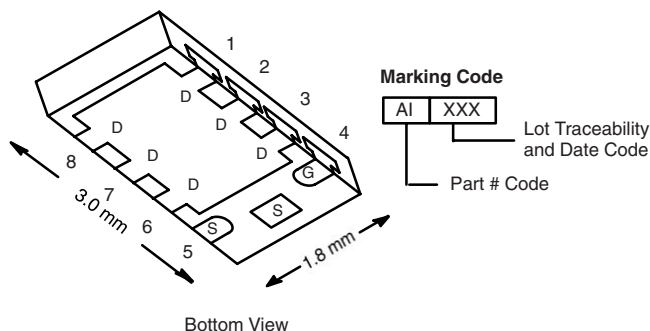


N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
30	0.0145 at $V_{GS} = 10$ V	12	9.5 nC
	0.0185 at $V_{GS} = 4.5$ V	12	

PowerPAK ChipFET Single



Ordering Information: Si5418DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

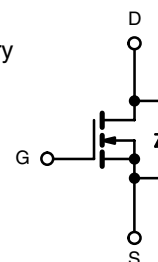
FEATURES

- Halogen-free
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile


RoHS
COMPLIANT

APPLICATIONS

- Load Switch, PA Switch, and Battery Switch for Portable Applications
- DC-DC Synchronous Rectification



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	12^a
		$T_C = 70^\circ\text{C}$	12^a
		$T_A = 25^\circ\text{C}$	$11.6^{b,c}$
		$T_A = 70^\circ\text{C}$	$9.3^{b,c}$
Pulsed Drain Current	I_{DM}	40	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	12^a
		$T_A = 25^\circ\text{C}$	$2.6^{b,c}$
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	31
		$T_C = 70^\circ\text{C}$	20
		$T_A = 25^\circ\text{C}$	$3.1^{b,c}$
		$T_A = 70^\circ\text{C}$	$2^{b,c}$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	34	40	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	3	4	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

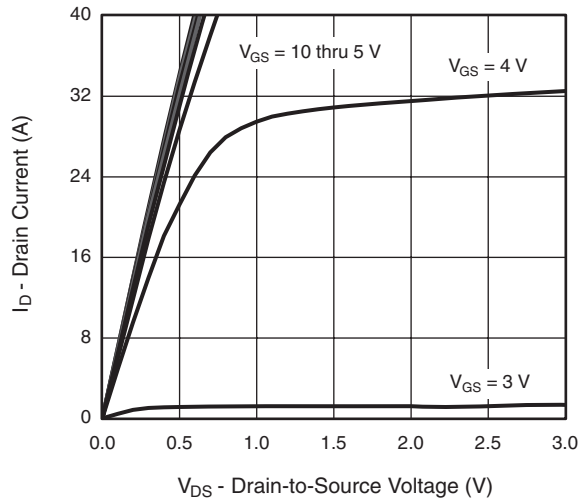
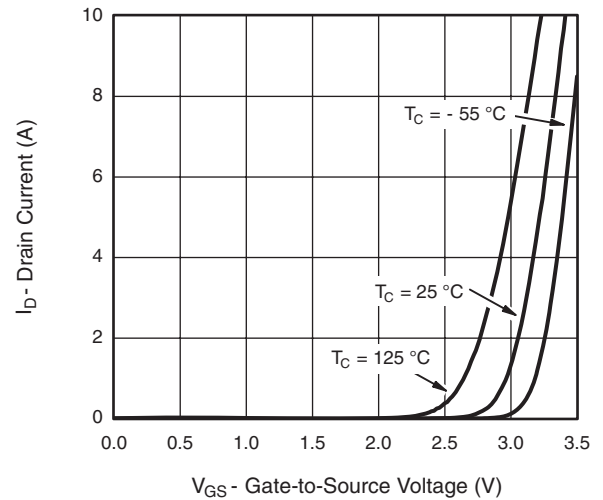
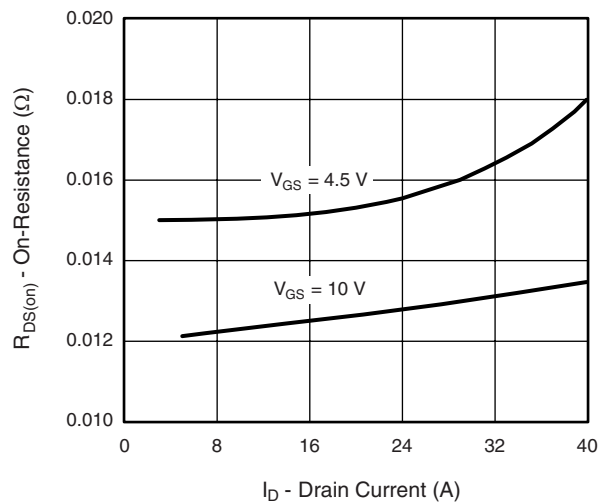
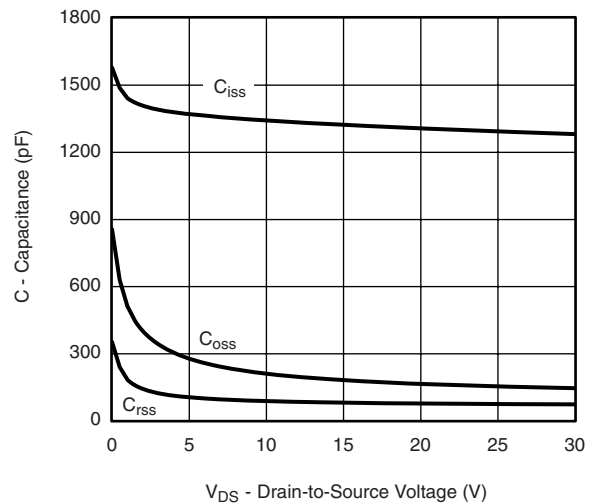
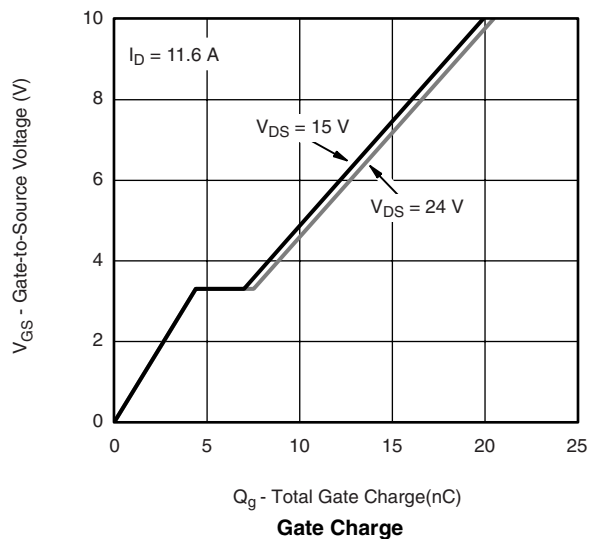
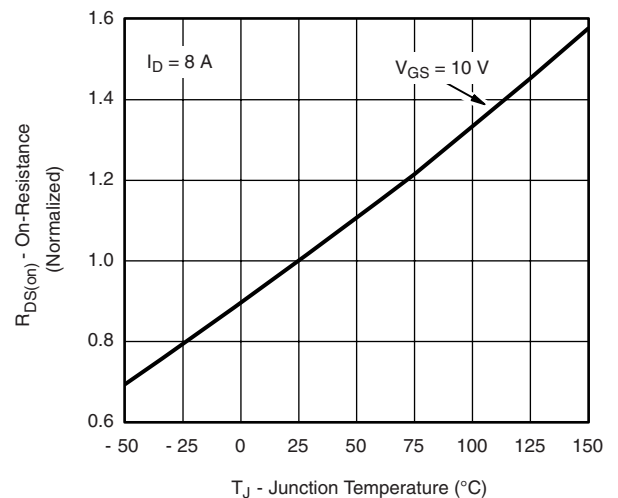
f. Maximum under Steady State conditions is 90°C/W .

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		40		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 7		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2		3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 7.7 A		0.012	0.0145	Ω
		V _{GS} = 4.5 V, I _D = 6.9 A		0.015	0.0185	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 7.7 A		31		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1350		pF
Output Capacitance	C _{oss}			190		
Reverse Transfer Capacitance	C _{rss}			80		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 11.6 A		20	30	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 11.6 A		9.5	15	
Gate-Source Charge	Q _{gs}			4.5		
Gate-Drain Charge	Q _{gd}			2.7		
Gate Resistance	R _g	f = 1 MHz		3.5		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.6 Ω I _D ≅ 9.3 A, V _{GEN} = 4.5 V, R _g = 1 Ω		20	30	ns
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			20	30	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.6 Ω I _D ≅ 9.3 A, V _{GEN} = 10 V, R _g = 1 Ω		10	15	
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			20	30	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			12	A
Pulse Diode Forward Current	I _{SM}				40	
Body Diode Voltage	V _{SD}	I _S = 9.3 A, V _{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 9.3 A, dI/dt = 100 A/μs, T _J = 25 °C		25	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}			19	30	nC
Reverse Recovery Fall Time	t _a			14		ns
Reverse Recovery Rise Time	t _b			11		

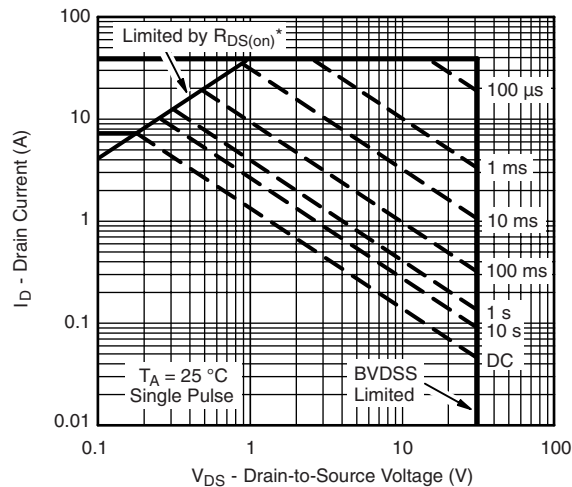
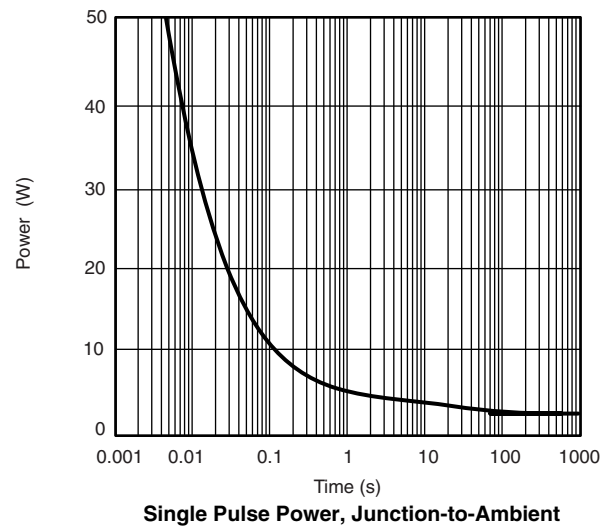
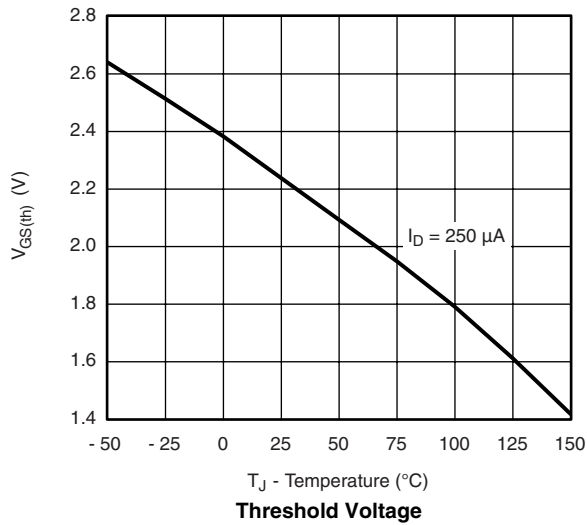
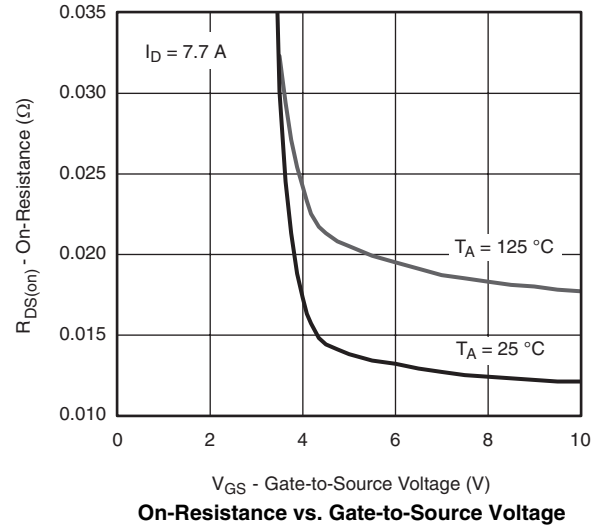
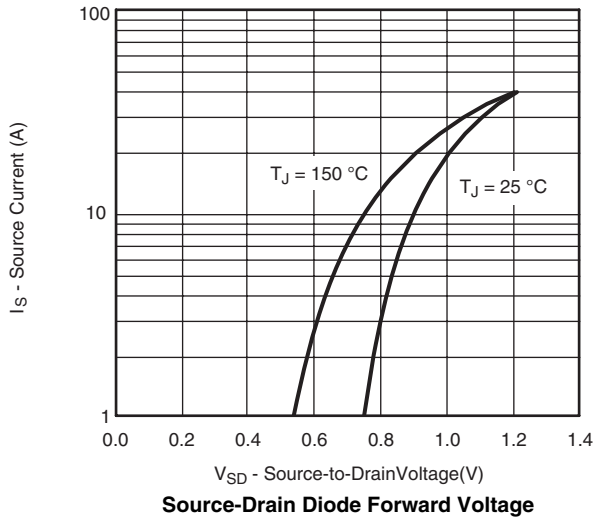
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

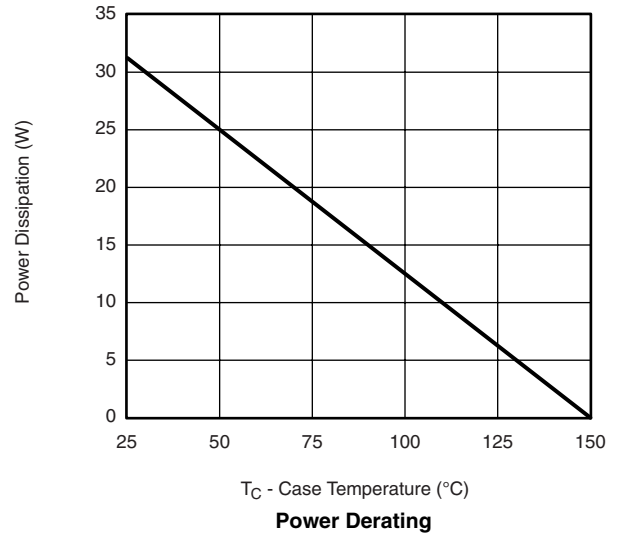
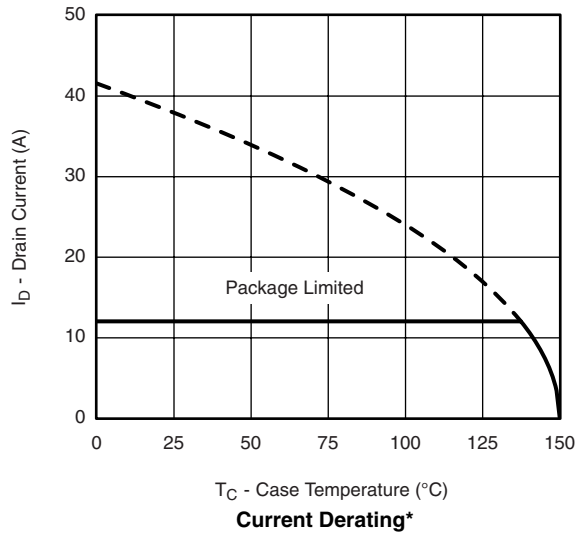


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

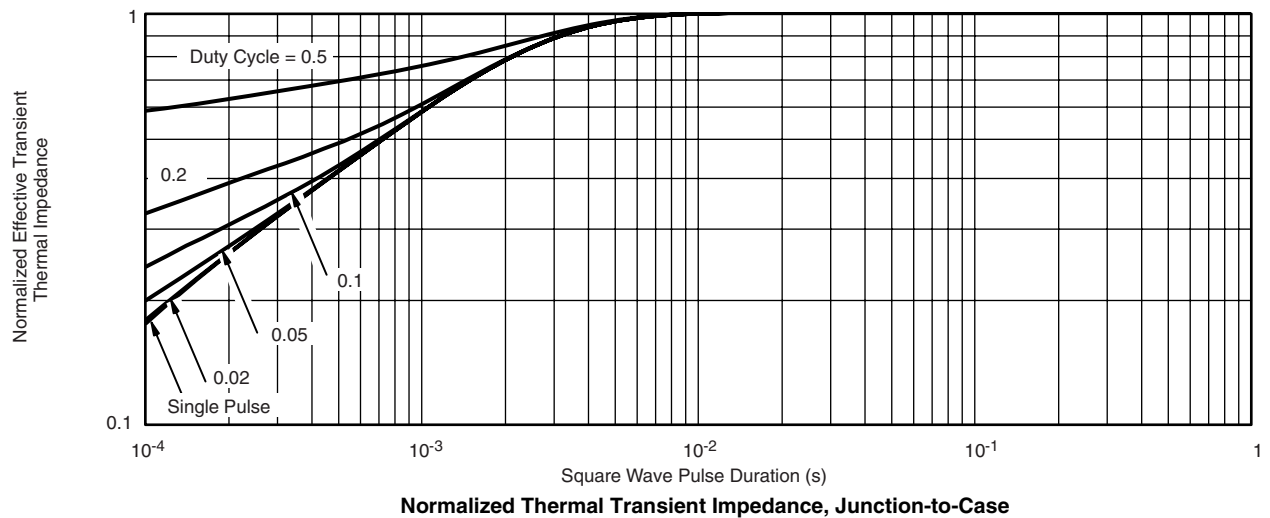
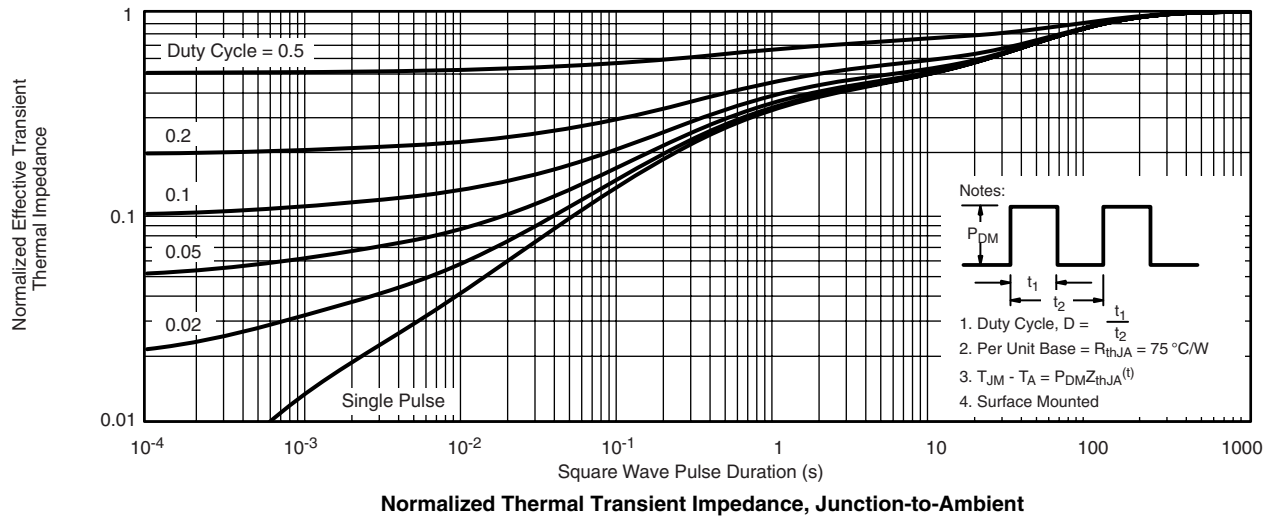
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



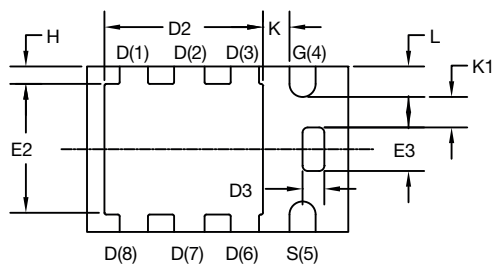
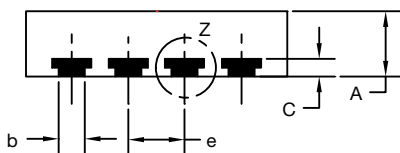
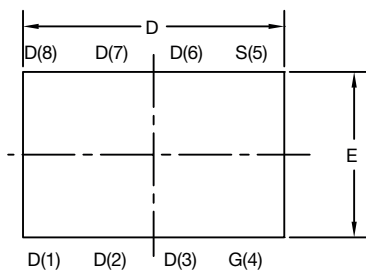
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

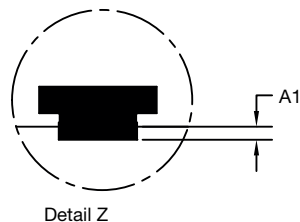
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?69822>.



PowerPAK® ChipFET® Single PAD



Backside view of single pad

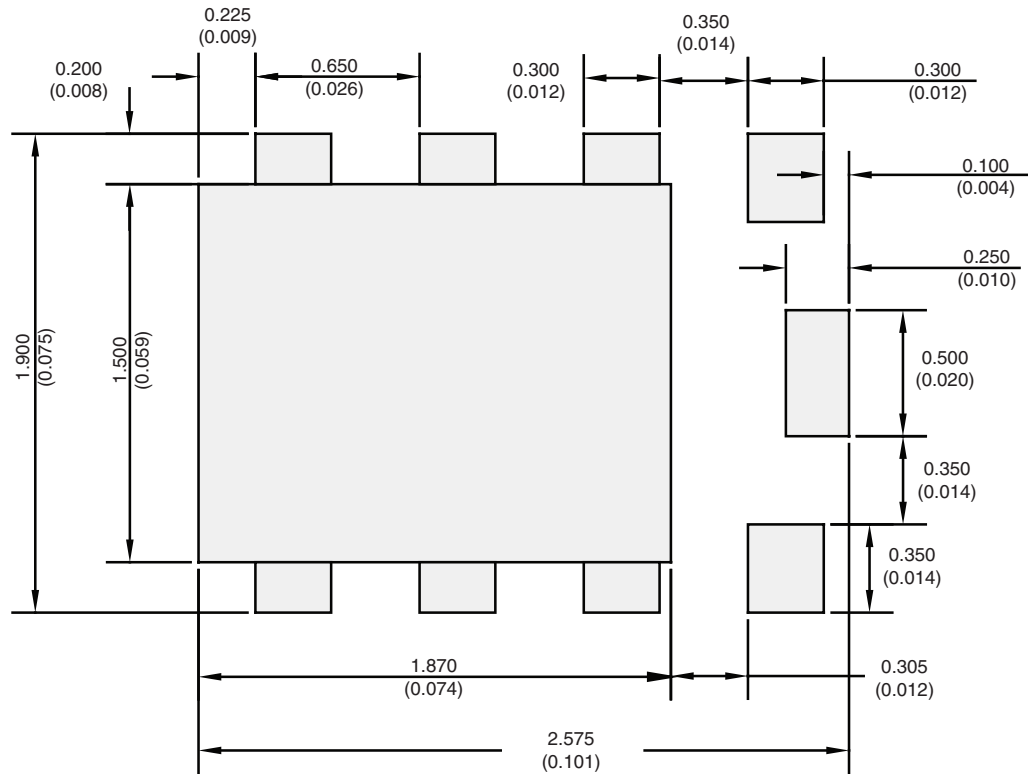


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D2	1.75	1.87	2.00	0.069	0.074	0.079
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E2	1.38	1.50	1.63	0.054	0.059	0.064
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0307-Rev. D, 05-May-14 DWG: 5940						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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