

PMD2001D

MOSFET driver

Rev. 02 — 28 August 2009

Product data sheet

1. Product profile

1.1 General description

NPN/PNP transistor pair connected as push-pull driver in a SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

1.2 Features

- Switching transistors in push-pull configuration
- Application-optimized pinout
- Space-saving solution
- Internal connections to minimize layout effort
- Reduces component count

1.3 Applications

- MOSFET driver
- Power bipolar transistor driver
- Output current booster for operational amplifier

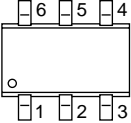
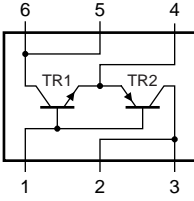
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CEO}	collector-emitter voltage	open base	-	-	40	V
I_C	collector current		-	-	0.6	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	1	A

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	base TR1, TR2		
2	collector TR2		
3	collector TR2		
4	emitter TR1, TR2		
5	collector TR1		
6	collector TR1		

006aaa659

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMD2001D	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PMD2001D	9E

5. Limiting values

Table 5. Limiting values

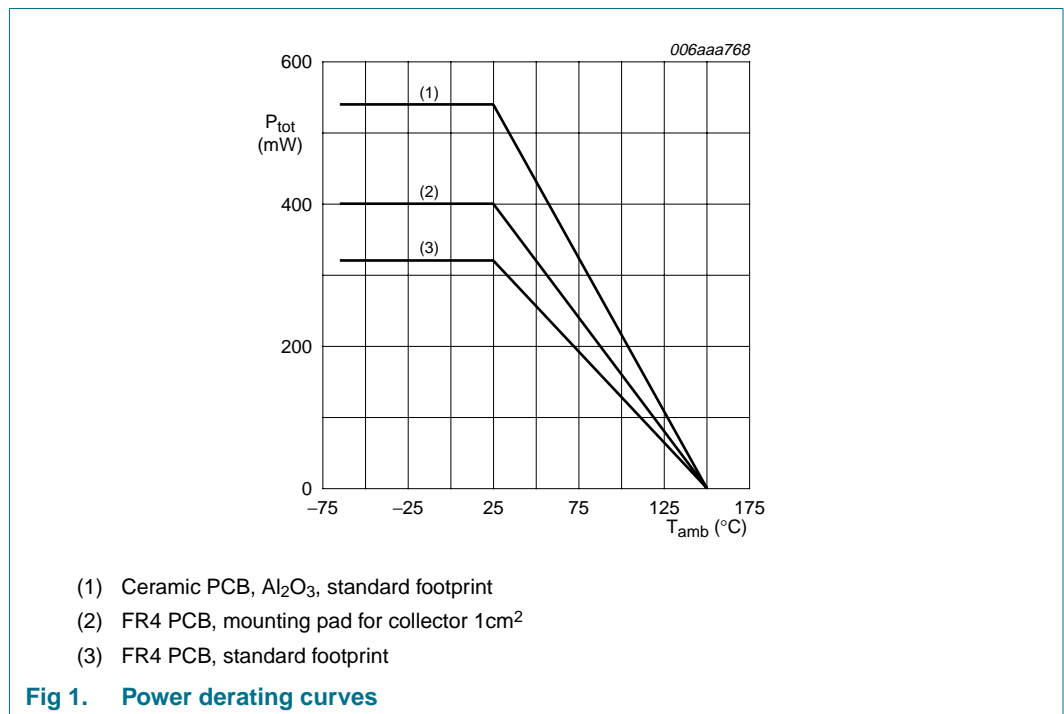
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter	-	40	V	
V_{CEO}	collector-emitter voltage	open base	-	40	V	
I_C	collector current		-	0.6	A	
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	1	A	
I_{BM}	peak base current		-	0.1	A	
		single pulse; $t_p \leq 1$ ms	-	0.2	A	
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	320	mW
			[2]	-	400	mW
			[3]	-	540	mW
T_j	junction temperature		-	150	°C	
T_{amb}	ambient temperature		-65	+150	°C	
T_{stg}	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



6. Thermal characteristics

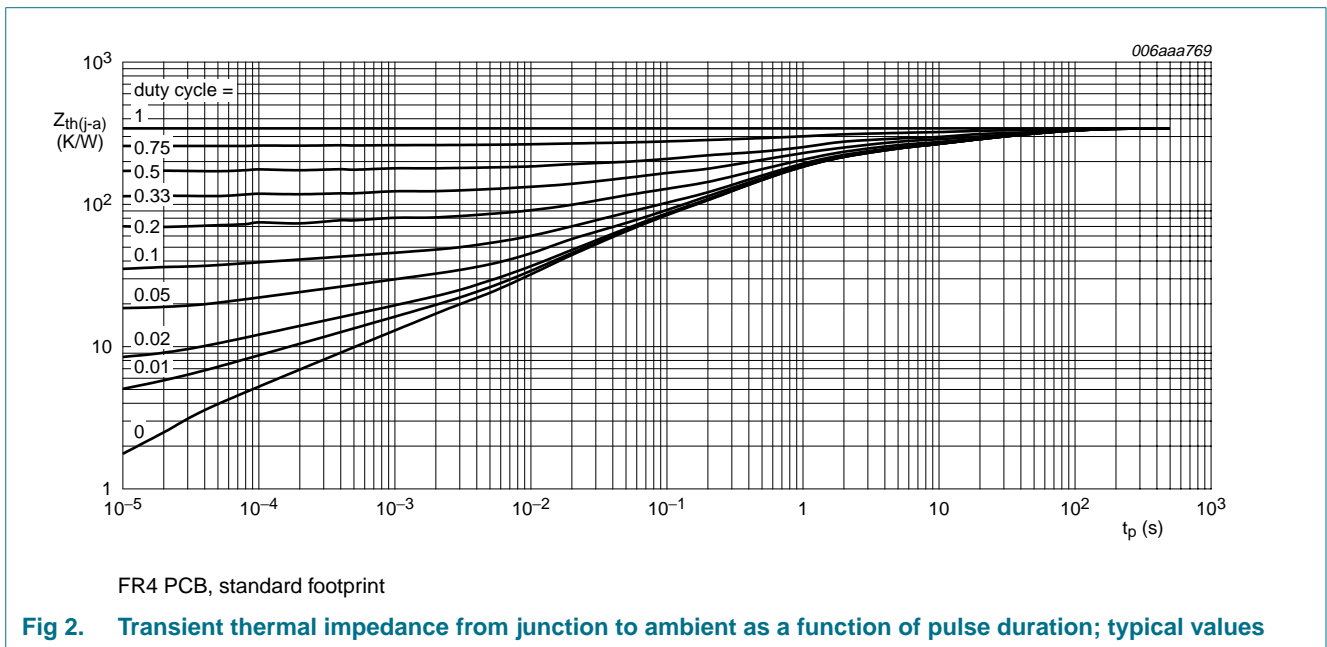
Table 6. Thermal characteristics

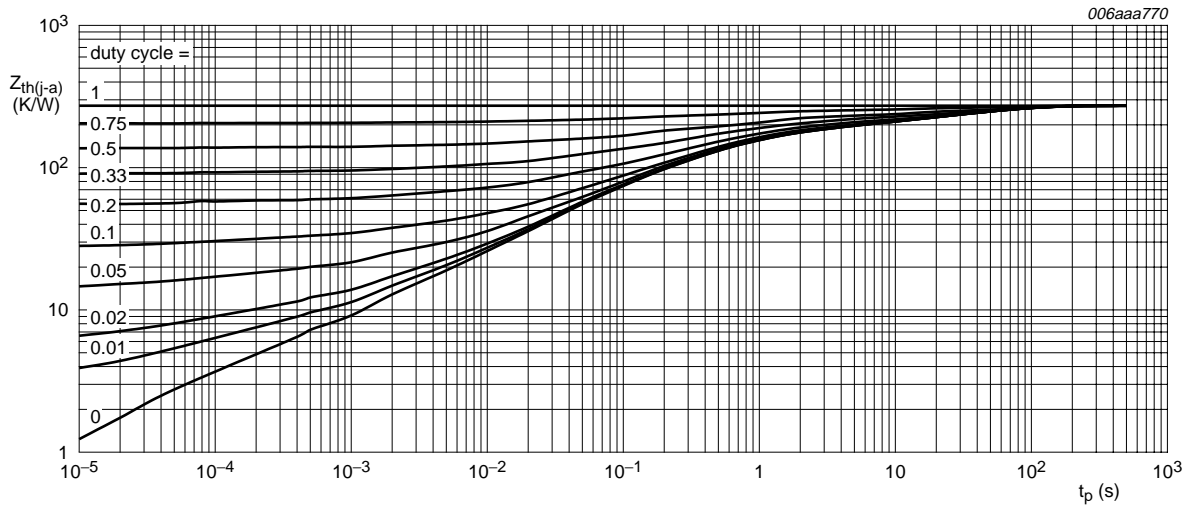
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	390	K/W
			[2]	-	-	315	K/W
			[3]	-	-	230	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1cm².

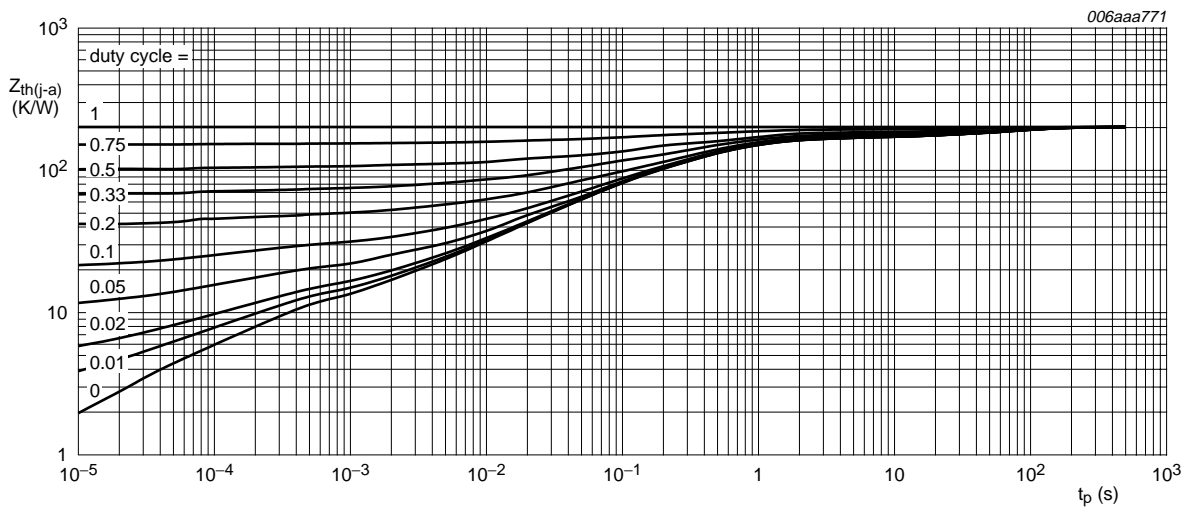
[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.





FR4 PCB, mounting pad for collector 1cm²

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al₂O₃, standard footprint

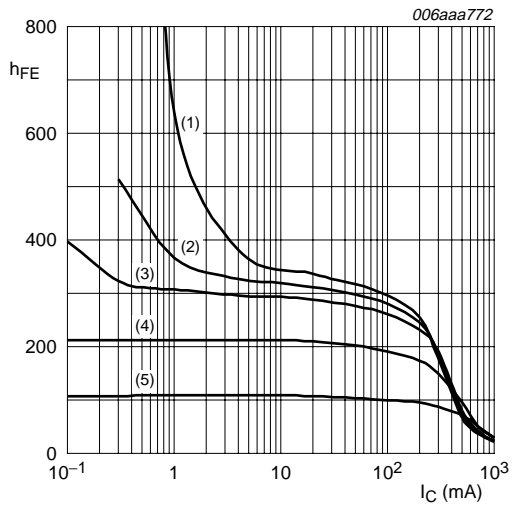
Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

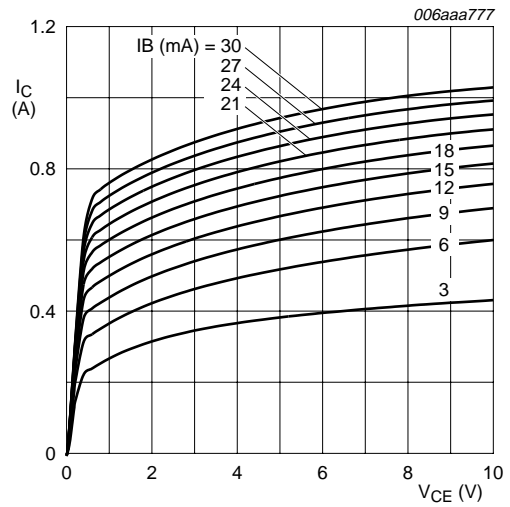
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per NPN transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = 40\text{ V}; I_E = 0\text{ A}$	-	-	10	nA
		$V_{CB} = 40\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	10	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	100	210	-	
		$V_{CE} = 5\text{ V}; I_C = 200\text{ mA}$	100	170	300	
		$V_{CE} = 5\text{ V}; I_C = 500\text{ mA}$	[1] 50	100	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 200\text{ mA}; I_B = 20\text{ mA}$	-	150	250	mV
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	[1] -	300	500	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 200\text{ mA}; I_B = 20\text{ mA}$	-	0.86	1	V
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	[1] -	0.95	1.1	V
Per PNP transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = -40\text{ V}; I_E = 0\text{ A}$	-	-	-10	nA
		$V_{CB} = -40\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	-10	μA
h_{FE}	DC current gain	$V_{CE} = -5\text{ V}; I_C = -1\text{ mA}$	100	180	-	
		$V_{CE} = -5\text{ V}; I_C = -200\text{ mA}$	80	125	300	
		$V_{CE} = -5\text{ V}; I_C = -500\text{ mA}$	[1] 50	80	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -200\text{ mA}; I_B = -20\text{ mA}$	-	-130	-250	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	[1] -	-280	-500	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = -200\text{ mA}; I_B = -20\text{ mA}$	-	-0.87	-1	V
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	[1] -	-0.98	-1.1	V
Per device						
t_d	delay time	$I_C = 0.15\text{ A}; V_I = 7.5\text{ V}$	-	3	-	ns
t_r	rise time		-	3	-	ns
t_{on}	turn-on time		-	6	-	ns
t_s	storage time		-	2	-	ns
t_f	fall time		-	3	-	ns
t_{off}	turn-off time		-	5	-	ns

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$



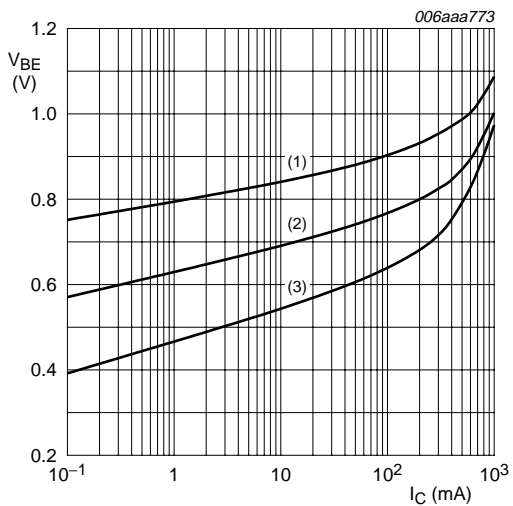
- $V_{CE} = 5\text{ V}$
- (1) $T_{amb} = 150\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 125\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (4) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (5) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 5. TR1 (NPN): DC current gain as a function of collector current; typical values



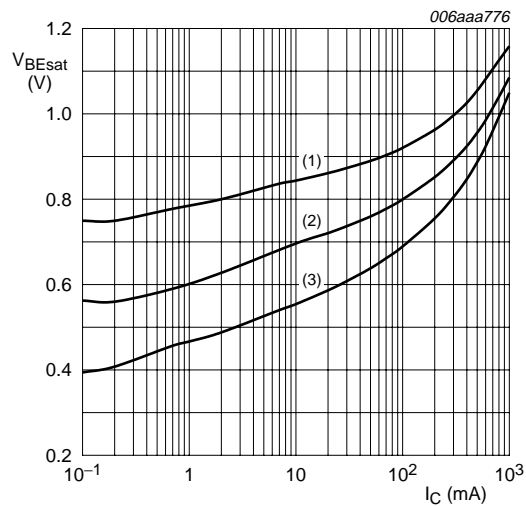
$T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 6. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values



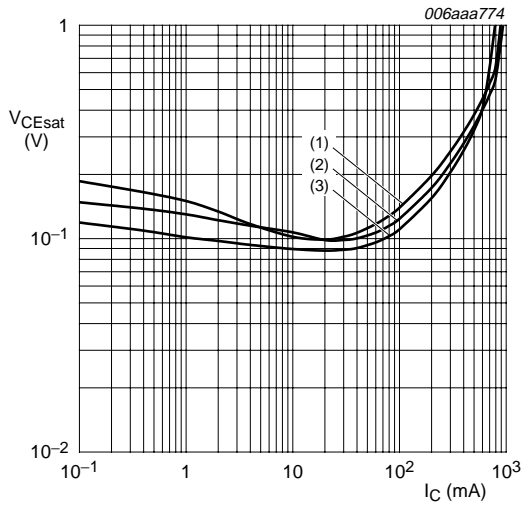
- $V_{CE} = 5\text{ V}$
- (1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 7. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values



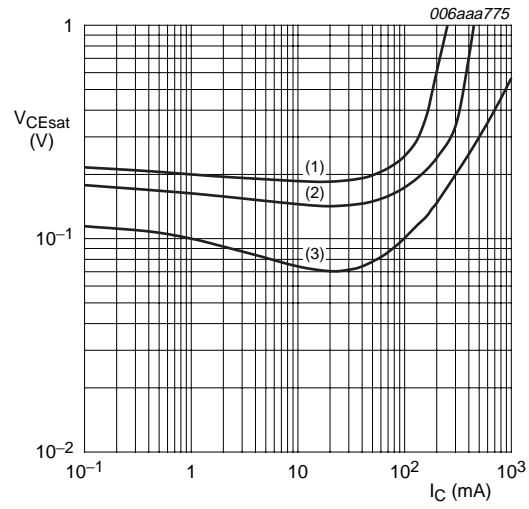
- $I_C/I_B = 20$
- (1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 8. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values



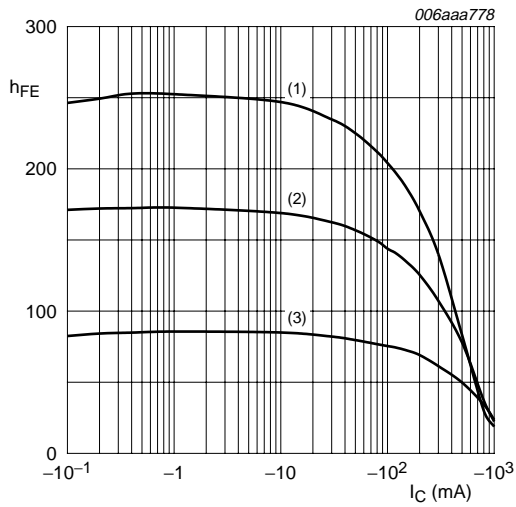
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -55\text{ °C}$

Fig 9. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



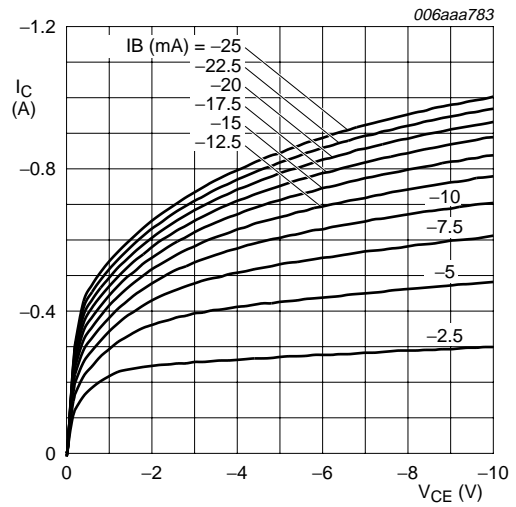
- $T_{amb} = 25\text{ °C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 10. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



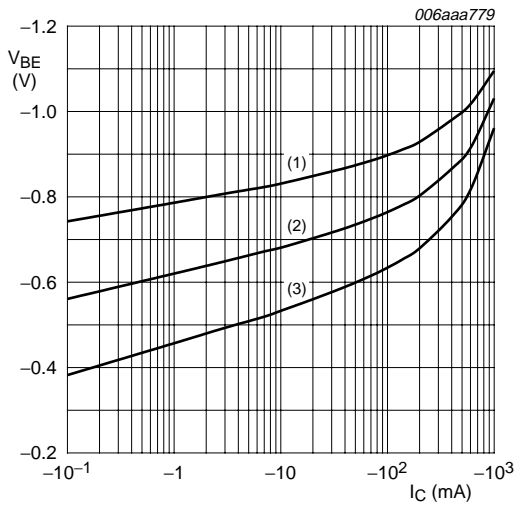
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 11. TR2 (PNP): DC current gain as a function of collector current; typical values



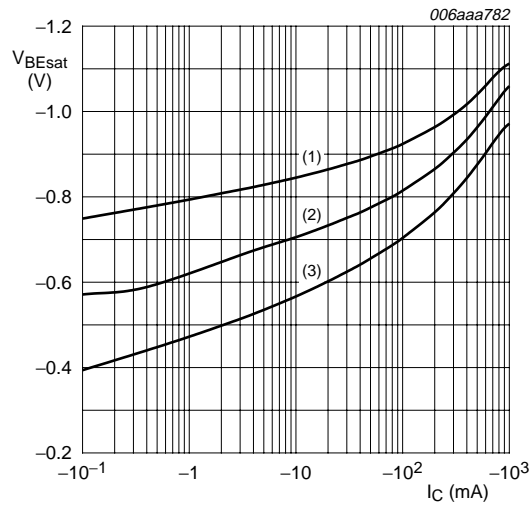
$T_{amb} = 25\text{ °C}$

Fig 12. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values



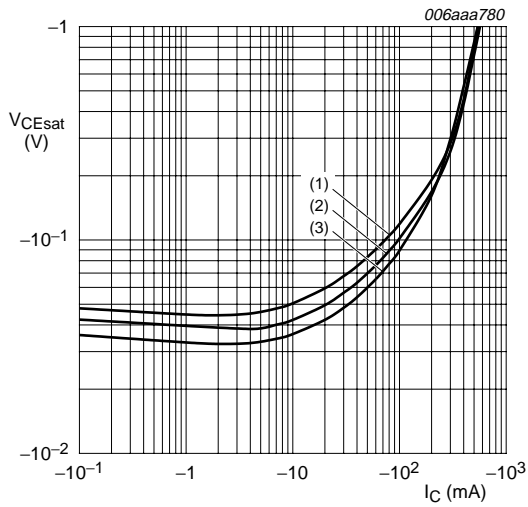
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 13. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values



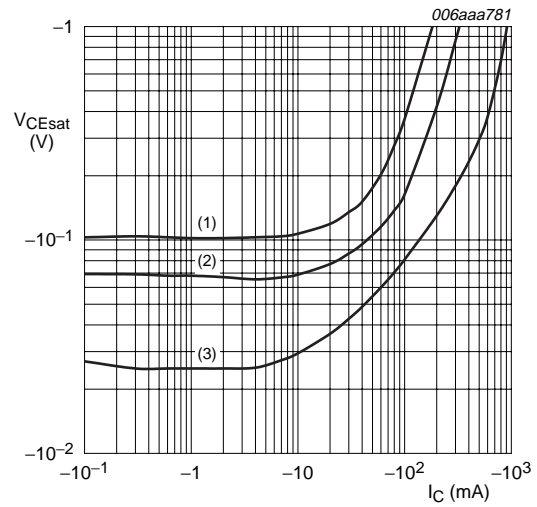
$I_C/I_B = 20$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 14. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

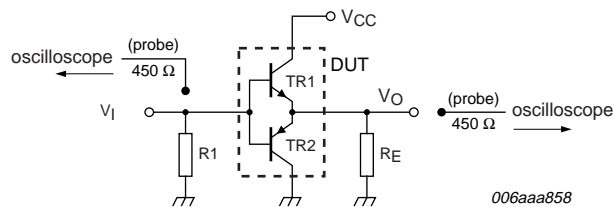
Fig 15. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 16. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

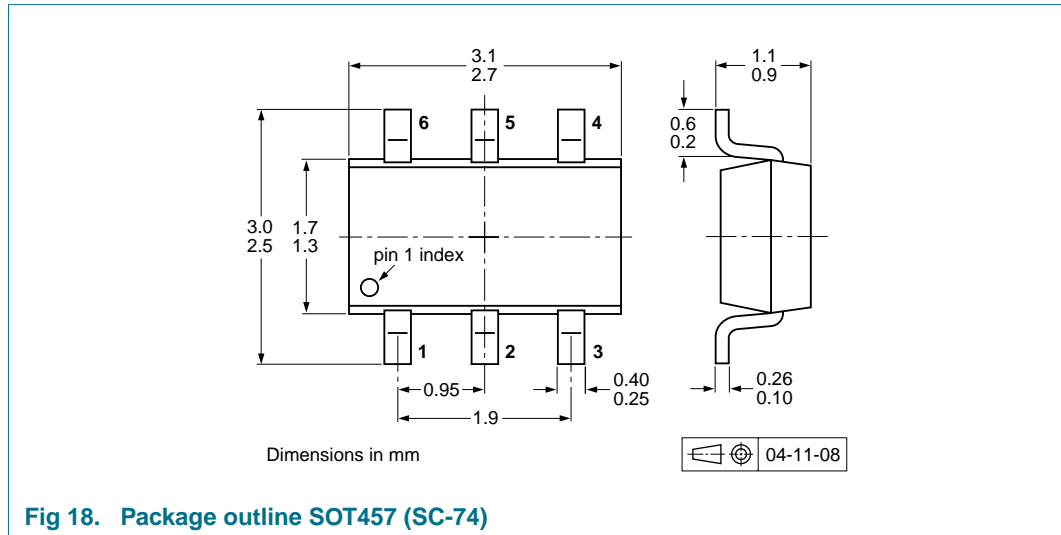
8. Test information



$I_C = 0.15\text{ A}; V_I = 7.5\text{ V}; R_1 = 56\text{ }\Omega; R_E = 47\text{ }\Omega$

Fig 17. Test circuit for switching times

9. Package outline



10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PMD2001D	SOT457	4 mm pitch, 8 mm tape and reel; T1 ^[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2 ^[3]	-125	-165

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering

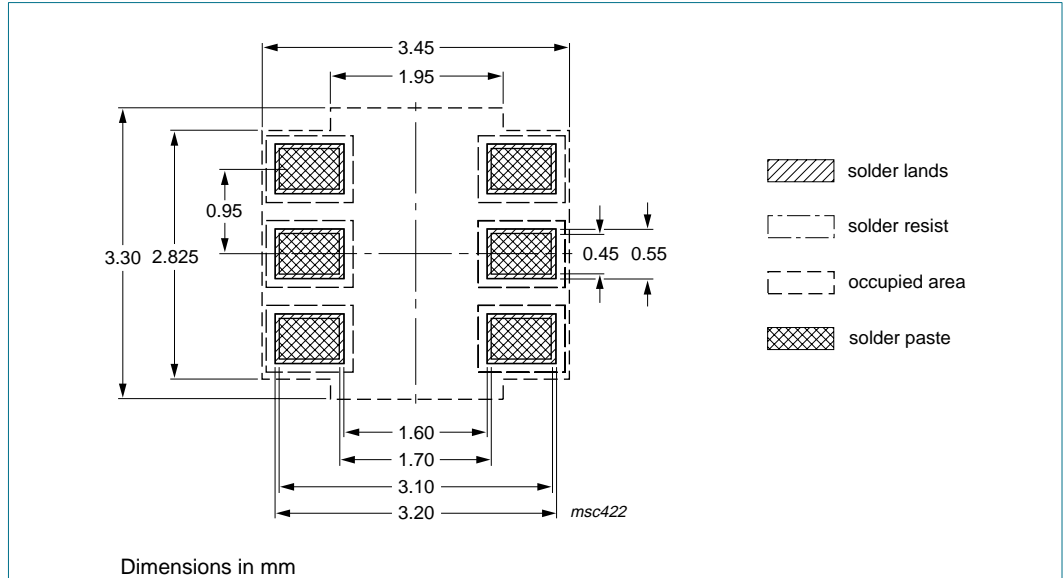


Fig 19. Reflow soldering footprint SOT457 (SC-74)

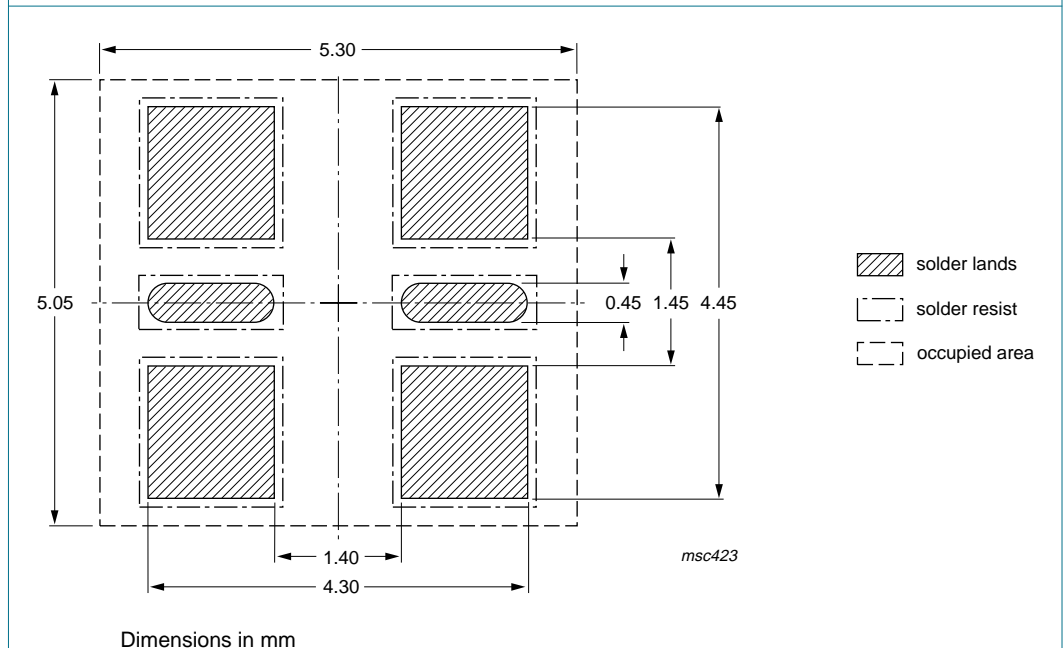


Fig 20. Wave soldering footprint SOT457 (SC-74)

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMD2001D_2	20090828	Product data sheet	-	PMD2001D_1
Modifications:		<ul style="list-style-type: none">This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.Figure 20 "Wave soldering footprint SOT457 (SC-74)": updated		
PMD2001D_1	20060925	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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