June 2014



# **FDA69N25**

# N-Channel UniFET<sup>TM</sup> MOSFET 250 V, 69 A, 41 m $\Omega$

### **Features**

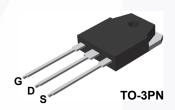
- $R_{DS(on)}$  = 34  $m\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 34.5 A
- Low Gate Charge (Typ. 77 nC)
- Low C<sub>rss</sub> (Typ. 84 pF)

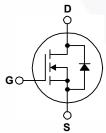
# **Applications**

- PDP TV
- · Uninterruptible Power Supply
- AC-DC Power Supply

# **Description**

UniFET<sup>TM</sup> MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





# **Absolute Maximum Ratings** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter			FDA69N25	Unit
V <sub>DSS</sub>	Drain-Source Voltage			250	V
V <sub>DS(Avalanche)</sub>	Repetitive Avalanche Voltage	(Note 1	, 2)	300	V
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C)		69	Α
		- Continuous (T <sub>C</sub> = 100°C)		44.2	Α
I <sub>DM</sub>	Drain Current	- Pulsed (Note 1)		276	Α
V <sub>GSS</sub>	Gate-Source Voltage			± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy		e 2)	1894	mJ
I <sub>AR</sub>	Avalanche Current		e 1)	69	А
E <sub>AR</sub>	Repetitive Avalanche Energy		e 1)	48	mJ
dv/dt	Peak Diode Recovery dv/dt		e 3)	4.5	V/ns
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C)		480	W
		- Derate above 25°C		3.84	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range			-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering, 1/8" from case for 5 seconds			300	°C

### **Thermal Characteristics**

Symbol	Parameter	FDA69N25	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.26	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDA69N25	FDA69N25	TO-3PN	Tube	N/A	N/A	30 units

# **Electrical Characteristics** $T_C = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	teristics			"		I.
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	250			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.25		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0 V			1	μΑ
		V <sub>DS</sub> = 200 V, T <sub>C</sub> = 125°C			10	μА
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	-		100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Charac	teristics					•
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	3.0		5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 34.5 A		0.034	0.041	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 34.5 A		25		S
Dynamic C	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		3570	4640	pF
C <sub>oss</sub>	Output Capacitance	f = 1 MHz	\	750	980	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			84	130	pF
Switching	Characteristics				1	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 69 A,		95	200	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS}$ = 10 V, $R_G$ = 25 $\Omega$		855	1720	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			130	270	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		220	450	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 200 V, I <sub>D</sub> = 69 A,	/	77	100	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V	-/	24		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)	/	37		nC
Drain-Soul	rce Diode Characteristics and Maximum Rati	ings				
Maximum Continuous Drain-Source Diode Forward Current					34	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				136	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 69 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 69 A,		210		ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F / dt = 100 A/\mu s$		5.7		иС

### Notes

<sup>1.</sup> Repetitive rating : pulse-width limited by maximum junction temperature.

<sup>2.</sup> L = 0.64 mH, I  $_{AS}$  = 69 A, V  $_{DD}$  = 50 V, R  $_{G}$  = 25  $\Omega,$  starting  $\,$  T  $_{J}$  = 25  $^{\circ}C.$ 

<sup>3.</sup>  $I_{SD} \le 69$  A, di/dt  $\le 200$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J = 25^{\circ}C$ 

<sup>4.</sup> Essentially independent of operating temperature typical characteristics.

1. V<sub>DS</sub> = 40V

2. 250µs Pulse Test

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

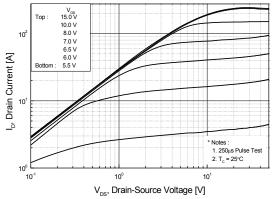


Figure 3. On-Resistance Variation vs. **Drain Current and Gate Voltage** 

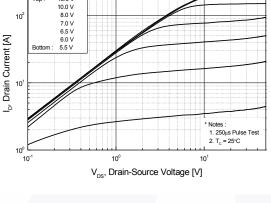
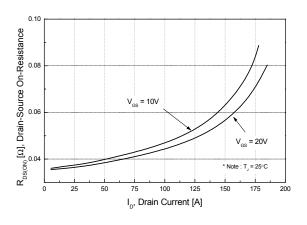


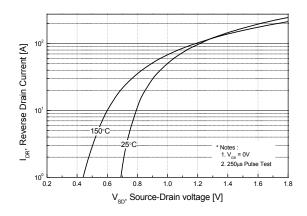


Figure 2. Transfer Characteristics

150°C

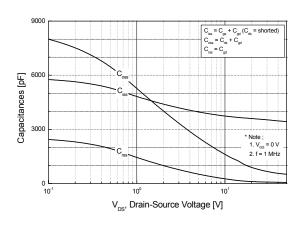
I<sub>D</sub>, Drain Current [A]



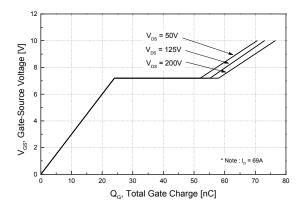


V<sub>GS</sub>, Gate-Source Voltage [V]

Figure 5. Capacitance Characteristics



**Figure 6. Gate Charge Characteristics** 



# Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

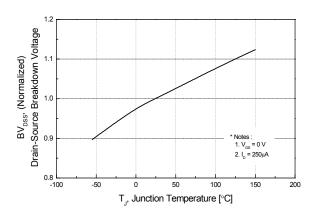


Figure 8. On-Resistance Variation vs. Temperature

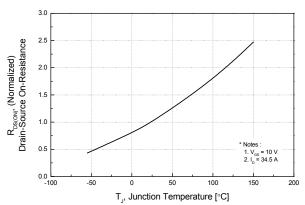
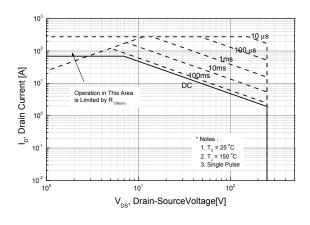


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature



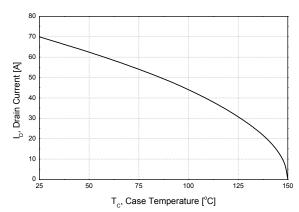
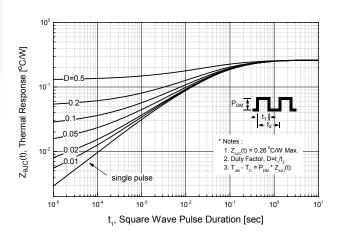


Figure 11. Transient Thermal Response Curve



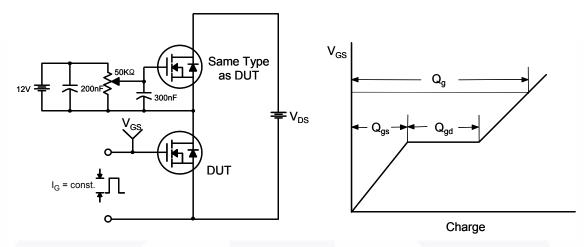


Figure 12. Gate Charge Test Circuit & Waveform

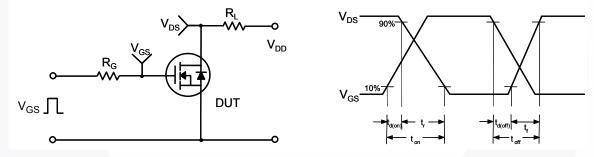


Figure 13. Resistive Switching Test Circuit & Waveforms

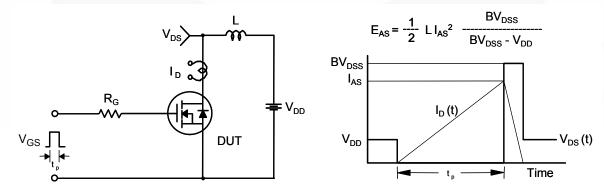


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

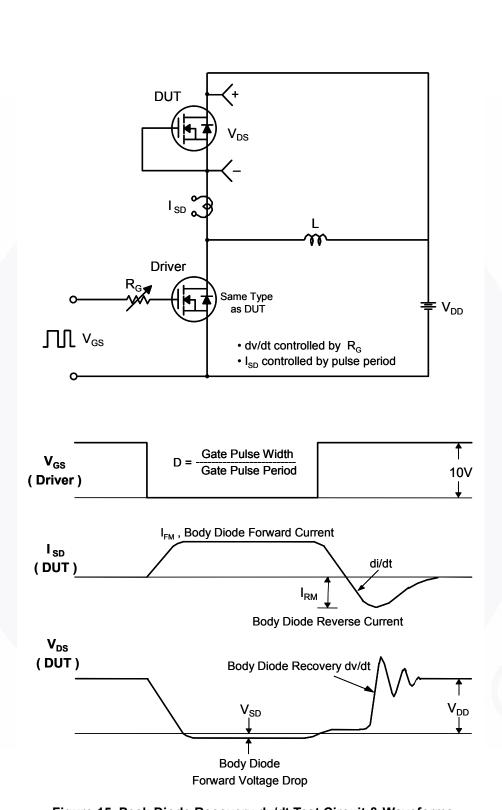
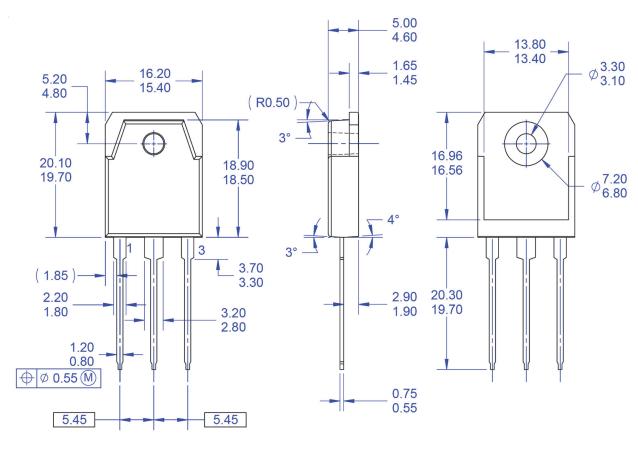
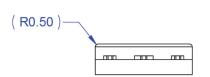


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

### **Mechanical Dimensions**





### NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- ALL DIMENSIONS ARE IN MILLIMETERS. C) DIMENSION AND TOLERANCING PER
- ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.
  DRAWING FILE NAME: TO3PN03AREV1.
  FAIRCHILD SEMICONDUCTOR.

### Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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Rev. 168

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