LM567x Tone Decoder

1 Features

- 20 to 1 Frequency Range With an External Resistor
- Logic Compatible Output With 100-mA Current Sinking Capability
- Bandwidth Adjustable From 0 to 14%
- High Rejection of Out of Band Signals and Noise
- Immunity to False Signals
- Highly Stable Center Frequency
- Center Frequency Adjustable from 0.01 Hz to 500 kHz

2 Applications

- Touch Tone Decoding
- Precision Oscillator
- Frequency Monitoring and Control
- Wide Band FSK Demodulation
- Ultrasonic Controls
- Carrier Current Remote Controls
- Communications Paging Decoders

3 Description

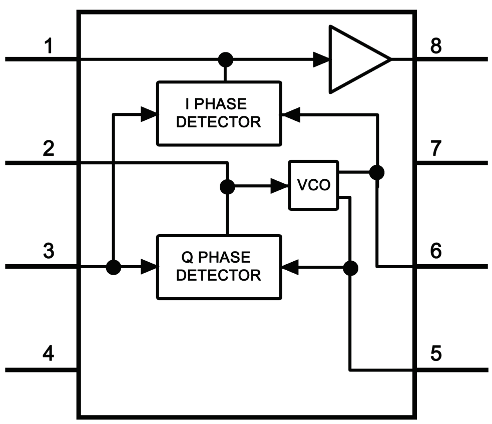
The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM567C	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	9

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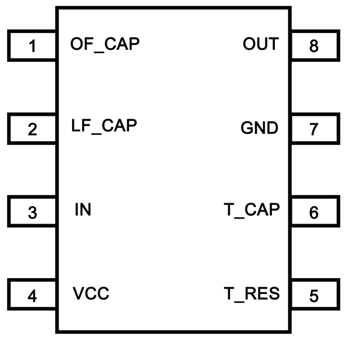
6 Device Comparison Table

DEVICE NAME	DESCRIPTION
LM567, LM567C	General Purpose Tone Decoder
LMC567	Same as LM567C, but lower power supply current consumption and double oscillator frequency

7 Pin Configuration and Functions

8-Pin
PDIP (P) and SOIC (D) Package
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	7	P	Circuit ground.
IN	3	I	Device input.
LF_CAP	2	I	Loop filter capacitor pin (LPF of the PLL).
OUT	8	O	Device output.
OF_CAP	1	I	Output filter capacitor pin.
T_CAP	5	I	Timing capacitor connection pin.
T_RES	6	I	Timing resistor connection pin.
VCC	4	P	Voltage supply pin.

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8 Specifications

8.1 Absolute Maximum Ratings[1][2][3]

			MIN	MAX	UNIT
Supply Voltage Pin				9	V
Power Dissipation[4]				1100	mW
V_8				15	V
V_3				−10	V
V_3				$V_4 + 0.5$	V
Operating Temperature Range	LM567CM, LM567CN		0	70	°C
	PDIP Package	Soldering (10 s)		260	°C
	SOIC Package	Vapor Phase (60 s)		215	°C
		Infrared (15 s)		220	°C
Storage temperature range, T_{stg}			−65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Recommended Operating Conditions. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) See http://www.ti.com for other methods of soldering surface mount devices.
(4) The maximum junction temperature of the LM567 and LM567C is 150°C. For operating at elevated temperatures, devices in the DIP package must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the SOIC package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

8.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	3.5	8.5	V
V_{IN}	Input Voltage Level	–8.5	8.5	V
T_A	Operating Temperature Range	–20	120	°C

8.3 Thermal Information

THERMAL METRIC[1]		LM567C D	LM567C P	UNIT
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.5	53.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.6	42.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	30.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.0	19.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.0	30.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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8.4 Electrical Characteristics

AC Test Circuit, T_A = 25°C, V^+ = 5 V

PARAMETER	TEST CONDITIONS	LM567			LM567C/LM567CM			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	8		7	10	mA
Power Supply Current Activated	R_L = 20k		11	13		12	15	mA
Input Resistance		18	20		15	20		kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1			±0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75 – 6.75 V		±1	±2		±1	±5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability (4.75 – 5.75 V)	$0 < T_A < 70$ $-55 < T_A < +125$		35 ± 60 35 ± 140			35 ± 60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75 V – 6.75 V 4.75 V – 9 V		0.5	1.0 2.0		0.4	2.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15 V		0.01	25		0.01	25	µA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA e_i = 25 mV, I_8 = 100 mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

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8.5 Typical Characteristics

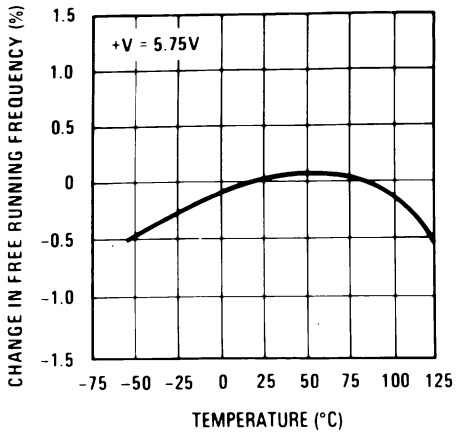

Figure 1. Typical Frequency Drift

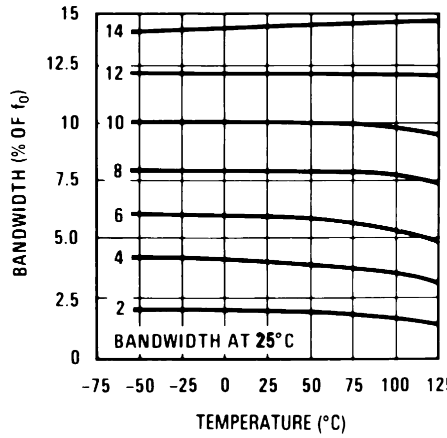

Figure 2. Typical Bandwidth Variation

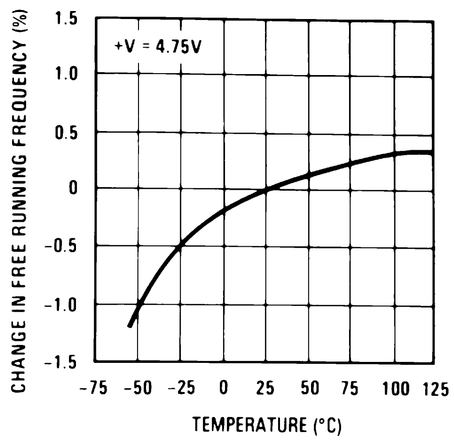

Figure 3. Typical Frequency Drift

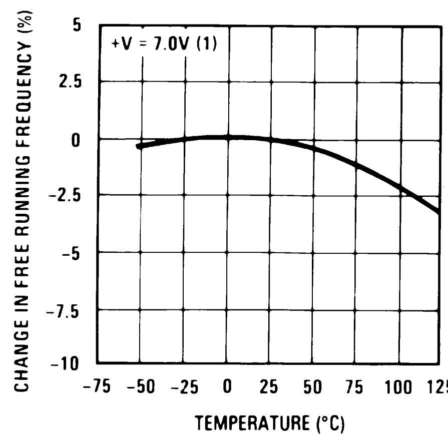

Figure 4. Typical Frequency Drift

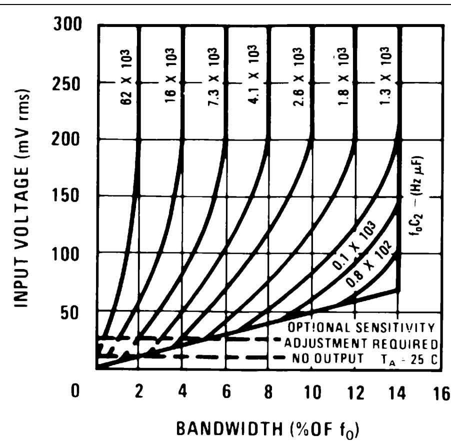

Figure 5. Bandwidth vs Input Signal Amplitude

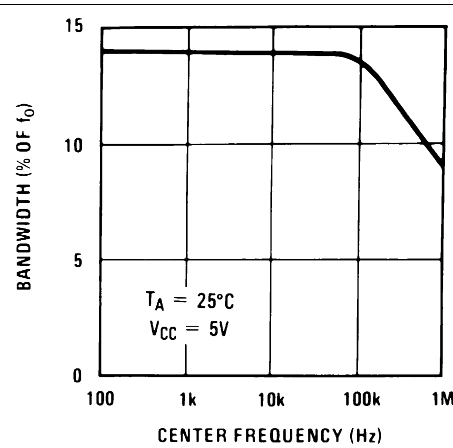

Figure 6. Largest Detection Bandwidth

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Typical Characteristics (continued)

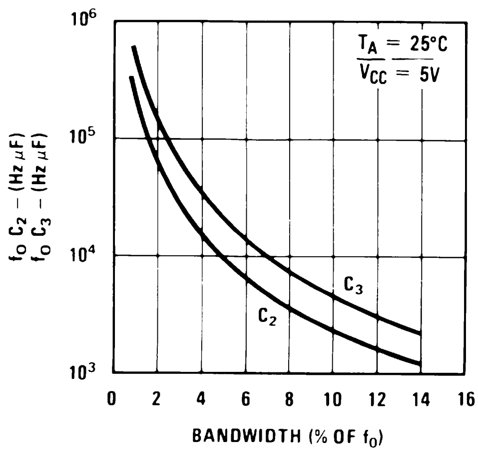


Figure 7. Detection Bandwidth as a Function of C_2 and C_3

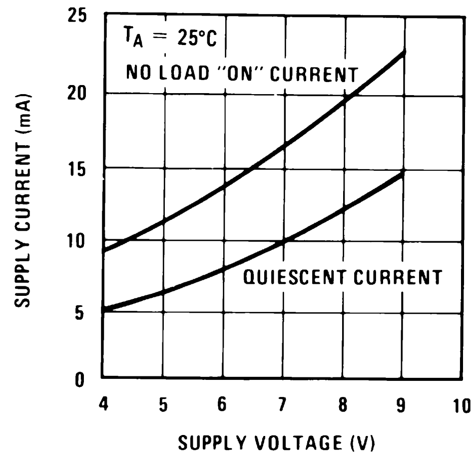


Figure 8. Typical Supply Current vs Supply Voltage

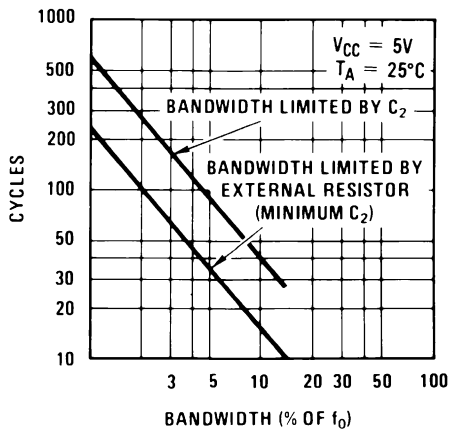


Figure 9. Greatest Number of Cycles Before Output

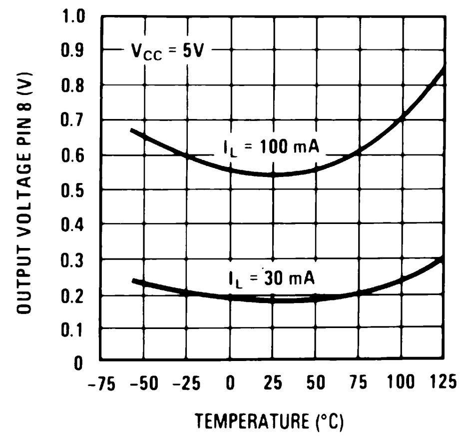


Figure 10. Typical Output Voltage vs Temperature

9 Parameter Measurement Information

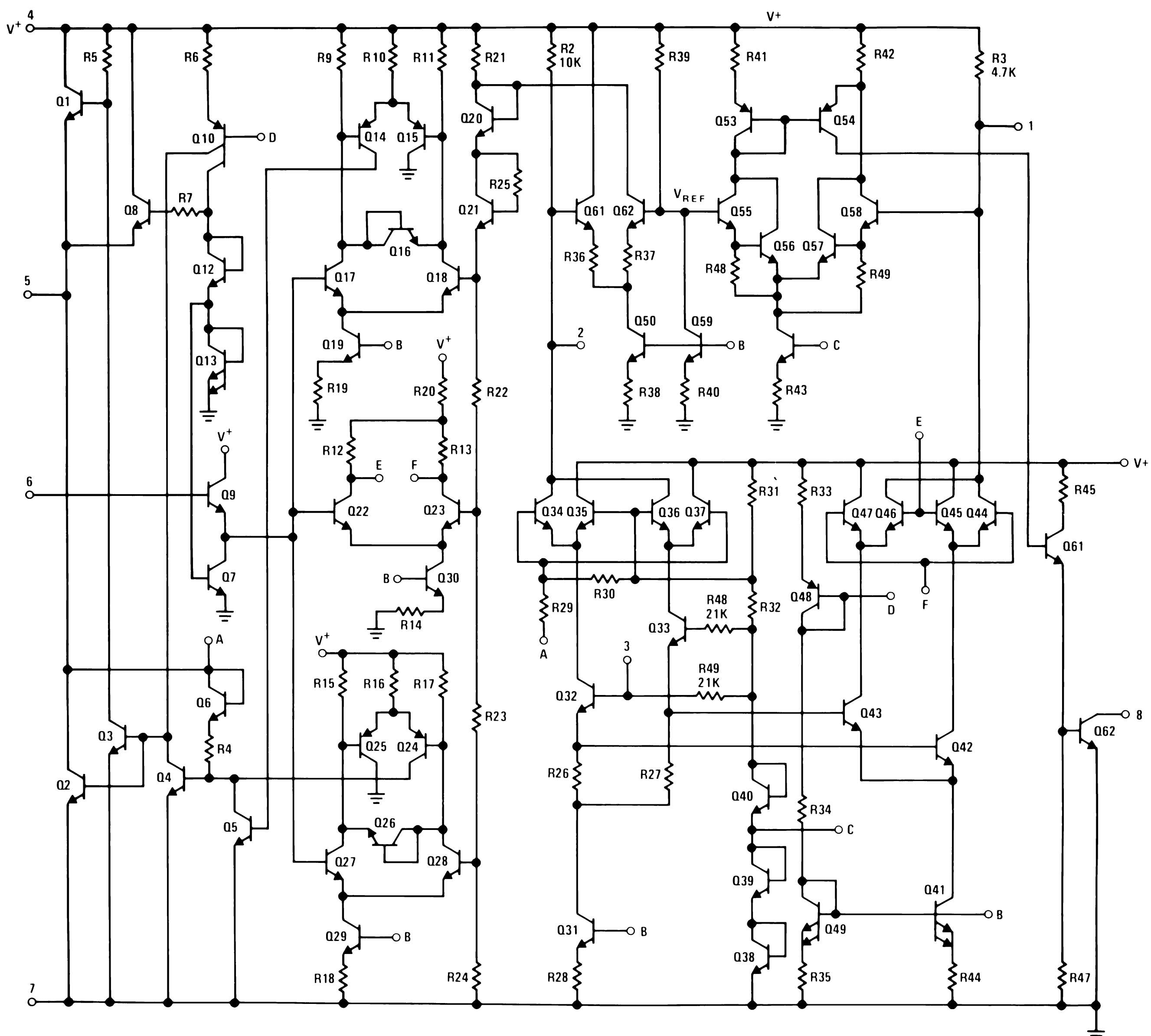
All parameters are measured according to the conditions described in the *Specifications* section.

10 Detailed Description

10.1 Overview

The LM567C is a general purpose tone decoder. The circuit consists of I and Q detectors driven by a voltage controlled oscillator which determines the center frequency of the decoder. This device is designed to provide a transistor switch to ground output when the input signal frequency matches the center frequency pass band. Center frequency is set by an external timing circuit composed by a capacitor and a resistor. Bandwidth and output delay are set by external capacitors.

10.2 Functional Block Diagram



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10.3 Feature Description

10.3.1 Center Frequency

The center frequency of the LM567 tone decoder is equal to the free running frequency of the voltage controlled oscillator. In order to set this frequency, external components should be placed externally. The component values are given by:

$$f_o \approx \frac{1.1}{R_1 C_1}$$

where

- R_1 = Timing Resistor
- C_1 = Timing Capacitor (1)

10.3.2 Output Filter

To eliminate undesired signals that could trigger the output stage, a post detection filter is featured in the LM567C. This filter consists of an internal resistor (4.7K-Ω) and an external capacitor. Although typically external capacitor value is not critical, it is recommended to be at least twice the value of the loop filter capacitor. If the output filter capacitor value is too large, the turn-on and turn off-time of the output will present a delay until the voltage across this capacitor reaches the threshold level.

10.3.3 Loop Filter

The phase locked loop (PLL) included in the LM567 has a pin for connecting the low pass loop filter capacitor. The selection of the capacitor for the filter depends on the desired bandwidth. The device bandwidth selection is different according to the input voltage level. Refer to the *Operation With V_i < 200m – V_{RMS}* section and the *Operation With V_i > 200m – V_{RMS}* section for more information about the loop filter capacitor selection.

10.3.4 Logic Output

The LM567 is designed to provide a transistor switch to ground output when the input signal frequency matches the center frequency pass band. The logic output is an open collector power transistor that requires an external load resistor that is used to regulate the output current level.

10.3.5 Die Characteristics

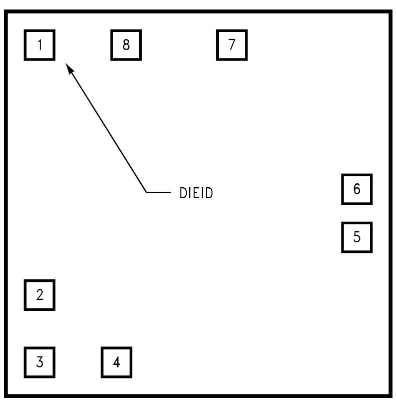

Figure 11. Die Layout (C - Step)

Feature Description (continued)

Table 1. Die and Wafer Characteristics

Fabrication Attributes		General Die Information	
Physical Die Identification	LM567C	Bond Pad Opening Size (min)	91µm x 91µm
Die Step	C	Bond Pad Metalization	0.5% COPPER_BAL. ALUMINUM
Physical Attributes		Passivation	VOM NITRIDE
Wafer Diameter	150mm	Back Side Metal	BARE BACK
Dise Size (Drawn)	1600µm x 1626µm 63.0mils x 64.0mils	Back Side Connection	Floating
Thickness	406µm Nominal		
Min Pitch	198µm Nominal		
Special Assembly Requirements:			
Note: Actual die size is rounded to the nearest micron.			

Die Bond Pad Coordinate Locations (C - Step)						
(Referenced to die center, coordinates in µm) NC = No Connection, N.U. = Not Used						
SIGNAL NAME	PAD# NUMBER	X/Y COORDINATES		PAD SIZE		
		X	Y	X		Y
OUTPUT FILTER	1	-673	686	91	x	91
LOOP FILTER	2	-673	-419	91	x	91
INPUT	3	-673	-686	91	x	91
V+	4	-356	-686	91	x	91
TIMING RES	5	673	-122	91	x	91
TIMING CAP	6	673	76	91	x	91
GND	7	178	686	117	x	91
OUTPUT	8	-318	679	117	x	104

10.4 Device Functional Modes

10.4.1 Operation With V_i < 200m – V_{RMS}

When the input signal is below a threshold voltage, typically 200m-VRMS, the bandwidth of the detection band should be calculated .

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o$$

where

- V_i = Input voltage (volts rms), $V_i \le 200mV$
- C_2 = Capacitance at Pin 2(µF)

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Device Functional Modes (continued)

10.4.2 Operation With V_i > 200m – V_{RMS}

For input voltages greater than 200m-VRMS, the bandwidth depends directly from the loop filter capacitance and free running frequency product. Bandwidth is represented as a percentage of the free running frequency, and according to the product of f0·C2, it can have a variation from 2 to 14%. Table 2 shows the approximate values for bandwidth in function of the product result.

Table 2. Detection Bandwidth in Function of $f_o \times C_2$

$f_o \times C_2$ (kHzµF)	Bandwidth (% of f_o)
62	2
16	4
7.3	6
4.1	8
2.6	10
1.8	12
1.3	14
< 1.3	14

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The LM567 tone decoder is a device capable of detecting if an input signal is inside a selectable range of detection. The device has an open collector transistor output, so an external resistor is required to achieve proper logic levels. When the input signal is inside the detection band, the device output will go to a LOW state. The internal VCO free running frequency establishes the detection band central frequency. An external RC filter is required to set this frequency. The bandwidth in which the device will detect the desired frequency depends on the capacitance of loop filter terminal. Typically a 1µF capacitor is connected to this pin. The device detection band has a different behavior for low and high input voltage levels. Refer to the *Operation With $V_i < 200m - V_{RMS}$* section and the *Operation With $V_i > 200m - V_{RMS}$* section for more information.

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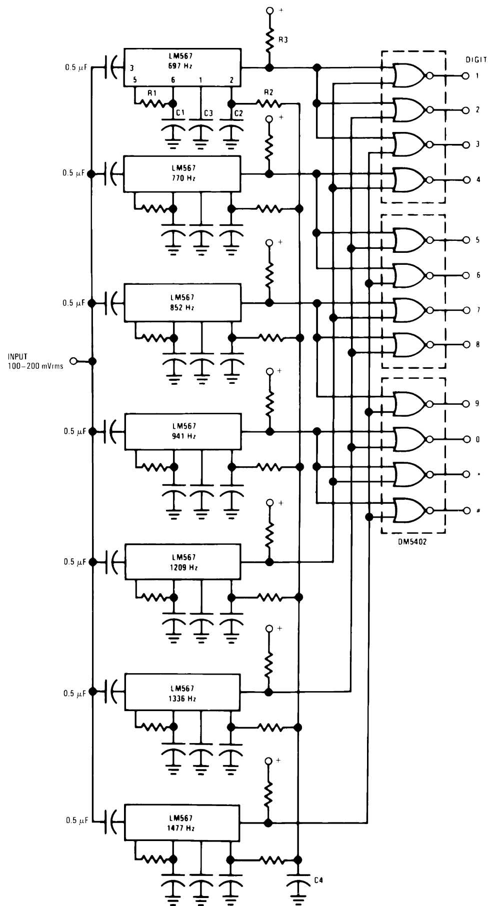
11.2 Typical Applications

11.2.1 Touch-Tone Decoder



Component values (typ)
R1 6.8 to 15k
R2 4.7k
R3 20k
C1 0.10 mfd
C2 1.0 mfd 6V
C3 2.2 mfd 6V
C4 250 mfd 6V

Figure 12. Touch-Tone Decoder

11.2.1.1 Design Requirements

PARAMETERS	VALUES
Supply Voltage Range	3.5 V to 8.5 V
Input Voltage Range	20 mV_{RMS} to VCC + 0.5
Input Frequency	1 Hz to 500 kHz
Output Current	Max. 15 mA

11.2.1.2 Detailed Design Procedure

11.2.1.2.1 Timing Components

To calculate the timing components for an approximated desired central detection frequency (f_0), the timing capacitor value (C_1) should be stated in order to calculate the timing resistor value (R_1). Typically for most applications, a 0.1-µF capacitor is used.

$$f_o \approx \frac{1.1}{R_1 C_1} \tag{2}$$

11.2.1.2.2 Bandwidth

Detection bandwidth is represented as a percentage of f0. It can be selected based on the input voltage levels (Vi). For Vi < 200 mV_{RMS},

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o \tag{3}$$

For Vi > 200 mV_{RMS}, refer to Table 2 or Figure 5.

11.2.1.2.3 Output Filter

The output filter selection is made considering the capacitor value to be at least twice the Loop filter capacitor.

$$C_3 \geq 2C_2 \tag{4}$$

11.2.1.3 Application Curve

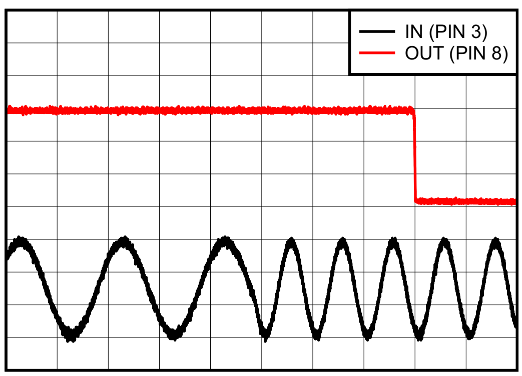


Figure 13. Frequency Detection

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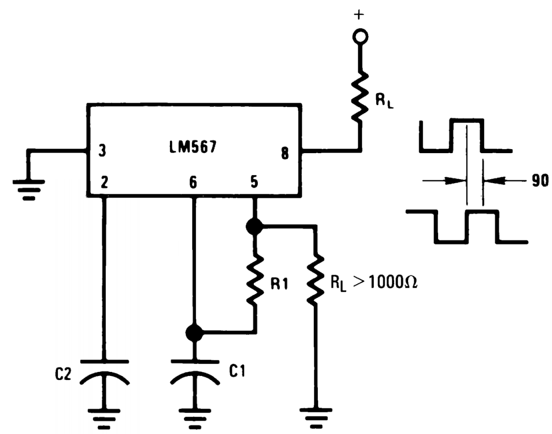
11.2.2 Oscillator with Quadrature Output



Connect Pin 3 to 2.8V to Invert Output

Figure 14. Oscillator with Quadrature Output

11.2.2.1 Design Requirements

Refer to the previous *Design Requirements* section.

11.2.2.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

11.2.2.3 Application Curve

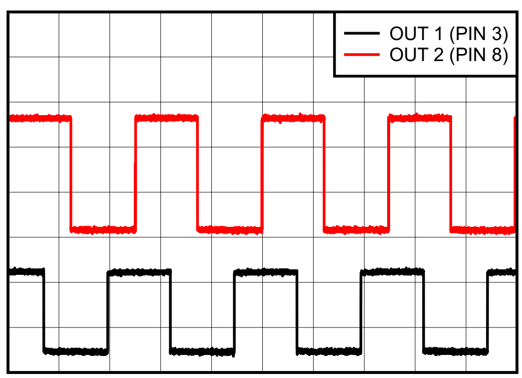


Figure 15. Quadrature Output

11.2.3 Oscillator with Double Frequency Output

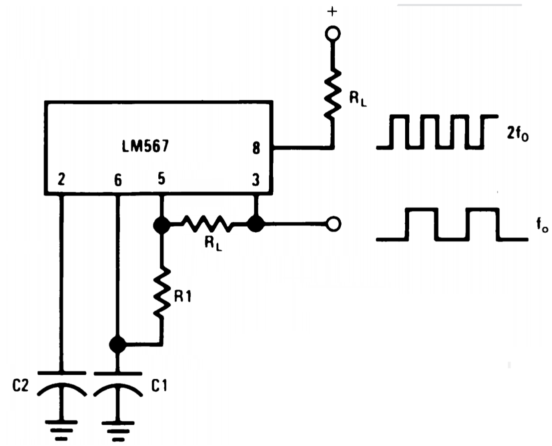


Figure 16. Oscillator with Double Frequency Output

11.2.3.1 Design Requirements

Refer to the previous *Design Requirements* section.

11.2.3.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

11.2.3.3 Application Curve

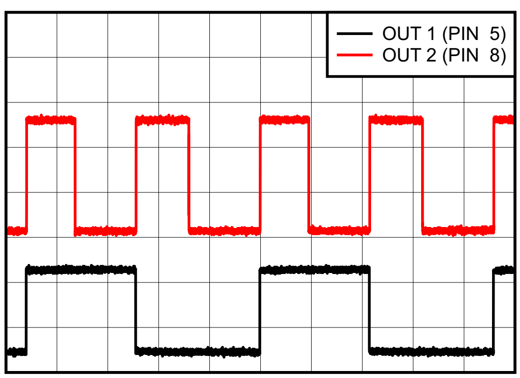


Figure 17. Double Frequency Output

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11.2.4 Precision Oscillator Drive 100-mA Loads

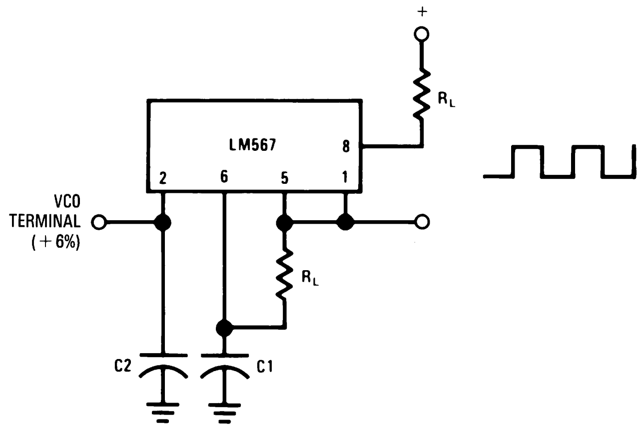


Figure 18. Precision Oscillator Drive 100-mA Loads

11.2.4.1 Design Requirements

Refer to the previous *Design Requirements* section.

11.2.4.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

11.2.4.3 Application Curve

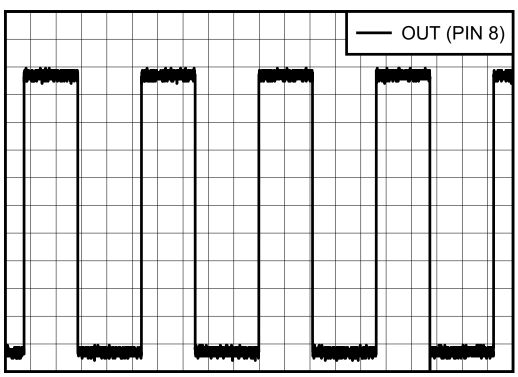
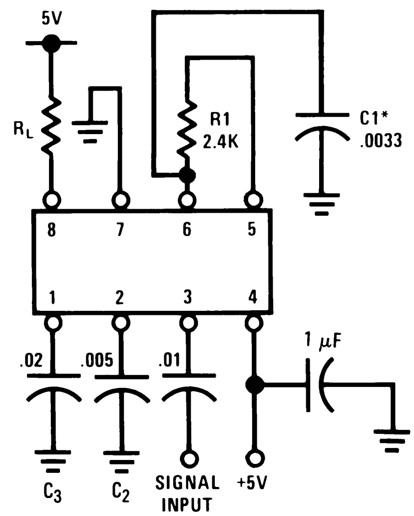


Figure 19. Output for 100-mA Load

11.2.5 AC Test Circuit



f_i = 100 kHz + 5 V
***Note:** Adjust for f_o = 100 kHz.

11.2.5.1 Design Requirements

Refer to the previous *Design Requirements* section.

11.2.5.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

11.2.5.3 Application Curve

Refer to the previous *Application Curve* section.

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12 Power Supply Recommendations

The LM567C is designed to operate with a power supply up to 9 V. It is recommended to have a well regulated power supply. As the operating frequency of the device could be very high for some applications, the decoupling of power supply becomes critical, so is required to place a proper decoupling capacitor as close as possible to VCC pin.

13 Layout

13.1 Layout Guidelines

The VCC pin of the LM567 should be decoupled to ground plane as the device can work with high switching speeds. The decoupling capacitor should be placed as close as possible to the device. Traces length for the timing and external filter components should be kept at minimum in order to avoid any possible interference from other close traces.

13.2 Layout Example

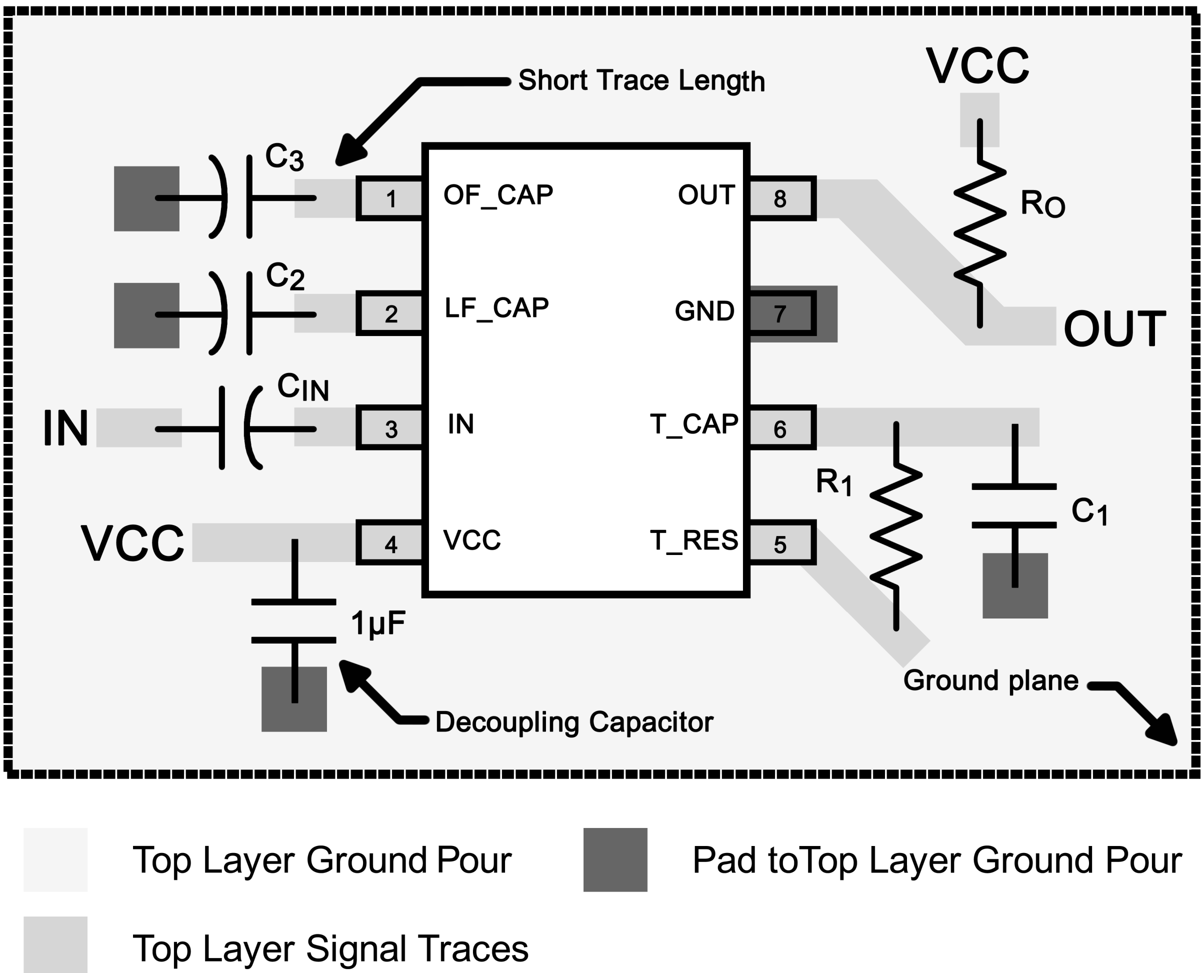

Figure 20. LM567 Layout Example

14 Device and Documentation Support

14.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM567	Click here	Click here	Click here	Click here	Click here
LM567C	Click here	Click here	Click here	Click here	Click here

14.2 Trademarks

All trademarks are the property of their respective owners.

14.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM567CM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM 567CM	Samples
LM567CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 567CM	Samples
LM567CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 567CM	Samples
LM567CN	LIFEBUY	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	LM 567CN	
LM567CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM 567CN	Samples
NE567V	LIFEBUY	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	LM 567CN	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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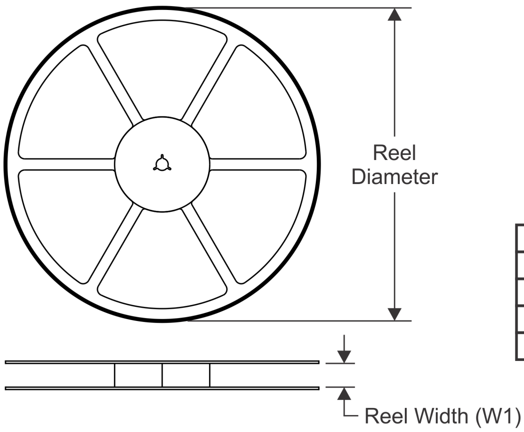
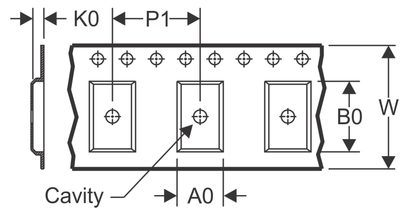
TAPE AND REEL INFORMATION

REEL DIMENSIONS

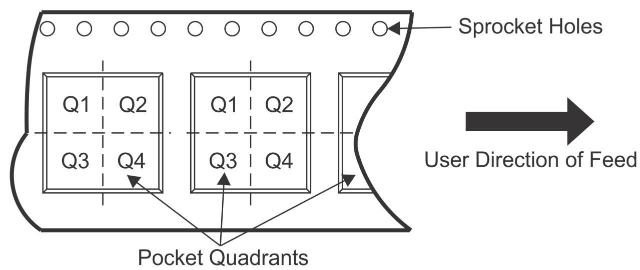


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

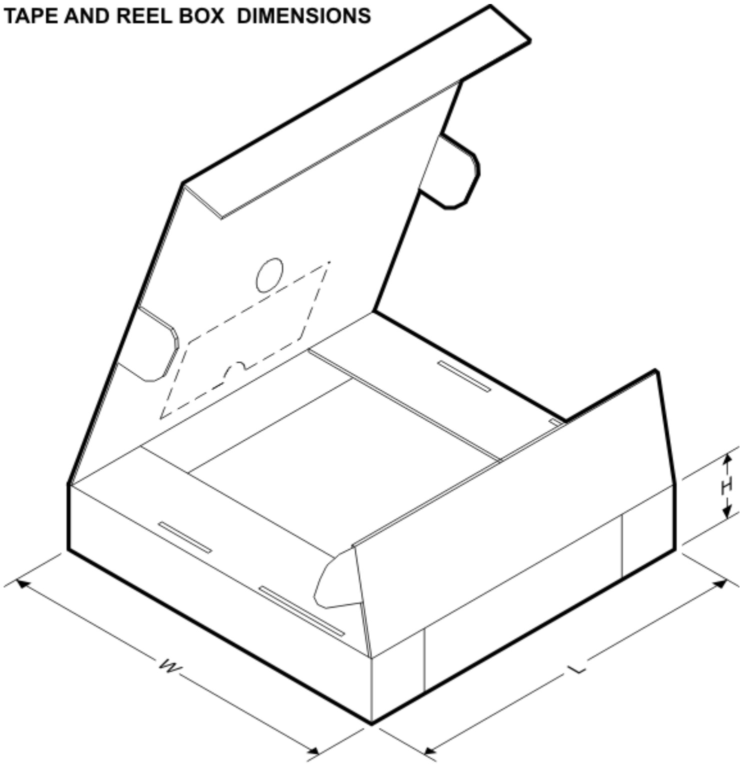
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM567CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

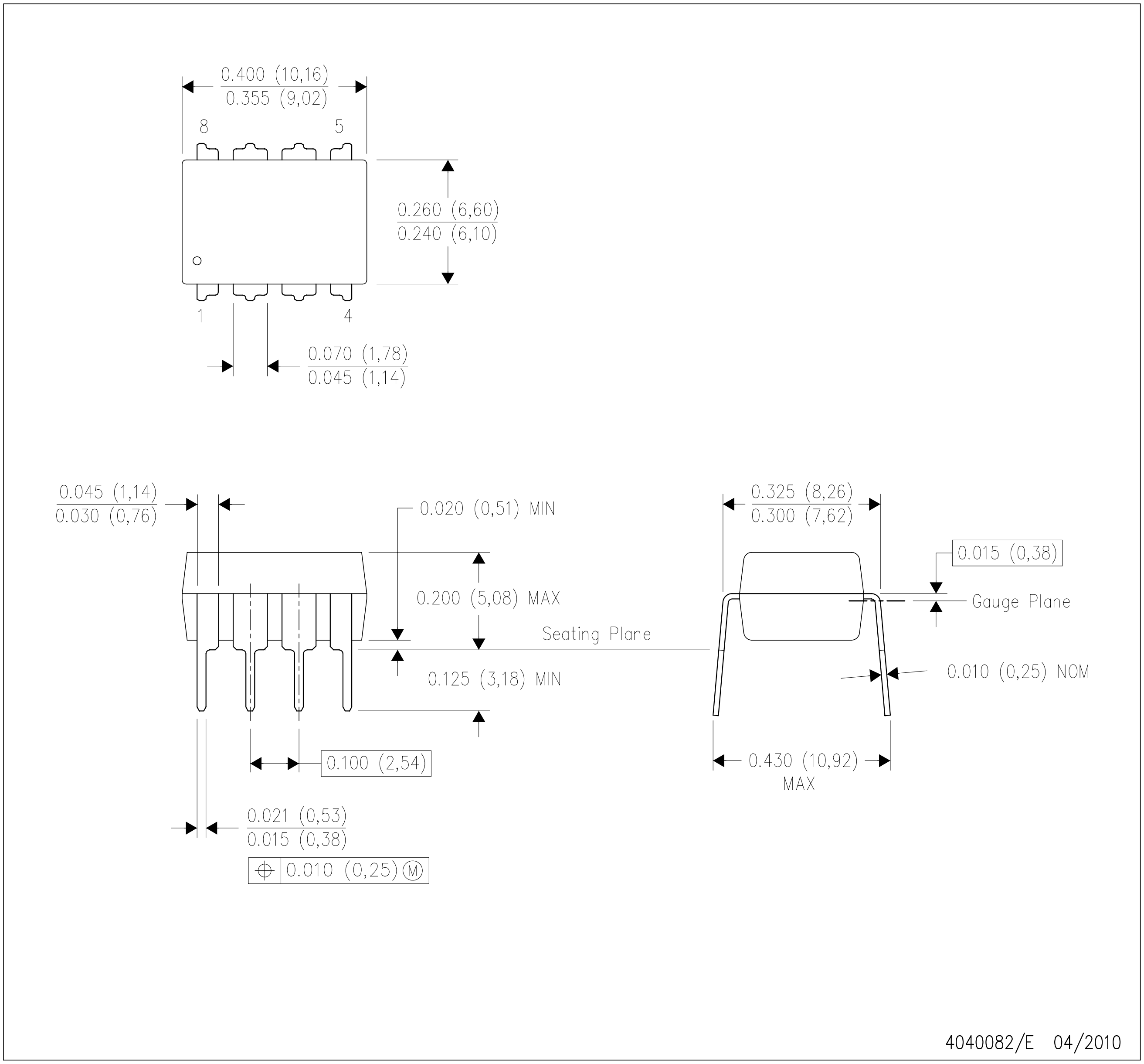
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

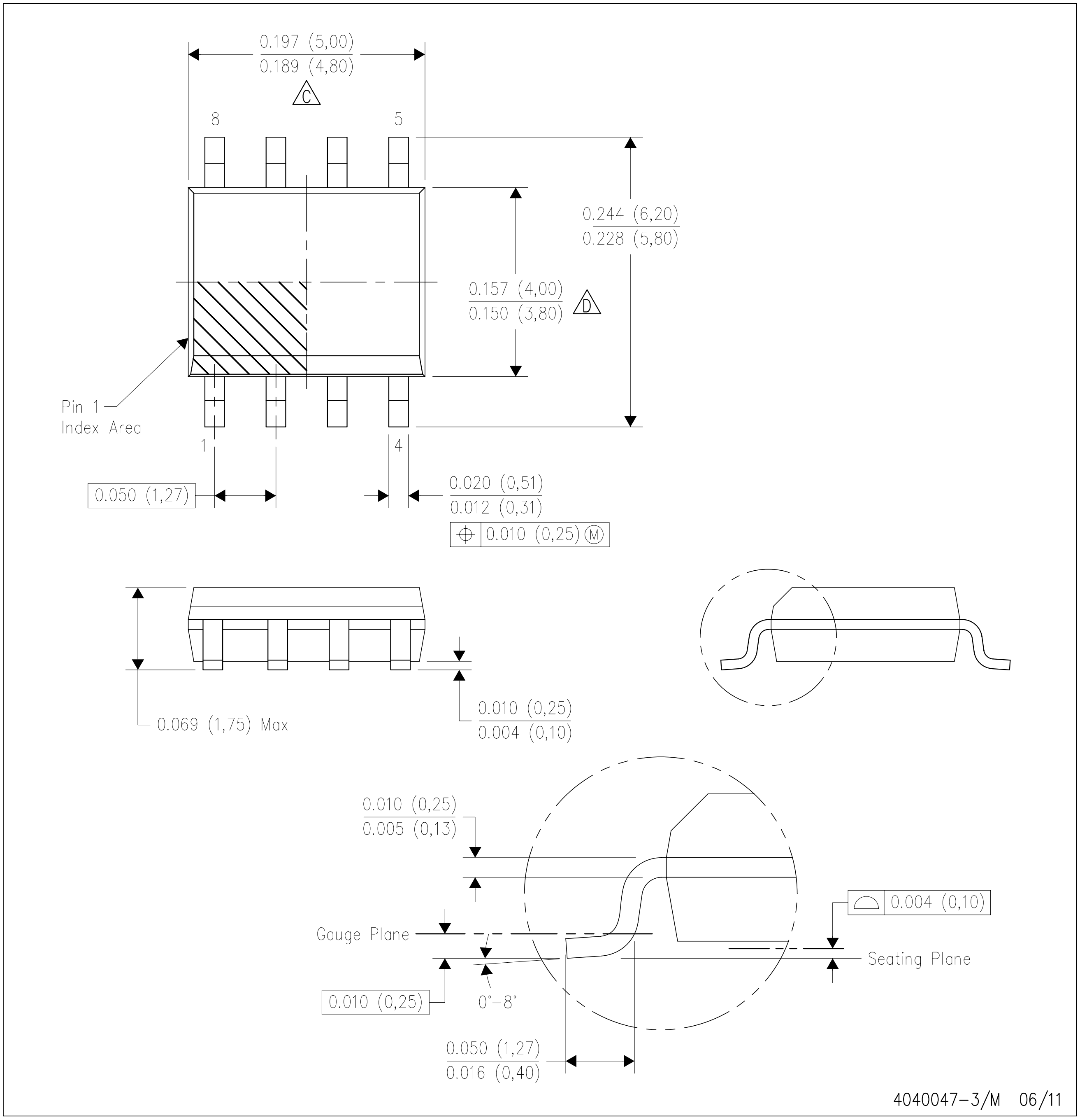
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM567CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

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