

CSD87333Q3D Synchronous Buck NexFET™ Power Block

1 Features

- Half-Bridge Power Block
- Optimized for High Duty Cycle
- Up to 24 V_{in}
- 94.7% System Efficiency at 8 A
- 1.5 W P_{LOSS} at 8 A
- Up to 15 A operation
- High Frequency Operation (Up to 1.5 MHz)
- High Density – SON 3.3-mm x 3.3-mm Footprint
- Optimized for 5 V Gate Drive
- Low Switching Losses
- Ultra-Low Inductance Package
- RoHS Compliant
- Halogen Free
- Pb-Free Terminal Plating

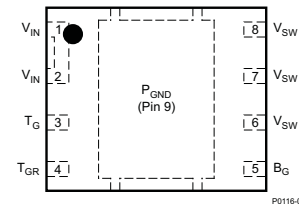
2 Applications

- Synchronous Buck Converters
 - High Frequency Applications
 - High Duty Cycle Applications
- Synchronous Boost Converters
- POL DC-DC Converters

3 Description

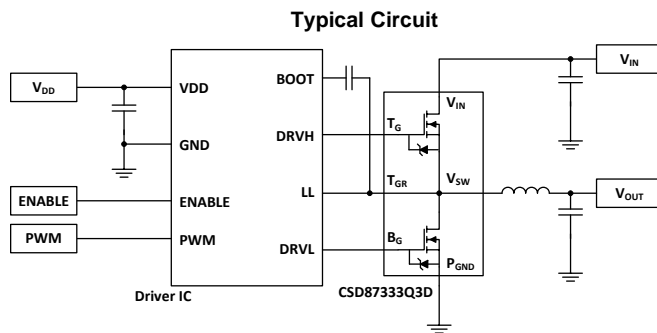
The CSD87333Q3D NexFET™ power block is an optimized design for synchronous buck and boost applications offering high current, high efficiency, and high frequency capability in a small 3.3-mm x 3.3-mm outline. Optimized for 5 V gate drive applications, this product offers a flexible solution in high duty cycle applications when paired with an external controller or driver.

Top View

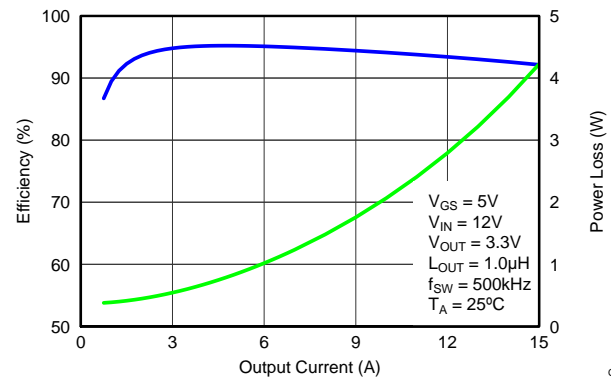


Ordering Information

Device	Qty	Media	Package	Ship
CSD87333Q3D	2500	13-Inch Reel	SON 3.3-mm x 3.3-mm Plastic Package	Tape and Reel
CSD87333Q3DT	250	7-Inch Reel		



Typical Power Block Efficiency and Power Loss



G001

Table of Contents

1 Features	1	6.2 Safe Operating Curves (SOA)	10
2 Applications	1	6.3 Normalized Curves	10
3 Description	1	6.4 Calculating Power Loss and SOA	11
4 Revision History	2	7 Recommended PCB Design Overview	12
5 Specifications	3	7.1 Electrical Performance	12
5.1 Absolute Maximum Ratings	3	7.1 Thermal Performance	13
5.2 Handling Ratings	3	8 Device and Documentation Support	14
5.3 Recommended Operating Conditions	3	8.1 Trademarks	14
5.4 Power Block Performance	3	8.2 Electrostatic Discharge Caution	14
5.5 Thermal Information	4	8.3 Glossary	14
5.6 Electrical Characteristics	4	9 Mechanical, Packaging, and Orderable Information	15
5.7 Typical Power Block Device Characteristics	6	9.1 Q3D Package Dimensions	16
5.8 Typical Power Block MOSFET Characteristics	8	9.2 Land Pattern Recommendation	18
6 Applications	10	9.3 Stencil Recommendation	18
6.1 Power Loss Curves	10	9.4 Q3D Tape and Reel Information	19

4 Revision History

DATE	REVISION	NOTES
February 2014	*	Initial release.

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Voltage Range	V_{IN} to P_{GND}	-0.8	30	V
	V_{SW} to P_{GND}		30	V
	V_{SW} to P_{GND} (10ns)		32	V
	T_G to T_{GR}	-0.3	10	V
	B_G to P_{GND}	-0.3	10	V
Pulsed Current Rating, I_{DM}			40	A
Power Dissipation, P_D			6	W
Avalanche Energy E_{AS}	Sync FET, $I_D = 19$, $L = 0.1\text{mH}$		18	mJ
	Control FET, $I_D = 19$, $L = 0.1\text{mH}$		18	
Operating Junction Temperature Range, T_J		-55	150	$^\circ\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{stg}	Storage Temperature Range	-55	150	$^\circ\text{C}$

5.3 Recommended Operating Conditions

 $T_A = 25^\circ$ (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{GS} Gate Drive Voltage		3.3	8	V
V_{IN} Input Supply Voltage			24	V
f_{SW} Switching Frequency	$C_{BST} = 0.1 \mu\text{F}$ (min)		1500	kHz
Operating Current			15	A
T_J Operating Temperature			125	$^\circ\text{C}$

5.4 Power Block Performance⁽¹⁾

 $T_A = 25^\circ$ (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS} Power Loss ⁽¹⁾	$V_{IN} = 12\text{ V}$, $V_{GS} = 5\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 8\text{ A}$, $f_{SW} = 500\text{ kHz}$, $L_{OUT} = 1 \mu\text{H}$, $T_J = 25^\circ\text{C}$		1.5		W
I_{QVIN} V_{IN} Quiescent Current	T_G to $T_{GR} = 0\text{ V}$ B_G to $P_{GND} = 0\text{ V}$		10		μA

(1) Measurement made with six 10- μF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5V driver IC.

5.5 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJA}	Junction to ambient thermal resistance (Min Cu) ⁽¹⁾			150	°C/W
	Junction to ambient thermal resistance (Max Cu) ⁽¹⁾⁽²⁾			80	
R _{θJC}	Junction to case thermal resistance (Top of package) ⁽¹⁾			36	
	Junction to case thermal resistance (P _{GND} Pin) ⁽¹⁾			3.7	

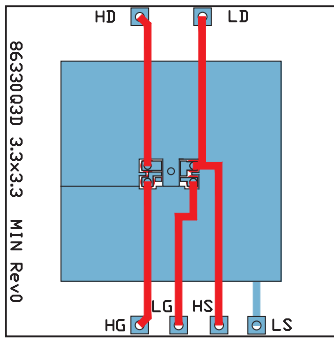
(1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2 oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 board. R_{θJC} is specified by design while R_{θJA} is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch² (6.45-cm²) Cu.

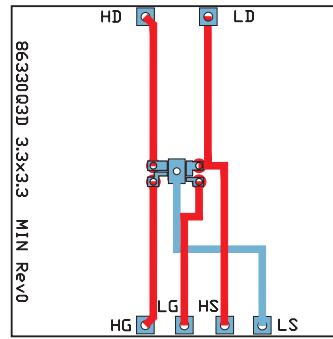
5.6 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER	TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
Static Characteristics									
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	30			30		V	
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 20 V			1		1	μA	
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = +10 / -8 V			100		100	nA	
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	0.75	0.95	1.20	0.75	0.95	1.20	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 3.5 V, I _{DS} = 4 A		14.7	17.7		14.7	17.7	mΩ
		V _{GS} = 4.5 V, I _{DS} = 4 A		13.4	16.1		13.4	16.1	
		V _{GS} = 8 V, I _{DS} = 4 A		11.9	14.3		11.9	14.3	
g _{fs}	Transconductance	V _{DS} = 15 V, I _{DS} = 4 A		43			43	S	
Dynamic Characteristics									
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		509	662		509	662	pF
C _{OSS}	Output Capacitance			222	289		222	289	pF
C _{RSS}	Reverse Transfer Capacitance			8.2	10.7		8.2	10.7	pF
R _G	Series Gate Resistance		3.4	6.8		3.4	6.8	Ω	
Q _g	Gate Charge Total (4.5 V)	V _{DS} = 15 V, I _{DS} = 4 A		3.5	4.6		3.5	4.6	nC
Q _{gd}	Gate Charge – Gate to Drain			0.3			0.3		nC
Q _{gs}	Gate Charge – Gate to Source			1.6			1.6		nC
Q _{g(th)}	Gate Charge at V _{th}			0.6			0.6		nC
Q _{OSS}	Output Charge		V _{DS} = 15 V, V _{GS} = 0 V		5.3			5.3	nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15 V, V _{GS} = 4.5 V, I _{DS} = 4 A, R _G = 2 Ω		2.1			2.1		ns
t _r	Rise Time			3.9			3.9		ns
t _{d(off)}	Turn Off Delay Time			9.4			9.4		ns
t _f	Fall Time			2.2			2.2		ns
Diode Characteristics									
V _{SD}	Diode Forward Voltage	I _{DS} = 4 A, V _{GS} = 0 V		0.80	1.0		0.80	1.0	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 15 V, I _F = 4 A, di/dt = 300 A/μs		10			10		nC
t _{rr}	Reverse Recovery Time			11			11		ns



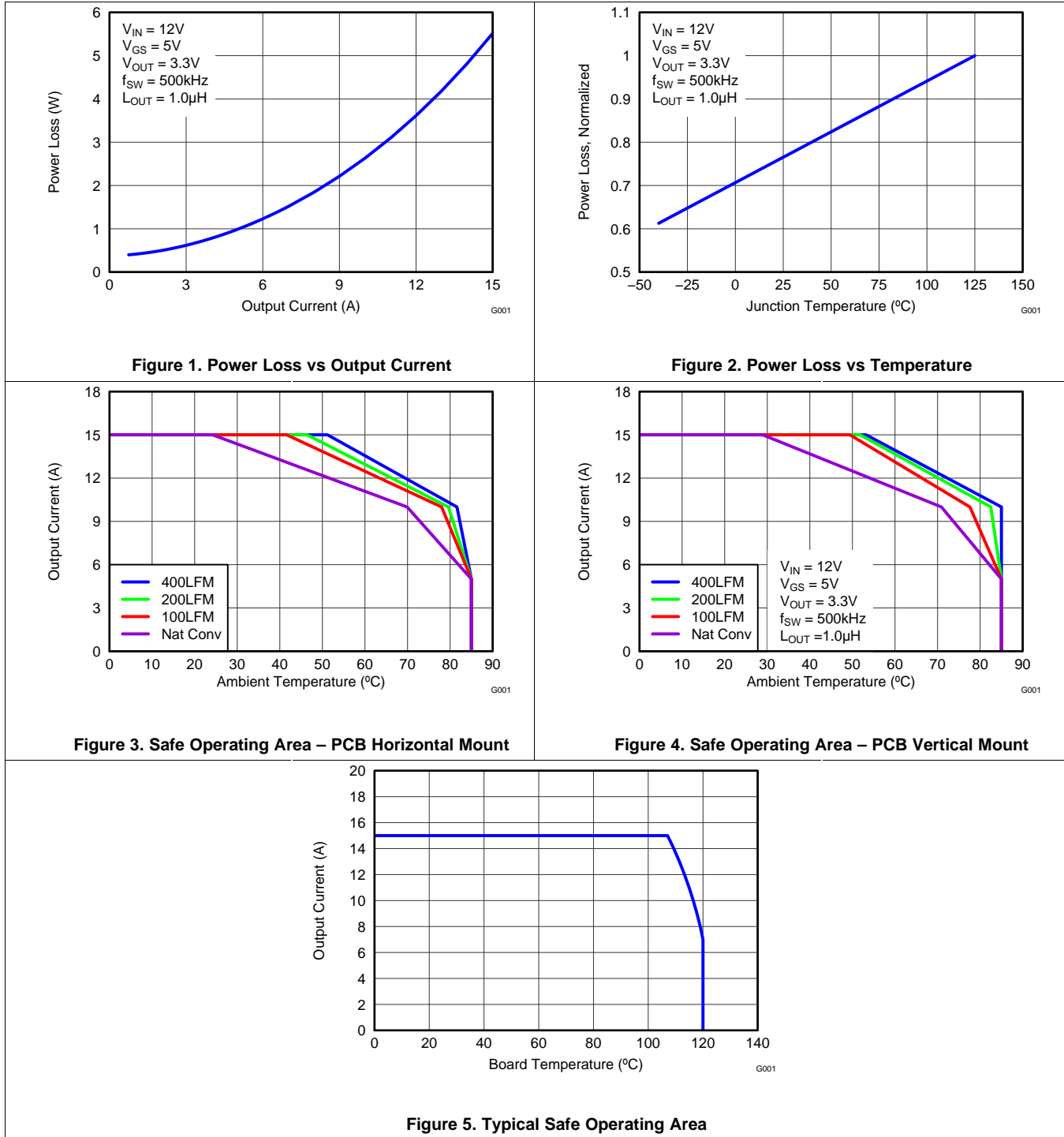
Max $R_{\theta JA} = 80^{\circ}\text{C/W}$
 when mounted on
 1 inch² (6.45 cm²) of 2-
 oz. (0.071-mm thick)
 Cu.



Max $R_{\theta JA} = 150^{\circ}\text{C/W}$
 when mounted on
 minimum pad area of
 2-oz. (0.071-mm thick)
 Cu.

5.7 Typical Power Block Device Characteristics

The Typical Power Block System Characteristic curves (Figure 1 through Figure 9) are based on measurements made on a PCB design with dimensions of 4.0-inch (W) × 3.5-inch (L) × 0.062-inch (H) and 6 copper layers of 1 oz. copper thickness. See Applications for detailed explanation. $T_A = 125^\circ\text{C}$, unless stated otherwise.



Typical Power Block Device Characteristics (continued)

The Typical Power Block System Characteristic curves (Figure 1 through Figure 9) are based on measurements made on a PCB design with dimensions of 4.0-inch (W) × 3.5-inch (L) × 0.062-inch (H) and 6 copper layers of 1 oz. copper thickness. See Applications for detailed explanation. $T_A = 125^\circ\text{C}$, unless stated otherwise.

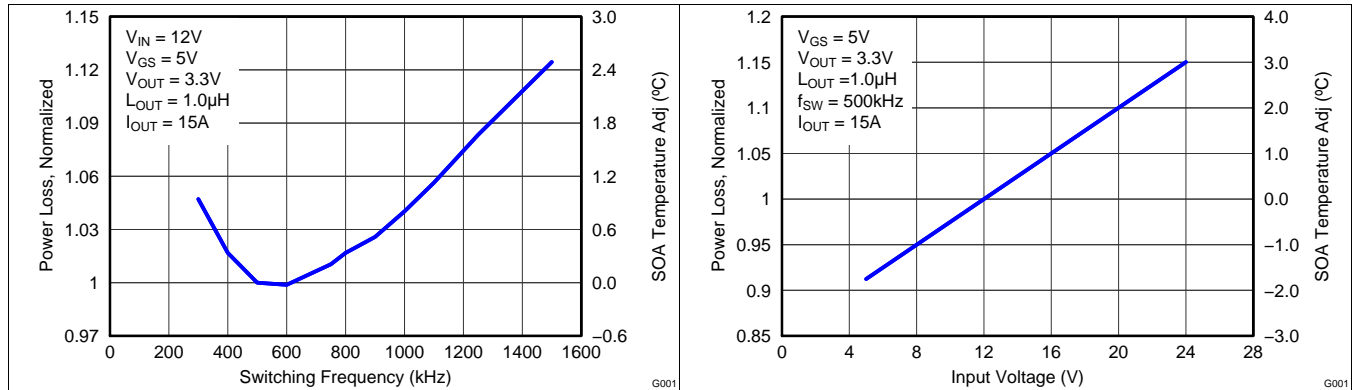


Figure 6. Normalized Power Loss vs Switching Frequency

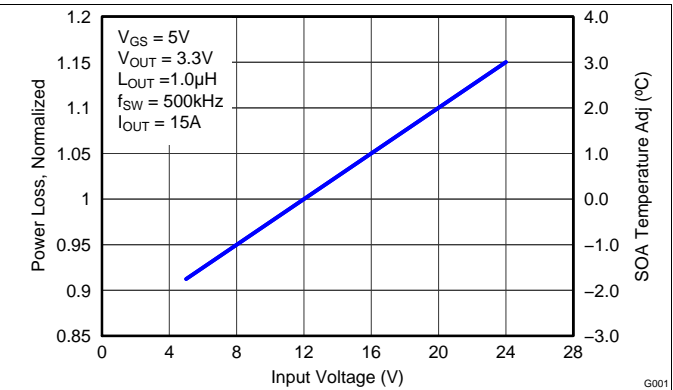


Figure 7. Normalized Power Loss vs Input Voltage

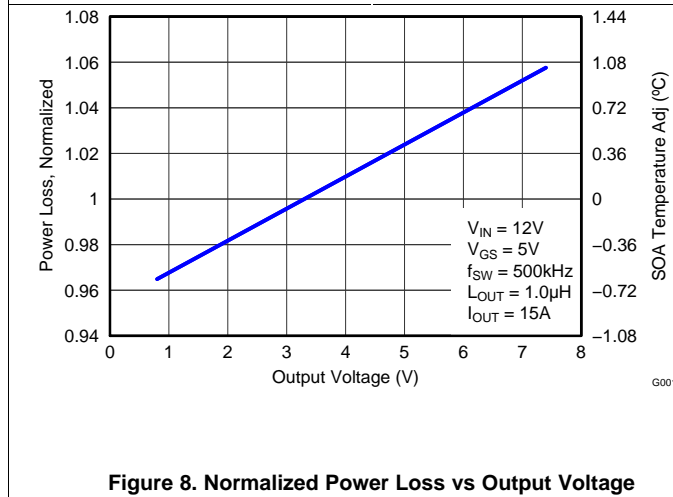


Figure 8. Normalized Power Loss vs Output Voltage

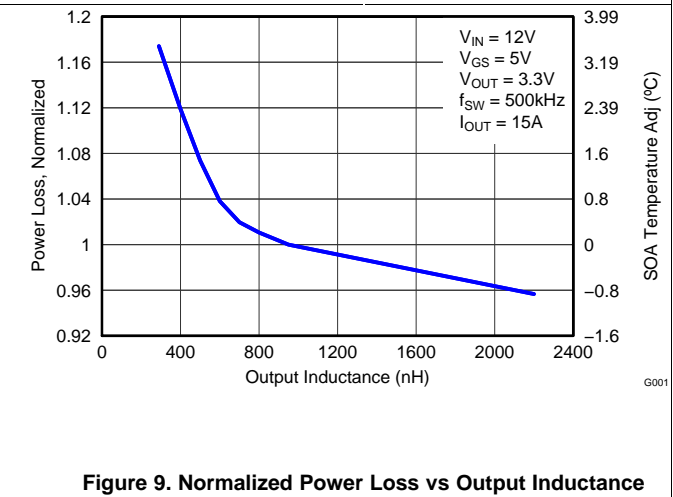


Figure 9. Normalized Power Loss vs Output Inductance

5.8 Typical Power Block MOSFET Characteristics

$T_A = 25^\circ\text{C}$, unless stated otherwise.

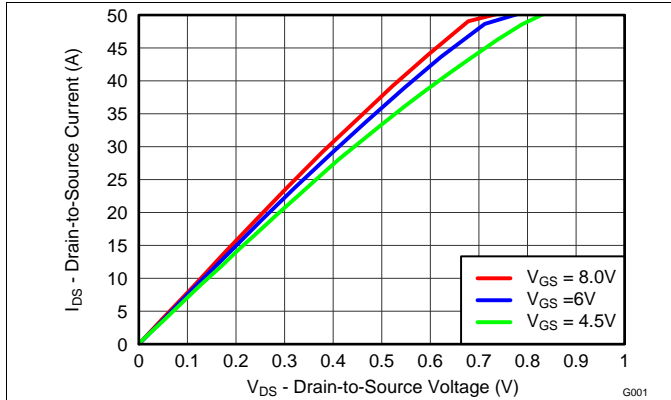


Figure 10. MOSFET Saturation Characteristics

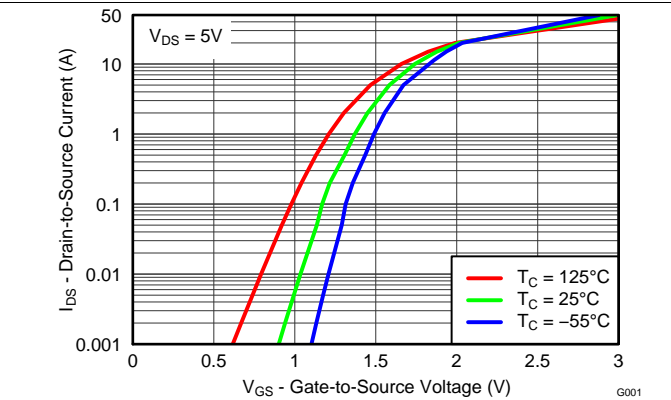


Figure 11. MOSFET Transfer Characteristics

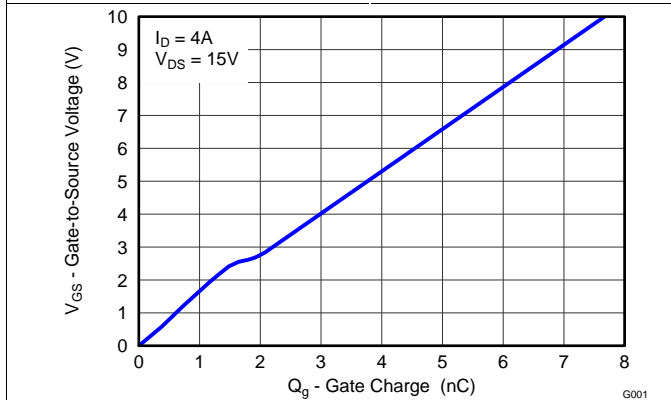


Figure 12. MOSFET Gate Charge

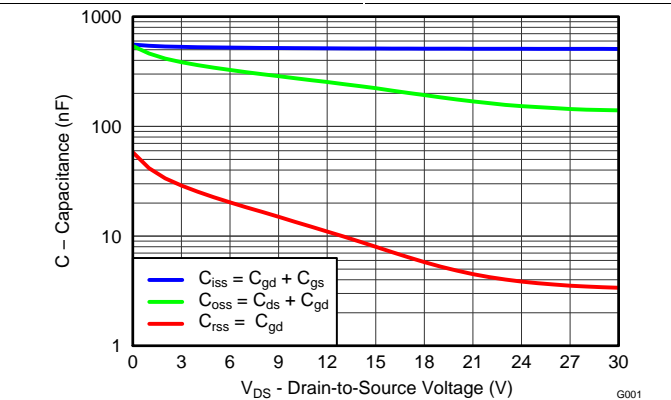


Figure 13. MOSFET Capacitance

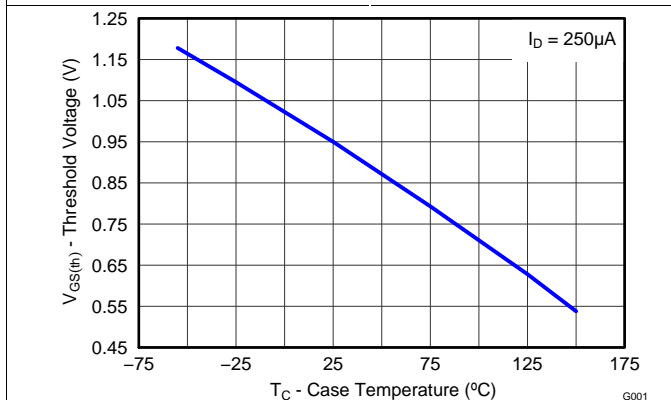


Figure 14. MOSFET $V_{GS(th)}$

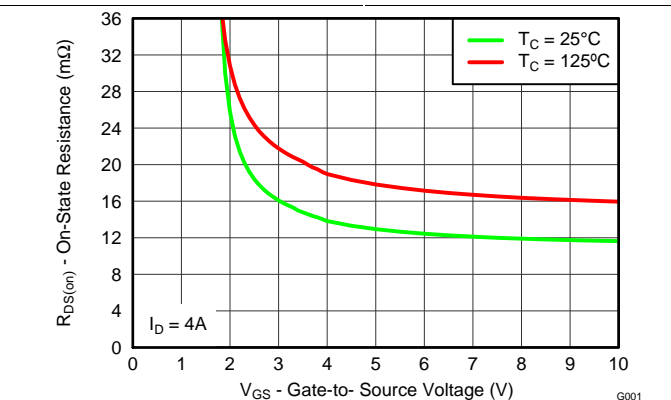


Figure 15. MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$, unless stated otherwise.

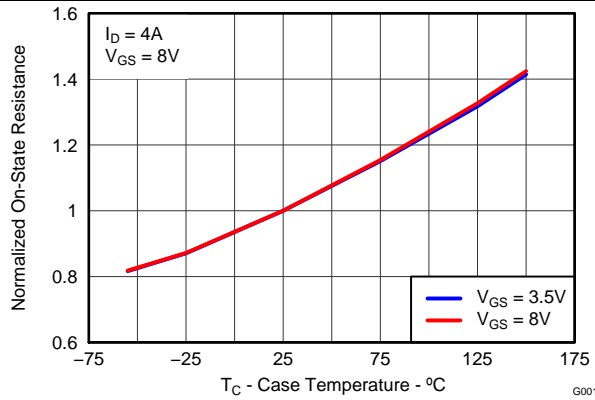


Figure 16. MOSFET Normalized $R_{DS(on)}$

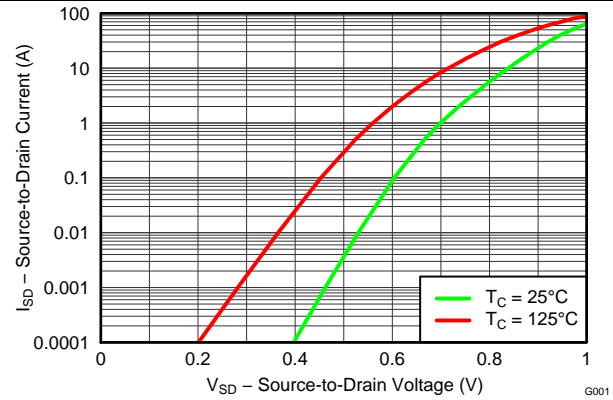


Figure 17. MOSFET Body Diode

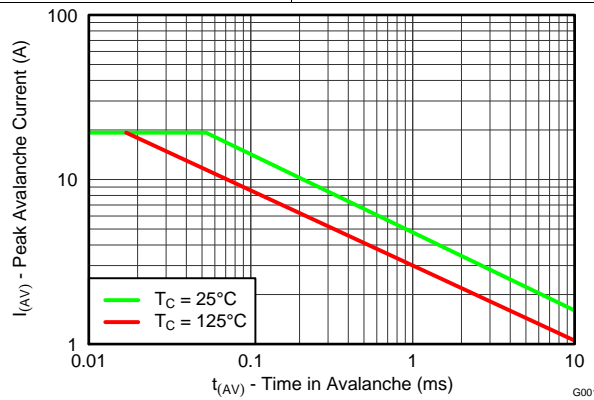


Figure 18. MOSFET Unclamped Inductive Switching

6 Applications

The CSD87333Q3D NexFET power block is an optimized design for synchronous buck applications using 5 V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems centric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.1 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87333Q3D as a function of load current. This curve is measured by configuring and running the CSD87333Q3D as it would be in the final application (see Figure 19). The measured power loss is the CSD87333Q3D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.2 Safe Operating Curves (SOA)

The SOA curves in the CSD87333Q3D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 5 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inches (T) and 6 copper layers of 1 oz. copper thickness.

6.3 Normalized Curves

The normalized curves in the CSD87333Q3D data sheet provides guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries adjust for a given set of system conditions. The primary Y-axis is the normalized change in power loss, and the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

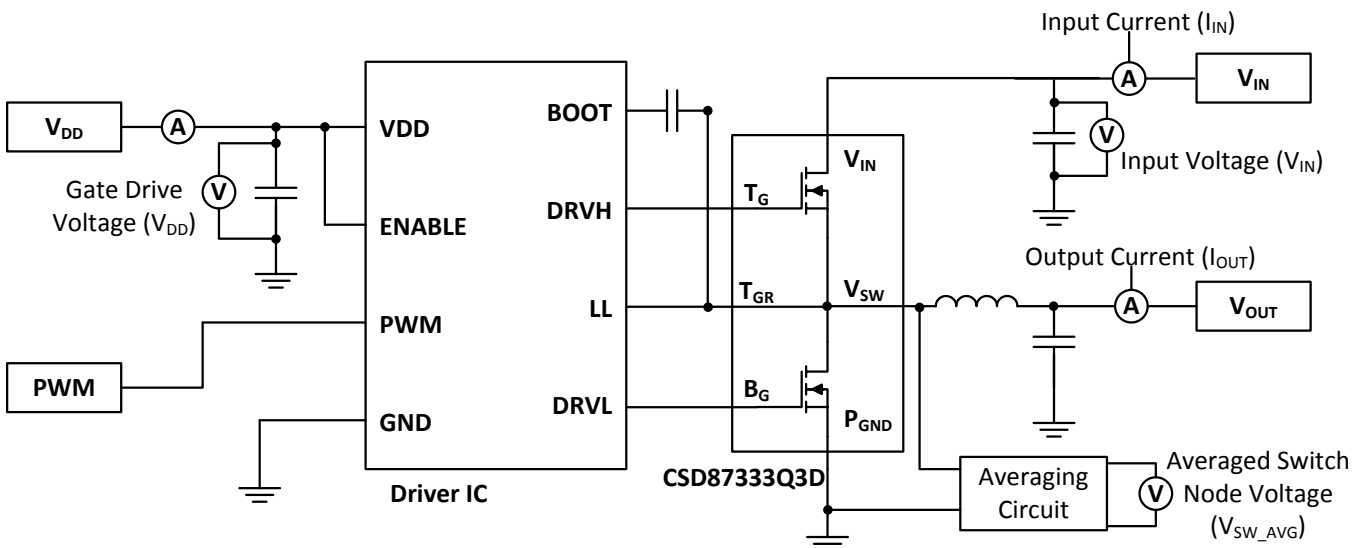


Figure 19. Typical Application

6.4 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see [Design Example](#)). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

6.4.1 Design Example

Operating Conditions:

- Output Current = 10 A
- Input Voltage = 20 V
- Output Voltage = 1 V
- Switching Frequency = 1000 kHz
- Inductor = 0.6 μ H

6.4.2 Calculating Power Loss

- Power Loss at 10 A = 2.6 W ([Figure 1](#))
- Normalized Power Loss for input voltage \approx 1.10 ([Figure 7](#))
- Normalized Power Loss for output voltage \approx 0.96 ([Figure 8](#))
- Normalized Power Loss for switching frequency \approx 1.04 ([Figure 6](#))
- Normalized Power Loss for output inductor \approx 1.03 ([Figure 9](#))
- **Final calculated Power Loss = 2.6 W x 1.10 x 0.96 x 1.04 x 1.03 \approx 2.9 W**

6.4.3 Calculating SOA Adjustments

- SOA adjustment for input voltage \approx 2.0°C ([Figure 7](#))
- SOA adjustment for output voltage \approx - 0.2°C ([Figure 8](#))
- SOA adjustment for switching frequency \approx 0.8°C ([Figure 6](#))
- SOA adjustment for output inductor \approx 0.8°C ([Figure 9](#))
- **Final calculated SOA adjustment = 2.0 + (-0.2) + 0.8 + 0.8 \approx 3.4°C**

In the [Design Example](#), the estimated power loss of the CSD87333Q3D would increase to 2.9 W. In addition, the maximum allowable board or ambient temperature, or both, would have to decrease by 3.4°C. [Figure 20](#) graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board or ambient temperature.
3. Adjust the SOA board or ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 3.4°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board or ambient temperature.

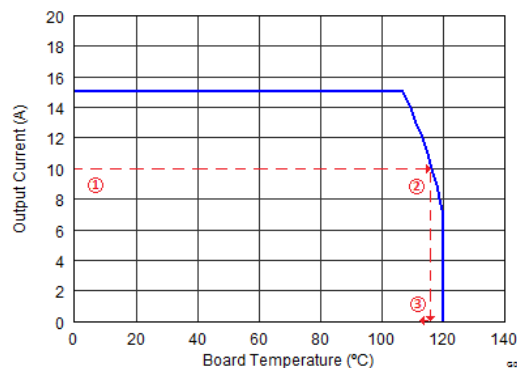


Figure 20. Power Block SOA

7 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: Electrical and Thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. A brief description on how to address each parameter is provided.

7.1 Electrical Performance

The Power Block has the ability to switch voltages at rates greater than 10 kV/ μ s. Special care must be then taken with the PCB layout design and placement of the input capacitors, Driver IC, and output inductor.

- The placement of the input capacitors relative to the Power Block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see [Figure 21](#)). The example in [Figure 21](#) uses 6 \times 10- μ F ceramic capacitors (TDK part number C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Block, C5, C7, C19, and C8 should follow in order.
 - The Driver IC should be placed relatively close to the Power Block Gate pins. T_G and B_G should connect to the outputs of the Driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the Phase pin of the IC (sometimes called LX, LL, SW, PH, and so forth). The bootstrap capacitor for the Driver IC will also connect to this pin.
 - The switching node of the output inductor should be placed relatively close to the Power Block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.⁽¹⁾ In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a Boost Resistor or RC snubber can be an effective way to easily reduce the peak ring level. The recommended Boost Resistor value will range between 1.0 to 4.7 Ω depending on the output characteristics of Driver IC used in conjunction with the Power Block. The RC snubber values can range from 0.5 to 2.2 Ω for the R and 330 to 2200 pF for the C. Please refer to TI Application Note [SLUP100](#) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the Vsw node and PGND (see [Figure 21](#)).⁽¹⁾
- (1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.1 Thermal Performance

The Power Block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in [Figure 21](#) uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

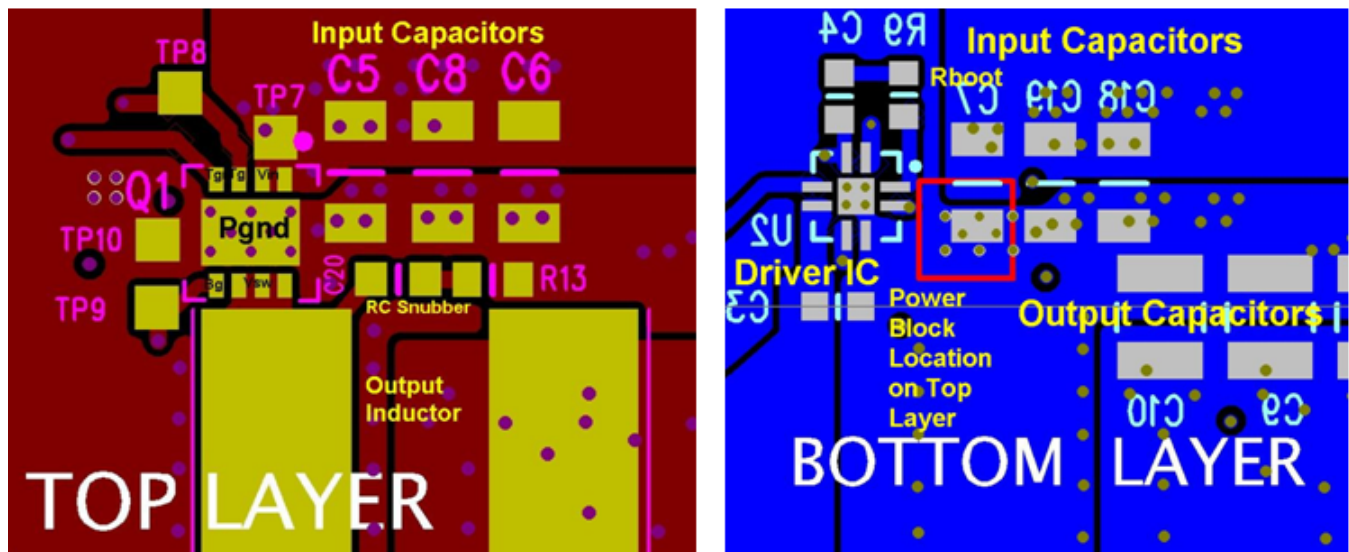


Figure 21. Recommended PCB Layout (Top Down)

8 Device and Documentation Support

8.1 Trademarks

NexFET is a trademark of Texas Instruments.

8.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.3 Glossary

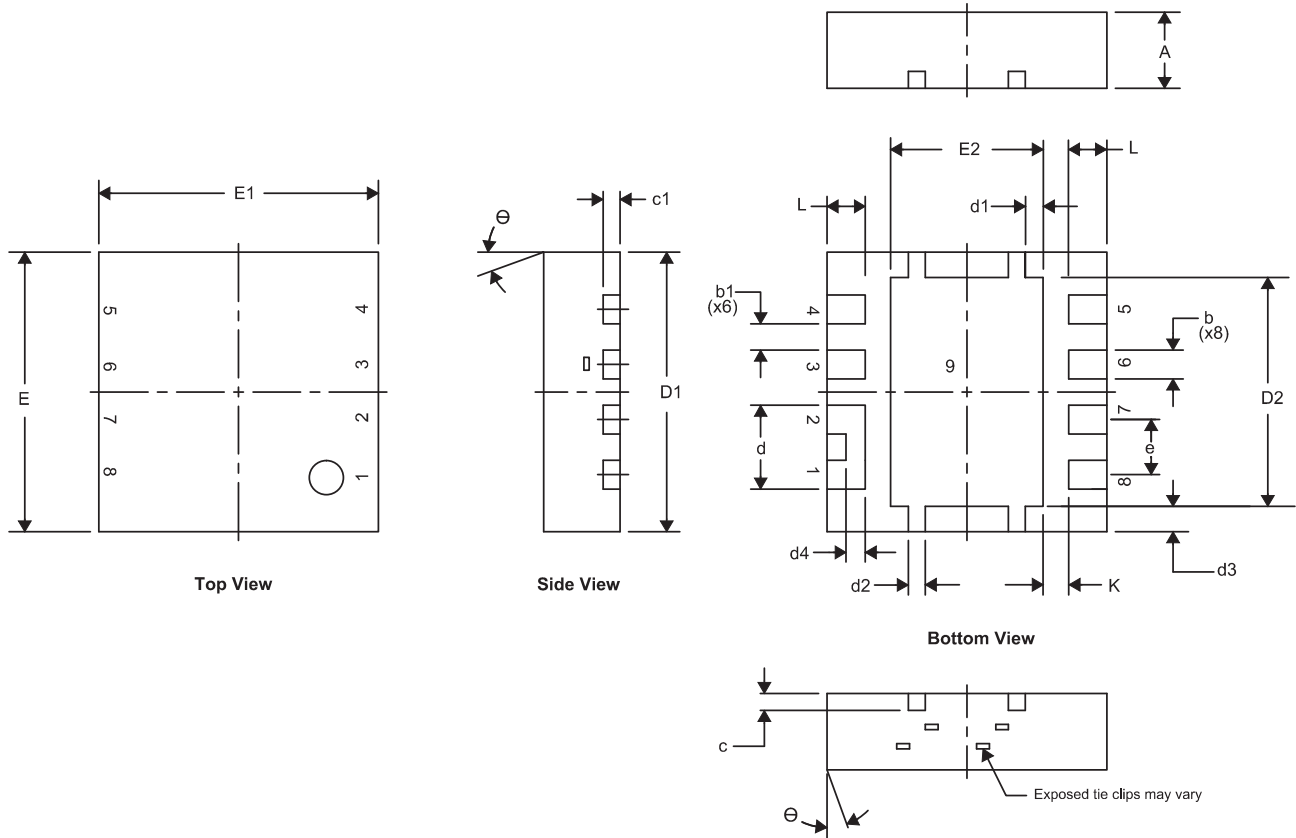
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Q3D Package Dimensions

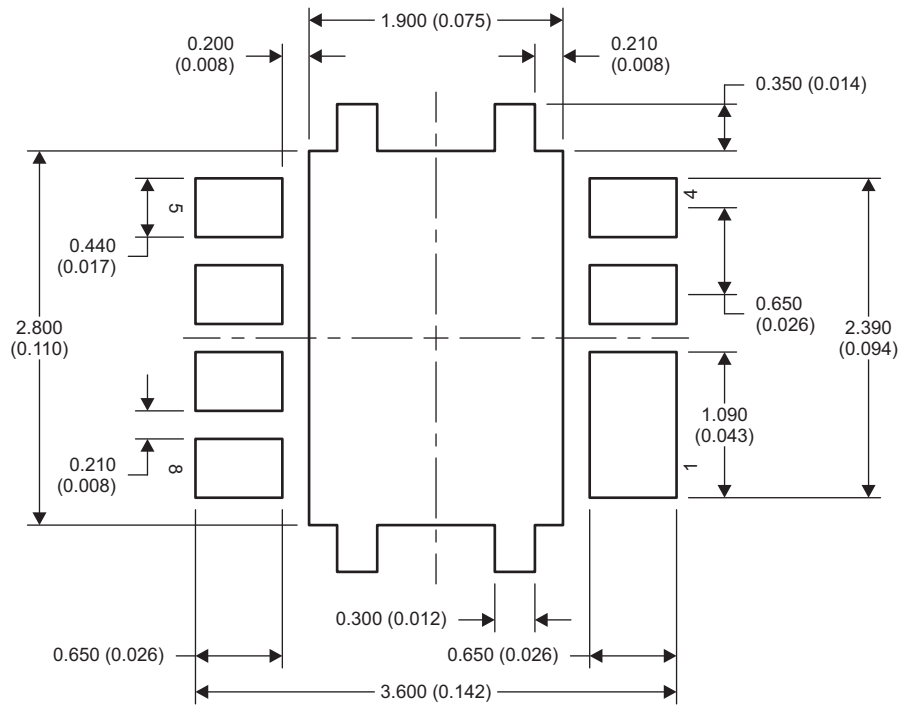


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.850	1.05	.033	.041
b	0.280	0.400	0.011	0.016
b1	0.310 Nom.		0.012 Nom.	
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	0.940	1.040	0.037	0.041
d1	0.160	0.260	0.006	0.010
d2	0.150	0.250	0.006	0.010
d3	0.250	0.350	0.010	0.014
d4	0.175	0.275	0.007	0.011
D1	3.200	3.400	0.126	0.134
D2	2.650	2.750	0.104	0.108
E	3.200	3.400	0.126	0.134
E1	3.200	3.400	0.126	0.134
E2	1.750	1.850	0.069	0.073
e	0.650 TYP		0.026 TYP	
L	0.400	0.500	0.016	0.020
θ	0.00	-	-	-
K	0.300 TYP		0.012 TYP	

Pinout Configuration

Position	Designation
Pin 1	V_{IN}
Pin 2	V_{IN}
Pin 3	T_G
Pin 4	T_{GR}
Pin 5	B_G
Pin 6	V_{SW}
Pin 7	V_{SW}
Pin 8	V_{SW}
Pin 9	P_{GND}

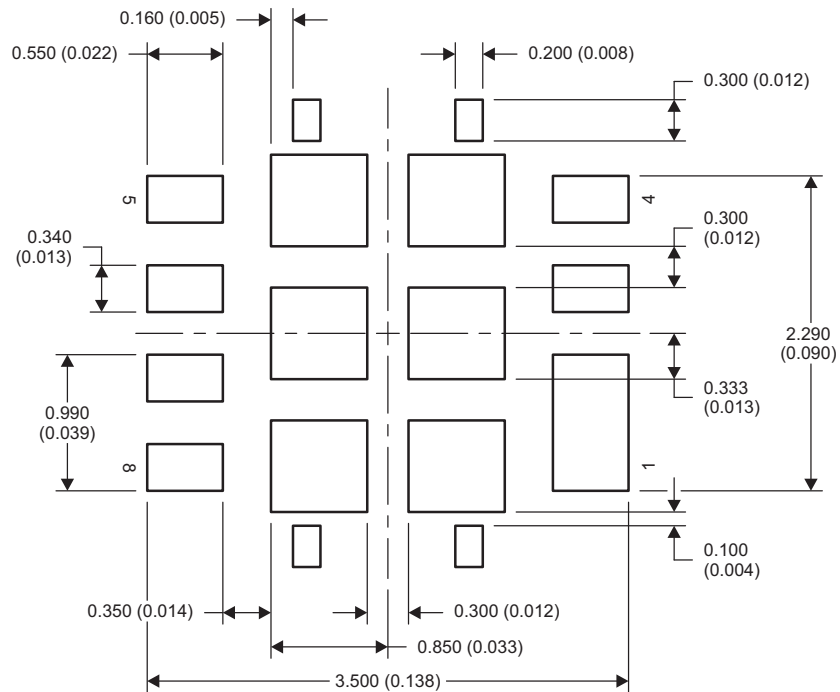
9.2 Land Pattern Recommendation



M0193-01

NOTE: Dimensions are in mm (inches).

9.3 Stencil Recommendation

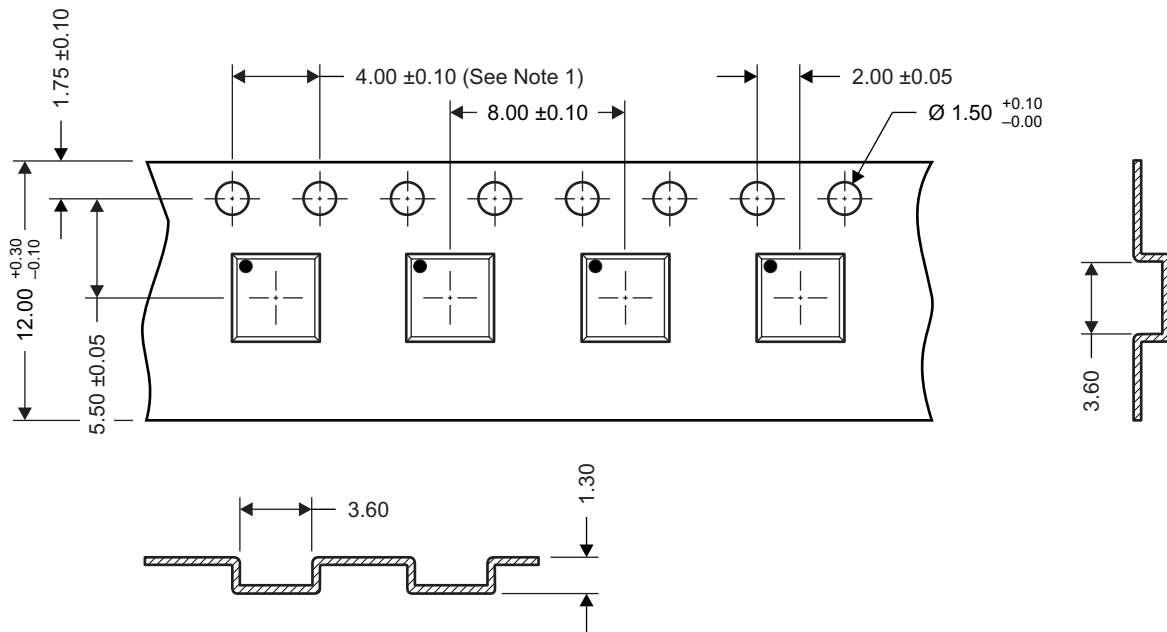


M0207-01

NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

9.4 Q3D Tape and Reel Information



M0144-01

- NOTES:
1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
 2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
 3. Material: black static-dissipative polystyrene
 4. All dimensions are in mm, unless otherwise specified.
 5. Thickness: 0.30 ± 0.05 mm
 6. MSL1 260°C (IR and convection) PbF reflow compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87333Q3D	ACTIVE	VSON-FET	DPB	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 150	87333D	Samples
CSD87333Q3DT	ACTIVE	VSON-FET	DPB	8	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	0 to 0	87333D	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87333Q3D	VSON-FET	DPB	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87333Q3D	VSON-FET	DPB	8	2500	367.0	367.0	35.0

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