
Table 1. Device summary

Symbol	Value
$I_{F(AV)}$	15 A
V_{RRM}	50 V
T_j (max)	+150 °C
V_F (typ)	0.30 V

Features

- ST proprietary process
- Stable leakage current over reverse voltage
- Low forward voltage drop
- High frequency operation

Description

This single rectifier is based on a proprietary technology, enabling to achieve the best in class V_F/I_R for a given silicon surface.

Packaged in PowerFLAT™ 5x6, this device is intended to be used in rectification and freewheeling operations in switch mode power supplies.

TM: PowerFLAT is a trademark of STMicroelectronics

1 Characteristics

Table 2. Absolute ratings (limiting values, per diode, at 25 °C, unless otherwise specified)

Symbol	Parameter	Value	Unit	
V _{RRM}	Repetitive peak reverse voltage	50	V	
I _{F(RMS)}	Forward rms current	25	A	
I _{F(AV)}	Average forward current, δ = 0.5	T _c = 120 °C	15	A
I _{FSM}	Surge non repetitive forward current	t _p = 10 ms sinusoidal	80	A
T _{stg}	Storage temperature range	-65 to + 175	°C	
T _j	Maximum operating junction temperature ⁽¹⁾	150	°C	

1. $\frac{dP_{tot}}{dT_j} < \frac{1}{R_{th(j-a)}}$ condition to avoid thermal runaway for a diode on its own heatsink

Table 3. Thermal resistance

Symbol	Parameter	Value (max)	Unit
R _{th(j-c)}	Junction to case	2.8	°C/W

Table 4. Static electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
I _R ⁽¹⁾	Reverse leakage current	T _j = 25 °C	V _R = V _{RRM}		250	650	μA
		T _j = 125 °C			20	40	mA
V _F ⁽²⁾	Forward voltage drop	T _j = 25 °C	I _F = 5 A		0.35		V
		T _j = 125 °C			0.30	0.35	
		T _j = 25 °C	I _F = 10 A		0.42	0.48	
		T _j = 125 °C			0.41	0.45	
		T _j = 25 °C	I _F = 15 A		0.48		

1. Pulse test: t_p = 5 ms, δ < 2%

2. Pulse test: t_p = 380 μs, δ < 2%

To evaluate the conduction losses use the following equation:

$$P = 0.25 \times I_{F(AV)} + 0.02 I_{F(RMS)}^2$$

Figure 1. Average forward power dissipation versus average forward current

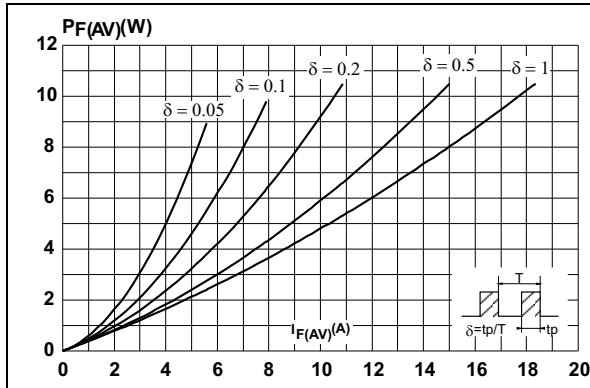


Figure 2. Average forward current versus ambient temperature (delta = 0.5)

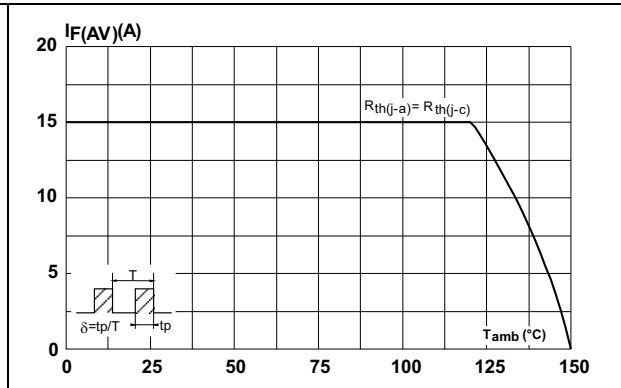


Figure 3. Relative variation of thermal impedance junction to case versus pulse duration

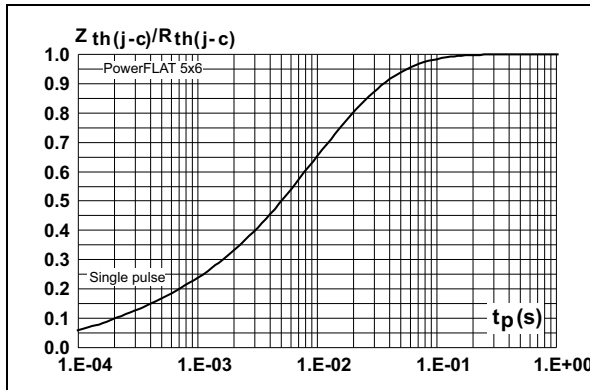


Figure 4. Reverse leakage current versus reverse voltage applied (typical values)

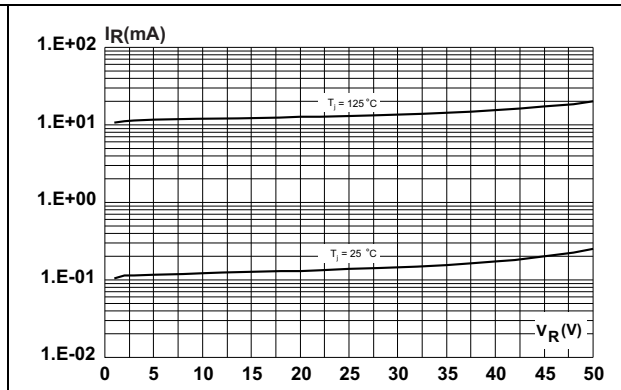


Figure 5. Junction capacitance versus reverse voltage applied (typical values)

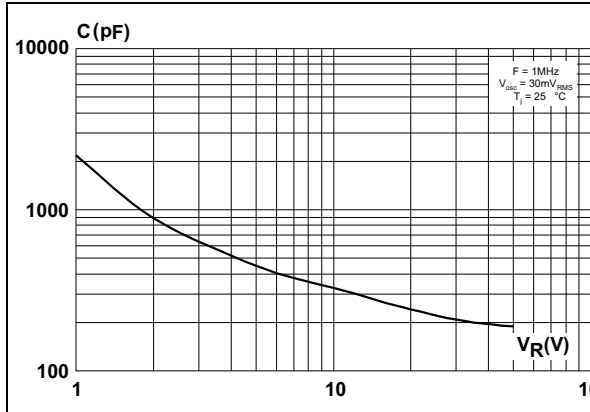


Figure 6. Forward voltage drop versus forward current (typical values)

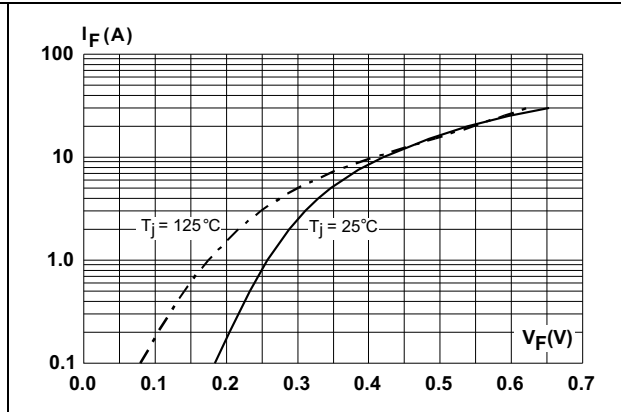
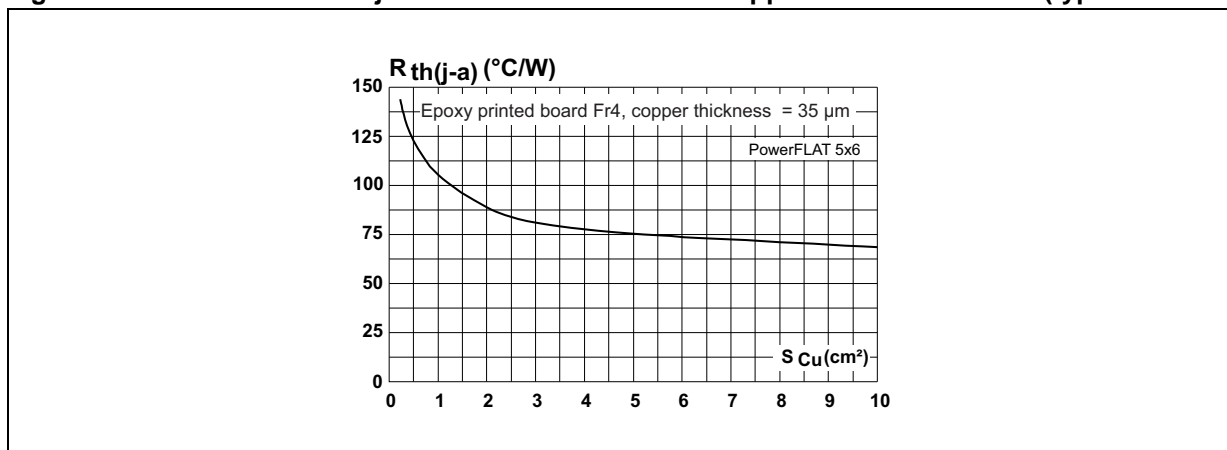


Figure 7. Thermal resistance junction to ambient versus copper surface under tab (typical values)



2 Package information

- Epoxy meets UL94, V0
- Cooling method: by conduction (C)

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 8. PowerFLAT-8L dimensions (definitions)

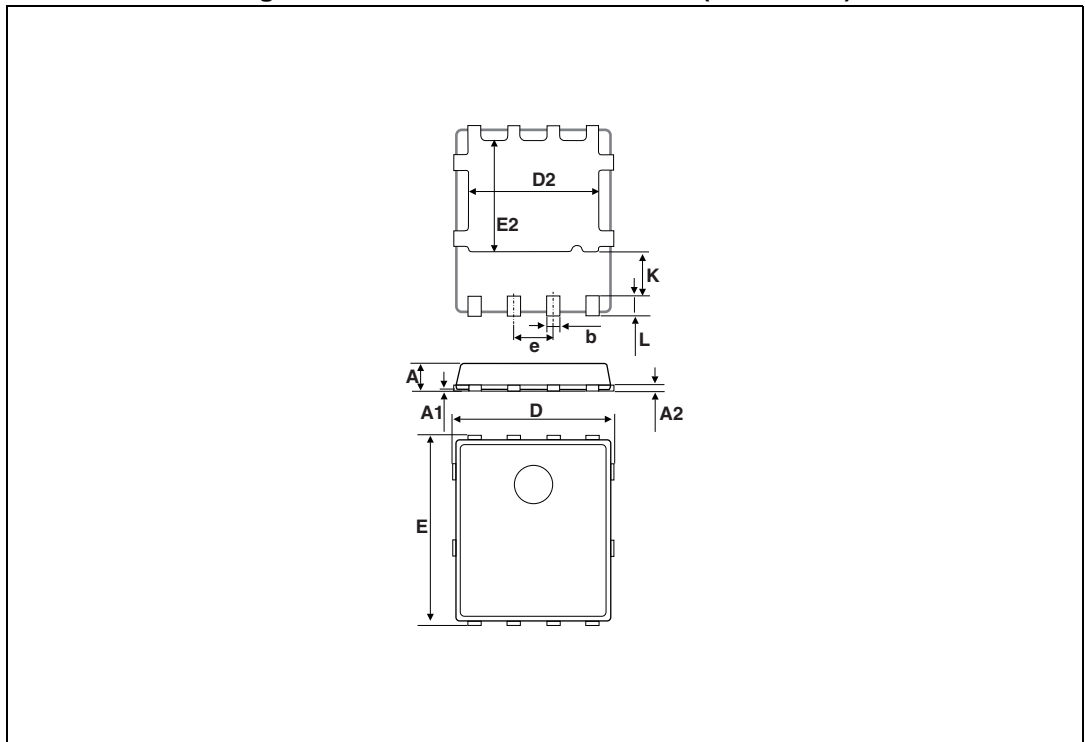
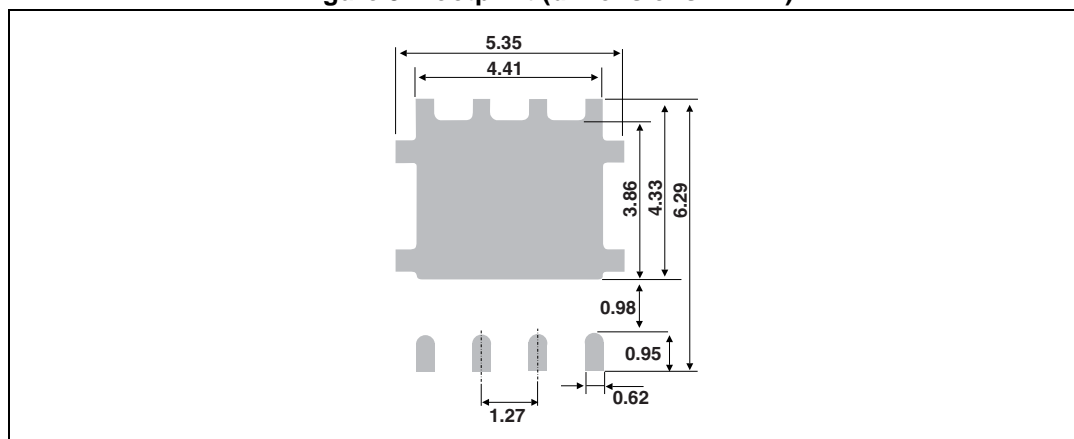


Table 5. PowerFLAT-8L dimensions (values)

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.031		0.039
A1	0.02		0.05	0.001		0.002
A2		0.25			0.010	
b	0.30		0.50	0.012		0.020
D		5.20			0.205	
D2	4.11		4.31	0.162		0.170
e		1.27			0.050	
E		6.15			0.242	
E2	3.50		3.70	0.138		0.146
L	0.50		0.80	0.020		0.031
K	1.275		1.575	0.050		0.062

Figure 9. Footprint (dimensions in mm)



3 Ordering information

Table 6. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
FERD15S50DJF-TR	FD15 S50	PowerFLAT™ 5x6	0.095 g	3000	Tape and reel

4 Revision history

Table 7. Document revision history

Date	Revision	Changes
09-Oct-2013	1	Initial release.

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