Crest Factor Reduction Processor

FEATURES

- **Reduces Signal Peaks to ≥ 6 dB PAR**
- **One- and Two-Channel Operation**
- **Programmable PAR With Four Stages**
- **Programmable Cancellation Pulse Coefficients**
- **256-Ball PBGA Package, 17-mm × 17-mm**
- **1.2-V Core, 3.3 V I/O**

APPLICATIONS

- **3GPP (W-CDMA, HSDPA) Base Stations**
- **3GPP2 (cdma2000) Base Stations**
- **TDSCDMA Base Stations**
- **PAPR Reduction of OFDM, Wibro, OFDMA Signals**
- **Two-Channel Transmit Diversity Applications**
- **Operates With TI DAC5687 (500 Msps)**

DESCRIPTION

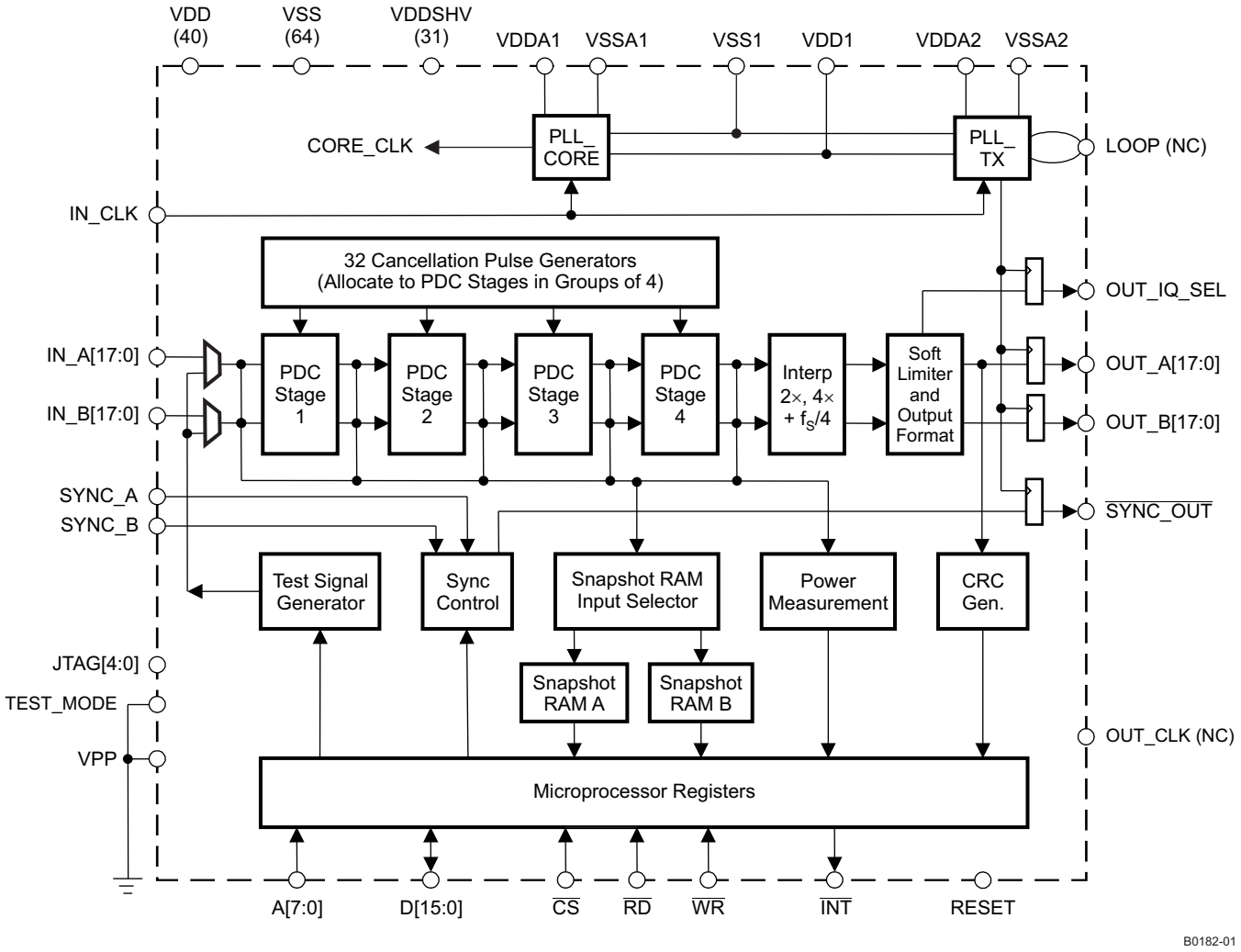
The GC1115 is a flexible, programmable, wideband crest factor reduction (CFR) processor with a maximum composite bandwidth of 32 MHz (4 clocks/complex sample, one channel) or 16 MHz (8 clocks/complex sample, two channels). The GC1115 selectively reduces the peak-to-average ratio (PAR) of wideband digital signals provided in quadrature (I and Q) format. By reducing the PAR of digital signals, the efficiency of follow-on power amplifiers (PAs) is improved, the D/A converter requirements are eased, and the out-of-band spectral regrowth caused by simple hard limiting is eliminated.

Manufacturers of 3G BTS equipment can realize significant savings on power amplifier costs by including the GC1115. The GC1115 meets multicarrier 3G performance standards (PCDE, composite EVM, and ACLR) at PAR levels down to 6 dB. The GC1115 integrates easily into the transmit signal chain, between a digital upconverter such as the Texas Instruments GC5016 or GC5316 and a high-quality D/A converter, such as the Texas Instruments DAC5687.

the GC1115 can be interleaved or parallel complex. The GC1115 uses four cascaded stages of peak detection and cancellation (PDC) to remove over-threshold peaks from the input signal. Each PDC stage can be independently programmed with detection target peak levels and cancellation pulse coefficients. A pool of 32 cancellation pulse generators can be flexibly assigned in groups of 4 to any PDC stage. Real or complex FIR cancellation coefficients are preprocessed into coefficients and derivative values. Cancellation pulses are designed to match the user's carrier frequency allocation. Cancellation pulse energy is bandlimited and thus is only added within allocated carrier bands. The GC1115 peak cancellation algorithm has minimal effect on the ACLR of the signal. The CFR data can be interpolated and output in complex or real formats.

Input sampling rates to 130 Msps are supported, in either parallel or multiplexed I/Q modes, and in either 2s complement or unsigned format. The GC1115 includes an interpolator that increases the output sampling rate by 2× or 4× and optionally modulates the output signal to the $f_S/4$ center frequency. Output sampling rates to 130 Msps are supported in either parallel or multiplexed I/Q modes, and in either 2s complement or unsigned format. A special one-channel, 2× output mode uses both GC1115 output ports to carry odd/even real output samples. Dual on-chip RAM provides either time-domain snapshots or long-term histogramming of the internal peak cancellation signal chain at five user-selected points, enabling real-time monitoring of the CCDF function. A power-level meter monitors either the GC1115 input or output power level.

FUNCTIONAL BLOCK DIAGRAM



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ORDERING INFORMATION

T_A	PACKAGE	DEVICE
–40C to 85C	256-PBGA Plastic Ball Grid Array	GC1115IZDJ

INTRODUCTION

Figure 1 shows the typical usage of the GC1115 crest factor reduction processor in the transmit signal chain of a wireless base station.

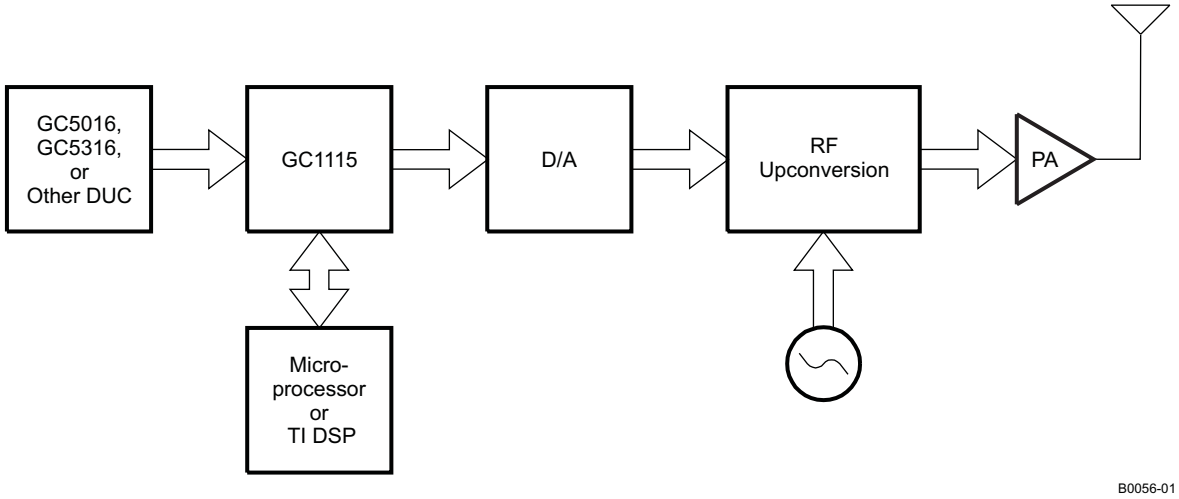


Figure 1. Wireless System Using the GC1115

The GC1115 is initialized and controlled using an 8-bit address (A) bus and a 16-bit data (D) bus. These pins, along with the read ($\overline{RD}$), write ($\overline{WR}$), and chip select ($\overline{CS}$) pins, allow users to modify the control registers of the GC1115.

Signals are provided to the GC1115 using two 18-bit input ports, IN_A[17:0] and IN_B[17:0], which are typically driven by a digital upconverter such as the TI GC5016 or GC5316. The GC1115 can accept either one or two input channels.

When the GC1115 is configured to process two input channels, IN_A[17:0] carries the channel-0 multiplexed I and Q samples, while IN_B[17:0] carries the channel-1 multiplexed I and Q samples. The GC1115 output samples are provided to a D/A converter using two 18-bit output ports, OUT_A[17:0] and OUT_B[17:0]. The GC1115 output may appear on one or both output ports, depending on which output mode (real or complex; parallel, multiplexed, or odd-even) is selected.

NOTE:

The D/A converter must **not** use the GC1115 OUT_CLK signal. OUT_CLK is for test purposes only. The OUT_CLK phase is not aligned with the data on the OUT_A and OUT_B ports. OUT_CLK may contain jitter in excess of that required to clock high-speed D/A converters.

Why Cancel Peaks?

The purpose of the GC1115 is to lower the peak-to-average ratio (PAR) of composite digital communication signals. Specifically, wideband code division multiple access (W-CDMA) and orthogonal frequency division multiplexed (OFDM) signals have high peak-to-average ratios (PARs) ranging from 10 dB to 15 dB. After D/A conversion, a power amplifier (PA) amplifies the resulting analog signal. In order to accommodate the high PAR of W-CDMA and OFDM signals, the peak signal level must be at or below the 1 dB compression point of the PA, which is usually accommodated by backing off the input drive to the power amplifier.

Figure 2 illustrates the effects of a decrease in peak-to-average ratio on the V_{in} vs V_{out} graph of a PA.

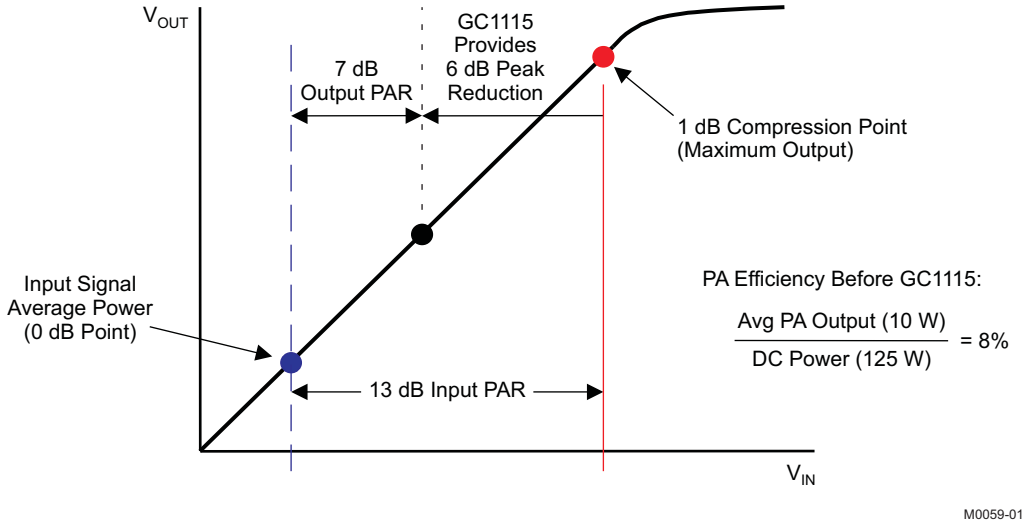


Figure 2. Reducing the Peak-to-Average Ratio (PAR)

However, because the peak-to-average ratio of CDMA signals is so high, the average power is relatively low, consequently resulting in a low PA efficiency (output power divided by input power). By decreasing the peak-to-average ratio, the average power of the peak-reduced signal at the output of the GC1115 can be increased, decreasing PA back-off, thus also increasing PA efficiency.

Figure 3 illustrates that the decrease in PAR can then be used to increase the average signal power while still keeping the peaks below the PA 1-dB compression point. The GC1115 can typically limit the output PAR of CDMA signals to between 6 dB and 7 dB while still meeting all relevant 3GPP or 3GPP2 requirements. This decreased PAR enables a 2-dB to 3-dB increase in PA drive, which in turn allows PA manufacturers to achieve 2 dB to 3 dB more PA output power. As PAs represent a significant percentage of the capital equipment cost of base stations, using a 10-W PA instead of a 20-W PA (for example) significantly decreases base station costs.

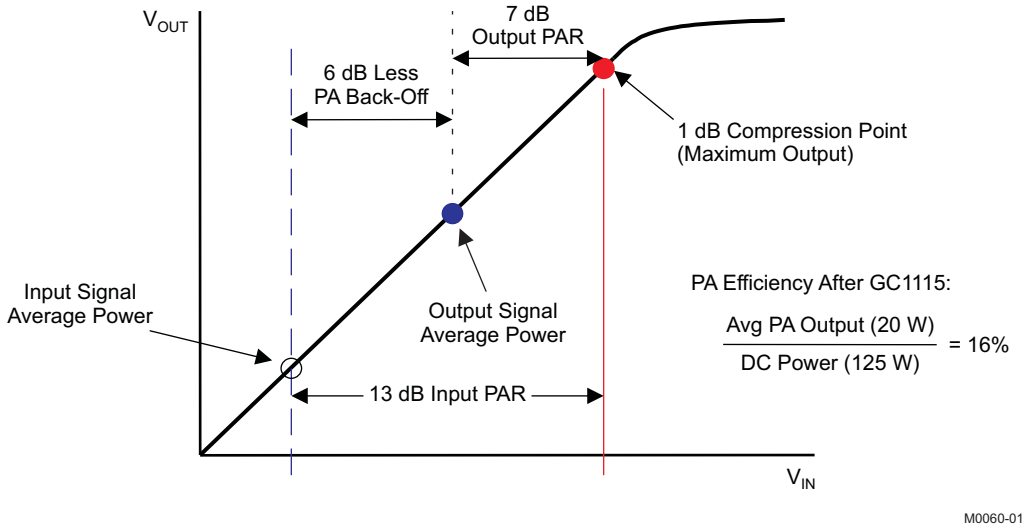


Figure 3. Increasing PA Efficiency

How Peak Cancellation Works: Time Domain View

Figure 4 provides a time-domain example of GC1115 operation. Figure 4 shows the magnitude of the complex input signal in blue, and the magnitude of the complex, peak-reduced signal (after GC1115 processing) in red. *[Note: for users who print this data sheet on a black-and-white printer, the input signal is a solid line, while the output signal is a finely dotted line.]* Notice that for most of the 130 samples in this example, the red output waveform is identical to the blue input waveform. However, the GC1115 has reduced the magnitude of samples around two peaks (one at sample 63, one at sample 95) that exceed the detection threshold. The aqua-colored waveform above the gain threshold line demonstrates the magnitude of the cancellation pulse that was subtracted from the complex input waveform. Notice that the GC1115 PDC stages each have two independent values:

1. Detection threshold: interpolated peaks above the detection threshold are candidates for cancellation
2. Target peak level: detected peaks are reduced to the target peak level. The inverse gain is the amplitude of the complex cancellation coefficients, subtracted from the signal.

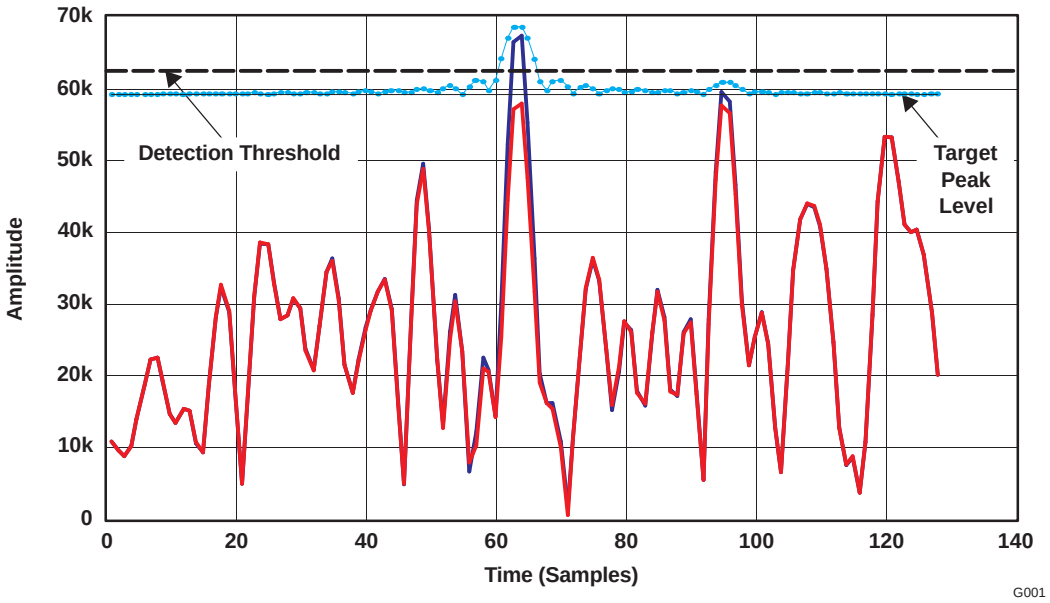


Figure 4. Peak Cancellation Example: Time Domain

How Peak Cancellation Works: Frequency Domain View

Figure 5 demonstrates the frequency-domain effects of peak cancellation. In Figure 5, the original frequency response of the signal is shown in blue. The frequency response of the output signal looks identical and is not shown. The yellow (8 dB PAR), red (7-dB PAR), green (6-dB PAR), and black (5-dB PAR) curves show the spectra of CFR distortion to the in-band signal.

The difference between the input and output signals is the signal distortion. *[Note: for users who print this data sheet on a black-and-white printer, the input spectrum is a solid line, while the output spectra are finely dotted lines.]* Note that the distortion is not significant in the spectral response:

1. The out-of-band energy relates to the cancellation coefficients, to the PAR reduction, and to whether the PAR reduction and cancellation coefficients completely reduce the peak input signal. The out-of-band energy is only a weak function of the target PAR level.
2. The amount of in-band distortion energy rises with increasing difference between the intput PAR and the P
3. ar set point. This is to be expected, because lower PAR thresholds result in more peaks being canceled. Lower PAR levels require more energy to cancel the peaks, thus increasing the distortion level.

Users can determine how much in-band distortion is acceptable by monitoring the effects of peak cancellation at a given output PAR, using two key in-band distortion metrics for CDMA signals:

1. Peak code domain error, or PCDE, and
2. Error vector magnitude, or EVM

Various CFR signal quality metrics (ACLR, PCDE, EVM, CCDF) are further discussed in a subsequent section.

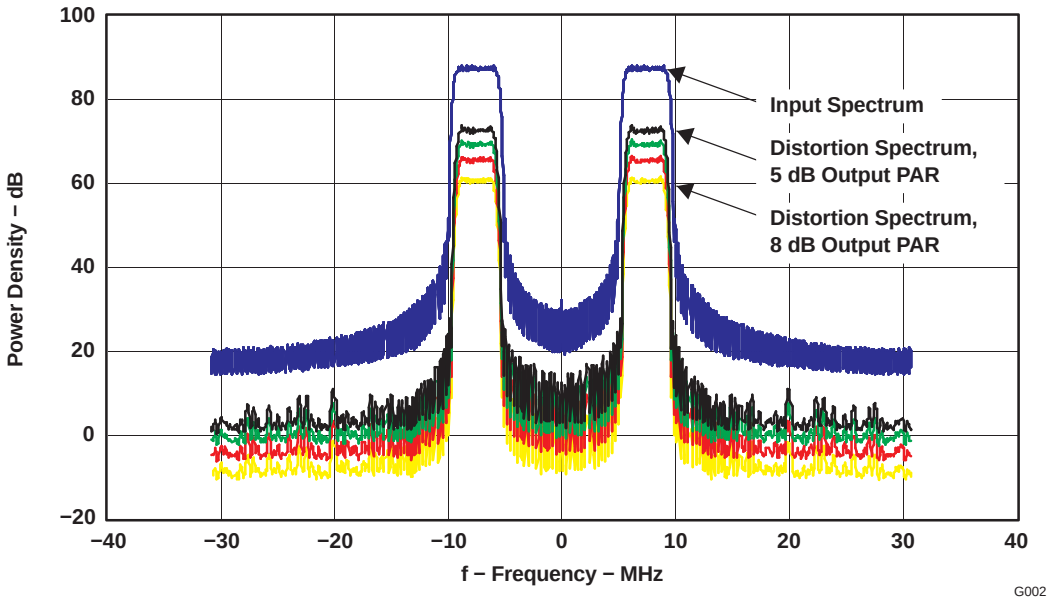


Figure 5. Spectral View of Distortion

SUMMARY OF GC1115 FEATURES

See the GC1115 functional block diagram for the following discussion.

The GC1115 removes peaks from an input signal stream by subtracting user-designed, spectrally shaped cancellation pulses from detected peaks. The peak is qualified when two conditions are met: the magnitude squared value is greater than the set point, and the hysteresis count indicates another larger peak has not occurred.

Cancellation pulses may be real or complex. Real cancellation pulses are used when the input signal spectrum is symmetric, while complex cancellation pulses are used when the input signal spectrum is asymmetric. A single cancellation pulse reduces the peak amplitude of multiple samples around each signal peak while maintaining both the in-band (PCDE, EVM) and out-of-band (ACLR) signal quality requirements. Peaks are cancelled to a user-specified level, which is called the PAR set point. The input signal reduction in peak value also reduces the average signal output by a small amount. The output peak-to-average ratio, PAR, is greater than or equal to the PAR set point. The GC1115 provides four sequential peak detection and cancellation (PDC) stages to remove peaks. The PDC stage thresholds are normally set so that earlier stages remove the largest peaks, while later stages remove smaller, remaining peaks.

The four peak detection cancellation (PDC) stages have a peak-detect, inverse-gain, and cancellation section. The peak detector searches for an interpolated peak within a span of three adjacent samples. The peak search provides an effective 256× interpolation to find the phase of the interpolated peak. When a valid peak is computed, the magnitude squared is compared with the detection threshold. If the peak is above the threshold, a timer is started to further discern adjacent peaks. If the timer finishes before another peak is detected, the peak sample that caused the timer to start is a valid peak, which will be cancelled if a pulse canceller is available. The valid peak magnitude squared and inverse gain threshold scale the pulse generator cancellation coefficients.

Each of the four PDC stages has a programmable number of pulse cancellers, typically 1→4, 2→8, 3→12, 4→8. The assigned pulse generator subtracts the scaled cancellation coefficients from the stage complex data. It is important to consider cancellation coefficient tap length for spectral shaping, latency, and that the individual pulse generator is unavailable (once triggered) for tap-length clock cycles. If all of the PDC resources are cancelling previous or current peaks, the further detected peaks will be missed until a pulse canceller is available.

The GC1115 contains a total of 32 cancellation pulse generators (also called cancelers) per channel that are allocated in groups of four to PDC stages. The normal allocation of the 32 cancelers is as follows:

- PDC stage 1 uses 4 cancelers.
- PDC stage 2 uses 8 cancelers.
- PDC stage 3 uses 12 cancelers.
- PDC stage 4 uses 8 cancelers.

The allocation of cancelers should correspond to the detection threshold (DETECT_TSQD) for each PDC stage. A PDC stage with a lower detection threshold finds more peaks than a PDC stage with a higher detection threshold. As mentioned above, the detection threshold for PDC stages 1 and 2 is set to detect and cancel the largest peaks (typically those more than 1 dB to 2 dB above the PAR set point), while PDC stages 3 and 4 detect and cancel peaks at the desired output PAR (typically between 6 and 8 dB).

Cancellation pulse coefficients are stored in special GC1115 RAM blocks. The GC1115 RAM blocks can store up to 256 real or 128 complex nonsymmetric cancellation pulse coefficients and their associated first and second derivatives. Cancellation coefficients are signed, 12-bit integer values between –2048 and 2047. Each cancellation coefficient RAM supports up to four cancelers. Cancellation pulse generator RAMs assigned to the same stage normally contain the same coefficients, but each of the eight GC1115 cancellation RAMs may contain different coefficients. The cancellation pulse coefficients are normalized, i.e., the largest coefficient magnitude is always 2047 (1.0). However, both the magnitude and the phase of the normalized cancellation pulses are adjusted before the cancellation pulse is subtracted from the input waveform during peak cancellation, ensuring proper alignment with the samples of the input signal.

While the subtraction of cancellation pulses reduces the peak amplitude in the region immediately surrounding a detected peak, this subtraction may also introduce new, smaller, over-threshold peaks. This phenomenon is called *peak regrowth*. Peak regrowth is an infrequent phenomenon whose effects are mitigated by using four serial PDC stages. The PDC detection threshold contour can be used to adjust for peak regrowth between PDC stages 1 through 3. If stage N causes peak regrowth, stage N + 1 and subsequent stages detect and cancel the regrowth peaks, assuming the PDC stages have available pulse cancelers. Regrowth peaks, when they occur, are usually just a few percent (or less) over the PAR threshold.

Following the four PDC stages, the GC1115 also contains an interpolator, soft limiter, and gain block. When enabled, the interpolator supports 2× real, 2× complex, and 4× real interpolation. The real output modes also mix the output frequency by real_output_rate/4. The soft limiter acts as a fixed-length AGC that optionally attenuates the input signal over a fixed-length window of up to 33 samples surrounding the detected over-threshold peak. Under nearly all circumstances, the soft limiter should be bypassed.

The GC1115 operates most efficiently when there are at least 2.5 complex samples per Hertz of bandwidth. For example, a four-carrier (20-MHz) 3G stack should be sampled at no less than 50 Msps, while a single-carrier 3G system can be sampled as low as 12.5 Msps. Under certain circumstances, the input signal can be represented using as few as 2 complex samples per Hz with reduced CFR performance.

The GC1115 contains two flexible, user-programmable snapshot RAMs. The snapshot memories operate either in capture or in histogram mode. In the capture mode, 1024 consecutive I and Q samples are stored in one of the snapshot RAMs. During capture mode, 32 bits per complex sample (16 bits I, 16 bits Q) are captured. The upper 16 bits of the selected input are stored.

Each of the two snapshot RAMs receives samples from one of five user-selected test probe points:

- At the GC1115 input
- After PDC stage 1
- After PDC stage 2
- After PDC stage 3
- After PDC stage 4

When operating in histogram mode, there are 1024 histogram bins. The snapshot RAMs generate a histogram of the real part, the imaginary part, or the power of each complex sample. In histogram mode, millions of samples can be characterized using the snapshot-RAM 32-bit bin counters, thus providing a statistically significant number of events for CCDF and related magnitude distribution measurements.

Each of the GC1115 PDC stages can be bypassed by clearing a corresponding bit in the CONTROL register. Although bypassing a stage removes the peak cancellation capability of that stage, it removes the latency introduced by the peak detection and cancellation process for this stage, and reduces power consumption as well.

The GC1115 includes an on-chip test signal generator that can create dc levels, sawtooth waveforms, and a filtered random number generator with Gaussian-like peak-to-average statistics (i.e., approximately 10-dB PAR). The CRC generator is substituted for the A snd B input poer signals in test mode. Given a specific GC1115 program configuration, a 16-bit CRC-type result can be read from a control register as an expected test result. The CRC generator processes the GC1115 output samples and generates a periodic, 16-bit checksum. Because both the test signal generator and the CRC generator can be synchronized to the same sync source, the presence of a predictable, periodic value in the CRC register indicates that the GC1115 internal circuitry is operating as expected. TI provides several GC1115 configurations (starting test generator register values, sample periods, and expected CRC value at the end of each period) that enable GC1115 users to test for proper GC1115 internal operation. The test signal generator can also be used without the CRC generator, providing a suite of general-purpose test signals (dc, sawtooth, pseudo-LFSR) to exercise ICs attached to the GC1115 output ports, OUT_A and OUT_B.

CFR PERFORMANCE METRICS FOR CDMA SIGNALS: CCDF, ACLR, PCDE, EVM

The GC1115 reduces peaks by subtracting phase- and amplitude-adjusted cancellation coefficients from detected peaks in the input signal whose interpolated magnitude is above a user-specified output PAR threshold.

A graph called the complementary cumulative distribution function, or CCDF, is used to display the probability that a particular sample has a given magnitude. The x-axis of a CCDF curve begins at 0 dB, defined as the average power of the signal, and extends to the peak value of the waveform. The y-axis of a CCDF curve lists the probability (usually on a log scale) that a given complex sample has a certain magnitude. Plotting the *before* and *after* CCDF curves on the same graph demonstrates that the GC1115 peak reduction algorithms have achieved their primary purpose: reducing peaks to a user-specified level. In Figure 6, the input CCDF curve is shown in blue and the output CCDF curve (after GC1115 peak reduction) is shown in red.

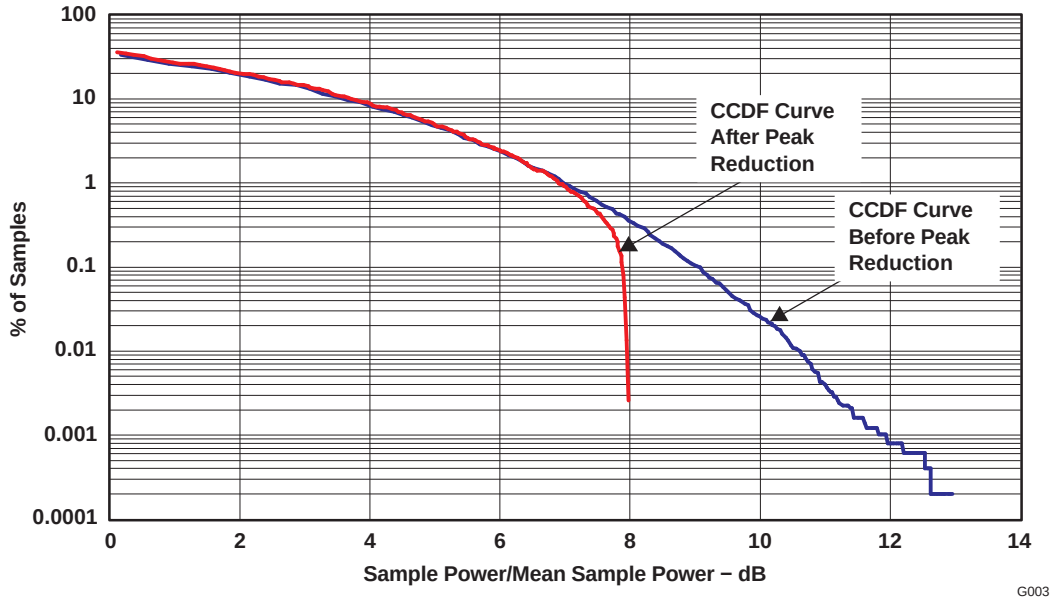


Figure 6. Example Complementary Cumulative Distribution Function (CCDF)

Because the GC1115 modifies the complex values of the input waveform during peak reduction, the peak reduction process introduces certain distortions. GC1115 users have great flexibility in determining the overall distortion level. Distortion can be quantified in several ways:

- By analyzing the spectrum of the distortion (input–output) signal
- By analyzing the out-of-band output noise level in neighboring channels (also called the adjacent channel leakage ratio, or ACLR)
- By measuring an error vector magnitude (EVM) level
- By determining the interference level (caused peak reduction) in the CDMA code *noise floor*; this metric is called the peak code domain error, or PCDE
- By monitoring bit error rate (BER) at the receiver

RESET

The GC1115 supports three kinds of reset:

- PLL reset (only the PLLs are reset)
- Hardware reset (all configuration registers are brought to their RESET values)
- Data-path hardware reset

Setting specific bits in the RESET register activates these resets. Asserting the $\overline{\text{RESET}}$ pin of the GC1115 causes hardware reset. Hardware reset results in the following GC1115 conditions:

- All output pins are put in their high-impedance state.
- All internal registers are reset to their RESET states.
- All state machines are placed in their initial (idle) states.
- No config registers can be modified before clearing the config reset.

GC1115 Initialization Sequence

The GC1115 initialization sequence requires the following register groups to be properly initialized:

1. RESET, PLL_CONTROL, CLK_CONTROL, IO_CONTROL
2. CONTROL, IO_MODE, DECIMATE, RESOURCE_MASK, DELAY_MASK
3. SYNC registers
4. TSQD detection threshold and target peak level registers
5. INTERP registers
6. OUT_GAIN, OUT_OFFSET
7. CANCEL_MODE, CANCEL_LENGTH, CANCEL_DELAY, cancellation coefficients

The following paragraphs describe in general terms how each of these registers is initialized to achieve the desired user-specified peak reduction performance.

RESET, PLL_CONTROL, CLK_CONTROL, IO_CONTROL

The RESET register contains four bits that can individually reset:

- The memory-mapped registers
- The GC1115 internal data path
- The core PLL
- The output PLL

At GC1115 startup, hardware RESET always precedes all other register accesses and this asserts all internal reset registers. Configuration control reset must also be cleared before performing subsequent configuration steps.

After the RESET bits have been asserted, the PLL_CONTROL and CLK_CONTROL registers should be initialized to the desired values.

The GC1115 normally operates at four or eight times the input sample rate, while the output clock rate is determined by several additional factors (decimation, interpolation, and output format and mode). The CLK_CONTROL register determines the PLL multiplying factors that control the GC1115 core clock and output clock frequencies. Finally, the IO_CONTROL register determines the input and output format (2s complement or unsigned), the output enabled state (high-impedance or enabled).

The GC1115 PLLs require a warm-up time of at least 1 s from PLL_CONTROL modification to PLL reset release, and at least 100 s from PLL_CONTROL and CLK_CONTROL modification to PLL reset release before the internal clock is stable.

CONTROL, IO_MODE, DECIMATE, RESOURCE_MASK, DELAY_MASK

The CONTROL register contains six control bits that selectively enable or disable the four PDC stages, the interpolator, and the soft limiter. The DECIMATE register allows users to decimate the input sample stream by 1 (no decimation) or 2. The RESOURCE_MASK register determines which of the eight cancellation pulse SRAMs are updated with new cancel pulse coefficients when a CANCEL_SYNC event occurs. The DELAY_MASK register determines which of the four PDC stages are affected by changes to the CANCEL_DELAY register when the DELAY_SYNC event occurs.

SYNC Registers

The GC1115 contains a group of SYNC registers that control the behavior of thirteen different sync-related functions. A subsequent section discusses GC1115 synchronization alternatives. This section only describes the registers that must be properly initialized prior to GC1115 operation. Four data-path SYNC registers (RCV_SYNC, STAGE_SYNC, DECIM_SYNC, and INTERP_SYNC) **must** be synchronized by a hardware event before the GC1115 can process input samples. Four additional ancillary SYNC registers (DELAY_SYNC, CANCEL_SYNC, RESOURCE_SYNC, and OUTGAIN_SYNC) must be synchronized by a hardware or software event before the GC1115 properly applies cancellation coefficients and gains. The four data-path SYNC registers should be synchronized using a SYNC_A or SYNC_B hardware event, and that the ancillary SYNC registers be synchronized using an SW_TRIGGER software event. Note that the SYNC registers must be initialized before the corresponding hardware or software event occurs. For example, CANCEL_SYNC must be initialized before the cancellation coefficients are transferred from the GC1115 shadow RAM to the internal canceler RAMs.

TSQD (Threshold) and RESOURCE_CNT Registers

The behavior of each PDC stage is controlled by two threshold registers (DETECT_TSQDx and GAIN_TSQDx), where *x* represents a specific stage (from 1 to 4). These 16-bit registers contain the scaled threshold-squared values for the stage detection threshold and target peak level. The 16-bit RESOURCE_CNTx (RESOURCE_CNT) registers contain the number of cancellation resources (from 0 to 8) assigned to the stage. NOTE: if a RESOURCE_CNT register is set to N ($0 \le N \le 8$), that PDC stage can cancel up to $4 \times N$ peaks simultaneously. A *resource* represents a canceler RAM. Four cancellation pulse generators are supported by each canceler RAM.

NOTE:

The *Setting Detection Thresholds and Target Peak Levels* section describes the calculation of the detection and inverse gain thresholds.

Interpolation Registers

A programmable output interpolator follows the four GC1115 PDC stages. The GC1115 interpolator operates in one of four modes:

- Bypass (the default condition)
- Interpolate by 2 (complex output)
- Interpolate by 2 (real output centered at $f_s/4$)
- Interpolate by 4 (real output centered at $f_s/4$)

The interpolator filter coefficients are programmable and must therefore be initialized, even in *bypass* mode, before the GC1115 starts processing input samples. A total of 40 interpolator registers (from D0_COEF0 through D3_COEF9) must be initialized before the GC1115 processes input data.

NOTE:

The *Interpolation Operation* section lists the bypass, interpolate-by-two, and interpolate-by-four coefficient design and coefficient loading.

OUT_GAIN and OUT_OFFSET Registers

The GC1115 output circuitry includes individual I and Q gain and offset registers that allow users to compensate for I/Q imbalances in subsequent D/A converters and/or subsequent analog I/Q modulators. Because the OUT_GAIN and OUT_OFFSET registers are user-programmable, they must be properly initialized before the GC1115 starts processing input samples. OUT_GAIN registers are normally initialized to 0x2000 (gain of 1), and OUT_OFFSET registers are usually initialized to 0x0000.

CANCEL_MODE, CANCEL_LENGTH, CANCEL_DELAY, Cancellation Coefficients

The GC1115 applies user-specified cancellation coefficients to detected peaks. Cancellation coefficients can contain either real or complex values, to support both symmetric and asymmetric input spectra. For this reason, the CANCEL_MODE, CANCEL_LENGTH, and CANCEL_DELAY registers must be properly initialized before the GC1115 begins processing input samples. The cancellation coefficients themselves (in either real or complex format) must be copied to the GC1115 canceler RAMs in a two-step process:

1. The microprocessor or FPGA writes the cancellation coefficients to memory-mapped shadow RAM registers.
2. The shadow RAM registers are copied to one or more (of a total of eight) cancellation pulse RAMs after a CANCEL_SYNC event occurs.

The CANCEL_MODE register determines whether the GC1115 is using real or complex coefficients (corresponding to a symmetric or an asymmetric input spectrum), as well as whether coefficient symmetry is to be exploited. The CANCEL_MODE register also contains a four-bit field that indicates a timeout or hysteresis value. A non-zero timeout value indicates that the PDCs are to examine the envelope of the input signal, rather than the magnitude of the input signal. TI-provided cancel-pulse design functions for MATLAB® automatically calculate the timeout value.

The CANCEL_LENGTH register specifies the number of unique cancellation coefficients used to cancel peaks. The CANCEL_MODE register settings affect the interpretation of CANCEL_LENGTH. The following table describes how CANCEL_LENGTH and CANCEL_DELAY are used, depending on CANCEL_MODE:

Table 1. Relationship Between CANCEL_MODE, CANCEL_LENGTH, and CANCEL_DELAY

CANCEL_MODE	CANCEL_LENGTH	CANCEL_DELAY
0 (Real, unique coefficients)	N (odd, from 15 to 255)	(N + 1)/2
1 (Real, mirrored coefficients)	N (odd, from 15 to 511)	N
1 (Complex, unique coefficients)	N (odd, from 15 to 127)	(N + 1)/2
1 (Complex, mirrored coefficients)	N (odd, from 15 to 255)	(N + 1)/2

OPERATING MODES

The GC1115 supports a variety of operating modes that accommodate a range of input formats, number of channels, and follow-on D/A converter and transmit architectures. Users select a specific input and output operating mode that depends upon:

- The number of channels (one or two)
- The input sampling rate:
  - Up to 130 Msps in 1-channel mode
  - Up to 65 Msps in 2-channel mode
  - Down to 25 Msps in 1-channel parallel mode
  - Down to 12.5 Msps in 1-channel multiplexed mode, or in 2-channel mode
- The input format (parallel or multiplexed)
- The input decimation factor (1 or 2)
- The output interpolator mode (bypass, 2× real, 2× complex, 4× real)
- The output format (parallel, multiplexed, or odd-even; real or complex)
- The internal GC1115 clock rate (up to 320 MHz)
- The PLL multiplier (1×, 2×, or 4×)

The following constraints restrict the allowed combinations of the previously listed parameters:

- Maximum input pin toggling rate: 130 MHz
- Maximum output pin toggling rate: 130 MHz
- Maximum internal GC1115 clock rate: 320 MHz (IN_CLK ×1, ×2, ×4)
- Minimum PLL-driven internal GC1115 clock rate (at divide-by-1 PLL output): 100 MHz
- Minimum IN_CLK rate: 25 MHz (using the 4× PLL multiplier with IN_CLK = 25 MHz generates the 100 MHz minimum PLL output rate, at divide-by-1 PLL output)

Table 2 and Table 3 summarize the available one-channel and two-channel operating modes of the GC1115, respectively.

Table 2. One-Channel Operating Modes (Core Clock = Complex Inpute Rate × 4)

INPUT FORMAT	OUTPUT FORMAT	DECIM	INTERP	PLL MULT	IN_CLK (MHz)	CORE CLK (MHz)	OUT_CLK (MHz)	f_S/4 (MHz)
Parallel(1)	Parallel	1	1	4	25–80	100–320(2)	25–80	NA
Parallel	Parallel	1	2c	4	25–65	100–260	50–130(2)	NA
Parallel	Parallel	2	1	2	50–130(2)	100–260	25–65	NA
Parallel(1)	Parallel	2	2c	2	50–130(2)	100–260	50–130(2)	NA
Parallel	Multiplexed	1	1	4	25–65	100–260	50–130(2)	NA
Parallel	Multiplexed	1	2c	4	25–32.5	100–130	100–130(2)	NA
Parallel	Multiplexed	2	1	2	50–130(2)	100–260	50–130(2)	NA
Parallel	Multiplexed	2	2c	2	50–130(2)	100–260	50–130(2)	NA
Parallel	Odd/even	1	2r	4	25–80	100–320(2)	50–160	12.5–40
Parallel	Odd/even	1	4r	4	25–65	100–260	50–130(2)	25–65
Parallel	Odd/even	2	2r	2	50–130(2)	100–260	25–65	12.5–32
Parallel	Odd/even	2	4r	2	50–130(2)	100–260	50–130(2)	25–65
Multiplexed	Parallel	1	1	2	50–130(2)	100–260	25–65	NA
Multiplexed	Parallel	1	2c	2	50–130(2)	100–260	50–130(2)	NA
Multiplexed	Parallel	2	1	1	100–130(2)	100–130	25–32.5	NA
Multiplexed	Parallel	2	2c	1	100–130(2)	100–130	50–65	NA
Multiplexed(1)	Multiplexed	1	1	2	50–130(2)	100–260	50–130(2)	NA
Multiplexed	Multiplexed	1	2c	2	50–65	100–130	100–130(2)	NA
Multiplexed	Multiplexed	2	1	1	100–130(2)	100–130	50–65	NA
Multiplexed(1)	Multiplexed	2	2c	1	100–130(2)	100–130	100–130(2)	NA
Multiplexed	Odd/even	1	2r	2	50–130(2)	100–260	25–65	12.5–32.5
Multiplexed	Odd/even	1	4r	2	50–130(2)	100–260	50–130(2)	25–32.5
Multiplexed	Odd/even	2	2r	1	100–130(2)	100–130	25–32.5	12.5–16.25
Multiplexed	Odd/even	2	4r	1	100–130(2)	100–130	50–65	25–32.5

(1) Most-common configurations
(2) Limiting condition

Table 3. Two-Channel Operating Modes (Core Clock = Complex Inpute Rate × 8)

INPUT FORMAT	OUTPUT FORMAT	DECIM	INTERP	PLL MULT	IN_CLK (MHz)	CORE CLK (MHz)	OUT_CLK (MHz)	f_S/4 (MHz)
Multiplexed(1)	Multiplexed	1	1	4	25–80	100–320(2)	25–80	NA
Multiplexed	Multiplexed	1	2c	4	25–65	100–260	50–130(2)	NA
Multiplexed	Multiplexed	2	1	2	50–130(2)	100–260	25–65	NA
Multiplexed(1)	Multiplexed	2	2c	2	50–130(2)	100–260	50–130(2)	NA
Multiplexed	Real	1	2r	4	25–65	100–260	50–130(2)	12.5–32.5
Multiplexed	Real	2	2r	2	50–130(2)	100–260	50–130(2)	12.5–32.5

(1) Most-common configurations
(2) Limiting condition

Clock Generation and PLL Operation

The GC1115 internal clock is normally generated through an on-board PLL. The PLL output frequency is 1, 2, or 4 times the frequency of the user-provided IN_CLK signal. For example, if the GC1115 is provided with an input signal stream at 61.44 Msps and the PLL is configured to operate at 4×, the GC1115 internal clock rate is 245.76 MHz. In single-channel mode, the GC1115 requires four core clocks per complex imput sample. In two-channel mode, eight core clocks are required per complex input sample. This rule affects the selection of related decimation and interpolation factors at a given input sampling rate. In addition, the PLL divide-by-1 output frequency of the GC1115 must fall between 100 MHz and 320 MHz. The 100 MHz minimum PLL output clock rate is driven by the PLL design, while the 320 MHz maximum PLL output clock rate is limited by the GC1115 internal logic design.

Alternately, the GC1115 internal PLL can be bypassed, effectively using IN_CLK directly as the GC1115 chip clock. However, in this mode, each input sample must be presented to the input port(s) for four consecutive clock cycles, and the DECIM register must be set to 4. Using this *bypass PLL* configuration allows users to operate the GC1115 at input sampling rates lower than 25 Msps.

NOTE:

Users may have to adjust the clock phase, relative to the data, for proper operation during *bypass PLL* mode. Note that DECIM_SYNC may also have to be enabled on a particular user-selected sample phase (1 of 4 phases) in order to achieve proper operation during bypass PLL mode.

GC1115 users should be aware that the choice of input operating mode affects IN_CLK and thus also affects the PLL clock. Specifically, GC1115 users must ensure the relationships shown in Table 4:

Table 4. IN_CLK, PLL Mode, and Core Clock

IN_CLK (MHz)	PLL MODE	GC1115 CORE CLOCK (MHz)
25–80	4×	100–320
50–130	2×	100–260
100–130	1×	100–130
1–125	Bypass	1–125

GC1115 users should also be aware that the core clock affects the choice of output operating mode. Specifically, GC1115 users must ensure the relationships shown in Table 5. Notice that the odd-even output mode requires that the interpolator operate in one of its two real-output modes: 2x real or 4x real.

Table 5. Core Clock and Interp Mode

GC1115 CORE CLOCK (MHz)	INTERP MODE	OUTPUT FORMAT	OUTPUT CLOCK RATE (MHz)
100–320	Bypass	Parallel	25–80
100–260	Bypass	Multiplexed I/Q	50–130
100–260	2x (complex)	Parallel	50–130
100–130	2x (complex)	Multiplexed I/Q	100–130
100–320	2x (real)	Odd/even	25–80
100–260	4x (real)	Odd/even	50–130

Summary of Registers Affecting GC1115 Clocks

The following GC1115 registers affect the input, core, and output clocks:

- PLL_CONTROL (0x1): determines PLL multiplier (1×, 2×, 4×, bypass) and source of Tx feedback
- CLK_CONTROL (0x2): determines relationship of IN_CLK and OUT_CLK to CORE_CLK
- IO_MODE (0x9): determines the number of channels (1 or 2), the input data format (parallel, multiplexed), and the output data format (parallel, multiplexed, odd-even)
- DECIMATE (0xC): determines the downsampling of the input stream prior to GC1115 processing
- INTERP_CTL (0x80): determines the interpolator operating mode (bypass, 2× complex, 2× real, 4× real). Note that INTERP_CTL and IO_MODE must be consistent to ensure proper operation.

Figure 7 demonstrates the GC111 registers that determine the various internal clock frequencies.

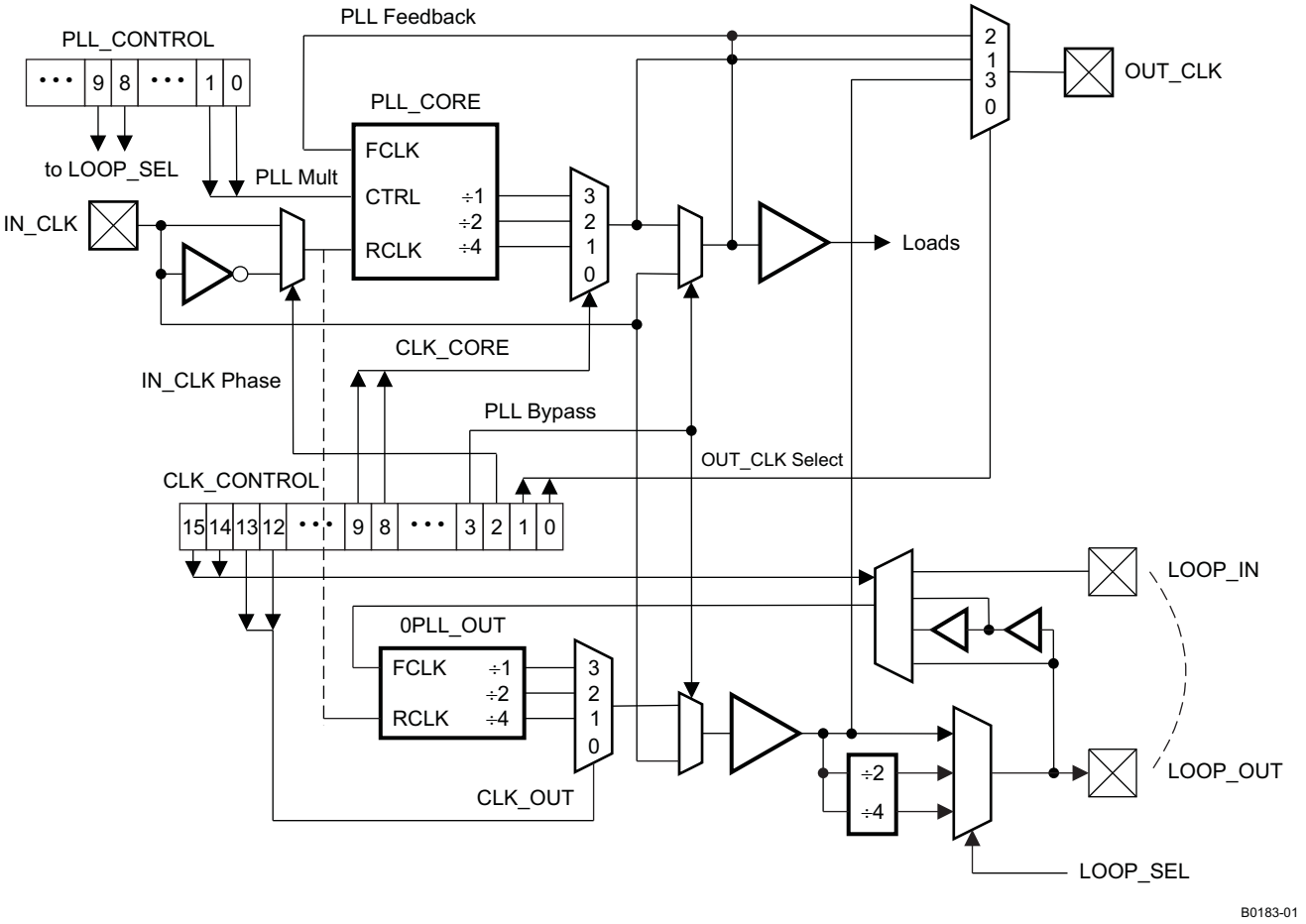


Figure 7. PLL_CONTROL and CLK_CONTROL Registers

DETAILED DESCRIPTION OF GC1115 FUNCTIONAL BLOCKS

Microprocessor Interface Registers and Interrupts

The GC1115 microprocessor interface presents the device as a set of memory-mapped registers to the controlling microprocessor or DSP. All aspects of the GC1115 are configured, monitored, and controlled through these registers. The microprocessor interface consists of a 16-bit bidirectional data bus D[15:0], an 8-bit address bus A[7:0], a write strobe $\overline{WR}$, a read strobe $\overline{RD}$, and a chip select $\overline{CS}$. Two-pin or three-pin mode is selected by using (or grounding) the $\overline{RD}$ pin :

- Three-pin mode ($\overline{RD}$ is used): separate read strobe on $\overline{RD}$ pin and write strobe on $\overline{WR}$ pin
- Two-pin mode ($\overline{RD}$ is grounded): $\overline{WR}$ low (gnd) means *write to GC1115*; $\overline{WR}$ high (3.3 V) means *read GC1115*.

NOTE:

The GC1115 rev0 silicon does not support three-pin mode. Use two-pin mode with rev0 silicon.

Figure 8 demonstrates a glueless interface between a generic Texas Instruments TMS320Cxx DSP chip and a GC1115, assuming that the CG1115 is the only device in the DSP I/O memory space. If the TMS320Cxx DSP controls multiple devices in its I/O memory space, additional external address decoding is required to generate $\overline{CS}$.

The microprocessor or DSP can configure the GC1115 to generate an interrupt at the occurrence of various GC1115 internal events. Please refer to the description of the INT_MAP and INT_MASK registers for a complete description of these events.

The GC1115 microprocessor interface operates at speeds less than 33 MHz. Register read/write accesses are faster than RAM read/write accesses. RAM access is used for snapshot RAM and shadow RAM. See the Timing Parameter Information section for specific information on GC1115 register access rates. RAM access is limited to less than 33 MHz.

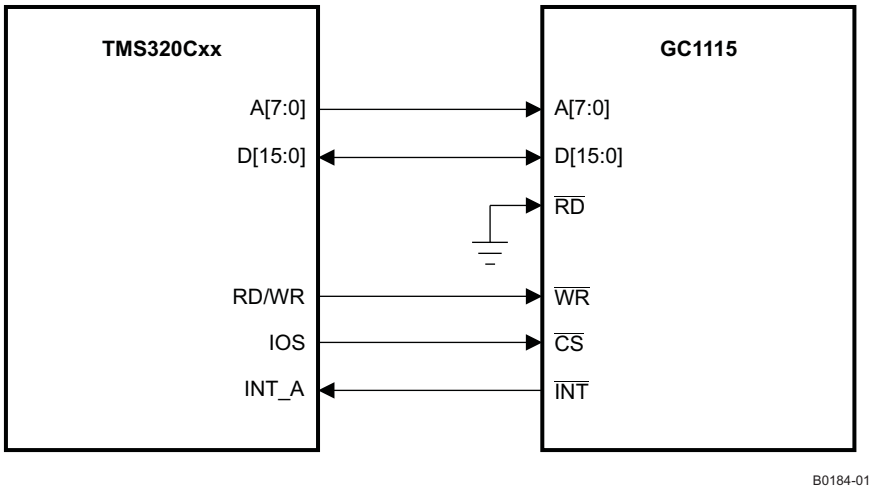


Figure 8. TMS320Cxx – GC1115 Interface

Users configure the GC1115 by writing control information into a set of 16-bit memory-mapped registers. The registers are accessed using the A[7:0], D[15:0], $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ pins of the GC1115. The complete register map is described in detail in a subsequent section. Certain GC1115 registers can be modified at any time during GC1115 operation, while other registers may not be modified until certain conditions are met. Table 6 summarizes these restrictions. The GC1115 strictly enforces the update restrictions listed in Table 6. If a particular update condition is not met, the GC1115 does not update the specified register.

Table 6. GC1115 Register Updates

ADDRESS	NAME	WHEN CAN REGISTER BE UPDATED?
0	RESET	Any time
1	PLL_CONTROL	Any time
2	CLK_CONTROL	Any time
3	CONTROL	Any time
4	INT_MAP	After GC1115 sends an interrupt
5	INT_MASK	Any time
6	MASK_REV	READ-ONLY
7	SW_TRIGGER	Any time
8	IO_CONTROL	Any time
9	IO_MODE	After GC1115 receives IN_CLK
10 (0xA)	POWER_CTL	Any time
11 (0xB)	POWER	READ-ONLY
12 (0xC)	DECIMATE	Any time (after change, output may be invalid for PDC delay samples)
13 (0xD)	TIMER_HI_RST	When timer is OFF
14 (0xE)	TIMER_LO_RST	When timer is OFF
15 (0xF)	CANCEL_MODE	Any time
16 (0x10)	CANCEL_LENGTH	Any time
17 (0x11)	CANCEL_ADDRESS	Any time
18 (0x12)	CANCEL_DATA	Any time
19 (0x13)	RESOURCE_MASK	Any time
20 (0x14)	DELAY_MASK	Any time
21 (0x15)	SIG_GEN_CTL	Any time
22 (0x16)	SIG_GEN_BASE	Any time
23 (0x17)	SIG_GEN_INC	Any time
24 (0x18)	CRC_RESULT	Any time
25 (0x19)	RCV_SYNC	Any time (after change, output may be invalid for PDC delay samples)
26 (0x1A)	STAGE_SYNC	Any time (after change, output may be invalid for PDC delay samples)
27 (0x1B)	DECIM_SYNC	Any time (after change, output may be invalid for PDC delay samples)
28 (0x1C)	TIMER_SYNC	Any time (after change, output may be invalid for PDC delay samples)
29 (0x1D)	DELAY_SYNC	Any time (after change, output may be invalid for PDC delay samples)
30 (0x1E)	CANCEL_SYNC	Any time (after change, output may be invalid for PDC delay samples)
31 (0x1F)	RESOURCE_SYNC	Any time (after change, output may be invalid for PDC delaysamples)
32 (0x20)	INTERP_SYNC	Any time (after change, output may be invalid for PDC delay samples)
33 (0x21)	OUTGAIN_SYNC	Any time
34 (0x22)	OUTPIN_SYNC	Any time (after change, output may be invalid for PDC delay samples)
35 (0x23)	SIG_GEN_SYNC	Any time
36 (0x24)	SNAP_A_SYNC	Any time
37 (0x25)	SNAP_B_SYNC	Any time
48 (0x30)	RESOURCE_CNT1	Any time(1)
49 (0x31)	DETECT_TSQD1	Any time(2)
50 (0x32)	GAIN_TSQD1	Any time(2)
51 (0x33)	CANCEL_DELAY1	Any time(1)
56 (0x38)	RESOURCE_CNT2	Any time(1)
57 (0x39)	DETECT_TSQD2	Any time(2)
58 (0x3A)	GAIN_TSQD2	Any time(2)

(1) When PDC stage is bypassed
(2) May cause PDC stage upset if programmed during stage operation

Table 6. GC1115 Register Updates (continued)

ADDRESS	NAME	WHEN CAN REGISTER BE UPDATED?
59 (0x3B)	CANCEL_DELAY2	Any time(1)
64 (0x40)	RESOURCE_CNT3	Any time(1)
65 (0x41)	DETECT_TSQD3	Any time(2)
66 (0x42)	GAIN_TSQD3	Any time(2)
67 (0x43)	CANCEL_DELAY3	Any time(1)
72 (0x48)	RESOURCE_CNT4	Any time(1)
73 (0x49)	DETECT_TSQD4	Any time(2)
74 (0x4A)	GAIN_TSQD4	Any time(2)
75 (0x4B)	CANCEL_DELAY4	Any time(1)
96 (0x60)	SNAP_A_CONTROL	Any time
97 (0x61)	SNAP_A_STATUS	READ-ONLY
98 (0x62)	SNAP_A_ADDRESS	Any time
99 (0x63)	SNAP_A_DATA	Any time
100 (0x64)	SNAP_A_MINVAL	When Snap A is OFF
101 (0x65)	SNAP_A_MAXVAL	When Snap A is OFF
102 (0x66)	SNAP_A_SCALER	When Snap A is OFF
103 (0x67)	SNAP_A_HISTCOUNT	When Snap A is OFF
112 (0x70)	SNAP_B_CONTROL	Any time
113 (0x71)	SNAP_B_STATUS	READ-ONLY
114 (0x72)	SNAP_B_ADDRESS	Any time
115 (0x73)	SNAP_B_DATA	Any time
116 (0x74)	SNAP_B_MINVAL	When Snap B is OFF
117 (0x75)	SNAP_B_MAXVAL	When Snap B is OFF
118 (0x76)	SNAP_B_SCALER	When Snap B is OFF
119 (0x77)	SNAP_B_HISTCOUNT	When Snap B is OFF
127 (0x7F)	COUNTER_VAR	Any time
128 (0x80)	INTERP_CTL	When interpolator is bypassed
129 (0x81)	(reserved)	(reserved)
130 (0x82)	D0_COEF0	When interpolator is bypassed
. . .	. . .	. . .
169 (0xA9)	D3_COEF9	When interpolator is bypassed
192 (0xC2)	SOFT_LENGTH	When soft limiter is bypassed
193 (0xC3)	SOFT_TSQD	When soft limiter is bypassed
194 (0xC4)	SOFT_COEF0	When soft limiter is bypassed
. . .	. . .	. . .
209 (0xD1)	SOFT_COEF15	When soft limiter is bypassed
210 (0xD2)	SOFT_TAB_SCALE	When soft limiter is bypassed
211 (0xD3)	SOFT_INVGAIN0	When soft limiter is bypassed
. . .	. . .	. . .
242 (0xF2)	SOFT_INVGAIN31	When soft limiter is bypassed
243 (0xF3)	OUT_GAIN0	When soft limiter is bypassed
244 (0xF4)	OUT_GAIN1	When soft limiter is bypassed
245 (0xF5)	OUT_OFFSET_I0	When soft limiter is bypassed
246 (0xF6)	OUT_OFFSET_Q0	When soft limiter is bypassed
247 (0xF7)	OUT_OFFSET_I1	When soft limiter is bypassed
248 (0xF8)	OUT_OFFSET_Q1	When soft limiter is bypassed

Setting Detection Thresholds and Target Peak Levels

The most obvious user-specified parameter for a CFR processor is the desired output PAR. The output PAR determines the largest sample magnitude on the output ports of the GC1115. Ultimately, the PAR determines the maximum Vin voltage of the PA. This maximum value is then adjusted to fit just under the 1-dB compression point of the PA. The average power of the GC1115 input samples (0-dB point on the CCDF curve) can be calculated from a group of input samples. TI provides a MATLAB function that uses a group of input samples to calculate the 16-bit threshold-squared values that are loaded into the GC1115 DETECT_TSQD and GAIN_TSQD registers (one pair of registers for each of four stages; total of eight TSQD registers). Upon request, TI will provide the MATLAB source code (m-file) for the threshold calculations based on input samples.

Alternatively, GC1115 users can use the GC1115 built-in hardware power measurement capability to determine the average input power. The detection thresholds and target peak levels can then be calculated from the average input power.

GC1115 threshold settings are based on a threshold SQUARED (power) value, not a threshold (magnitude) value. The following example demonstrates how the GC1115 threshold-squared values are calculated, using the MATLAB language:

```
%
%    Calculate the average power of the complex input array x, and the desired fractional (magnitude)
%    threshold, given the user-specified target peak level (in dB).

avgMag     = sqrt(mean(abs(x).^2));
frac    = avgMag * 10 ^ (dB_target / 20);

%
%     Derive the following threshold-related values from the target PAR magnitude:
%
%    thresh     signed, 14-bit threshold value (a magnitude!)
%    threshSqd  threshold set as a 16-bit mag-squared value (reduced from a 29-bit mag-squared value)
%

thresh      = floor (frac * 2^13);          %  set the threshold relative to signed 14-bit samples
threshSqd   = floor((thresh ^ 2)/ (2^13));  %  mag-sqd of a 14-bit value = 28 bits plus an add = 29
                                            %  bits
                                            %  Divide by 2^13 to convert to 16-bit thresh-sqd value
```

The GC1115 uses four sequential PDC stages to achieve the desired output PAR. For output PAR levels below 8 dB, both EVM and PCDE performance is improved if the earlier stages have higher detection thresholds (set to 8 dB or 7 dB), while later stages contain the final, desired threshold (7 dB, 6 dB, or 5 dB, for instance). In all cases, the GAIN_TSQD registers should be set to the target peak level (desired output PAR). When the desired output PAR is at or above 8 dB, the DETECT_TSQD and GAIN_TSQD registers are set as shown in Table 7:

Table 7. Detection and Gain Thresholds, PAR ≥ 8 dB

STAGE	DETECT_TSQD	GAIN_TSQD
1	(Input PAR – PAR set pt) × 2/3	my_tsqd
2	(Input PAR – PAR set pt) × 1/3	my_tsqd
3	my_tsqd	my_tsqd
4	my_tsqd	my_tsqd

NOTE:

The TSQD detection threshold for stage 3 is used for both stage 3 and stage 4. This is a hardware limitation.

When the desired output PAR is below 8 dB, the recommended DETECT_TSQD and GAIN_TSQD register settings are set as shown in Table 8:

Table 8. Detection and Gain Thresholds, PAR < 8 dB

STAGE	DETECT_TSQD	GAIN_TSQD
1	min(8 dB, my_tsqd + 2 dB)	my_tsqd
2	min(7 dB, my_tsqd + 1 dB)	my_tsqd
3	my_tsqd	my_tsqd
4	my_tsqd	my_tsqd

GC1115 Cancellation Filter Design

The GC1115 can support real and complex filter design, and symmetric and asymmetric filters. The choice the the filter type depends on the application; normally, the filter design is a real, low-pass filter.

The GC1115 filter design has a clock rate, pass-band frequency, stop-band frequency, and number of coefficients; in addition, if there are multiple carriers, additional requirements must be considered. After the initial low-pass design, a TI-supplied MATLAB program converts the coefficients into the coefficient, first-, and second-derivative formats for the GC1115 cancellation filter.

Standard designs:

- Single carrier at 0IF → real-coefficient, low-pass (or RRC) design (see Figure 9)
- Multiple carriers centered at 0IF → real-coefficient, low-pass design; filter is designed for composite bandwidth (see Figure 10 and Figure 11).
- Single carrier at offset frequency → the initial filter design is the single carrier at 0IF; the offset frequency is mixed with the coefficients in the TI-supplied MATLAB program; the result is a complex filter.
- Multiple carrier with frequency gaps → the individual carrier filter is designed as if it is at 0IF; each of the offset frequencies is mixed with the coefficients in the TI supplied MATLAB program; the result is a complex filter.

Other designs:

- Single wideband carriers with 2× oversampling and specific ACLR requirements can use a special real filter to place distortion energy other than in the pass band.
- Multiple carriers centered at 0IF that tend to distort carriers at different distortion levels can use multiband filter techniques to equalize the carrier distortions (see Figure 12).

Filter Design

The cancellation filter has a sample rate based on the input to the GC1115, the input mode, and whether the input is decimated. The equation for filter clock rate (FCR) follows:

$$FCR = InputClockFrequency/(is\_muxed) \times 1 / (input\ dec + 1)$$

where

is_muxed = 1 if input is not interleaved
is_muxed = 2 if input is interleaved

Number of Coefficients

The number of GC1115 cancellation coefficients can reduce the digital filter error from the desired response. There is a tradeoff between the latency and the spectrum accuracy. In the low-pass design, typically the number of coefficients ranges from 121 to 249. It must be an odd number.

Stop-Band Rejection and Stop-Band Frequency

In a single-carrier design, this is typically 50 kHz less than the pass-band frequency. In some designs, part of the transition band is used. The stop-band rejection is usually set for 25 dB to 40 dB during the design. In multiple carriers at 0IF, the pass-band frequency is designed for the composite bandwidth.

Pass-Band Frequency

The pass-band frequency is adjusted for the maximum bandwidth that supports the desired stop-band rejection. In multiple carriers at 0IF, the pass-band frequency is designed for the composite bandwidth.

The filter can be designed for a single-carrier range or can have individual carrier allocations with gaps in frequency.

Scaling and Rounding

The coefficients must be scaled so the center tap is 2047. The coefficients must be rounded and saturated to 2047 to –2048. Figure 9 is an example of a single-carrier cancellation filter design. Figure 10 is an example of a cancellation filter design for multiple carriers centered at 0IF. Figure 11 is an example of a cancellation filter design for multiple carriers with frequency gaps. Figure 12 is an example of a cancellation-filter design for multiple carriers using a single, wide filter. Note that in this case, the filter places noise energy in the gaps between carriers.

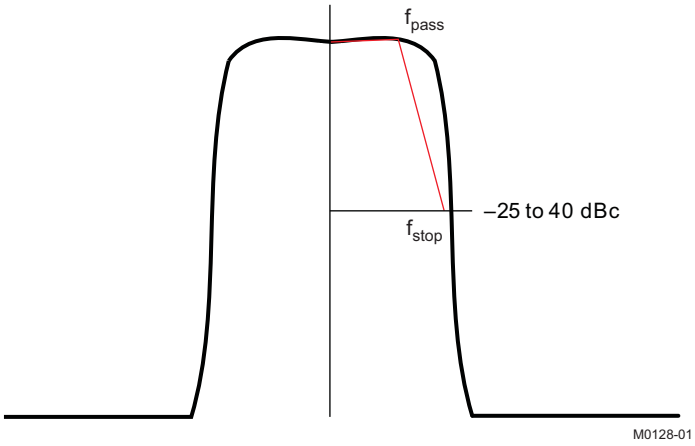


Figure 9. GC1115 Cancellation Filter Single-Carrier Design

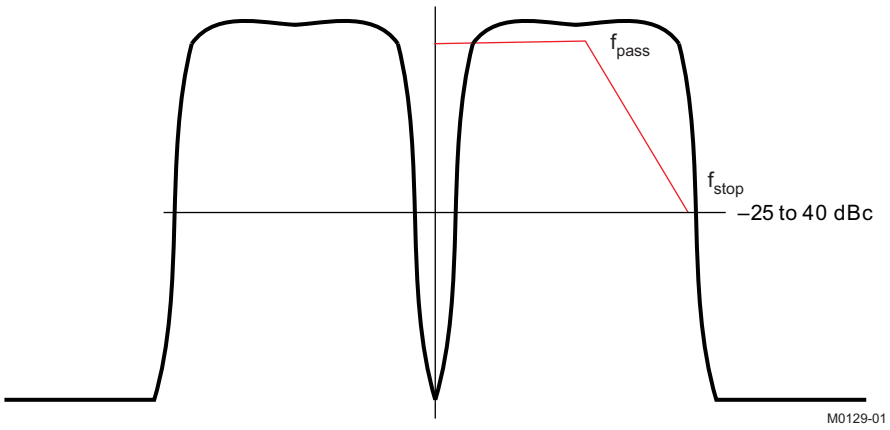


Figure 10. GC1115 Cancellation-Filter Multicarrier Design Using Two Single-Carrier Filters

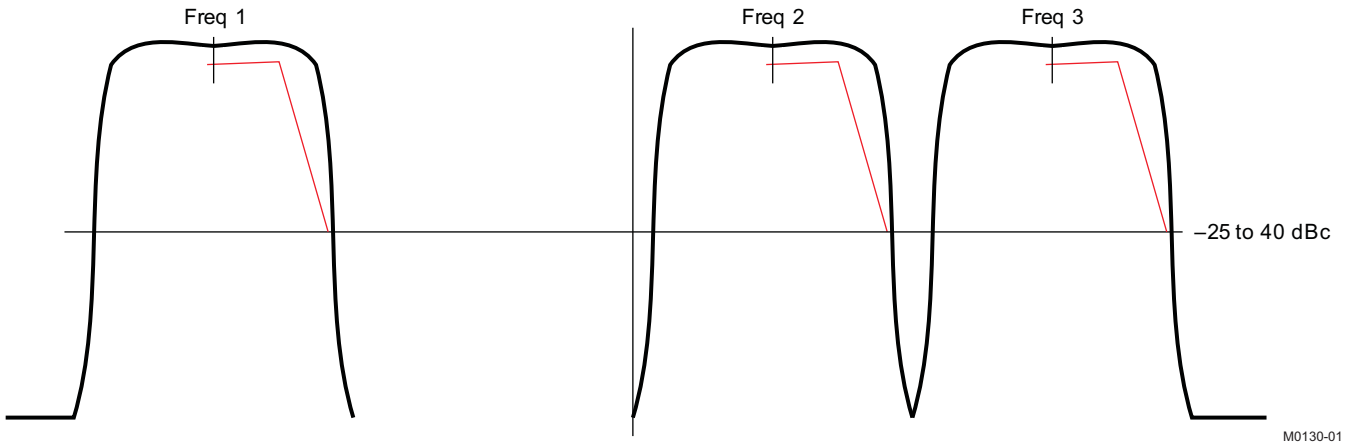


Figure 11. GC1115 Cancellation-Filter Asymmetric Multicarrier Design Using Three Single-Carrier Filters

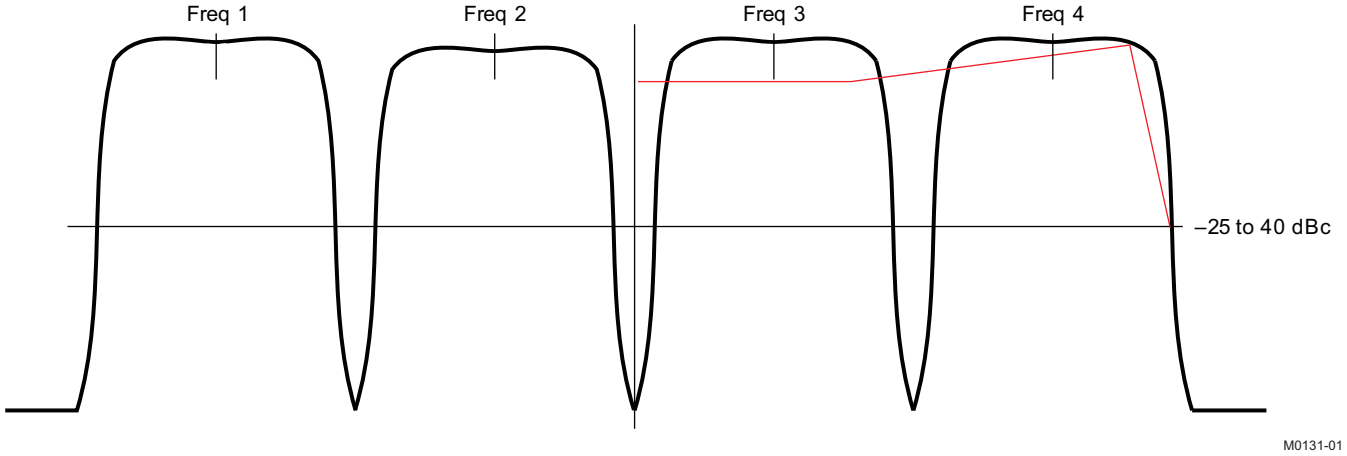


Figure 12. GC1115 Cancellation Filter Design Using a Single Multiband Filter

The input coefficients are convolved with an additional seven-tap set of coefficients. This limits the input coefficients to:

Coefficient Type	Number
Real, symmetric	505
Real, nonsymmetric	249
Complex, symmetric	249
Complex, nonsymmetric	121

NOTE:

See the SLWC090 for a MATLAB script that calculates the proper first and second derivatives from user-designed cancellation coefficients.

Cancellation Coefficient Shadow RAM

The GC1115 uses a derivative-based approximation method to calculate highly accurate phase shifts of the cancellation pulse. The approximation method requires not only the cancellation coefficients themselves to be stored in the GC1115, but also the first and second derivatives of the coefficients. The cancellation coefficient shadow RAM contains 768 unique addresses that hold up to 256 unique cancellation coefficients and their first and second derivatives.

Shadow RAM is physically distinct from canceler RAM. This distinction is fully explained in a following section entitled *Shadow RAM and Canceler RAMs*. The microprocessor or DSP controlling the GC1115 can only access the shadow RAM.

Cancellation coefficient shadow RAM is used differently, depending on the CANCEL_MODE setting (real or complex coefficients; unique or mirrored coefficients). Table 9, Table 10, and Table 11 illustrate how cancellation coefficients are stored and accessed in the GC1115 cancellation coefficient shadow RAM.

Table 9. Real, Unique Coefficients

TYPE OF DATA	ADDRESS	COEFFICIENT
Coefficients	0	coef[0]
	1	coef[1]
	2	coef[2]
	. . .	. . .
	CANCEL_LENGTH – 1	coef[CANCEL_LENGTH – 1]
First derivative	256	deriv1[0]
	257	deriv1[1]
	258	deriv1[2]
	. . .	. . .
	255 + CANCEL_LENGTH	deriv1[CANCEL_LENGTH – 1]
Second derivative	512	deriv2[0]
	513	deriv2[1]
	514	deriv2[2]
	. . .	. . .
	511+ CANCEL_LENGTH	deriv2[CANCEL_LENGTH – 1]

Coefficient access pattern:

coef[0], coef[1], …, coef[CANCEL_LENGTH – 2], coef[CANCEL_LENGTH – 1]

Table 10. Real, Mirrored Coefficients

TYPE OF DATA	ADDRESS	COEFFICIENT
Coefficients	Same as Table 9	Same as Table 9
First derivative	Same as Table 9	Same as Table 9
Second derivative	Same as Table 9	Same as Table 9

Coefficient access pattern:

coef[0], coef[1], …, coef[CANCEL_LENGTH – 2], coef[CANCEL_LENGTH – 1], coef[CANCEL_LENGTH – 2], coef[CANCEL_LENGTH – 3], …, coef[1], coef[0].

Table 11. Complex Coefficients

TYPE OF DATA	ADDRESS	COEFFICIENT
Complex coefficients (real part)	0	coef_re[0]
	1	coef_re[1]
	2	coef_re[2]
	. . .	. . .
	CANCEL_LENGTH – 1	coef_re[CANCEL_LENGTH – 1]
Complex coefficients (imaginary part)	128	coef_im[0]
	129	coef_im[1]
	130	coef_im[2]
	. . .	. . .
	127 + CANCEL_LENGTH	coef_im[CANCEL_LENGTH – 1]
First derivative (real part)	256	deriv1_re[0]
	257	deriv1_re[1]
	258	deriv1_re[2]
	. . .	. . .
	255 + CANCEL_LENGTH	deriv1_re[CANCEL_LENGTH – 1]
First derivative (imaginary part)	384	deriv1_im[0]
	385	deriv1_im[1]
	386	deriv1_im[2]
	. . .	. . .
	383 + CANCEL_LENGTH	deriv1_im[CANCEL_LENGTH – 1]
Second derivative (real part)	512	deriv2_re[0]
	513	deriv2_re[1]
	514	deriv2_re[2]
	. . .	. . .
	511 + CANCEL_LENGTH	deriv2_re[CANCEL_LENGTH – 1]
Second derivative (imaginary part)	640	deriv2_im[0]
	641	deriv2_im[1]
	642	deriv2_im[2]
	. . .	. . .
	639 + CANCEL_LENGTH	deriv2_im[CANCEL_LENGTH – 1]

Coefficient access pattern:

{coef_re[0], coef_im[0]}, {coef_re[1], coef_im[1]}, …,
{coef_re[CANCEL_LENGTH – 1], coef_im[CANCEL_LENGTH – 1]}

Writing Cancellation Coefficients to Shadow RAM

The GC1115 uses the CANCEL_ADDR register as a coefficient memory pointer to access cancellation coefficient shadow RAM. This indirect addressing method requires only two registers (CANCEL_ADDR and CANCEL_DATA) in the GC1115 memory map, while allowing GC1115 users access to 768 unique shadow RAM addresses.

To access a particular shadow RAM location, the microprocessor or DSP that controls the GC1115 first writes the desired address into the CANCEL_ADDR register. To write to the shadow RAM, the microprocessor or DSP then writes the desired coefficient value to the CANCEL_DATA register. A write to (or read from) the CANCEL_DATA register automatically post-increments the address in the CANCEL_ADDR register. The following example demonstrates how the CANCEL_ADDR auto-increment feature is used to initialize the first three cancellation coefficient shadow RAM locations mem[0], mem[1], and mem[2]:

STEP	REGISTER	VALUE	CANCEL_ADDR AUTO-INCREMENT	COMMENTS
1	CANCEL_ADDR	0	0	addr = 0
2	CANCEL_DATA	0x111	0→1	mem[0] = 0x111
3	CANCEL_DATA	0x456	1→2	mem[1] = 0x456
4	CANCEL_DATA	0x321	2→3	mem[2] = 0x321

Alternately, the microprocessor or DSP software can specify a shadow RAM address (0..767) with each CANCEL_DATA access. This mode is useful when updating non-contiguous shadow RAM addresses. The following example demonstrates how the CANCEL_ADDR direct-addressing mode is used to initialize the first three cancellation coefficient shadow RAM locations mem(0), mem(2), and mem(1), in non-sequential order (just to demonstrate the direct addressing capability):

STEP	REGISTER	VALUE	CANCEL_ADDR AUTO-INCREMENT	COMMENTS
1	CANCEL_ADDR	0	0	addr = 0
2	CANCEL_DATA	0x111	0→1	mem[0] = 0x111
3	CANCEL_ADDR	2	2	addr = 2
4	CANCEL_DATA	0x321	2→3	mem[2] = 0x321
5	CANCEL_ADDR	1	1	addr = 1
6	CANCEL_DATA	0x456	1→2	mem[1] = 0x456

Shadow RAM and Canceler RAMs

The GC1115 contains eight unique canceler RAM memories that hold cancellation coefficients and their derivatives. Each of the eight unique canceler RAMs can be accessed up to four times per IN_CLK clock period, and each of the cancelers has its own canceler RAM pointer. This structure allows four cancelers to be supported by one canceler RAM per IN_CLK clock period. This structure also makes it possible to store eight different cancellation coefficient sets in the GC1115 (although this option is not recommended). With a total of eight canceler RAMs, the GC1115 can have up to 32 cancelers running independently per channel (four cancelers per canceler RAM per channel). Cancellation pulse resources are allocated in groups of four per channel, i.e., one canceler RAM at a time, to the four PDC stages. The registers RESOURCE_CNT1 thru RESOURCE_CNT4 specify how many canceler RAMs are allocated to each PDC stage. The total number of resources cannot exceed 8.

The CANCEL_ADDR and CANCEL_DATA registers are used to write to an independent *shadow RAM*. Using the CANCEL_ADDR and CANCEL_DATA registers, the GC1115 controlling microprocessor or DSP writes cancellation coefficients and derivative values to this shadow RAM, and not directly to the canceler RAMs themselves. When a COEF_SYNC synchronization event occurs, the contents of the shadow RAM are copied (one value per internal GC1115 clock cycle) to those canceler RAMs whose corresponding bit is set in the RESOURCE_MASK register. Using the RESOURCE_CNT registers, cancelers may be separately taken off-line, updated, and brought back on-line in seamless operation. This approach ensures that the GC1115 is never without cancellation resources.

To summarize, cancellation coefficients and their derivatives are written to canceler RAMs as follows:

1. Using CANCEL_ADDR and CANCEL_DATA, write up to 768 canceler coefficients and their derivatives to shadow RAM.
2. Using the RESOURCE_MASK register, specify which canceler RAMs are to be initialized from shadow RAM when the COEF_SYNC event occurs.
3. Using the COEF_SYNC register, specify which event (SW_TRIGGER, timer, SYNC_A, SYNC_B, etc.) is to trigger the COEF_SYNC event.
4. After the COEF_SYNC event occurs, the GC1115 copies 3 × CANCEL_LENGTH values from shadow RAM to the canceler RAMs selected by the RESOURCE_MASK register. During each internal clock cycle, one shadow RAM value is copied simultaneously to the canceler RAMs enabled by their corresponding RESOURCE_MASK bits. The total canceler RAM copy time depends on CANCEL_LENGTH and on the time spent waiting for the selected RAMs to become idle, not on how many canceler RAMs are enabled for update in the RESOURCE_MASK register.
5. After the GC1115 has copied 3 × CANCEL_LENGTH values from shadow RAM to canceler RAM, the microprocessor or DSP can optionally be interrupted, if bit 6 of INT_MASK was set prior to Step 3. Alternatively, bit 6 of INT_MAP can be polled to determine when the shadow RAM copy completes.

Once the shadow RAM has been initialized, the process of copying the shadow RAM values to the canceler RAMs occurs very quickly. For example, assuming an IN_CLK frequency of 61.44 MHz (16.3 ns), a GC1115-internal clock rate of 4 × 61.44 MHz (4.1 ns), and a CANCEL_LENGTH of 87, the GC1115 only requires 3 × 87 × 4.1 ns = 1.07 s to initialize all RESOURCE_MASK-enabled canceler RAMs, assuming all cancelers to be updated were idle when the CANCEL_SYNC trigger occurred.

Software Timer

The GC1115 provides a flexible, user-controlled software timer that can serve as a programmable synchronization source (see Synchronization Registers, and the TIMER_HI_RST, TIMER_LO_RST, and TIMER_SYNC register descriptions. The timer is controlled through the TIMER_SYNC register, which allows users to select the event that triggers the timer. Before enabling the timer to start (via the TIMER_CTL register), the user specifies a timer period using the TIMER_HI_RST and TIMER_LO_RST registers. The timer is decremented with each internal clock edge (normally at a frequency of 4 × IN_CLK). When the TIMER_SYNC event occurs, the timer copies the 32-bit values contained in TIMER_HI_RST and TIMER_LO_RST into a GC1115-internal 32-bit timer register. This 32-bit timer is then decremented with each internal chip clock (normally, chip clock = 4 × IN_CLK). When the timer reaches zero, the timer is reloaded from TIMER_HI_RST and TIMER_LO_RST (periodic timer event), or the timer is disabled (for one-time timer events). Bit 15 of the TIMER_SYNC register determines the timer mode (periodic or one-time).

The microprocessor or DSP can be interrupted when the timer expires by setting bit 4 of INT_MASK. It is expected that the software-initiated *timer start* operation most often is used in one-time mode (and not periodic mode), thus giving the microprocessor or DSP time to monitor a GC1115 event, such as reading the snapshot RAM contents.

Signal Generator and CRC Generator

The GC1115 contains a simple signal generator that can be used to drive the GC1115 PDC stages. The signal generator capability is useful when debugging a board containing a GC1115, or to debug the GC1115 itself. When enabled, the signal generator output drives the input of PDC stage 1. The signal generator can be configured to generate one of several types of signals:

- A dc level
- A sawtooth waveform
- A pseudo-LFSR waveform with PAR of approximately 10 dB

The signal generator is configured using the SIG_GEN_CTL, SIG_GEN_BASE, and SIG_GEN_INC registers. The signal generator period is determined by SIG_GEN_CTL, SIG_GEN_BASE, SIG_GEN_INC, and SIG_GEN_SYNC registers. In LFSR mode, the LFSR generator and the CRC generators are reset whenever a SIG_GEN_SYNC trigger occurs. Because the GC1115 pipeline must contain predictable information, the minimum SIG_GEN_SYNC period should be at least 1000 IN_CLK periods.

The GC1115 also contains a cyclic redundancy check (CRC) generator. The CRC generator receives its input from the output of PDC stage 4. The CRC generator is enabled whenever the signal generator is enabled. The CRC generator can also be fed using user-provided data on input ports A and B, and by setting SIG_GEN_CTL to 0x3. CRC generation using sawtooth or LFSR data provides a predictable, periodic way to determine proper internal GC1115 operation, independent of a user-provided input sequence. Note that the LFSR sequence is not band-limited, but the distribution of its magnitudes is Gaussian.

Contact TI to receive an appropriate set of CRC initialization and test parameters.

Snapshot RAM Operation

The GC1115 contains two independent, identically operating snapshot RAMs for signal capture and histogram generation. The snapshot RAMs operate in one of three modes:

- No operation (OFF)
- Capture mode (RAM is configured as a 2K × 16-bit memory, with 1K each of I and Q samples interleaved)
- Histogram mode (RAM is configured with even addresses storing the 16 MSBs, and odd addresses storing the 16 LSBs, of 32-bit counters)

These RAMs can capture or histogram sample streams at five independent locations within the GC1115:

- At the GC1115 input (after the decimator and prior to stage 1)
- After PDC stage 1
- After PDC stage 2
- After PDC stage 3
- After PDC stage 4

In capture mode, the 16 MSBs of each 18-bit sample are stored in the snapshot RAM as follows:

ADDRESS	VALUE
i = 0, 2, 4, …	I[17:2] (sixteen MSBs of 18-bit I value)
j = 1, 3, 5, …	Q[17:2] (sixteen MSBs of 18-bit Q value)

In histogram mode, each snapshot RAM monitors the output of a function generator that generates one of the following values from its I and Q source samples:

- I sample
- Q sample
- Magnitude squared (I × I + Q × Q)

The arithmetic processing of samples in histogram mode is shown in Figure 13. First, the user-selected function of the complex input sample I + jQ is calculated. Second, the calculated value is compared to SNAP_MINVAL and SNAP_MAXVAL. If the calculated value is not within the desired range, no further action occurs for this sample. If the calculated value is within the desired range, then SNAP_MINVAL is subtracted from the calculated value, and the result is shifted by SNAP_SCALE to generate a 10-bit histogram index (between 0 and 1023).

Consider a histogram example in which users are interested in monitoring the power of samples above the average power (to calculate CCDF, for instance). Assume that the average power corresponds to 16-bit samples with magnitude-squared values of $2 \times (10{,}000^2)$, or 2×10^8. For 16-bit samples, the largest possible magnitude-squared value is $2 \times 32{,}767^2 = 2.14 \times 10^9$. The GC1115 removes the lower 16 bits from each 32-bit magnitude-squared value, so that the function generator output is always in the signed 16-bit range. The initial values for SNAP_MINVAL, SNAP_MAXVAL, and SNAP_SCALE are calculated as follows:

- SNAP_MINVAL = 3052 ($2 \times [10{,}000^2] / 2^{16}$)
- SNAP_MAXVAL = 32,767 ($2 \times [32{,}767^2] / 2^{16}$)
- SNAP_SCALE = shift value in bits $2^{15} \rightarrow 2^9$ (6)

If users want to monitor the input signal for 30 seconds (about 1.8×10^9 samples – plenty of statistical significance), SNAP_HISTCOUNT = 27,465 ($1.8 \times 10^9 / 65{,}536$).

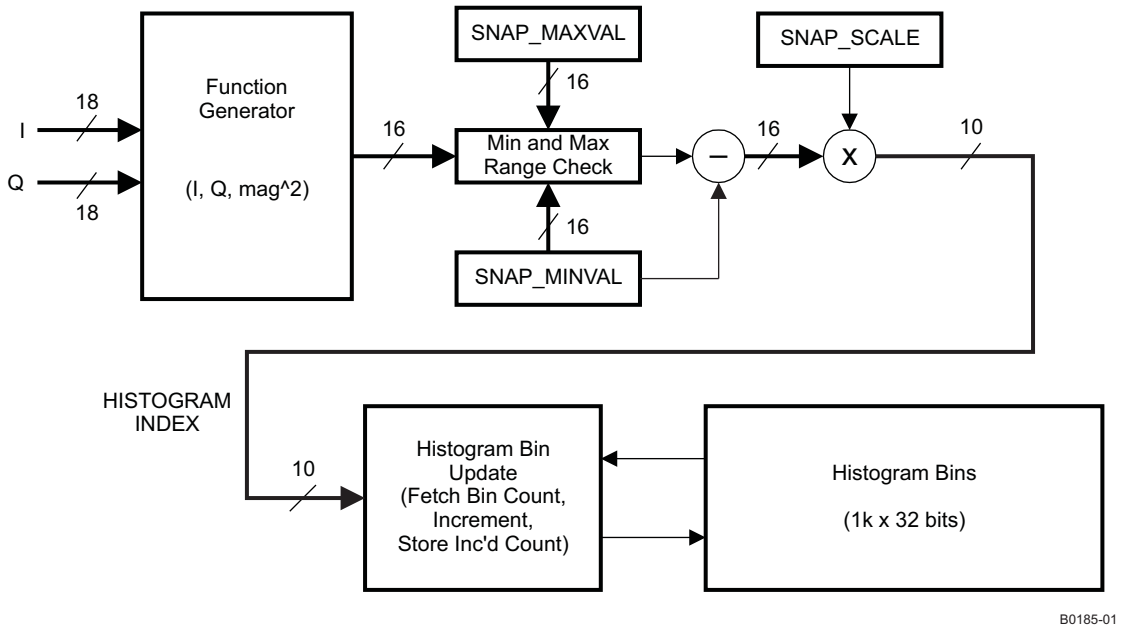


Figure 13. Snapshot RAM Histogram Operation

- SNAP_MINVAL: minimum value of interest (–32,768..32,767)
- SNAP_MAXVAL: maximum value of interest (–32768..32,767)
- SNAP_SCALE: a 16-bit multiplier that scales the 16-bit (value – SNAP_MINVAL) into the 10-bit range 0..1,023.

In C pseudo-code, the GC1115 histogram index calculation and bin update is performed as follows:

```
if ( (funcGen[i] >= SNAP_MINVAL) && (funcGen[i] <= SNAP_MAXVAL) ) {
        shift = 6;
  j      = funcGen[i]   SNAP_MINVAL;
        index  = int(j >>shift);
        index &= 0x3FF;

        hist[index]++
}
```

The minimum histogram index is never less than 0, while the maximum histogram index should never exceed 1,023. The SNAP_MINVAL and SNAP_MAXVAL values allow GC1115 users to bracket specific sample ranges of interest, while ignoring values outside of this range. The SNAP_SCALE multiplier then maps the range of interest into the available histogram bins (0..1,023).

In histogram mode, the GC1115 snapshot RAMs collect statistics on the frequency of occurrence of certain sample or magnitude-squared values. Because the GC1115 contains two snapshot RAMs, these statistics can be used to monitor the signal simultaneously at two different stages of processing (such as at the input and at the output). After a time, the histograms stored in RAM A and RAM B are read by the microprocessor or DSP, which allows derived values (such as CCDF) to be obtained from the histogram bin counts.

Snapshot RAMs can be individually cleared (i.e., all entries set to zero) via control bits in the SNAP_A_CONTROL and SNAP_B_CONTROL registers. Snapshot RAMs must be cleared prior to histogram processing in order to zero all histogram counts.

Table 12 shows how the snapshot RAM is used in capture and histogram modes. The addresses in Table 12 are those that appear in the SNAP_A_ADDRESS or SNAP_B_ADDRESS registers.

Table 12. Snapshot RAM Addressing in Capture and Histogram Modes

MODE	ADDRESS	CONTENTS
Capture	0	I[0](1)
	1	Q[0](1)
	2	I[1](1)
	3	Q[1](1)
	. . .	. . .
	2046	I[1023](1)
	2047	Q[1023](1)
Histogram	0	HIST_MSW[0]
	1	HIST_LSW[0]
	2	HIST_MSW[1]
	3	HIST_LSW[1]
	. . .	. . .
	2046	HIST_MSW[1023]
	2047	HIST_LSW[1023]

(1) In capture mode, the 16 MSBs of the 18-bit samples are saved. MSW = most significant word (upper 16 bits), LSW = least significant word (lower 16 bits)

The SNAP_ADDRESS registers autoincrement with each SNAP_DATA access. This autoincrementing can result in addresses that exceed the allowed snapshot RAM address range. The GC1115 resolves this address overflow condition by resetting the SNAP_ADDRESS register to zero if an autoincrement generates an address value greater than 2,047.

Input Decimator

When the input signal is highly oversampled, the GC1115 user may want to decimate the complex input stream prior to PDC processing. The DECIMATE register is provided for such circumstances. GC1115 users wanting to use the 2× decimation settings must be aware of decimation effects on GC1115 clock generation and output interpolation. See the Operating Modes section of this document for details about how DECIMATE = 2 affects GC1115 operation.

Interpolation Operation

The GC1115 contains an interpolation stage after the fourth (final) PDC stage. This interpolation stage can be bypassed by clearing bit 4 of the CONTROL register.

GC1115 Output Interpolator

The GC1115 output interpolator can be used in single- or dual-channel modes. The interpolator can interpolate by 2 or 4, and can convert the complex data to real with an internal mixer, shifting the complex data up by the interpolator clock rate/4.

The interpolator modes are:

- Bypass
- Interpolate-by-2, complex
- Interpolate-by-2, complex; conversion of complex to real
- Interpolate-by-4, complex; conversion of complex to real

The GC1115 holds 40 coefficient registers for the interpolation filter. These must be configured even if the output interpolator is in bypass mode. The 40 bypass coefficients are –32,768, 0, 0, ..., 0, 0.

In the interpolate-by-2 mode, there are 20 coefficients, programmed to the 0 coefficient in indices of 2 (0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38).

In the interpolate-by-4 mode, all 40 coefficients are used.

The filter design for the interpolator is based on the following elements (see Figure 14):

- Interpolation filter sample or clock rate → Interp × InClk / [(muxed + 1) × (dec + 1)]
- Pass frequency (f_{pass}) – carrier or multicarrier highest pass frequency
- Stop-band frequency (f_{stop}) – InClk / [(muxed + 1) × (dec + 1)] – Pass Frequency

NOTE:

The desired stop-band rejection may be limited by the number of taps and the stop-band frequency.

NOTE:

Coefficient scaling must be within the range of 32,767 to –32,768. However, interpolation gain of 1 occurs when the sum of the coefficients is 65,536.

Example interpolate-by-2:

1. Design a 21-tap low-pass filter, using the foregoing conditions.
2. Scale the sum of coefficients for 65,536, then round.
3. Multiply the coefficients by –1.
4. Zero-pad the coefficients to generate a 41-tap result.
5. Truncate the last tap for a 40-tap result filter.

Example interpolate-by-4:

1. Design a 41-tap low-pass filter, using the foregoing conditions.
2. Scale the sum of coefficients for 65,536, then round.
3. Multiply the coefficients by –1.
4. Truncate the last tap for a 40-tap result filter.

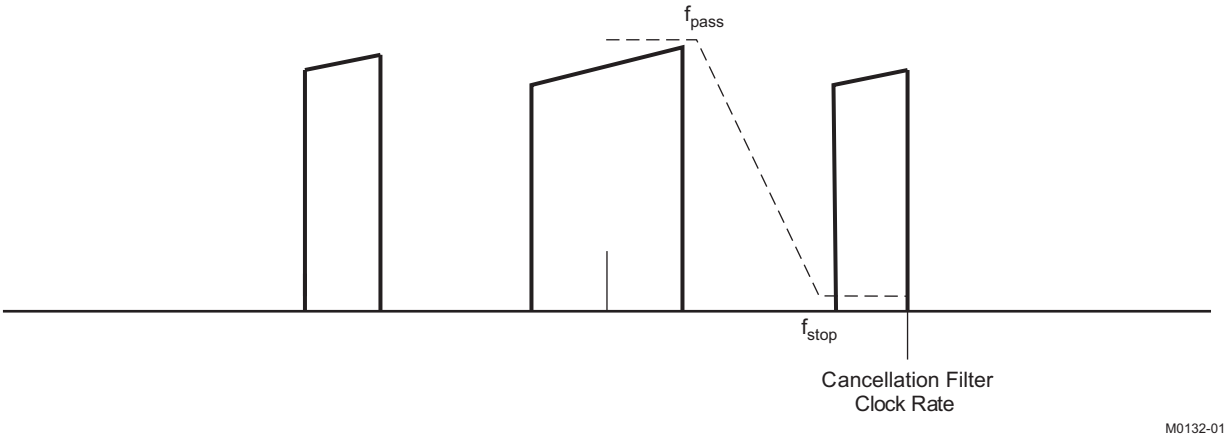


Figure 14. Output Interpolator Filter Parameters

The interpolate-by-4 stage uses 40 interpolation coefficients. These interpolate-by-4 coefficients are stored at addresses 0x82 through 0xA9. When the interpolate-by-4 stage is bypassed, the GC1115 requires the interpolate-by-4 coefficients shown in Table 13 (these are the default interpolate-by-4 values after a GC1115 RESET):

Table 13. Interpolate-by-4 Bypass Coefficients

ADDRESS RANGE	INTERPOLATE-BY-4 COEFFICIENTS
0x82–0x85	0x8000, 0, 0, 0
0x86–0x89	0, 0, 0, 0
0x8A–0x8D	0, 0, 0, 0
0x8E–0x91	0, 0, 0, 0
0x92–0x95	0, 0, 0, 0
0x96–0x99	0, 0, 0, 0
0x9A–0x9D	0, 0, 0, 0
0x9E–0xA1	0, 0, 0, 0
0xA2–0xA5	0, 0, 0, 0
0xA6–0xA9	0, 0, 0, 0

When the interpolate-by-4 stage is active, the GC1115 requires the interpolate-by-4 coefficients shown in Table 14:

Table 14. Interpolate-by-4 2× and 4× Interpolation Coefficients

ADDRESS RANGE	INTERPOLATE-BY-4 COEFFICIENTS (decimal)	INTERPOLATE-BY-4 COEFFICIENTS (hex)
0x82 – 0x85	0, –4, –21, –35	0x0, 0XFFFC, 0XFFEB, 0XFFDD
0x86 – 0x89	0, 122, 287, 319	0x0, 0x7A, 0x11F, 0x13F
0x8A – 0x8D	0, –700, –1401, –1372	0x0, 0xFD44, 0xFA87, 0xFAA4
0x8E – 0x91	0, 2,519, 4,781, 4,558	0x0, 0x9D7, 0x12AD, 0x11CE
0x92 – 0x95	0, –8,970, –20,028, –29,203	0x0, 0xDCF6, 0xB1C4, 0x8DED
0x96 – 0x99	–32,768, –29,203, –20,028, –8,970	0x8000, 0x8DED, 0xB1C4, 0xDCF6
0x9A – 0x9D	0, 4,558, 4,781, 2,519	0x0, 0x11CE, 0x12AD, 0x9D7
0x9E – 0xA1	0, –1,372, –1,401, –700	0x0, 0xFAA4, 0xFA87, 0xFD44
0xA2 – 0xA5	0, 319, 287, 122	0x0, 0x13F, 0x11F, 0x7A
0xA6 – 0xA9	0, –35, –21, –4	0x0, 0xFFDD, 0xFFEB, 0xFFFC

When the interpolate-by-4 stage operates in *real output* mode (i.e., not in complex output mode), it also modulates the input (baseband) signal to an intermediate frequency. For example, if IN_CLK is 61.44 Msps, interp-by-2 real mode would raise the sampling rate to 122.88 Msps (real samples) and the interpolated output signal would be centered at 122.88 / 4 = 30.72 MHz after the interpolate-by-4 stage.

If the interpolated output sampling rate exceeds 130 Msps, the output ports must be configured in odd/even mode. In odd/even mode, successive samples are demultiplexed between OUT_A and OUT_B ports, effectively lowering the sampling rate on each output port by a factor of 2.

Soft Limiter Operation

NOTE:

Under nearly all operating conditions, the GC1115 soft limiter can safely be bypassed by clearing bit 5 of the CONTROL register at address 0x3. The soft limiter is only required for output PAR levels below 6 dB, when PDC canceler resources may become continuously busy. However, at PAR levels below 6 dB, the EVM and PCDE levels are also likely to be out of spec, even if the soft limiter is enabled.

The soft limiter block is the final block in the GC1115 processing chain. The soft limiter provides a final check of the output samples values after all four PDC stages and can optionally apply a user-specified, multiplicative attenuation curve to over-threshold samples. When enabled, the soft limiter limits the output samples to the SOFT_TSQD threshold-squared value. Values above SOFT_TSQD are adjusted over N samples, where N is specified by the 2 LSBs in SOFT_LENGTH. Valid values for N are 5, 9, 17, or 33. Longer soft limiter lengths provide more gradual roll-offs and thus provide smaller ACLR increases when the soft limiter is active.

A user-specified, normalized taper table (maximum of 16 table entries) is stored starting at address 0xC2. The taper table entries are read twice: once in the forward direction, and once in the reverse direction. The taper table is always used starting at SOFT_COEF0.

The inverse gain table (32 entries) works in conjunction with the SOFT_TAB_SCALE value. When the soft limiter block finds an over-threshold peak, it calculates the difference between the magnitude-squared value and the SOFT_TSQD threshold of the peak, and then shifts the difference to the right by SOFT_TAB_SCALE bits. The resulting value should always be between 0 and 31, as this shifted value is used as the index into the inverse gain lookup table. If the scaled index is greater than 31, the GC1115 hardware sets the index to 31. The inverse gain lookup is applied to the taper table and (with a bit of extra math), the scaled taper table values are applied to the input samples. After this soft limiter processing, the over-threshold amplitude of the peak is reduced to a value that is just below the SOFT_TSQD threshold.

In pseudocode, the soft limiter performs the following operations:

```
//    k is the index of the current sample.

in_pwr = in_I[k] ^ 2 + in_Q[k] ^ 2;

if (in_pwr > SOFT_TSQD) {
    //
    //    The difference between the current over-threshold sample's
    //    power and the threshold power is a measure of how much
    //    over threshold the current sample is.
    //
    //    Because the inverse gain lookup table has only 32 entries, we
    //    must guarantee that the lookup table index does not exceed 31.
    //
    diff = in_pwr  -  SOFT_TSQD;
    table_index = diff >> SOFT_TAB_SCALE;
    if (table_index > 31)
        table_index = 31;
    //
    //    Get the inverse gain for this over-threshold peak.  We
    //    will use the inverse gain to scale the normalized taper
    //    coefficients (SOFT_COEFS).
    //
    inverse_gain = SOFT_INVGAIN[table_index];
    //
    //    Scale the tapered gain with the inverse gain, and apply
    //    the tapered, scaled values to the input samples
    //
    //    N is the number of samples in the taper coefficient table.
    //
    //    We will taper N/2 samples BEFORE the peak and N/2 samples
//    AFTER the peak.
    //
    j = k - (N/2);
    for (i=0; i<N; i++, j++) {
        sampleGain = 1 - (inverse_gain * SOFT_COEF[i]);
        sample[j] *= sampleGain;
    }
}
```

Output Gain and Offset Operation

The GC1115 includes output gains OUT_GAIN0 and OUT_GAIN1, which can provide up to a 4× increase in the output signal gain. The OUT_GAIN registers allow users to apply a signed 16-bit output gain to both the I and Q output sample streams just prior to output formatting (rounding to the user-selected number of output bits and conversion to unsigned binary if requested).

The GC1115 also implements two or four dc offset adjustments (which are applied after the OUT_GAIN0 and OUT_GAIN1 adjustments) for the I and Q data paths, to adjust for dc offsets in quadrature modulators that may be present in the transmit chain after GC1115 processing. GC1115 users must calibrate the transmit path to determine the appropriate values for the OUT_OFFSET_I0, _Q0, _I1, and _Q1 registers. When the GC1115 is configured for real output, only the OUT_OFFSET_I0 value, and the OUT_OFFSET_I1 value if in two-channel mode, are used.

Power Measurement

The GC1115 can measure signal power of a complex I/Q signal at one of two locations in the GC1115 data path:

- At the input to PDC stage 1
- At the output of PDC stage 4

The POWER_CTL and _POWER_CNT registers configure the GC1115 to measure power at one of these two locations. The total number of samples observed during power measurement is POWER_CNT × POWER_CTL[13:0]. After power measurement has completed, the resulting average power value is available in the POWER register.

The total number of samples used for the power calculation is the product of an inner loop count (determined by the POWER_CNT register) and an outer loop count (determined by bits [13:0] of POWER_CTL):

POWER_CNT	inner loop count (# samples)
0x1	15
0x3	255
0x7	4095
0xF	65535

The outer loop count is specified by the lower 14 bits of the POWER_CTL register, but only the most-significant 1 matters—the other bits are ignored:

POWER_CTL[13:0]	outer loop count (# samples)
1	1
2 - 3	2
4 - 7	4
8 - 15	8
16 - 31	16
32 - 63	32
64 - 127	64
128 - 255	128
256 - 511	256
512 - 1023	512
1024 - 2047	1024
2048 - 4095	2048
4096 - 8191	4096
8192 - 16383	8192

For example, to calculate the average power over about a million samples, the GC1115 registers would be initialized as follows:

POWER_CNT = 0xF (inner loop count = 65,535)

POWER_CTL = 0x10 (outer loop count = 16)

Total # samples used to calculate power: 16 × 65,536 = 1,048,560 samples

To summarize, the GC1115 performs the following steps during power measurement:

1. Use 18 bits I and 18 bits Q from each sample to calculate a 37-bit power value

NOTE:

Input samples must be left-justified, that is, the most-significant bit of the input sample is always aligned to bit 17 (MSB) of input ports IN_A and IN_B.

2. Add the upper 16 bits of each 37-bit power value to a 40-bit power accumulator
3. Accumulate N = POWER_CNT × POWER_CTL[13:0] sample powers
4. Shift the final accumulator value by 4 to 18 bits to calculate the average power over N samples, depending on how POWER_CNT and POWER_CTL are set. The GC1115 does this shifting (divide by N) automatically.
5. Transfer the resulting 16 bits to the POWER register.

GC1115 users also must set the two MSBs of POWER_CTL properly, to specify whether the input or output power is to be measured, and (in two-channel configuration) the channel number (channel 0 or channel 1) whose power is to be measured.

High-Speed Real Output: Odd/Even Mode

When the output sampling rate exceeds 130 MHz (which may occur when the interp-by-4 block is enabled), the GC1115 provides a high-speed odd-even output mode. This high-speed output mode requires that the interp-by-4 block is either in interp-by-2, real output mode, or in interp-by-4, real output mode. The special high-speed output mode is configured using bits [3:2] of IO_MODE (address 0x9): IO_MODE[3:2] = 11.

NOTE:

GC1115 users should only use the odd/even output mode when the output pin-toggling rate on OUT_A and OUT_B exceeds 130 MHz.

SYNCHRONIZATION

Figure 15 demonstrates the various registers, input and output pins, and functional blocks that are involved in synchronizing a variety of functional blocks within the GC1115. GC1115 synchronization involves three functional areas:

- SYNC sources
- SYNCed functional blocks, and
- SYNC registers

Refer to Figure 15 for the following discussion.

SYNC Sources

The GC1115 uses two hardware SYNC sources (pins), $\overline{\text{SYNC\_A}}$ and $\overline{\text{SYNC\_B}}$. SYNC_A or SYNC_B events are edge-triggered. Because hardware SYNC sources are active-low signals, the SYNC trigger occurs at the rising edge, i.e., when SYNC is deasserted.

The GC1115 has two software SYNC sources: SW_TRIGGER and TIMER. The SW_TRIGGER register generates a trigger signal for each 1 in the SW_TRIGGER register. The SW_TRIGGER has individual SYNC bits for each of the functional blocks that can be triggered. The software TIMER is a general-purpose, 32-bit timer that controls the duration of various events, such as the number of samples captured by a snapshot RAM. The software TIMER can be configured (via bit 15 of TIMER_SYNC) either to run once or periodically, resetting to its initial value whenever the timer count reaches zero. Whenever the software timer count reaches zero (it is a count-down timer), it generates a timer SYNC event.

Two other SYNC sources are provided for completeness: NEVER (i.e., the functional block never is triggered) and ALWAYS (i.e., the functional block is updated as soon as its corresponding parameter is updated). For some functional blocks that consist of multiple registers (such as the snapshot RAMs or the cancellation coefficients), the ALWAYS state is invalid.

NOTE:

Setting a functional block SYNC register to NEVER is not the same as disabling the functional block.

The external sync pins should be logic-0 for one clock (IN_CLK) cycle and return to logic-1. This is important for I data alignment when using multiplexed input timing.

Functional Blocks and SYNC Registers

The operation of thirteen GC1115 functional blocks can be triggered by one of the SYNC sources:

- The receive block (GC1115 input) *[use only SYNC_A or SYNC_B]*
- The pipeline stages *[use only SYNC_A or SYNC_B]*
- The decimation function (to select a particular input sample phase) *[use only SYNC_A or SYNC_B]*
- The software timer
- The PDC stage delay values (CANCEL_DELAY registers)
- The cancellation pulse coefficient shadow RAM
- The canceler RAM allocation variables (RESOURCE_CNT registers)
- The interpolate-by-4 block *[use only SYNC_A or SYNC_B]*
- The output gain registers (OUT_GAIN0 and OUT_GAIN1)
- The $\overline{\text{SYNC\_OUT}}$ pin (for debugging or for synchronizing multiple GC1115s)
- The signal generator functions
- Snapshot RAM A
- Snapshot RAM B

As shown in Table 15, SYNC selection registers control which SYNC source is assigned to each functional block. Table 15 summarizes the SYNC source selection encoding, using the 3 LSBs of each SYNC register.

Table 15. SYNC Register Source Selection

SYNC SELECTION	SYNC REGISTER VALUE (3 LSBs)
NEVER	0
SW_TRIGGER	1
TIMER	2
SYNC_A	3
SYNC_B	4
ALWAYS	5
Reserved	6
Reserved	7

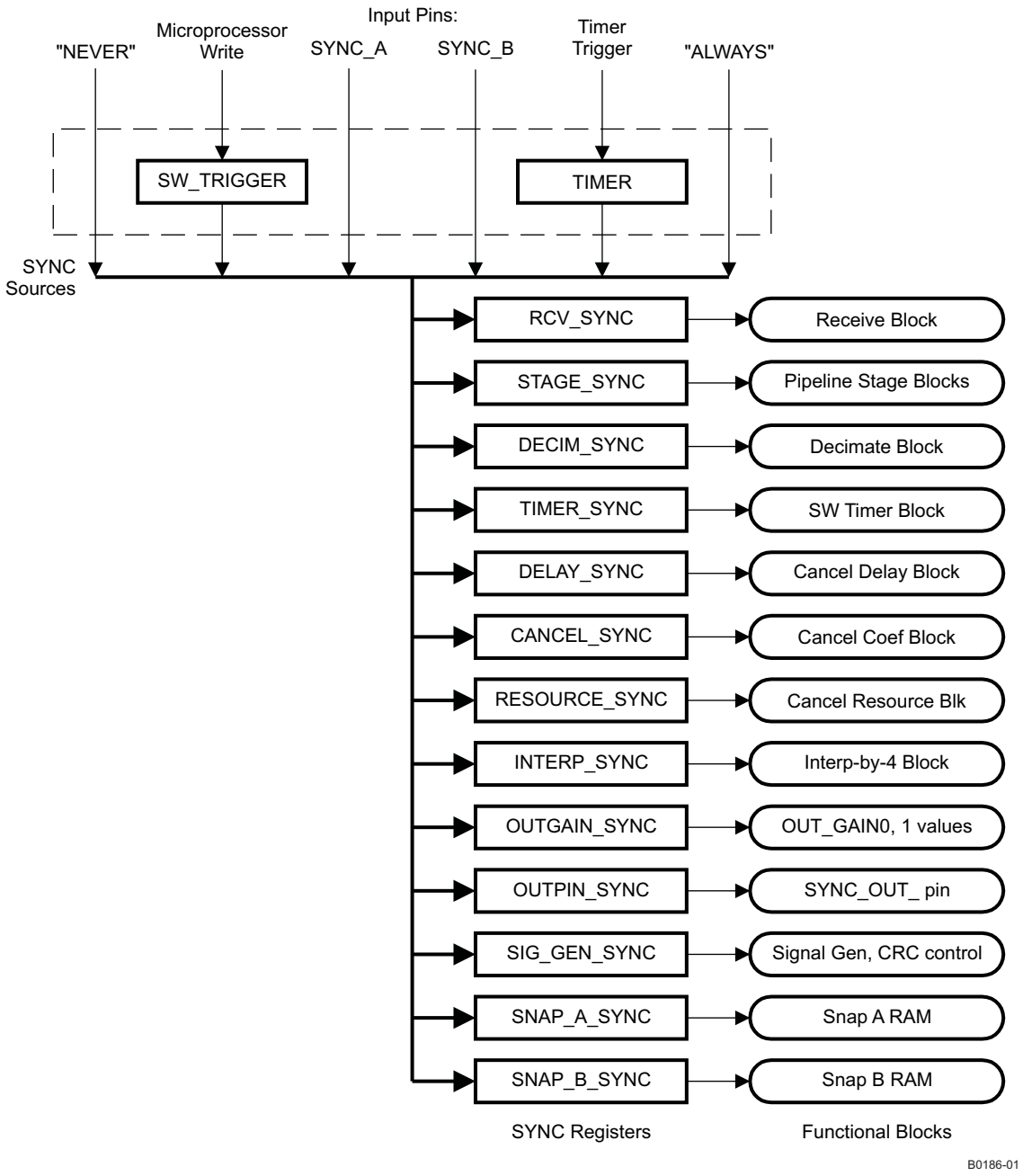


Figure 15. GC1115 Synchronization Elements

REGISTER DESCRIPTIONS

Global Registers (Addresses 0–14)

RESET **0x0** **Type: Read/Write** **Value at RESET: 0x0033**

The RESET register provides separate bits to reset the GC1115 registers, the data path, and the two PLLs. Writing a *1* at a given bit location resets the functions mapped to that bit. Multiple bits can be set during each write to the RESET register. **The RESET register is unclocked, i.e., IN_CLK does not have to be toggling to change RESET.**

BITS	DESCRIPTION		
0	Configuration reset	0: Running	1: Reset
1	Data-path reset	0: Running	1: Reset
[3:2]	Reserved		
4	CORE_PLL reset	0: Running	1: Reset
5	TX_PLL reset	0: Running	1: Reset
[16:6]	Reserved		

PLL_CONTROL **0x1** **Type: Read/Write** **Value at RESET: 0x0000**

The PLL_CONTROL register provides separate bits to control the GC1115 core and transmit PLLs. **The PLL_CONTROL register is unclocked, i.e., IN_CLK does not have to be toggling to change PLL_CONTROL.**

Figure 7 demonstrates how the various bits of the PLL_CONTROL and CLK_CONTROL registers interact to determine various GC1115 clock frequencies.

BITS	DESCRIPTION	
[1:0]	Core PLL control:	
	00: PLL_CLL = IN_CLK	01: PLL_CLK = 2 × IN_CLK
	10: Do not use	11: PLL_CLK = 4 × IN_CLK
2	Core PLL test enable	0: ____, 1: ____
3	Core PLL bypass enable (internal)	0: ____, 1: ____
4	Core PLL power-down enable	0: ____, 1: ____
[7:5]	Reserved	
[9:8]	Transmit PLL control:	
	00: PLL_CLL = IN_CLK	01: PLL_CLK = 2 × IN_CLK
	10: Do not use	11: PLL_CLK = 4 × IN_CLK
10	Tx PLL test enable	0: ____, 1: ____
11	Tx PLL internal bypass enable	0: ____, 1: ____
12	Tx PLL power-down enable	0: ____, 1: ____
[15:13]	Reserved	

CLK_CONTROL 0x2 Type: Read/Write Value at RESET: 0x1310

The CLK_CONTROL register provides separate bits to control the GC1115 input, core, and output clocks. **The CLK_CONTROL register is unclocked, i.e., IN_CLK need not be toggling to change CLK_CONTROL.**

Figure 7 demonstrates how the various bits of the PLL_CONTROL and CLK_CONTROL registers interact to determine various GC1115 clock frequencies.

BITS	DESCRIPTION	
[1:0]	Reserved	
2	IN_CLK edge selector	0: Rising, 1: Falling
3	PLL bypass	0: Use PLLs, 1: Bypass PLLs
[5:4]	Input clock rate:	
	00: OFF	01: $f_{inClk} = f_{IN\_CLK} \times 1$
	10: $f_{inClk} = f_{IN\_CLK} \times 2$	11: $f_{inClk} = f_{IN\_CLK} \times 4$
[7:6]	Reserved	
[9:8]	Core clock rate:	
	00: OFF	01: $f_{coreClk} = f_{IN\_CLK} \times 1$
	10: $f_{coreClk} = f_{IN\_CLK} \times 2$	11: $f_{coreClk} = f_{IN\_CLK} \times 4$
[11:10]	Reserved	
[13:12]	Output clock rate:	
	00: OFF	01: $f_{outClk} = f_{IN\_CLK} \times 1$
	10: $f_{outClk} = f_{IN\_CLK} \times 2$	11: $f_{outClk} = f_{IN\_CLK} \times 4$
[15:14]	OUT_CLK source:	
	00: CLK_TX (after pad)	01: Do not use
	10: Do not use	11: Do not use

CONTROL 0x3 Type: Read/Write Value at RESET: 0x0000

The CONTROL register provides separate bits to enable or to bypass the four peak detection and cancellation (PDC) stages, the interpolate-by-4 block, and the soft limiter. If all bits are cleared, the GC1115 is in *bypass* mode, during which no peaks are processed but the samples still flow through the GC1115 internal delay buffers.

BITS	DESCRIPTION	
0	PDC stage 1	0 = bypassed without delay, 1 = enabled
1	PDC stage 2	0 = bypassed without delay, 1 = enabled
2	PDC stage 3	0 = bypassed without delay, 1 = enabled
3	PDC stage 4	0 = bypassed without delay, 1 = enabled
4	Interpolator	0 = bypassed, 1 = enabled
5	Soft limiter	0 = bypassed, 1 = enabled
[7:6]	Reserved	
8	PDC stage 1	0 = bypassed with delay, 1 = enabled
9	PDC stage 2	0 = bypassed with delay, 1 = enabled
10	PDC stage 3	0 = bypassed with delay, 1 = enabled
11	PDC stage 4	0 = bypassed with delay, 1 = enabled
[15:12]	Reserved	

INT_MAP **0x4** **Type: Read/Write** **Value at RESET: 0x0000**

The INT_MAP register indicates the reason(s) for a GC1115-initiated interrupt on the $\overline{INT}$ pin. Read INT_MAP to determine whether that condition occurred (indicated by a 1). Write a 1 to individual bits of INT_MAP to clear (reset) specific interrupt conditions. INT_MAP operates in conjunction with INT_MASK (0x5) in generating an $\overline{INT}$ signal.

The INT_MAP and INT_MASK registers work together to control interrupt sources that trigger the $\overline{INT}$ (interrupt) output pin, which is normally tied to the hardware interrupt pin of the microprocessor or DSP chip that controls the GC1115. Setting one or more bits of the INT_MASK register unmasks (enables) the corresponding interrupt source in the INT_MAP register. The GC1115 contains eight possible interrupt sources. When the microprocessor receives a signal on its $\overline{INT}$ pin, INT_MAP should be read to determine the specific cause (or causes) of the interrupt.

BITS	DESCRIPTION
0	Snapshot RAM A capture completion
1	Snapshot RAM B capture completion
2	Snapshot RAM A histogram bin overflow
3	Snapshot RAM B histogram bin overflow
4	Timer counted down to zero
5	Power measurement completed
6	Cancellation update has completed
7	CRC is available in the CRC_RESULT register
[15:8]	Reserved

INT_MASK **0x5** **Type: Read/Write** **Value at RESET: 0x0000**

The INT_MASK register determines whether the corresponding individual interrupt conditions in the INT_MAP register cause an $\overline{INT}$ interrupt. A 0 in a bit position disables the condition from causing an $\overline{INT}$ interrupt. A 1 in a bit position allows the condition to cause an $\overline{INT}$ interrupt. The INT_MAP and INT_MASK registers work together to control interrupt sources that trigger the $\overline{INT}$ (interrupt) output pin, which is normally tied to the hardware interrupt pin of the microprocessor or DSP chip that controls the GC1115. Setting one or more bits of the INT_MASK register unmasks (enables) the corresponding interrupt source in the INT_MAP register.

BITS	DESCRIPTION	
0	Snapshot RAM A capture completed:	0: Disable interrupt, 1: Enable interrupt
1	Snapshot RAM B capture completed:	0: Disable interrupt, 1: Enable interrupt
2	Snapshot RAM A histogram bin overflow occurred:	0: Disable interrupt, 1: Enable interrupt
3	Snapshot RAM B histogram bin overflow occurred:	0: Disable interrupt, 1: Enable interrupt
4	Timer counted down to zero:	0: Disable interrupt, 1: Enable interrupt
5	Power measurement completed:	0: Disable interrupt, 1: Enable interrupt
6	Cancellation update completed:	0: Disable interrupt, 1: Enable interrupt
7	CRC available in CRC_RESULT:	0: Disable interrupt, 1: Enable interrupt
[15:8]	Reserved	

MASK_REV **0x6** **Type: Read-Only** **Value at RESET: 0x0001 (HW Version-Dependent)**

The MASK_REV register allows the controlling microprocessor or DSP to determine the hardware revision of a particular GC1115. MASK_REV is useful in determining, via software, which version of the GC1115 is present on a board or in a system, in the event that different functionality exists in two or more revisions of GC1115 silicon.

BITS	DESCRIPTION
[15:0]	GC1115 mask revision (a 16-bit, non-zero value), 0x0001

SW_TRIGGER **0x7** **Type: Read/Write** **Value at RESET: 0x0000**

The SW_TRIGGER register is a software trigger source that can synchronize one or more of thirteen internal GC1115 components via software command. If the SYNC register (from address 0x19 to address 0x25) of a component selects SW_TRIG as its SYNC source, setting that component bit in the SW_TRIGGER register syncs the component. The GC1115 automatically clears the SW_TRIGGER bits after the trigger occurs.

BITS	DESCRIPTION	
0	RCV_SYNC (receive data path)	0: No effect, 1: Trigger (SW_TRIGGER not recommended)
1	STAGE_SYNC (PDC stage)	0: No effect, 1: Trigger (SW_TRIGGER not recommended)
2	DECIM_SYNC (decimator)	0: No effect, 1: Trigger (SW_TRIGGER not recommended)
3	TIMER_SYNC (SW timer)	0: No effect, 1: Trigger
4	DELAY_SYNC (apply CANCEL_DELAY)	0: No effect, 1: Trigger
5	CANCEL_SYNC (change cancel coefficients)	0: No effect, 1: Trigger
6	RESOURCE_SYNC (apply RESOURCE_CNT)	0: No effect, 1: Trigger
7	INTERP_SYNC (sync interp-by-4 block)	0: No effect, 1: Trigger (SW_TRIGGER not recommended)
8	OUTGAIN_SYNC (change outgain)	0: No effect, 1: Trigger
9	OUTPIN_SYNC (apply OUT_SYNC)	0: No effect, 1: Trigger
10	SIG_GEN_SYNC (signal generator)	0: No effect, 1: Trigger
11	SNAP_A_SYNC (snapshot RAM A)	0: No effect, 1: Trigger
12	SNAP_B_SYNC (snapshot RAM B)	0: No effect, 1: Trigger
[15:13]	Reserved	

IO_CONTROL **0x8** **Type: Read/Write** **Value at RESET: 0x0000**

The IO_CONTROL register controls various input and output port characteristics.

BITS	DESCRIPTION		
0	Input port format	0: 2s complement	1: Unsigned
1	Output port format	0: 2s complement	1: Unsigned
2	Output port A enable(1)	0: High-impedance state	1: Enabled
3	Output port B enable(1)	0: High-impedance state	1: Enabled
4	Output force zeros(2)	0: Normal	1: Force zeros
[6:5]	Output sample width		
	00: 18 bits	01, 10, 11: Reserved	
7	Reserved		
8	Non-port output enable(3)	0: High-impedance state	1: Driven
[15:9]	Reserved		

(1) If bit 2 AND bit 3 are both zeros, OUT_CLK, OUT_IQ_SEL, $\overline{\text{SYNC\_OUT}}$, and $\overline{\text{INT}}$ all are put into a **high-impedance state**.
(2) When forcing zeros, the output port format (Bit 1) determines the values used to drive the output ports. Twos complement drives the output ports with all zeros, while unsigned drives the output ports with a 1 for the MSB and zeros for all other output bits.
(3) Bit 8 affects all output pins (OUT_CLK, OUT_IQ_SEL, $\overline{\text{SYNC\_OUT}}$, and $\overline{\text{INT}}$) except port-A and port-B pins, which are separately enabled using bits 2 and 3.

IO_MODE **0x9** **Type: Read/Write** **Value at RESET: 0x0000**

The IO_CONTROL register controls various input and output port characteristics.

BITS	DESCRIPTION		
0	Number of channels	0 = one channel	1 = two channels
1	Input port I/Q multiplex	0 = parallel	1 = multiplexed
[3:2]	Bits [3:2]: One-channel output port mode:		
	Bits 3:2	**OUT_A**	**OUT_B**
	00	Reserved	Reserved
	01 (complex)	I/Q multiplexed samples, ch. A	(not used)
	(2-channel only)	IQ multiplexed, ch. A	IQ multiplexed, ch. B
	10 (complex)	I sample, ch. A	Q sample, ch. A
	11 (real)	Samples 0, 2, 4, ... , ch, A	Samples 1, 3, 5, ... , ch. A
	During two-channel operation, the interpolate-by-4 mode determines which samples are carried on ports A and B:		
	Interpolate-by-4 mode	**OUT_A**	**OUT_B**
	Bypass	Channel 0, I/Q multiplexed	Channel 1, I/Q multiplexed
	2× (complex)	Channel 0, I/Q multiplexed	Channel 1, I/Q multiplexed
	2× (real)	Channel 0, real samples	Channel 1, real samples
	4× (real)	Channel 0, real samples	Channel 1, real samples
[15:4]	Reserved		

POWER_CTL 0xA (10) Type: Read/Write Value at RESET: 0x0000

The POWER_CTL register controls various power measurement parameters. Power measurement begins automatically when bits [13:0] of POWER_CTL contain a non-zero value. The results of power measurement are returned in the POWER register. The microprocessor controlling the GC1115 can request an interrupt at the conclusion of power measurement by setting Bit 5 of INT_MASK (address 0x5).

BITS	DESCRIPTION		
[13:0]	Number of POWER_CNT blocks(1) used to measure the average power (a value from 0 to 8191).		
14	Measure in/out power	0 = Input	1 = Output
15	Measure channel-0/channel-1 power(2)	0 = Channel 0	1 = Channel 1

(1) The number of samples per block is specified in the POWER_CNT register (address 0x7F). Normally POWER_CNT is set to 0xFFFF (65,536 samples per block).
(2) During one-channel operation, setting POWER_CTL[15] to 1 results in unpredictable power measurements.

POWER 0xB (11) Type: Read-Only Value at RESET: 0x0000

The POWER register contains the results of a power measurement process that was initiated according to the parameters in the POWER_CTL register. The microprocessor controlling the GC1115 can request an interrupt at the conclusion of power measurement by setting bit 5 of INT_MASK (address 0x5).

BITS	DESCRIPTION
[15:0]	Average power measurement (0x0000 to 0xFFFF)

DECIMATE 0xC (12) Type: Read/Write Value at RESET: 0x0001

The DECIMATE register determines the decimation factor at the input of the GC1115. When set to 2, only every second input sample is processed by the GC1115 data path. A decimation factor of 2 is required only when input clock rates below 25 MHz or above 75 MHz are used. When DECIMATE = 2, the GC1115 user must provide a properly aligned synchronization signal (normally SYNC_A or SYNC_B) to select which input sample phase is used to align the GC1115 decimator. The DECIM_SYNC register selects the source of the decimator SYNC signal.

BITS	DESCRIPTION	
[3:0]	Decimation factor:	
	0001: No decimation	0010: Decimate by 2
	0100: Decimate by 4	Other values not allowed
[15:4]	Reserved	

TIMER_HI_RST 0xD (13) Type: Read/Write Value at RESET: 0x0000

The TIMER_HI_RST and TIMER_LO_RST registers (each 16 bits wide) determine the reset value of the GC1115 programmable software timer. This timer can be enabled to control the occurrence of SYNC events during GC1115 processing. TIMER_HI_RST and TIMER_LO_RST are combined into a 32-bit unsigned value that is clocked with every internal GC1115 clock. The TIMER_HI_RST and TIMER_LO_RST registers operate in conjunction with the TIMER_SYNC register.

BITS	DESCRIPTION
[15:0]	Upper 16 bits of the GC1115 32-bit timer reset value

TIMER_LO_RST 0xE (14) Type: Read/Write Value at RESET: 0x0000

The TIMER_LO_RST and TIMER_HI_RST registers (each 16 bits wide) determine the reset value of the GC1115 programmable software timer. This timer can be enabled to control the occurrence of SYNC events during GC1115 processing. TIMER_HI_RST and TIMER_LO_RST are combined into a 32-bit unsigned value which is clocked with every internal GC1115 clock. The TIMER_HI_RST and TIMER_LO_RST registers operate in conjunction with the TIMER_SYNC register.

BITS	DESCRIPTION
[15:0]	Lower 16 bits of the GC1115 32-bit timer reset value

Cancellation Coefficient Registers (Addresses 15–20)

CANCEL_MODE 0xF (15) Type: Read/Write Value at RESET: 0x0000

The CANCEL_MODE register sets the characteristics of the cancellation coefficients. The GC1115 operates using either real (symmetric carrier spectra) or complex (asymmetric carrier spectra) cancellation coefficients. For symmetric spectra, the cancellation coefficients can also be unique or mirrored. Mirrored coefficients are only needed when a cancellation pulse with more than 255 coefficients is desired. **[Note: cancellation pulses with about 100 unique coefficients are more than adequate to meet all 3G or cdma2000 requirements].** Mirrored mode is also useful because only half of the coefficients must be downloaded, thus shortening the time required to provide the GC1115 with a new set of cancellation coefficients. When mirrored mode is used, the GC1115 applies N real cancellation coefficients in the following order:

coef[0], coef[1], …, coef[N – 2], coef[N – 1], coef[N – 2], …, coef[1], coef[0]

Bits [11:8] of CANCEL_MODE contain a peak hysteresis (timeout) count whose value is determined during cancellation pulse design. Under most operating conditions, the hysteresis count is zero. However, for some configurations with large gaps between carriers (*missing* carriers), the hysteresis count has a non-zero value of 6 or less. Contact TI to determine how to calculate the peak hysteresis count for such cancellation coefficients.

BITS	DESCRIPTION		
0	Cancel coefficient format	0 = Real	1 = Complex
1	Mirrored coefficients	0 = Unique	1 = Mirrored
[7:2]	Reserved		
[11:8]	Peak hysteresis count (0 to 6, 2 channels; 0 to 12, 1 channel)		
[15:12]	Reserved		

CANCEL_LENGTH 0x10 (16) Type: Read/Write Value at RESET: 0x0000

The CANCEL_LENGTH register determines the number of unique cancellation coefficients present in each cancellation pulse (ignoring the *mirror* mode bit of the CANCEL_MODE register). The CANCEL_LENGTH must be an odd value. See Table 9, Table 10, and Table 11 for details on the proper use of CANCEL_LENGTH. Note that CANCEL_LENGTH and CANCEL_DELAY are related – see the discussion in the previous section entitled (*CANCEL_LENGTH and CANCEL_DELAY* was deleted).

BITS	DESCRIPTION	
[7:0]	Number of unique cancellation coefficients:	
	For real coefficients:	Odd number from 5 to 255
	For complex coefficients:	Odd number from 5 to 127
[15:8]	Reserved	

NOTE:

In most circumstances, CANCEL_LENGTH should be at least 15. For 3GPP processing, CANCEL_LENGTH of 101 or less achieves all relevant requirements.

CANCEL_ADDR 0x11 (17) Type: Read/Write Value at RESET: 0x0000

The CANCEL_ADDR register is used to access the GC1115 shadow RAM memory. The previous Cancellation Coefficient Shadow RAM section describes the structure of the cancellation coefficient shadow RAM. After writing a unique address (from 0 to 767) to CANCEL_ADDR, subsequent writes to (or reads from) the CANCEL_DATA register auto-increment CANCEL_ADDR. The auto-increment and direct-address modes are described in the *Writing Cancellation Coefficients to the GC1115* section.

BITS	DESCRIPTION
[9:0]	Cancellation coefficient shadow RAM memory address (0 to 767)
[15:10]	Reserved

CANCEL_DATA 0x12 (18) Type: Read/Write Value at RESET: 0x0000

The CANCEL_DATA register holds the 12-bit value to be written to (or read from) GC1115 cancellation coefficient shadow RAM. The structure of the cancellation coefficient memory is described in the Cancellation Coefficient Shadow RAM section. After writing a unique address (from 0 to 767) to CANCEL_ADDR, subsequent writes to (or reads from) the CANCEL_DATA register auto-increment CANCEL_ADDR.

BITS	DESCRIPTION
[11:0]	Data
[15:12]	Reserved (sign extended during reads)

RESOURCE_MASK **0x13 (19)** **Type: Read/Write** **Value at RESET: 0x00FF**

The RESOURCE_MASK register contains an 8-bit field that determines which canceler RAMs are initialized after a CANCEL_SYNC trigger. By setting RESOURCE_MASK one bit at a time, canceler RAMs can be updated one at a time. If all canceler RAMs were updated at the same time, there would be some short time period (a few microseconds) in which no cancelers would be active. During this time, over-threshold peaks would pass through the GC1115 without being canceled, which may be undesirable. Changing canceler RAMs one PDC stage at a time allows subsets of canceler RAMs to be modified without disabling all cancelers.

BITS	DESCRIPTION		
0	Canceler RAM 0 update status:	0 = Do not update	1 = Update
1	Canceler RAM 1 update status:	0 = Do not update	1 = Update
2	Canceler RAM 2 update status:	0 = Do not update	1 = Update
3	Canceler RAM 3 update status:	0 = Do not update	1 = Update
4	Canceler RAM 4 update status:	0 = Do not update	1 = Update
5	Canceler RAM 5 update status:	0 = Do not update	1 = Update
6	Canceler RAM 6 update status:	0 = Do not update	1 = Update
7	Canceler RAM 7 update status:	0 = Do not update	1 = Update
8	Resource node(1)	0 = Auto	1 = Manual
[15:9]	Reserved		

(1) See a RESOURCE_CNT register description.

NOTE:

The GC1115 user must ensure that the values in RESOURCE_CNT1, RESOURCE_CNT2, RESOURCE_CNT3, and RESOURCE_CNT4 sum to 8 or less, because there are only 8 canceler RAMs.

DELAY_MASK **0x14 (20)** **Type: Read/Write** **Value at RESET: 0x00FF**

The DELAY_MASK register determines which peak detect and cancel (PDC) stages are updated when the CANCEL_DELAY value is changed (i.e., when a DELAY_SYNC event occurs). Each of the four PDC stages has its own CANCEL_DELAY value, so that different cancellation pulse delays could in theory be used by each PDC stage. Under normal circumstances, however, CANCEL_DELAY is identical for all PDC stages, because the same cancellation pulse normally is stored in all canceler RAMs.

BITS	DESCRIPTION		
0	PDC stage-0 update status:	0 = Do not update	1 = Update
1	PDC stage-1 update status:	0 = Do not update	1 = Update
2	PDC stage-2 update status:	0 = Do not update	1 = Update
3	PDC stage-3 update status:	0 = Do not update	1 = Update
[15:4]	Reserved		

Signal Generator and CRC Registers (Addresses 21–24)

SIG_GEN_CTL 0x15 (21) Type: Read/Write Value at RESET: 0x0000

The SIG_GEN_CTL register controls the operation of a signal generator. When enabled, the signal generator outputs feed the I and Q inputs of PDC stage 1. In pseudo-LFSR mode, the GC1115 generates a signal with a PAR of approximately 10 dB. In order to properly generate a periodic signal and its related periodic CRC, the GC1115 must be initialized by parameters provided by TI. If CRC generation is not required, the CRC_RESULT register can simply be ignored, and the signal generator can be used without any restrictions.

Bit 7 of INT_MAP indicates when the CRC result is available. When bit 7 of INT_MASK is set, the GC1115 interrupts the controlling microprocessor or DSP to indicate that the CRC_RESULT register can be read. Once this bit is set, the microprocessor or DSP must manually clear bit 7 of INT_MAP prior to subsequent *CRC result available* interrupts.

BITS	DESCRIPTION
[1:0]	Signal generator and CRC control:
	00 = Signal generator and CRC generator are DISABLED
	01 = Signal generator in dc or sawtooth mode (CRC enabled) If SIG_GEN_INC = 0, generate dc value of SIG_GEN_BASE. If SIG_GEN_INC > 0, generate a sawtooth waveform.
	10 = Pseudo-LFSR with 10 dB PAR (CRC generator enabled)
	11 = External (CRC generator enabled)
[15:2]	Reserved

SIG_GEN_BASE 0x16 (22) Type: Read/Write Value at RESET: 0x0000

The SIG_GEN_BASE register specifies the output value for dc signal generation, or the starting accumulator value for sawtooth signal generation. While SIG_GEN_BASE is a 16-bit value, the GC1115 dc/sawtooth signal generator uses an 18-bit signed accumulator. SIG_GEN_BASE initializes the 16 LSBs of this 18-bit accumulator, with proper sign extension. If bit 15 of SIG_GEN_BASE is set, bits 17, 16, and 15 of the internal 18-bit accumulator also are set. If bit 15 of SIG_GEN_BASE is clear, bits 17, 16, and 15 of the internal 18-bit accumulator also are clear. When the signal generator is enabled in dc or sawtooth mode, the 18-bit accumulator value drives the 18-bit I input of PDC stage 1. The bit-reversed version of the 18-bit accumulator drives the 18-bit Q input of PDC stage 2.

If GC1115 users want to observe the signal generator output at OUT_A and OUT_B, the detection and gain thresholds for all enabled PDC stages should be set to 0xFFFF (i.e., no peaks are found). Alternately, there are two ways of achieving this: 1. All PDC stages are disabled in the CONTROL register, 2. No cancelers are assigned to any PDC stages (using the four RESOURCE_CNT registers).

BITS	DESCRIPTION
[15:0]	Signal generator accumulator value (for dc and sawtooth signals) [initial value of a signed, 18-bit internal accumulator]

SIG_GEN_INC 0x17 (23) Type: Read/Write Value at RESET: 0x0000

The SIG_GEN_INC register specifies the signed increment value for sawtooth signal generation. At each IN_CLK, the signal generator adds the signed, 16-bit SIG_GEN_INC value to the current 18-bit accumulator.

BITS	DESCRIPTION
[15:0]	Signal generator increment value (for sawtooth signals) [increment value applied to a signed, 18-bit internal accumulator]

CRC_RESULT **0x18 (24)** **Type: Read-Only** **Value at RESET: 0x0000**

The CRC_RESULT register holds the CRC generator value. The signal generator must be properly configured to ensure a periodic signal for the CRC_RESULT to be repeatable. The SIG_GEN_SYNC event must have the same period as the signal generator; otherwise, the CRC_RESULT is invalid. Contact TI to receive an appropriate set of signal generator configuration and CRC_RESULT values.

BITS	DESCRIPTION
[15:0]	CRC result (reaches steady state after four SIG_GEN_SYNC events)

Synchronization Registers (Addresses 25–37)

RCV_SYNC **0x19 (25)** **Type: Read/Write** **Value at RESET: 0x0000**

The RCV_SYNC register selects the synchronization source for the GC1115 receive data path. $\overline{\text{SYNC\_A}}$ or $\overline{\text{SYNC\_B}}$ **must** be used as the RCV_SYNC source.

BITS	DESCRIPTION		
[2:0]	RCV_SYNC selection:		
	0: Invalid	1: Invalid	2: Invalid
	3: SYNC_A	4: SYNC_B	5: Invalid
	6: Invalid	7: Invalid	
[15:3]	Reserved		

STAGE_SYNC **0x1A (26)** **Type: Read/Write** **Value at RESET: 0x0000**

The STAGE_SYNC register selects the synchronization source for the GC1115 PDC stages. $\overline{\text{SYNC\_A}}$ or $\overline{\text{SYNC\_B}}$ **must** be used as the STAGE_SYNC source.

BITS	DESCRIPTION		
[2:0]	STAGE_SYNC selection:		
	0: Invalid	1: Invalid	2: Invalid
	3: SYNC_A	4: SYNC_B	5: Invalid
	6: Invalid	7: Invalid	
[15:3]	Reserved		

DECIM_SYNC **0x1B (27)** **Type: Read/Write** **Value at RESET: 0x0000**

The DECIM_SYNC register selects the synchronization source for the GC1115 decimator. Because the decimator processes input samples, a hardware synchronization source ($\overline{\text{SYNC\_A}}$ or $\overline{\text{SYNC\_B}}$) **must** be used when DECIMATE = 2, allowing the user to select which phase of the input signal stream is processed by the decimator.

BITS	DESCRIPTION		
[2:0]	STAGE_SYNC selection:		
	0: Invalid	1: Invalid	2: Invalid
	3: SYNC_A	4: SYNC_B	5: Invalid
	6: Invalid	7: Invalid	
[15:3]	Reserved		

TIMER_SYNC **0x1C (28)** **Type: Read/Write** **Value at RESET: 0x0000**

The TIMER_SYNC register selects the synchronization source for the GC1115 software timer. In addition, bit 15 of TIMER_SYNC determines whether the software timer runs once (bit 15 = 0) or runs repeatedly (bit 15 = 1).

BITS	DESCRIPTION		
[2:0]	STAGE_SYNC selection:		
	0: NEVER	1: SW_TRIGGER	2: TIMER
	3: SYNC_A	4: SYNC_B	5: ALWAYS
	6: Invalid	7: Invalid	
[14:3]	Reserved		
15	Timer repeat:	0: Do not repeat (run once)	1: Repeat

DELAY_SYNC **0x1D (29)** **Type: Read/Write** **Value at RESET: 0x0000**

The DELAY_SYNC register selects the synchronization source that triggers the GC1115 CANCEL_DELAY being copied to PDC stages selected by DELAY_MASK. Under normal circumstances, all cancel RAMs contain the same set of cancellation coefficients. When this is the case, DELAY_MASK is set to 0xF, and CANCEL_DELAY1 thru CANCEL_DELAY4 are copied to their respective internal registers as soon as DELAY_SYNC is triggered. Under normal circumstances, DELAY_SYNC can be set to ALWAYS, i.e., as soon as CANCEL_DELAY1 thru CANCEL_DELAY4 are written, their corresponding internal registers are immediately updated.

BITS	DESCRIPTION		
[2:0]	DELAY_SYNC selection:		
	0: NEVER	1: SW_TRIGGER	2: TIMER
	3: SYNC_A	4: SYNC_B	5: ALWAYS
	6: Invalid	7: Invalid	
[15:3]	Reserved		

CANCEL_SYNC **0x1E (30)** **Type: Read/Write** **Value at RESET: 0x0000**

The CANCEL_SYNC register selects the synchronization source that causes the GC1115 cancel-coefficient shadow RAM values to be copied to the canceler RAMs whose corresponding RESOURCE_MASK bit is set. At GC1115 initialization, all cancel RAMs are normally initialized using the same set of cancellation coefficients. When this occurs, RESOURCE_MASK is set to 0xFF and the shadow RAM coefficients are copied to all canceler RAMs as soon as the CANCEL_SYNC trigger occurs. It is convenient for the microprocessor or DSP to use SW_TRIGGER as the CANCEL_SYNC source. As soon as the shadow RAM has been initialized, the microprocessor or DSP can then simply write a 0x20 to SW_TRIGGER, causing a trigger that only affects the CANCEL_SYNC functional block.

BITS	DESCRIPTION		
[2:0]	CANCEL_SYNC selection:		
	0: NEVER	1: SW_TRIGGER	2: TIMER
	3: SYNC_A	4: SYNC_B	5: ALWAYS
	6: Invalid	7: Invalid	
[15:3]	Reserved		

RESOURCE_SYNC 0x1F (31) Type: Read/Write Value at RESET: 0x0000

The RESOURCE_SYNC register determines the synchronization source when canceler resources are allocated or reallocated. The GC1115 contains a total of 32 cancelers, which can be assigned in groups of four to the four PDC stages. Each stage contains a RESOURCE_CNT register that specifies how many canceler RAMs (0 to 8) are assigned to that stage. The canceler allocation changes when the RESOURCE_SYNC trigger occurs. The RESOURCE_SYNC register determines the source of the trigger event that configures the GC1115 with the specified RESOURCE_CNT values. It is convenient for the microprocessor or DSP to use SW_TRIGGER as the RESOURCE_SYNC source. As soon as the RESOURCE_CNT registers have been initialized, the microprocessor or DSP can then simply write a 0x40 to SW_TRIGGER, causing a sync event that only affects the RESOURCE_SYNC functional block.

BITS	DESCRIPTION		
[2:0]	RESOURCE_SYNC selection:		
	0: NEVER	1: SW_TRIGGER	2: TIMER
	3: SYNC_A	4: SYNC_B	5: ALWAYS
	6: Invalid	7: Invalid	
[15:3]	Reserved		

INTERP_SYNC 0x20 (32) Type: Read/Write Value at RESET: 0x0000

The INTERP_SYNC register determines the synchronization source for the GC1115 interpolator. The GC1115 interpolator operates in four modes:

1. Bypass
2. 2× interpolate with real output at $f_S/4$
3. 2× interpolate with complex output
4. 4× interpolate with real output at $f_S/4$

To ensure proper operation in the non-bypass interpolator modes, the GC1115 interpolator **must** use either SYNC_A or SYNC_B as its synchronization source.

BITS	DESCRIPTION		
[2:0]	INTERP_SYNC selection:		
	0: Invalid	1: Invalid	2: Invalid
	3: SYNC_A	4: SYNC_B	5: Ivalid
	6: Invalid	7: Invalid	
[15:3]	Reserved		

OUTGAIN_SYNC 0x21 (33) Type: Read/Write Value at RESET: 0x0000

The OUTGAIN_SYNC register determines the synchronization source for the GC1115 output gain and offset values, stored in the OUT_GAIN0, OUT_GAIN1, OUT_OFFSET_I0, OUT_OFFSET_I1, OUT_OFFSET_Q0, and OUT_OFFSET_Q1 registers. OUTGAIN_SYNC can normally be set to ALWAYS, so that the microprocessor or DSP writing to the OUT_GAINx and OUT_OFFSETy registers immediately causes the change. All OUT_GAIN and OUT_OFFSET registers are modified when the OUT_SYNC trigger occurs.

BITS	DESCRIPTION		
[2:0]	OUTGAIN_SYNC selection:		
	0: NEVER	1: SW_TRIGGER	2: TIMER
	3: SYNC_A	4: SYNC_B	5: ALWAYS
	6: Invalid	7: Invalid	
[15:3]	Reserved		

OUTPIN_SYNC 0x22 (34) Type: Read/Write Value at RESET: 0x0000

The OUTPIN_SYNC register determines the synchronization source for the $\overline{\text{SYNC\_OUT}}$ pin. Because the $\overline{\text{SYNC\_OUT}}$ pin is often used to synchronize hardware that follows the GC1115, OUTPIN_SYNC is normally set to $\overline{\text{SYNC\_A}}$ or $\overline{\text{SYNC\_B}}$.

BITS	DESCRIPTION		
[2:0]	OUTPIN_SYNC selection:		
	0: NEVER	1: SW_TRIGGER	2: TIMER
	3: SYNC_A	4: SYNC_B	5: ALWAYS
	6: Invalid	7: Invalid	
[15:3]	Reserved		

SIG_GEN_SYNC 0x23 (35) Type: Read/Write Value at RESET: 0x0000

The SIG_GEN_SYNC register determines the synchronization source for the GC1115 internal signal generator. After the SIG_GEN_CTL, SIG_GEN_BASE, and SIG_GEN_INC registers have been initialized, a SIG_GEN_SYNC trigger starts the signal generator. It is convenient for the microprocessor or DSP to use SW_TRIGGER as the SIG_GEN_SYNC source. As soon as the SIG_GEN_CTL, SIG_GEN_BASE, and SIG_GEN_INC registers have been initialized, the microprocessor or DSP can then simply write a 0x400 to SW_TRIGGER, causing a sync event that only affects the SIG_GEN_SYNC functional block.

BITS	DESCRIPTION		
[2:0]	SIG_GEN_SYNC selection:		
	0: NEVER	1: SW_TRIGGER	2: TIMER
	3: SYNC_A	4: SYNC_B	5: ALWAYS
	6: Invalid	7: Invalid	
[15:3]	Reserved		

SNAP_A_SYNC 0x24 (36) Type: Read/Write Value at RESET: 0x0000

The SNAP_A_SYNC register determines the synchronization source for the GC1115 snapshot RAM A. After the appropriate SNAP_A registers (from SNAP_A_CONTROL to SNAP_A_HISTCOUNT) have been initialized, a SNAP_A_SYNC trigger enables snapshot RAM A. Snapshot RAM A can be triggered either by software or by hardware. If a particular snapshot RAM A timing relationship must be established with the input samples, SNAP_A_SYNC should be associated with $\overline{\text{SYNC\_A}}$ or $\overline{\text{SYNC\_B}}$. Alternatively, the microprocessor or DSP can initiate a snapshot RAM A capture by assigning SW_TRIGGER as the SNAP_A_SYNC event. Snapshot RAM A and snapshot RAM B can operate simultaneously, and both may be triggered by the same SYNC event.

NOTE:

SNAP_A_SYNC cannot be associated with a repeating TIMER trigger.

BITS	DESCRIPTION		
[2:0]	SNAP_A_SYNC selection:		
	0: NEVER	1: SW_TRIGGER	2: TIMER
	3: SYNC_A	4: SYNC_B	5: ALWAYS
	6: Invalid	7: Invalid	
[15:3]	Reserved		

SNAP_B_SYNC 0x25 (37) Type: Read/Write Value at RESET: 0x0000

The SNAP_B_SYNC register determines the synchronization source for the GC1115 snapshot RAM B. After the appropriate SNAP_B registers (from SNAP_B_CONTROL to SNAP_B_HISTCOUNT) have been initialized, a SNAP_B_SYNC trigger enables snapshot RAM B. Snapshot RAM B can be triggered either by software or by hardware. If a particular snapshot RAM B timing relationship must be established with the input samples, SNAP_B_SYNC should be associated with SYNC_A or SYNC_B. Alternatively, the microprocessor or DSP can initiate a snapshot RAM B capture by assigning SW_TRIGGER as the SNAP_B_SYNC event. Snapshot RAM A and snapshot RAM B can operate simultaneously, and both may be triggered by the same SYNC event.

NOTE:

SNAP_B_SYNC cannot be associated with a repeating TIMER trigger.

BITS	DESCRIPTION		
[2:0]	SNAP_B_SYNC selection:		
	0: NEVER	1: SW_TRIGGER	2: TIMER
	3: SYNC_A	4: SYNC_B	5: ALWAYS
	6: Invalid	7: Invalid	
[15:3]	Reserved		

Cancellation Stage Control Registers (Addresses 48–75)

RESOURCE_CNT1 0x30 (48) Type: Read/Write Value at RESET: 0x0000

The RESOURCE_CNT1 register specifies how many canceler RAMs are associated with PDC stage 1. RESOURCE_CNT1 contains a value between 0 and 8. The sum of canceler RAMs in RESOURCE_CNT1, RESOURCE_CNT2, RESOURCE_CNT3, and RESOURCE_CNT4 must be 8 or less. Resource allocations become effective only after a RESOURCE_SYNC event occurs. The RESOURCE_SYNC register selects the source of the RESOURCE_SYNC event.

BITS	DESCRIPTION
[3:0]	Number of canceler RAMs assigned to PDC stage 1 (from 0 to 8)
[15:4]	Reserved

When RESOURCE_MASK[8] is set, use RESOURCE_MASK[7:0] to assign cancel resources literally to stage 1 in binary format.

DETECT_TSQD1 0x31 (49) Type: Read/Write Value at RESET: 0x0000

The DETECT_TSQD1 register contains the detection threshold-squared value for PDC stage 1. The detection threshold-squared value is usually calculated from the average power (0-dB point) of the GC1115 input signal. Interpolated peaks found by PDC stage 1 whose magnitude is above DETECT_TSQD1 are decreased to the magnitude-squared value specified in GAIN_TSQD1, assuming that PDC stage 1 has an available canceler.

BITS	DESCRIPTION
[15:0]	Detection threshold-squared value for PDC stage 1

GAIN_TSQD1 0x32 (50) Type: Read/Write Value at RESET: 0x0000

The GAIN_TSQD1 register contains the gain threshold-squared value for PDC stage 1. The gain threshold-squared value is usually calculated from the average power (0-dB point) of the GC1115 input signal. Interpolated peaks found by PDC stage 1 whose magnitude is above DETECT_TSQD1 are decreased to the magnitude-squared value specified in GAIN_TSQD1, assuming that PDC stage 1 has an available canceler.

BITS	DESCRIPTION
[15:0]	Gain threshold-squared value for PDC stage 1.

CANCEL_DELAY1 0x33 (51) Type: Read/Write Value at RESET: 0x0000

The CANCEL_DELAY1 register contains the PDC stage 1 cancellation pulse delay, in samples. For real cancellation pulses, CANCEL_DELAY = (CANCEL_LENGTH + 1) / 2. If minimum-phase cancellation pulses are used, CANCEL_DELAY < (CANCEL_LENGTH + 1) / 2. The contents of the CANCEL_DELAY1 register are applied to the GC1115 hardware delay block only after a CANCEL_SYNC event occurs.

BITS	DESCRIPTION
[7:0]	Cancel pulse delay for PDC stage 1 (a value from 5 to 255)
[15:8]	Reserved

RESERVED 0x34–0x37 (51–55)

RESOURCE_CNT2 0x38 (56) Type: Read/Write Value at RESET: 0x0000

The RESOURCE_CNT2 register specifies how many canceler RAMs are associated with PDC stage 2. RESOURCE_CNT2 contains a value between 0 and 8. The sum of canceler RAMs in RESOURCE_CNT1, RESOURCE_CNT2, RESOURCE_CNT3, and RESOURCE_CNT4 must be 8 or less. Resource allocations become effective only after a RESOURCE_SYNC event occurs. The RESOURCE_SYNC register selects the source of the RESOURCE_SYNC event.

BITS	DESCRIPTION
[3:0]	Number of canceler RAMs assigned to PDC stage 2 (from 0 to 8)
[15:4]	Reserved

When RESOURCE_MASK[8] is set, use RESOURCE_MASK[7:0] to assign cancel resources literally to stage 2 in binary format.

DETECT_TSQD2 0x39 (57) Type: Read/Write Value at RESET: 0x0000

The DETECT_TSQD2 register contains the detection threshold-squared value for PDC stage 2. The detection threshold-squared value is usually calculated from the average power (0-dB point) of the GC1115 input signal. Interpolated peaks found by PDC stage 2 whose magnitude is above DETECT_TSQD2 are decreased to the magnitude-squared value specified in GAIN_TSQD2, assuming that PDC stage 2 has an available canceler.

BITS	DESCRIPTION
[15:0]	Detection threshold-squared value for PDC stage 2.

GAIN_TSQD2 0x3A (58) Type: Read/Write Value at RESET: 0x0000

The GAIN_TSQD2 register contains the gain threshold-squared value for PDC stage 2. The gain threshold-squared value is usually calculated from the average power (0-dB point) of the GC1115 input signal. Interpolated peaks found by PDC stage 2 whose magnitude is above DETECT_TSQD2 are decreased to the magnitude-squared value specified in GAIN_TSQD2, assuming that PDC stage 2 has an available canceler.

BITS	DESCRIPTION
[15:0]	Gain threshold-squared value for PDC stage 2.

CANCEL_DELAY2 0x3B (59) Type: Read/Write Value at RESET: 0x0000

The CANCEL_DELAY2 register contains the PDC stage 2 cancellation pulse delay, in samples. For real cancellation pulses, CANCEL_DELAY = (CANCEL_LENGTH + 1) / 2. If minimum-phase cancellation pulses are used, CANCEL_DELAY < (CANCEL_LENGTH + 1) / 2. The contents of the CANCEL_DELAY2 register are applied to the GC1115 hardware delay block only after a CANCEL_SYNC event occurs.

BITS	DESCRIPTION
[7:0]	Cancel pulse delay for PDC stage 2 (a value from 5 to 255)
[15:8]	Reserved

RESERVED 0x3C–0x3F (60–63)

RESOURCE_CNT3 0x40 (64) Type: Read/Write Value at RESET: 0x0000

The RESOURCE_CNT3 register specifies how many canceler RAMs are associated with PDC stage 3. RESOURCE_CNT3 contains a value between 0 and 8. The sum of canceler RAMs in RESOURCE_CNT1, RESOURCE_CNT2, RESOURCE_CNT3, and RESOURCE_CNT4 must be 8 or less. Resource allocations become effective only after a RESOURCE_SYNC event occurs. The RESOURCE_SYNC register selects the source of the RESOURCE_SYNC event.

BITS	DESCRIPTION
[3:0]	Number of canceler RAMs assigned to PDC stage 3 (from 0 to 8)
[15:4]	Reserved

When RESOURCE_MASK[8] is set, use RESOURCE_MASK[7:0] to assign cancel resources literally to stage 3 in binary format.

DETECT_TSQD3 0x41 (65) Type: Read/Write Value at RESET: 0x0000

The DETECT_TSQD3 register contains the detection threshold-squared value for PDC stage 3. The detection threshold-squared value is usually calculated from the average power (0 dB point) of the GC1115 input signal. Interpolated peaks found by PDC stage 3 whose magnitude is above DETECT_TSQD3 are decreased to the magnitude-squared value specified in GAIN_TSQD3, assuming that PDC stage 3 has an available canceler.

BITS	DESCRIPTION
[15:0]	Detection threshold-squared value for PDC stage 1

GAIN_TSQD3 0x42 (66) Type: Read/Write Value at RESET: 0x0000

The GAIN_TSQD3 register contains the gain threshold-squared value for PDC stage 3. The gain threshold-squared value is usually calculated from the average power (0-dB point) of the GC1115 input signal. Interpolated peaks found by PDC stage 3 whose magnitude is above DETECT_TSQD3 are decreased to the magnitude-squared value specified in GAIN_TSQD3, assuming that PDC stage 3 has an available canceler.

BITS	DESCRIPTION
[15:0]	Gain threshold-squared value for PDC stage 3

CANCEL_DELAY3 0x43 (67) Type: Read/Write Value at RESET: 0x0000

The CANCEL_DELAY3 register contains the PDC stage-3 cancellation pulse delay, in samples. For real cancellation pulses, CANCEL_DELAY = (CANCEL_LENGTH + 1) / 2. If minimum-phase cancellation pulses are used, CANCEL_DELAY < (CANCEL_LENGTH _ 1) / 2. The contents of the CANCEL_DELAY3 register are applied to the GC1115 hardware delay block only after a CANCEL_SYNC event occurs.

BITS	DESCRIPTION
[7:0]	Cancel pulse delay for PDC stage 3 (a value from 5 to 255)
[15:8]	Reserved

RESERVED 0x44–0x47 (68–71)

RESOURCE_CNT4 0x48 (72) Type: Read/Write Value at RESET: 0x0000

The RESOURCE_CNT4 register specifies how many canceler RAMs are associated with PDC stage 4. RESOURCE_CNT1 contains a value between 0 and 8. The sum of canceler RAMs in RESOURCE_CNT1, RESOURCE_CNT2, RESOURCE_CNT3, and RESOURCE_CNT4 must be 8 or less. Resource allocations become effective only after a RESOURCE_SYNC event occurs. The RESOURCE_SYNC register selects the source of the RESOURCE_SYNC event.

BITS	DESCRIPTION
[3:0]	Number of canceler RAMs assigned to PDC stage 4 (from 0 to 8)
[15:4]	Reserved

When RESOURCE_MASK[8] is set, use RESOURCE_MASK[7:0] to assign cancel resources literally to stage 4 in binary format.

DETECT_TSQD4 0x49 (73) Type: Read/Write Value at RESET: 0x0000

The DETECT_TSQD4 register contains the detection threshold-squared value for PDC stage 4. The detection threshold-squared value is usually calculated from the average power (0-dB point) of the GC1115 input signal. Interpolated peaks found by PDC stage 4 whose magnitude is above DETECT_TSQD4 are decreased to the magnitude-squared value specified in GAIN_TSQD4, assuming that PDC stage 4 has an available canceler.

BITS	DESCRIPTION
[15:0]	Detection threshold-squared value for PDC stage 4

GAIN_TSQD4 **0x4A (74)** **Type: Read/Write** **Value at RESET: 0x0000**

The GAIN_TSQD4 register contains the gain threshold-squared value for PDC stage 4. The gain threshold-squared value is usually calculated from the average power (0-dB point) of the GC1115 input signal. Interpolated peaks found by PDC stage 4 whose magnitude is above DETECT_TSQD4 are decreased to the magnitude-squared value specified in GAIN_TSQD4, assuming that PDC stage 4 has an available canceler.

BITS	DESCRIPTION
[15:0]	Gain threshold-squared value for PDC stage 4.

CANCEL_DELAY4 **0x4B (75)** **Type: Read/Write** **Value at RESET: 0x0000**

The CANCEL_DELAY4 register contains the PDC stage 4 cancellation pulse delay, in samples. For real cancellation pulses, CANCEL_DELAY = (CANCEL_LENGTH + 1) / 2. If minimum-phase cancellation pulses are used, CANCEL_DELAY < (CANCEL_LENGTH + 1) / 2. The contents of the CANCEL_DELAY4 register are applied to the GC1115 hardware delay block only after a CANCEL_SYNC event occurs.

BITS	DESCRIPTION
[7:0]	Cancel pulse delay for PDC stage 4 (a value from 5 to 255)
[15:8]	Reserved

RESERVED **0x4C–0x59 (76–95)**

Snapshot RAM Registers (Addresses 96–119)

SNAP_A_CONTROL **0x60 (96)** **Type: Read/Write** **Value at RESET: 0x0000**

The SNAP_A_CONTROL register controls the operation of snapshot RAM A, including the selection of its data source and the type of data being captured. When using snapshot RAM A in histogram mode, the RAM must first be cleared by writing a 0x0002 to SNAP_A_CONTROL. If the GC1115 is operating in two-channel mode, snapshot RAM A can monitor the samples of either Channel 0 or Channel 1. Snapshot RAM A does not begin a capture or histogram until the SNAP_A_SYNC event occurs. SNAP_A_SYNC cannot be triggered by a periodic TIMER event.

BITS	DESCRIPTION		
[1:0]	Snapshot RAM A command:	00: DISABLE (ignore all other bits in word) 01: ENABLE (observe all other bits) 1x:CLEAR_RAM (ignore all other bits)	
2	Two-channel data source:	0: Channel 0	1: Channel 1
[5:3]	Snapshot RAM A data source:	001: Input 011: After stage 2 101: After stage 4	010: After stage 1 100: After stage 3
[7:6]	Snapshot RAM A operating mode:	00: Capture 1k samples 10: Histogram Q samples	01: Histogram I samples 11: Histogram ($I^2 + jQ^2$)
[15:8]	Reserved		

SNAP_A_STATUS 0x61 (97) Type: Read-Only Value at RESET: 0x0000

The SNAP_A_STATUS register can be read to determine the current status (state) of snapshot RAM A. After sending a 0x2 command (clear RAM) to SNAP_A_CONTROL, SNAP_A_STATUS can be polled to determine when the RAM has been cleared. After a snapshot RAM A capture completes, the microprocessor or DSP can receive an interrupt by enabling bit 0 of INT_MASK. During histogram operation, if one or more snapshot RAM A histogram bins overflows its 32-bit count, bit 2 of INT_MAP is set. If bit 2 of INT_MASK is set, a snapshot RAM A bin overflow also generates an interrupt. Snapshot RAM A does not begin a capture or histogram until the SNAP_A_SYNC event occurs. SNAP_A_SYNC cannot be triggered by a periodic TIMER event.

BITS	DESCRIPTION		
[2:0]	Snapshot RAM A status:	000: OFF	001: Enabled (waiting) (after histogram completed)
		010: Active (capturing)	011: Capture complete
		100: Resetting (clearing all snapshot RAM bins)	
[15:3]	Reserved		

SNAP_A_ADDRESS 0x62 (98) Type: Read-Only Value at RESET: 0x0000

The SNAP_A_ADDRESS register contains a pointer into snapshot RAM A memory (2048 locations × 16 bits per locations). SNAP_A_ADDRESS is written by the microprocessor or DSP. As when accessing cancellation coefficient shadow RAM, SNAP_A_ADDRESS auto-increments after each SNAP_A_DATA register access (read or write). In capture mode, snapshot RAM A contains I samples at even addresses (0, 2, 4, …), and Q samples at odd addresses (1, 3, 5, …). In histogram mode, snapshot RAM A contains 32-bit counter entries, with the upper 16 bits at even addresses (0, 2, 4, …) and the lower 16 bits at odd addresses (1, 3, 5, …).

BITS	DESCRIPTION
[10:0]	Snapshot RAM A address: 0 to 2047
	In capture mode: Snap_RAM_A[0] = sample_I(0) [16 MSBs of 18-bit I sample] Snap_RAM_A[1] = sample_Q(0) [16 MSBs of 18-bit Q sample] . . . Snap_RAM_A[2046] = sample_I(1023) [16 MSBs of I sample] Snap_RAM_A[2047] = sample_Q(1023) [16 MSBs of Q sample]
	In histogram mode: Snap_RAM_A[0] = hist_hi_word(0) Snap_RAM_A[1] = hist_lo_word(0) . . . Snap_RAM_A[2046] = hist_hi_word(1023) Snap_RAM_A[2047] = hist_lo_word(1023)
[15:11]	Reserved

SNAP_A_DATA 0x63 (99) Type: Read/Write Value at RESET: 0x0000

The SNAP_A_DATA register allows access to the snapshot RAM A memory location addressed by SNAP_A_ADDRESS. Snapshot RAM A contains 2048 × 16-bit values, whose organization is described in the preceding table. After SNAP_A_DATA is read or written, the value in SNAP_A_ADDRESS is auto-incremented.

BITS	DESCRIPTION
[15:0]	Snapshot RAM A data

SNAP_A_MINVAL **0x64 (100)** **Type: Read/Write** **Value at RESET: 0x0000**

The SNAP_A_MINVAL register is used only during snapshot RAM A histogram mode. In histogram mode, the microprocessor or DSP can specify a desired range of values to be histogrammed. The minimum value of interest is SNAP_A_MINVAL, while the maximum value of interest is SNAP_A_MAXVAL. Input values ≤ SNAP_A_MINVAL are counted in the snapshot RAM A histogram bin 0. Input values ≥ SNAP_A_MAXVAL are counted in the snapshot RAM A histogram bin 1023.

BITS	DESCRIPTION
[15:0]	Snapshot RAM A (in histogram mode): minimum allowable value

SNAP_A_MAXVAL **0x65 (101)** **Type: Read/Write** **Value at RESET: 0x0000**

The SNAP_A_MAXVAL register is used only during snapshot RAM A histogram mode. In histogram mode, the microprocessor or DSP can specify a desired range of values to be histogrammed. The minimum value of interest is SNAP_A_MINVAL, while the maximum value of interest is SNAP_A_MAXVAL. Input values ≤ SNAP_A_MINVAL are counted in the snapshot RAM A histogram bin 0. Input values ≥ SNAP_A_MAXVAL are counted in the snapshot RAM A histogram bin 1023.

BITS	DESCRIPTION
[15:0]	Snapshot RAM A (in histogram mode): maximum allowable value

SNAP_A_SCALE **0x66 (102)** **Type: Read/Write** **Value at RESET: 0x0000**

The SNAP_A_SCALE register is used only during snapshot RAM A histogram mode. In histogram mode, the microprocessor or DSP can specify a desired range of values to be histogrammed, using SNAP_A_MINVAL and SNAP_A_MAXVAL. However, the difference between SNAP_A_MAXVAL and SNAP_A_MINVAL can be larger than the number of histogram bins (1024). SNAP_A_SCALE is used to scale the difference between the input value (to be histogrammed) and SNAP_A_MINVAL into the allowed 10-bit histogram index range (0..1023). The GC1115 user is responsible for selecting the appropriate shift value from the table.

BITS	DESCRIPTION
[2:0]	Snapshot RAM A (in histogram mode): maximum allowable value
[15:3]	Reserved

SELECT BITS	SIGNAL BITS
7	15:6
6	14:5
5	13:4
4	12:3
3	11:2
2	10:1
1	9:0

Histogram index calculation:

```
shift = 0x7;
if ( (sample[i] >= SNAP_MINVAL) && (sample[i] <= SNAP_MAXVAL) ) {
            j = sample[i] - SNAP_MINVAL;
   index = int(j >> shift);
   hist[index]++
}
```

The GC1115 user is responsible for ensuring that the index (the product of j × SNAP_SCALE) is in the allowed range of 0..1023.

SNAP_A_HISTCOUNT 0x67 (103) Type: Read/Write Value at RESET: 0x0000

The SNAP_A_HISTCOUNT register determines how many groups of samples are observed in histogram mode. SNAP_A_HISTCOUNT is used only during snapshot RAM A histogram mode operation. SNAP_A_HISTCOUNT works in conjunction with POWER_CNT (0x7E). The number of samples in a group is specified in POWER_CNT, while the number of groups monitored during histogram mode is specified in SNAP_A_HISTCOUNT. Thus, the total number of samples observed in histogram mode is POWER_CNT × SNAP_A_HISTCOUNT. At reset, POWER_CNT = 0xFFFF, or 65,535.

BITS	DESCRIPTION
[15:0]	Number of POWER_CNT sample groups to be histogrammed.

RESERVED 0x68–0x6F (104–111)

SNAP_B_CONTROL 0x70 (112) Type: Read/Write Value at RESET: 0x0000

The SNAP_B_CONTROL register controls the operation of snapshot RAM B, including the selection of its data source and the type of data being captured. When using snapshot RAM B in histogram mode, the RAM must first be cleared by writing a 0x0002 to SNAP_B_CONTROL. If the GC1115 is operating in two-channel mode, snapshot RAM B can monitor the samples of either channel 0 or channel 1. Snapshot RAM B does not begin a capture or histogram until the SNAP_B_SYNC event occurs. SNAP_B_SYNC cannot be triggered by a periodic TIMER event.

BITS	DESCRIPTION		
[1:0]	Snapshot RAM B command:	00: DISABLE (ignore all other bits in word)	
		01: ENABLE (observe all other bits)	
		1x: CLEAR_RAM (ignore all other bits until clear is done)	
2	Channel-channel data source:	0: Channel 0	1: Channel 1
[5:3]	Snapshot RAM B data source:	001: Input	010: After stage 1
		011: After stage 2	100: After stage 3
		101: After stage 4	
[7:6]	Snapshot RAM B operating mode:	00: Capture 1k samples	01: Histogram I samples
		10: Histogram Q samples	11: Histogram ($I^2 + Q^2$)
[15:8]	Reserved		

SNAP_B_STATUS 0x71 (113) Type: Read-Only Value at RESET: 0x0000

The SNAP_B_STATUS register can be read to determine the current status (state) of snapshot RAM B. After sending a 0x2 command (clear RAM) to SNAP_B_CONTROL, SNAP_B_STATUS can be polled to determine when the RAM has been cleared. After a snapshot RAM B capture completes, the microprocessor or DSP can receive an interrupt by enabling bit 0 of INT_MASK. During histogram operation, if one or more snapshot RAM B histogram bins overflows its 32-bit count, bit 2 of INT_MAP is set. If bit 2 of INT_MASK is set, a snapshot RAM B bin overflow also generates an interrupt. Snapshot RAM B does not begin a capture or histogram until the SNAP_B_SYNC event occurs. SNAP_B_SYNC cannot be triggered by a periodic TIMER event.

BITS	DESCRIPTION		
[2:0]	Snapshot RAM B status:	000: OFF	001: enabled (waiting) (after histogram completed)
		010: active (capturing)	011: capture complete
		100: resetting (clearing all snapshot RAM bins)	
[15:3]	Reserved		

SNAP_B_ADDRESS **0x72 (114)** **Type: Read-Only** **Value at RESET: 0x0000**

The SNAP_B_ADDRESS register contains a pointer into snapshot RAM B memory (2048 locations × 16 bits per locations). SNAP_B_ADDRESS is written by the microprocessor or DSP. As when accessing cancellation coefficient shadow RAM, SNAP_B_ADDRESS auto-increments after each SNAP_B_DATA register access (read or write). In capture mode, snapshot RAM A contains I samples at even addresses (0, 2, 4, ...), and Q samples at odd addresses (1, 3, 5, ...). In histogram mode, snapshot RAM B contains 32-bit counter entries, with the upper 16 bits at even addresses (0, 2, 4, ...) and the lower 16 bits at odd addresses (1, 3, 5, ...).

BITS	DESCRIPTION
[10:0]	Snapshot RAM B address: 0 to 2047
	In capture mode: Snap_RAM_A[0] = sample_I(0) [16 MSBs of 18-bit I sample] Snap_RAM_A[1] = sample_Q(0) [16 MSBs of 18-bit Q samp] . . . Snap_RAM_A[2046] = sample_I(1023) [16 MSBs of I sample] Snap_RAM_A[2047] = sample_Q(1023) [16 MSBs of Q sample]
	In histogram mode: Snap_RAM_A[0] = hist_hi_word(0) Snap_RAM_A[1] = hist_lo_word(0) . . . Snap_RAM_A[2046] = hist_hi_word(1023) Snap_RAM_A[2047] = hist_lo_word(1023)
[15:11]	Reserved

SNAP_B_DATA **0x73 (115)** **Type: Read/Write** **Value at RESET: 0x0000**

The SNAP_B_DATA register allows access to the snapshot RAM B memory location addressed by SNAP_B_ADDRESS. Snapshot RAM B contains 2048 × 16-bit values, whose organization is described in the discussion of SNAP_B_ADDRESS. After SNAP_B_DATA is read or written, the value in SNAP_B_ADDRESS is auto-incremented.

BITS	DESCRIPTION
[15:0]	Snapshot RAM B data

SNAP_B_MINVAL **0x74 (116)** **Type: Read/Write** **Value at RESET: 0x0000**

The SNAP_B_MINVAL register is used only during snapshot RAM B histogram mode. In histogram mode, the microprocessor or DSP can specify a desired range of values to be histogrammed. The minimum value of interest is SNAP_B_MINVAL, while the maximum value of interest is SNAP_B_MAXVAL. Input values ≤ SNAP_B_MINVAL are counted in the snapshot RAM B histogram bin 0. Input values ≥ SNAP_B_MAXVAL are counted in the snapshot RAM B histogram bin 1023.

BITS	DESCRIPTION
[15:0]	Snapshot RAM B (in histogram mode): minimum allowable value

SNAP_B_MAXVAL 0x75 (117) Type: Read/Write Value at RESET: 0x0000

The SNAP_B_MAXVAL register is used only during snapshot RAM B histogram mode. In histogram mode, the microprocessor or DSP can specify a desired range of values to be histogrammed. The minimum value of interest is SNAP_B_MINVAL, while the maximum value of interest is SNAP_B_MAXVAL. Input values ≤ SNAP_B_MINVAL are counted in the snapshot RAM B histogram bin 0. Input values ≥ SNAP_B_MAXVAL are counted in the snapshot RAM B histogram bin 1023.

BITS	DESCRIPTION
[15:0]	Snapshot RAM B (in histogram mode): maximum allowable value

SNAP_B_SCALE 0x76 (118) Type: Read/Write Value at RESET: 0x0000

The SNAP_B_SCALE register is used only during snapshot RAM B histogram mode. In histogram mode, the microprocessor or DSP can specify a desired range of values to be histogrammed, using SNAP_B_MINVAL and SNAP_B_MAXVAL. However, the difference between SNAP_B_MAXVAL and SNAP_B_MINVAL can be larger than the number of histogram bins (1024). SNAP_B_SCALE is used to scale the difference between the input value (to be histogrammed) and SNAP_B_MINVAL into the allowed 10-bit histogram index range (0..1023). The GC1115 user is responsible for selecting the appropriate shift value from the table.

BITS	DESCRIPTION
[2:0]	Snapshot RAM B (in histogram mode): maximum allowable value
[15:3]	Reserved

SELECT BITS	SIGNAL BITS
7	15:6
6	14:5
5	13:4
4	12:3
3	11:2
2	10:1
1	9:0

Histogram index calculation:

```
shift = 0x7;
if ( (sample[i] >= SNAP_MINVAL) && (sample[i] <= SNAP_MAXVAL) ) {
       j = sample[i] - SNAP_MINVAL;
       index = int(j >> shift);
       hist[index]++
}
```

The GC1115 user is responsible for ensuring that index (the product of j × SNAP_SCALE) is in the allowed range of 0..1023.

SNAP_B_HISTCOUNT 0x77 (119) Type: Read/Write Value at RESET: 0x0000

The SNAP_B_HISTCOUNT register determines how many groups of samples are observed in histogram mode. SNAP_B_HISTCOUNT is used only during snapshot RAM B histogram mode operation. SNAP_B_HISTCOUNT works in conjunction with POWER_CNT (0x7E). The number of samples in a group is specified in POWER_CNT, while the number of groups monitored during histogram mode is specified in SNAP_B_HISTCOUNT. Thus the total number of samples observed in histogram mode is POWER_CNT × SNAP_B_HISTCOUNT. At reset, POWER_CNT = 0xFFFF, or 65,535.

BITS	DESCRIPTION
[15:0]	Number of POWER_CNT sample groups to be histogrammed.

RESERVED **0x78–0x7D (120–125)**

Power Control Register (Address 126)

POWER_CNT **0x7E (126)** **Type: Read/Write** **Value at RESET: 0xFFFF**

The POWER_CNT register determines how many samples are used in each group during snapshot histogram RAM operation. During snapshot RAM histogram operation, the total number of samples observed for the histogram is POWER_CNT × SNAP_HISTCOUNT. At GC1115 reset, POWER_CNT = 0xFFFF (65,535).

BITS	DESCRIPTION
[15:0]	Number of samples in a histogram group (0 to 65,535)

Interpolation Registers (Addresses 128–169)

INTERP_CTL **0x80 (128)** **Type: Read/Write** **Value at RESET: 0x0000**

BITS	DESCRIPTION	
[1:0]	Interpolator operation:	00: Interpolate by 2, complex output
		01: Interpolate by 2, $f_S/4$ enabled, real output
		1x: Interpolate by 4, $f_S/4$ enabled, real output
[15:2]	Reserved	

NOTE:

To bypass the interp-by-4 stage, clear bit 4 of the CONTROL register, set 0x82 to 0x8000, and clear 0x83 to 0xA9.

INTERP_COEFS **0x82–0xA9 (130–169)** **Type: Read/Write** **Value at RESET: 0x8000 (0x82), 0x0000 (0x83–0xA9)**

Addresses 0x82 to 0xA9 store the 40 interpolation coefficients of the interpolation stage. These coefficients are accessed even if the interpolation stage is bypassed, i.e., even when bit 4 of CONTROL (0x2) is cleared. GC1115 users must therefore ALWAYS initialize the interpolation coefficients. After RESET, the interpolation coefficients are initialized for bypass operation (value at address 0x82 = 0x8000; all other interpolation coefficients = 0). The section entitled *Interpolate-by-4 Operation* describes the required interp-by-4 coefficients during interpolation.

BITS	DESCRIPTION
[15:0]	Signed, 16-bit interp-by-4 coefficient, from –32768 to +32767

Soft Limiter Block (Addresses 192–248)

NOTE:

The soft limiter block can safely be bypassed under almost all operating conditions. The soft limiter is only required when very low PAR levels (≤ 5 dB output PAR) cause PDC canceler resources to be overwhelmed. At these low PAR levels, the EVM and PCDE specifications already cannot be met, and the soft limiter probably makes the ACLR worse.

SOFT_LENGTH 0xC0 (192) Type: Read/Write Value at RESET: 0x0000

The SOFT_LENGTH register controls the operation of the GC1115 soft limiter. In addition to providing a final limiter after the interpolation stage, the soft limiter also contains I and Q gain and offset values that can compensate for gain and offset imbalances in I/Q modulators that follow the GC1115. The soft limiter is bypassed by clearing bit 5 of the CONTROL register.

When SOFT_LENGTH[1:0] = 01, taper table uses SOFT_COEF0 to SOFT_COEF3

When SOFT_LENGTH[1:0] = 10, taper table uses SOFT_COEF0 to SOFT_COEF7

When SOFT_LENGTH[1:0] = 11, taper table uses SOFT_COEF0 to SOFT_COEF15

Because the I/Q gain and I/Q offset registers are always in the GC1115 data path (even when the soft limiter is bypassed), GC1115 users must initialize the gain and offset register appropriately.

The default OUT_GAIN0 and OUT_GAIN1 values are 0, so the GC1115 outputs zeros at RESET. **In order to generate non-zero GC1115 output values, OUT_GAIN0 and OUT_GAIN1 must be set to non-zero values (preferably 0x2000, which equates to 1.0). OUT_GAIN0 and OUT_GAIN1 must be written by the microprocessor or DSP, or the OUT_A and OUT_B ports always output zeros.**

The default I and Q offset is 0 (i.e., I and Q samples are not offset at RESET).

BITS	DESCRIPTION
[1:0]	Number of samples in the soft limiting interval: 01: 9-sample soft limit length (4 coefficients) 10: 17-sample soft limit length (8 coefficients) 11: 33-sample soft limit length (16 coefficients) The middle soft-limiter coefficient is always an implied 1
[15:2]	Reserved

SOFT_TSQD 0xC1 (193) Type: Read/Write Value at RESET: 0xFFFF

The SOFT_TSQD register contains the soft-limiter threshold-squared value. This threshold-squared value is scaled identically to the DETECT_TSQD and GAIN_TSQD PDC stage thresholds. Note that the default SOFT_TSQD value is 0xFFFF, ensuring that the soft limiter threshold is set to its maximum value at RESET.

BITS	DESCRIPTION
[15:0]	Soft-limiter threshold-squared value

SOFT_COEF[0:15] 0xC2–0xD1 (194–209) Type: Read/Write Value at RESET: 0x0000

The sixteen SOFT_COEF registers hold the soft limiter taper table. The taper table contains 4, 8, or 16 normalized coefficients, whose values are scaled by a variable that is proportional to the size of the detected, over-threshold soft limiter peak. SOFT_COEF0 at address 0xC2 is the smallest coefficient, while SOFT_COEFn (n=3, 7, or 15) is the largest coefficient (near to a normalized value of 1.0). The soft limiter uses an internal, normalized value of 1.0 at SOFT_COEFm (m = 4, 8, or 16) that is NOT stored in the SOFT_COEF taper table. The taper table values are applied to the N samples before the detected peak, and again to the N samples after the detected peak (N = 4, 8, or 16). See the section of this document entitled *Soft Limiter Operation* for a detailed description of the soft-limiter taper table.

When SOFT_LENGTH[1:0] = 01, taper table uses SOFT_COEF0 to SOFT_COEF3

When SOFT_LENGTH[1:0] = 10, taper table uses SOFT_COEF0 to SOFT_COEF7

When SOFT_LENGTH[1:0] = 11, taper table uses SOFT_COEF0 to SOFT_COEF15

BITS	DESCRIPTION
[15:0]	Soft-limiter taper table coefficient (unsigned, 16-bit value)

SOFT_TAB_SCALE **0xD2 (210)** **Type: Read/Write** **Value at RESET: 0xFFFF**

The SOFT_TAB_SCALE register contains the soft limiter lookup table scale factor. For a desired shift value of N bits, SOFT_TAB_SCALE should be set to N – 17. The valid range for SOFT_TAB_SCALE is 0 to 15, encoded in the 4 LSBs.

BITS	DESCRIPTION
[3:0]	Soft limiter lookup table scale factor (# bits to shift, 0 to 15)
[15:4]	Reserved

SOFT_INVGAIN[0:31] **0xD3–0xF2 (211–242)** **Type: Read/Write** **Value at RESET: 0x000**

The thirty-two SOFT_INVGAIN registers hold the soft limiter inverse gain lookup table. The taper table contains 31 inverse gain values between 1.0 and g, where g is the maximum expected over-threshold value. For example, if the soft limiter expects to see a peak after PDC stage 4 that is at most 50% higher than the SOFT_TSQD threshold, g would be set to 1.5. SOFT_INVGAIN0 (0xD3) contains the smallest inverse gain value. SOFT_INVGAIN31 contains the largest inverse gain value. See the section of this document entitled *Soft Limiter Operation* for a detailed description of the inverse gain lookup table.

BITS	DESCRIPTION
[15:0]	Soft-limiter inverse gain lookup coefficient (unsigned, 16-bit value)

OUT_GAIN0 **0xF3 (243)** **Type: Read/Write** **Value at RESET: 0x0000**

The OUT_GAIN0 register contains the OUT_A output gain. Under normal circumstances, the microprocessor or DSP should initialize OUT_GAIN0 to 0x2000, which corresponds to a normalized gain of 1.0. OUT_GAIN0 can provide up to two bits of boost: an OUT_GAIN0 value of 0x3FFF corresponds to a normalized gain of 3.999939. OUT_GAIN0 is a signed value, so negative OUT_GAIN0 values are permitted. Users should be aware that a negative OUT_GAIN0 value causes a 180° phase inversion of the OUT_A output signal.

The default OUT_GAIN0 value is 0, so the GC1115 outputs zeros at RESET. **In order to generate non-zero GC1115 output values, OUT_GAIN0 and OUT_GAIN1 must be set to non-zero values (preferably 0x2000, which equates to 1.0). OUT_GAIN0 and OUT_GAIN1 must be written by the microprocessor or DSP, or OUT_A and OUT_B always output zeros.**

BITS	DESCRIPTION		
[14:0]	Output port-A gain (2 MSBs are GAIN bits):	0x7FFF: Gain of 3.999939	0x4000: Gain of 2
		0x2000: Gain of 1	0x1FFF: Gain of 0.999893
		0x0000: Gain of 0 (zeros are output)	
15	Output gain sign bit:	0: Positive gain	1: Negative gain

NOTE:

Output gain above 2000× results in saturated output samples if any peak/minimum signals are not reduced.

OUT_GAIN1 0xF4 (244) Type: Read/Write Value at RESET: 0x0000

The OUT_GAIN1 register contains the OUT_B output gain. Under normal circumstances, the microprocessor or DSP should initialize OUT_GAIN1 to 0x2000, which corresponds to a normalized gain of 1. OUT_GAIN1 can provide up to two bits of boost; an OUT_GAIN1 value of 0x3FFF corresponds to a normalized gain of 3.999939. OUT_GAIN1 is a signed value, so negative OUT_GAIN1 values are permitted. Users should be aware that a negative OUT_GAIN1 value would cause a 180-degree phase inversion of the OUT_B output signal.

The default OUT_GAIN1 value is 0, so the GC1115 outputs zeros at RESET. **In order to generate non-zero GC1115 output values, OUT_GAIN0 and OUT_GAIN1 must be set to non-zero values (preferably 0x2000, which equates to 1.0). OUT_GAIN0 and OUT_GAIN1 must be written by the microprocessor or DSP, or OUT_A and OUT_B always output zeros.**

BITS	DESCRIPTION		
[14:0]	Output port-B gain (2 MSBs are GAIN bits):	0x7FFF: Gain of 3.999939	0x4000: Gain of 2
		0x2000: Gain of 1	0x1FFF: Gain of 0.999893
		0x0000: Gain of 0 (zeros are output)	
15	Output gain sign bit:	0: Positive gain	1: Negative gain

NOTE:

Output gain above 2000× results in saturated output samples if any peak/minimum signals are not reduced.

OUT_OFFSET_I0 0xF5 (245) Type: Read/Write Value at RESET: 0x0000

The OUT_OFFSET_I0 register contains the OUT_A offset value for the I0 channel. In one-channel operation, I0 is the I-channel offset. OUT_OFFSET register values are signed, 16-bit values that are aligned with the 16 MSBs of the 18-bit signed I-channel sample. OUT_OFFSET_I0 is also the channel-0 offset applied to the real output samples in real-output modes (i.e., when the interpolate block is generating 2× real or 4× real samples).

BITS	DESCRIPTION
[15:0]	Channel-0, I-leg dc offset (also the channel-0 real offset in real output mode)

OUT_OFFSET_Q0 0xF6 (246) Type: Read/Write Value at RESET: 0x0000

The OUT_OFFSET_Q0 register contains the OUT_A offset value for the Q0 channel. In one-channel operation, Q0 is the Q-channel offset. OUT_OFFSET register values are signed, 16-bit values that are aligned with the 16 MSBs of the 18-bit signed Q-channel sample.

BITS	DESCRIPTION
[15:0]	Channel-0, Q-leg dc offset

OUT_OFFSET_I1 0xF7 (247) Type: Read/Write Value at RESET: 0x0000

The OUT_OFFSET_I1 register contains the OUT_B I-offset value for the second channel during two-channel operation. OUT_OFFSET register values are signed, 16-bit values that are aligned with the 16 MSBs of the 18-bit signed I-channel sample. OUT_OFFSET_I1 is also the channel-1 offset applied to the real output samples in real-output modes (i.e., when the interpolate block is generating 2× real or 4× real samples).

BITS	DESCRIPTION
[15:0]	Channel-1, I-leg dc offset (also the channel-1 real offset in real output mode)

OUT_OFFSET_Q1 **0xF8 (248)** **Type: Read/Write** **Value at RESET: 0x0000**

The OUT_OFFSET_Q1 register contains the OUT_B Q-offset value for the second channel during two-channel operation. OUT_OFFSET register values are signed, 16-bit values that are aligned with the 16 MSBs of the 18-bit signed Q-channel sample.

BITS	DESCRIPTION
[15:0]	Channel-1, Q-leg dc offset

GC1115 Power Consumption

While GC1115 power consumption varies, depending on the number of input channels, the IN_CLK frequency, the output PAR level, the output interpolator, etc., the following GC1115 power consumption values were measured at room temperature and nominal voltage conditions using a 4-carrier W-CDMA Test Model 3 input signal, output PAR = 6 dB, 4 PDC stages, cancel pulse length 127.

Table 16. GC1115 Power Consumption

GC1115 CONDITIONS	DECIMATION	POWER
One-channel operation		
30.72 Msps	2	1.1 W
61.44 Msps	1	1.6 W
40 Msps	2	1.5 W
80 Msps	1	2.0 W
120 Msps	2	2.1 W
Two-channel operation		
30.72 Msps	1	1.8 W
40 Msps	1	2.3 W
61.44 Msps	2	2.5 W

Factors Affecting GC1115 Power Consumption

- GC1115 IN_CLK frequency linearly affects power consumption: the higher the GC1115 IN_CLK rate, the higher the power consumption.
- For higher (less demanding) output PAR levels, GC1115 users may consider disabling PDC stage 4, which reduces power consumption.
- GC1115 power consumption can be decreased by simultaneously enabling 2× decimation of the input signal and 2× interpolation of the output signal. With the 2× decimate/2× interp enabled, the GC1115 input and output rates are equivalent, but the PDC stages operate at half speed, decreasing power consumption by as much as 30%. However, *users considering this option should determine whether the decrease in output ACLR due to this 2× decimate/2× interpolate process is acceptable*.
- Power consumption increases with decreasing output PAR levels. As more peaks are cancelled, power consumption increases. This effect is small.
- Power consumption increases with cancel pulse length. The longer the cancel pulse, the higher the power consumption. This effect is small.

Latency

The latency (in samples) through the GC1115 is determined by the number of PDC stages enabled and by the CANCEL_DELAY value for a given cancel pulse. All PDC stages normally use the same CANCEL_DELAY value. Given these two paramenters, the sample latency through the GC1115 (in samples) is calculated as follows:

Latency = [(# of PDC stages disabled × 1.5) + {# of PDC stages enabled × (CANCEL_DELAY + 47.5)} + 16.5]

A fractional sample latency should be increased to the next-larger integer.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_{DD}	Core supply voltage range	–0.3 V to 1.32 V
V_{DD1}	PLL digital supply voltage range	–0.3 V to 1.32 V
$V_{DDA1,2}$	PLL analog supply voltage range	–0.3 V to 1.32 V
V_{DDSHV}	Input supply voltage range	–0.3 V to 3.6 V
V_{IN}	Input voltage range	–0.3 V to V_{DDSHV} + 0.3 V
T_{Jmax}	Maximum junction temperature	105C
T_C	Operating case temperature	–40C to 85C
T_{stg}	Storage temperature	–55C to 150C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}			0		V
Core supply votlage, V_{DD}		1.14	1.2	1.26	V
PLL digital supply voltage, V_{DD1}		1.08	1.2	1.32	V
PLL analog supply voltage, $V_{DDA1,2}$		1.14	1.2	1.26	V
I/O supply voltage, V_{DDSHV}		3	3.3	3.6	V
Input voltage range, V_{IN}		3	3.3	V_{DDSHV} + 0.3	V
Power consumption				3.3(1)	W
Operating case temperature, T_C		–45	25	85	°C
Maximum junction temperature, T_{Jmax}				105	°C

(1) Two-channel operation, IN_CLK = 80 MHz, decimate by 2, interpolate by 2.

PACKAGE THERMAL RESISTANCE CHARACTERISTICS(1)(2)

PACKAGE	AIRFLOW (m/s)	$R_{\theta JA}$ (°C/W)	$R_{\theta JC}$ (°C/W)
IZDJ	0	18.3	5.9
	1	16.2	5.9
	2.5	15.3	5.9

(1) Simulations based on 1S2P board type as defined by JEDEC, tested at 85°C ambient temperature. Reference JEDEC Standard JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*.

(2) Adding thermal vias significantly improves the thermal performance of the device. To use the thermal balls on the GC1115IZDJ package:
   a. An array of 36 land pads must be added on the top layer of the PCB where the package is to be mounted.
   b. The PCB land pads should be the same diameter as the vias in the package substrate for optimal board level reliability temperature cycle performance.
   c. The land pads on the PCB should be connected together and to PCB through-holes. The PCB through-holes should in turn be connected to the ground plane for heat dissipation.
   d. A solid internal plane is preferred for spreading the heat.

SWITCHING CHARACTERISTICS

	PARAMETER		MIN	MAX	UNIT
JTAG:					
tperiod	JTAG clock period		14		ns
tjt_ckh	JTAG clock high time		5		ns
tjt_ckl	JTAG clock low time				ns
tjt_su	JTAG input (TDI or TMS) setup time before TCK goes high		1		ns

SWITCHING CHARACTERISTICS (continued)

	PARAMETER		MIN	MAX	UNIT
JTAG:					
tjt_hd	JTAG input (TDI or TMS) hold time after TCK goes high		4		ns
tjt_dly	JTAG output (TDO) delay from falling edge of TCK		4		ns
tjt_oh	JTAG output (TDO) hold time from falling edge of TCK			1	ns
FUNC DATA PATH:					
tin_duty_cycle	Clock duty cycle		43.75%	56.25%	
tperiod	Clock period	1:4x(1)	12.5		ns
		1:2, 1:x(1)	7.7		ns
tin_ckh	Clock high time	1:4x(1)	5.47	7.03	ns
		1:2, 1:x(1)	3.37	4.33	ns
tin_ckl	Clock low time	1:4x(1)	5.47	7.03	ns
		1:2, 1:x(1)	3.37	4.33	ns
tin_su	Input setup before clock goes high		0.5		ns
tin_hd	Input hold time after clock goes high		1.0		ns
tout_dly	Output delay from rising edge of clock		2.4		ns
tout_hd	Output hold time from rising edge of clock			0.2	ns
MPUREG 2 WIRE MODE:					
tup_cenh	CE_N high time		4		ns
tup_cenl	CE_N low time		7		ns
tup_a_su	Address setup time before read or write		6		ns
tup_a_hd	Address hold time after read or write		3		ns
tup_rc_su	Control setup time before read		6		ns
tup_wc_su	Control setup time before write		2		ns
tup_rc_hd	Control hold after read		0		ns
tup_wc_hd	Control hold after write		2		ns
tup_wd_su	Control data setup before read or write		2		ns
tup_wd_hd	Control data hold after read or write		3		ns
tup_dly	Control ouput delay CE low and A stable to C(read operation)			6.5	ns
MUPRAM 2 WIRE MODE:					
tup_cenh	CE_N high time		3		ns
tup_cenl(2)	CE_N low time		2 × tcore		ns
tup_a_su	Address setup time before read or write		7		ns
tup_a_hd	Address hold time after read or write		3.5		ns
tup_rc_su	Control setup time before read		7		ns
tup_wc_su	Control setup time before write		4		ns
tup_rc_hd	Control hold after read		0		ns
tup_wc_hd	Control hold after write		0		ns
tup_wd_su	Control data setup before read or write		2		ns
tup_wd_hd	Control data hold after read or write		3.5		ns
tup_dly(2)	Control output delay CE low and A stable to C(read operation)			2 × tcore	ns

(1) These are for different clocking modes. One clocking mode is identified as (1:4:x) and means the internal clock is 4× the chip's input clock (IN_CLK) and the transmit clock can be 1×, 2×, or 4× IN_CLK's rate. The second clocking mode is (1:2,1:x) and means the internal clock is 2× or 1× the chip's input clock (IN_CLK) and the transmit clock can be 1× (or 2× if the core clock is 2×) IN_CLK's rate.

(2) tup_cenl and tup_dly are a function of tcore, the GC1115 internal clock period. tcore's relationship to IN_CLK is determined by the core PLL setup (options are 1×, 2×, and 4× multiples of the IN_CLK rate). Under normal operating conditions, the core PLL is set to 4 × IN_CLK. Under these conditions, the duration of tcore is 1/4 of IN_CLK.

TIMING PARAMETER INFORMATION

Control Timing for Edge With Single Strobe (2-Wire Mode)

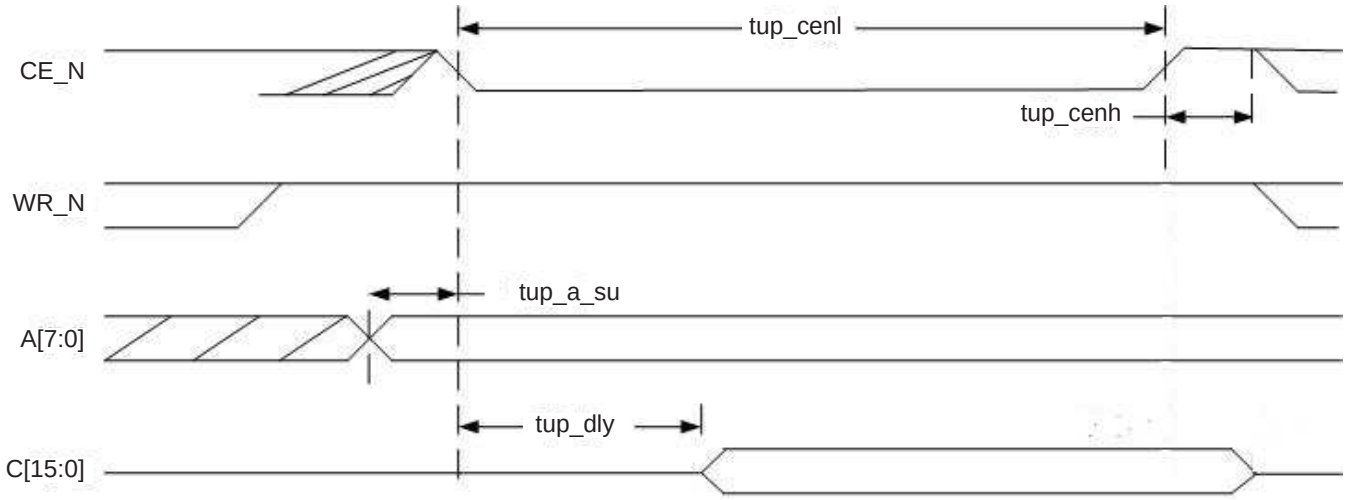


Figure 16. Read Cycle – $\overline{RD}$ Held Low

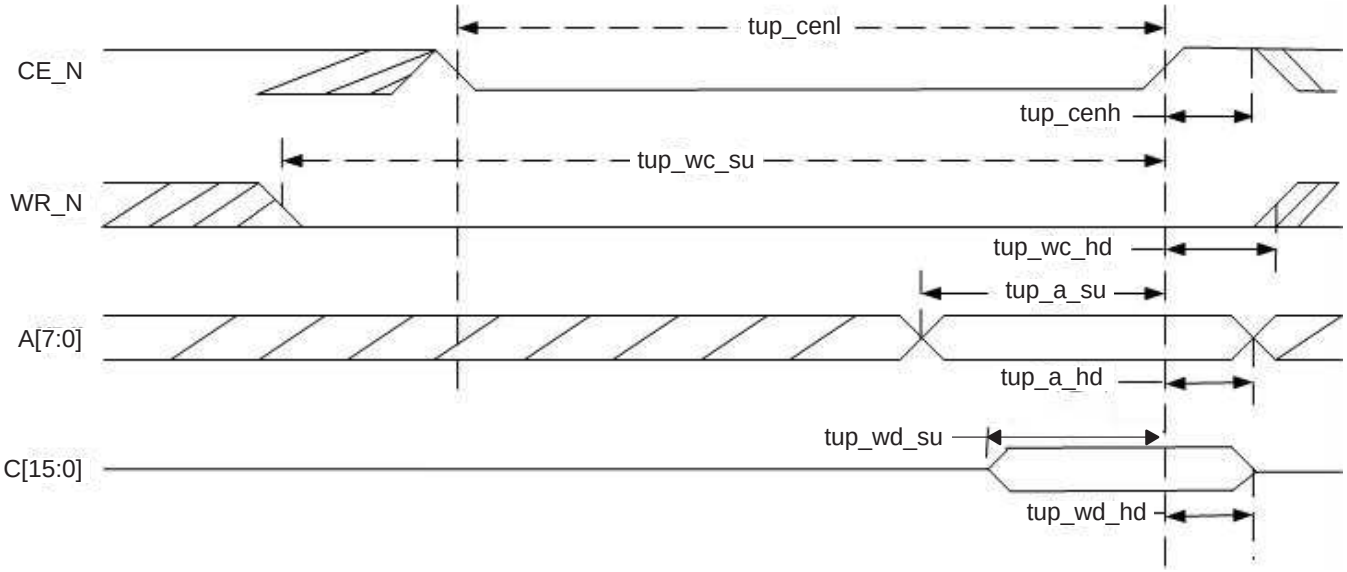


Figure 17. Write Cycle – $\overline{RD}$ Held Low

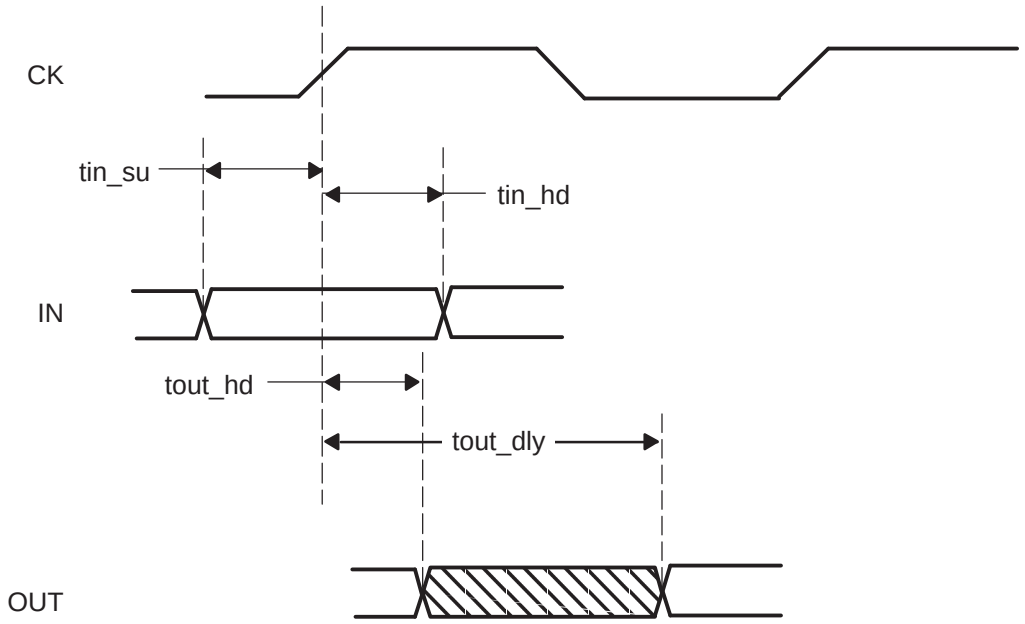


Figure 18. Generic Data Setup and Hold. Data Output Hold and Delay

DEVICE INFORMATION

ZDJ Package
(Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
T	VSS	VSS	OUT_A12	OUT_A15	OUT_IQ_SEL	OUT_B1	OUT_B3	OUT_B5	OUT_B6	OUT_B8	OUT_B11	OUT_B14	OUT_B17	$\overline{\text{SYNC\_B}}$	VSS	VSS	T
R	VSS	VSS	OUT_A11	OUT_A14	OUT_A17	OUT_B0	OUT_B2	OUT_B4	OUT_B7	OUT_B10	OUT_B13	OUT_B15	$\overline{\text{SYNC\_OUT}}$	$\overline{\text{SYNC\_A}}$	VSS	VSS	R
P	OUT_A9	OUT_A10	VSS	VDD	VDDSHV	OUT_A13	OUT_A16	LOOP	OUT_B9	OUT_B12	OUT_B16	VDDSHV	VDD	VSS	IN_B17	IN_B15	P
N	OUT_A6	OUT_A8	VDD	VSS	VDD	VDDSHV	VDDSHV	VDDSHV	VDDSHV	VDDSHV	VDDSHV	VDD	VSS	VDD	IN_B13	IN_B12	N
M	OUT_A3	OUT_A5	VDDSHV	VDD	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VDD	VDDSHV	IN_B10	IN_B9	M
L	OUT_A0	OUT_A1	OUT_A7	VDDSHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDSHV	IN_B16	IN_B8	IN_B7	L
K	D0	OUT_CLK	OUT_A4	VDDSHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDSHV	IN_B14	IN_B6	IN_B5	K
J	D2	D1	OUT_A2	VDDSHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDSHV	IN_B11	IN_B4	IN_B3	J
H	D3	D4	D7	VDDSHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDSHV	IN_B0	IN_B2	IN_B1	H
G	D5	D6	D9	VDDSHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDSHV	IN_A14	IN_A16	IN_A17	G
F	D8	D10	D13	VDDSHV	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDSHV	IN_A11	IN_A13	IN_A15	F
E	D11	D12	VDDSHV	VDD	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VDD	VDDSHV	IN_A10	IN_A12	E
D	D14	D15	VDD	VSS	VDD	VDDSHV	VDDSHV	VDDSHV	VDDSHV	VDDSHV	VDDSHV	VDD	VSS	VDD	IN_A8	IN_A9	D
C	A1	A0	VSS	VDD	VDDSHV	A2	A6	TCK	IN_A3	VDDA2	VSS1	IN_CLK	VDD	VSS	VSSA1	VDDA1	C
B	VSS	VSS	A3	A5	A7	$\overline{\text{RD}}$	TEST_MODE	TRST	TMS	IN_A2	IN_A5	IN_A7	$\overline{\text{RESET}}$	VDD1	VSS	VSS	B
A	VSS	VSS	A4	$\overline{\text{INT}}$	$\overline{\text{WR}}$	$\overline{\text{CS}}$	TDO	TDI	IN_A0	IN_A1	VPP	IN_A4	IN_A6	VSSA2	VSS	VSS	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

P0050-01

Table 17. TERMINAL FUNCTIONS (Alphabetical Listing)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A[7:0]	B5, C7, B4, A3, B3, C6, C1, C2	I	Address bus – active-high inputs
$\overline{CS}$	A6	I	CHIP SELECT – active-low chip select
D[15:0]	D2, D1, F3, E2, E1, F2, G3, F1, H3, G2, G1, H2, H1, J1, J2, K1	I/O	Data bus - active-high bidirectional I/O
IN_A[17:0]	G16, G15, F16, G14, F15, E16, F14, E15, D16, D15, B12, A13, B11, A12, C9, B10, A10, A9	I	Input port A, bits 17 (MSB) through 0 (LSB). IN_A carries I samples in parallel input mode; I/Q samples in multiplexed one-channel input mode
IN_B[17:0]	P15, L14, P16, K14, N15, N16, J14, M15, M16, L15, L16, K15, K16, J15, J16, H15, H16, H14	I	Input port B, bits 17 (MSB) through 0 (LSB).IN_B carries Q samples in parallel mode; I/Q samples of second channel in 2-channel mode
IN_CLK	C12	I	Input data clock (drives the PLL that generates CHIP_CLK) Note: This pin is also the scan clock when GC1115 is in scan mode.
$\overline{INT}$	A4	O	INTERRUPT – active-low output
LOOP	P8	O	Output pad for Tx PLL loopback (MUST BE UNCONNECTED – NO LOAD)
OUT_A[17:0]	R5, P7, T4, R4, P6, T3, R3, P2, P1, N2, L3, N1, M2, K3, M1, J3, L2, L1	O	Output port A, bits 17 (MSB) through 0 (LSB) OUT_A carries I samples in parallel output mode; I/Q samples in multiplexed 1-channel output mode
OUT_B[17:0]	T13, P11, R12, T12, R11, P10, T11, R10, P9, T10, R9, T9, T8, R8, T7, R7, T6, R6	O	Output port B, bits 17 (MSB) through 0 (LSB) OUT_B carries Q samples in parallel mode; I/Q samples of second channel in 2-channel mode
OUT_CLK	K2	O	Output data clock (do NOT use to drive other parts – for test purposes only)
OUT_IQ_SEL	T5	O	Output I/Q select pin (low = I, high = Q) – only active in multiplexed I/Q output modes
$\overline{RD}$	B6	I	READ – Active-low read input (option: ground $\overline{RD}$ to use $\overline{WR}$ as a write/read pin)
$\overline{RESET}$	B13	I	CHIP RESET – Active-low input
$\overline{SYNC\_A}$	R14	I	Input synchronization pin A (active-low)
$\overline{SYNC\_B}$	T14	I	Input synchronization pin B (active-low)
$\overline{SYNC\_OUT}$	R13	O	Output sync pin (active-low)
TCK	C8	I	JTAG clock
TDI	A8	I	JTAG data in
TDO	A7	O	JTAG data out
TEST_MODE	B7	I	Test mode (not required for operation; pull to GND)
TMS	B9	I	JTAG mode select
TRST	B8	I	JTAG reset (during GC1115 reset, TRST must be pulled low, then high)
VDD	C4, C13, D3, D5, D12, D14, E4, E6, E7, E8, E9, E10, E11, E13, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12, M4, M6–M11, M13, N3, N5, N12, N14, P4, P13	–	Digital core supply voltage, 1.2 V (40 pins)
VDD1	B14	–	Digital supply voltage for both PLLs (1 pin)
VDDA1	C16	–	PLL 1 analog supply voltage (1 pin)
VDDA2	C10	–	PLL 2 analog supply voltage (1 pin)

Table 17. TERMINAL FUNCTIONS (Alphabetical Listing) (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VDDSHV	C5, D6–D11, E3, E14, F4, F13, G4, G13, H4, H13, J4, J13, K4, K13, L4, L13, M3, M14, N6–N11, P5, P12	–	I/O supply voltage, 3.3 V (31 pins)
VPP	A11	–	E-fuse program supply voltage (not required for operation; pull to GND)
VSS	A1, A2, A15, A16, B1, B2, B15, B16, C3, C14, D4, D13, E5, E12, F6–F11, G6–G11, H6–H11, J6–J11, K6–K11, L6–L11, M5, M12, N4, N13, P3, P14, R1, R2, R15, R16, T1, T2, T15, T16,	–	Digital ground (64 pins)
VSS1	C11	–	Digital ground for both PLLs (1 pin)
VSSA1	C15	–	PLL 1 analog ground (1 pin)
VSSA2	A14	–	PLL 2 analog ground (1 pin)
$\overline{WR}$	A5	I	WRITE - Active-low write input (option: ground $\overline{RD}$ to use $\overline{WR}$ as a write/read pin)

APPLICATION INFORMATION

PC Board Layout Notes

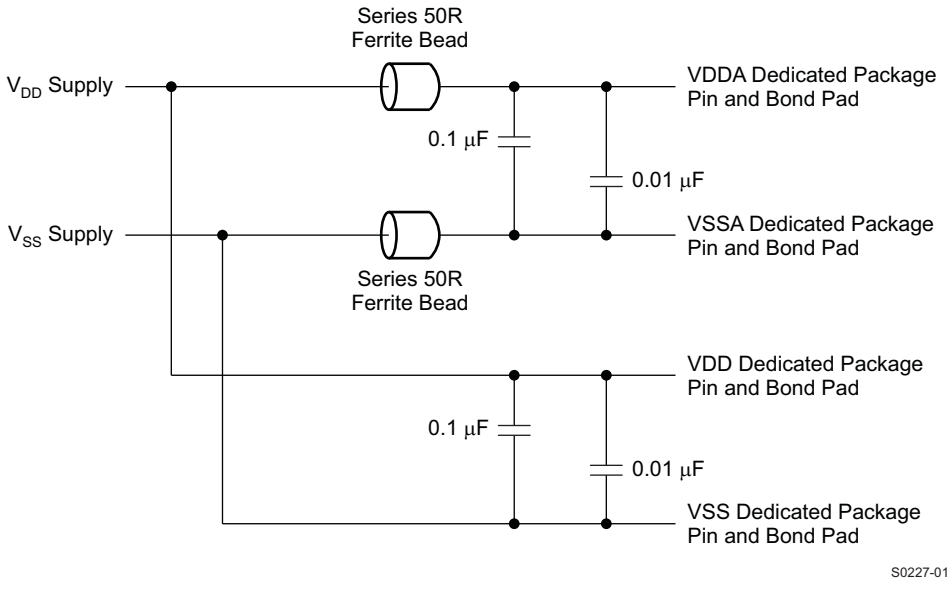
1. Leave the LOOP pin unconnected.
2. VPP is used only in manufacturing (for die ID). Attach VPP via a pulldown resistor to GND.
3. $\overline{\text{SYNC\_A}}$ and $\overline{\text{SYNC\_B}}$ are input synchronization signals. $\overline{\text{SYNC\_OUT}}$ is only needed to synchronize multiple GC1115s, or if exact notification of a GC1115-internal event is needed (such as when a snapshot RAM capture ends, or when the software timer count reaches zero). Wire $\overline{\text{SYNC\_A}}$, $\overline{\text{SYNC\_B}}$, and $\overline{\text{SYNC_OUT}}$_ to test points so they can be observed on a scope or logic analyzer.
4. During chip start-up, TRST must be pulled low and then high, or the GC1115 does not reset. A general-purpose pin on the microprocessor or DSP that controls the GC1115 can do this operation. All other JTAG signals are no-connects.
5. Place power-supply bypass capacitors on the back side of the board, if possible.

Suggested Test Points:

- IN_CLK, OUT_CLK
- A few IN_A, IN_B, OUT_A, and OUT_B pins
- $\overline{\text{SYNC\_A}}$, $\overline{\text{SYNC\_B}}$, $\overline{\text{SYNC\_OUT}}$
- $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, plus a few A[ ] and D[ ] pins

Power Connections

The PLL supplies should connect to dedicated pads with filtering as shown in Figure 19.



A. The 50R ferrite beads should be similar to: Murata P/N: BLM31P500SPT.

Figure 19. Power-Supply Filter

The PLL analog supply wires

- Should be 30 m or wider and located in metal level 2, 3, or 4
- Should be routed directly to the PLL analog supply pads
- Should avoid crossing or running parallel to any other supply or signal wires

Recommended GC1115 Board Bring-Up Procedures

When customers bring up a GC1115-based printed circuit board for the first time, TI recommends the following sequence of checks:

1. Check the GC1115 power pins for proper voltage levels (VDD, VDDSHV, VDDA1, VDDA2, and VDD1).
2. Check IN_CLK pin to verify the expected GC1115 input sampling rate and clock quality.
3. Pull TRST low and then high to release the JTAG tap controller of the GC1115.
4. Perform a write/read test of all GC1115 control registers.
5. Enable the GC1115 internal pattern generator to perform an internal checksum (CRC) test on the GC1115.
6. Enable the GC1115 to bypass all PDC stages, enable the internal pattern generator to generate a sawtooth waveform, and verify that the sawtooth waveform is observed on the GC1115 OUT_A and OUT_B pins.
7. While driving the GC1115 IN_A and IN_B pins with a test input signal and while bypassing all PDC stages, verify that the data on OUT_A and OUT_B pins matches the input data (adjusted for the internal GC1115 delay).
8. If the GC1115 is connected to a DAC, drive the IN_A and IN_B pins with a high-quality sine wave and verify that the expected SNR is achieved at the DAC output.
9. Finally, after determining the proper threshold and cancellation pulse coefficients, enable the PDC stages and drive the GC1115 with a test signal whose CCDF, ACLR, EVM, and PCDE values can be measured by suitable test equipment.

About the GC1115 JTAG Interface

- The GC1115 JTAG implementation supports both standard boundary scan (used for board test) and chip identification commands. A BSDL file for the GC1115 is available on the TI web site, http://focus.ti.com/docs/prod/folders/print/gc1115.html#productmodels.
- The GC1115 identification string is a 32-bit string:

Hex:	0x8	0x8	0xC	0x1	0x1	0x1	0x5	0x1
Binary:	1000	1000	1100	0001	0001	0001	0101	0001
	sync	mfr		device ID				chip revision

- At GC1115 power-up, the state of the JTAG controller is indeterminate until after TRST is asserted.
- For GC1115 designs that do not use JTAG, TRST must be pulled low and then high during initial GC1115 RESET, disabling JTAG. All other JTAG pins can be left unconnected (open).

APPENDIX – GLOSSARY OF TERMS

3G — Third generation (refers to next-generation wideband cellular systems that use CDMA)

3GPP2 — Third-generation partnership project 2 (cdma2000 specification, www.3gpp2.org)

ACLR — Adjacent-channel leakage ratio (measure of out-of-band energy from one CDMA carrier)

ACPR — Adjacent-channel power ratio

ADC — Analog-to-digital converter

AWGN — Additive white Gaussian noise

BER — Bit error rate

BW — Bandwidth

CCDF — Complementary cumulative distribution function

CDF — Cumulative distribution function

CDMA — Code division multiple access (spread spectrum)

cdma2000 — Qualcomm's next-generation CDMA standard (see www.3gpp2.org)

CDP — Code domain power

CFR — Crest factor reduction

CMOS — Complementary metal oxide semiconductor

DAC — Digital-to-analog converter

dB — decibels

dBm — decibels relative to 1 mW (30 dBm = 1 W)

DSP — Digital signal processing or digital signal processor

DSSS — Direct sequence spread spectrum

DUC — Digital up-converter (usually provides the GC1115 input)

EVM — Error vector magnitude

FIR — Finite impulse response (type of digital filter)

I and Q — In-phase and quadrature (signal representation)

IF — Intermediate frequency

IIR — Infinite impulse response (type of digital filter)

JTAG — Joint Test Action Group (chip debug and test standard 1149.1)

LO — Local oscillator

LSB — Least significant bit

MSB — Most significant bit

Msps — Megasamples per second (1×10E6 samples/s)

NPR — Noise power ratio

PA — Power amplifier

PAR — Peak-to-average ratio

PCDE — Peak code domain error

PDC — Peak detection and cancellation (stage)

PDF — Probability density function

RF — Radio frequency

RMS — Root mean square (method to quantify error)

SEM — Spectrum emission mask

SNR — Signal-to-noise ratio (usually measured in dB or dBm)

UMTS — Universal mobile telephone service

VSA — Vector signal analyzer

W-CDMA — Wideband code division multiple access (synonymous with 3GPP)

Errata Page for rev0 Silicon

1. 3-wire up mode does not work as described – use 2-wire mode.
2. Detection thresholds for stages 3 and 4 are wired together under normal operating circumstances.

Revision History

Changes from Revision C (June 2006) to Revision D **Page**

- Deleted section describing test model results 9
- Deleted 16-, 14-, and 12-bit output formats from IO control register 10
- Changed (N – 1) to (N + 1) in cancellation corfficients table 11
- Added *GC1115 Cancellation Filter Design* section 20
- Changed From: On request, TI will provide a MATLAB To: See the SLWS090 for a MATLAB 22
- Added *GC1115 Output Interpolator* section 29
- Deleted output rounding options 41

Changes from Revision B (October 2005) to Revision C **Page**

- Added an equation to calculate the latency of the device 65
- Corrected OUT_A and OUT_B pin labeling 70
- Corrected OUT_A and OUT_B pin labeling 71

Changes from Revision A (July 2005) to Revision B **Page**

- Changed valid decimation values to 1 and 2 12
- Clarified two-pin and three-pin operation 16
- New section on power consumption 65
- Added maximum power consumptin specification 66
- Updated tperiod, tout_hd, tout_dly 67
- Updated tout_hd and tout_dly in diagram 69
- $\overline{WR}$ is used in two-pin mode to distinguish between read and write. 71
- Changed G7–G11 to G6–G11 and L7–L11 to L6–L11 72
- $\overline{RD}$ is grounded in two-pin mode. 72
- Removed extraneous text from Figure 19 73
- Added section on JTAG usage 74

Changes from Original (February 2005) to Revision A **Page**

- Changed PLL1 to PLL_CORE and PLL2 to PLL_TX 2
- Corrected PLL_MULT column entries 13
- Table was double-labeled ("Table 15. Table 17."). Also added a column for hex values as well as decimal values. 31
- Cancel coefficients are 12 bits wide, not 16 bits wide. 44
- Changed hex address 0x12 to 0x14 (20 decimal). 45
- Updated various table values (Dissipation, Capacitance, etc.) 66
- Updated various switching and timing parameters. 66
- Removed figure captioned "Read Cycle – Normal Mode" 69
- Added a *Recommended GC1115 Board Bring-Up Procedures* section 74

PACKAGING INFORMATION

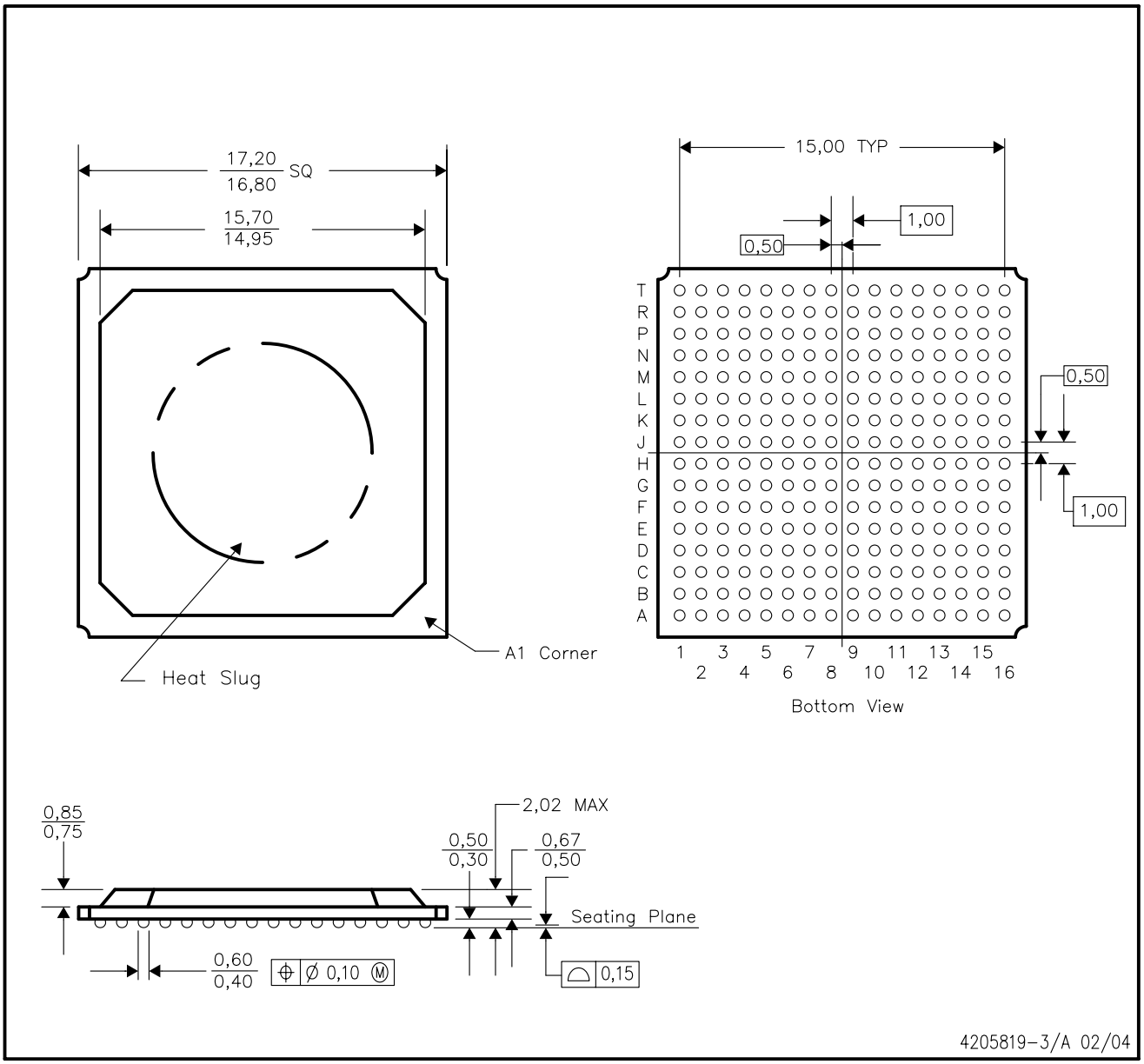
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
GC1115IZDJ	ACTIVE	BGA	ZDJ	256	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZDJ (S–PBGA–N256) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced plastic package with heat slug (HSL).
D. This package is lead–free.

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