Errata Sheet for Arria II GX Devices

This errata sheet provides updated information about known device issues affecting Arria® II GX devices.

Table 1 lists the specific issues and which Arria II GX devices are affected.

Table 1. Issues for Arria II GX Devices (Part 1 of 2)

Issue	Affected Devices	Planned Fix
"EDCRC False Error" The error detection CRC (SEU detection) feature may falsely assert the CRC_ERROR signal when no SEU event has occurred.	All production devices	—
"PLL phasedone Signal Stuck at Low" In some cases, the Arria II GX phase-locked loop (PLL) blocks exhibit the phasedone signal stuck at low during the PLL dynamic phase shift.	All production devices	Quartus II software version 12.0 and later.
"Transmitter PLL Lock (pll_locked) Status Signal" The transmitter PLL lock status signal (pll_locked) does not de-assert when the pll_powerdown signal is asserted in configurations that use the reference clock pre-divider of 2, 4, or 8.	All production devices	No plan to fix silicon. For a soft-fix solution, refer to "Transmitter PLL Lock (pll_locked) Status Signal".
"Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode" The transceiver may not be initialized correctly if your application uses dynamic reconfiguration to change the transceiver channel between PCI Express® (PCIe®) mode and any other transceiver mode.	All Arria II GX (ES and Production) Devices	No plan to fix silicon. Apply the reset workaround in "Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode".
"Quartus II Software Incorrect Setting for the Transceiver CDR in All Modes Except PCIe Mode" The Quartus® II software incorrectly sets the CDR unit when the transceiver channel is configured in any mode except PCIe mode and you configure the CDR to automatic lock mode.	All Arria II GX (ES and Production) Devices	Quartus II software version 10.1 and later. Patches are available for the Quartus II software versions 9.1SP2 and 10.0SP1.
External Memory Interface DLL Frequency Range Update New f_{MIN} for the DLL frequency range and a new frequency mode 6.	All Arria II GX (ES and Production) devices	Software fix
Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block The Quartus II software incorrectly maps the PCIe interfaces when using the hard IP block.	All Arria II GX (ES and production) devices	Software fix

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Table 1. Issues for Arria II GX Devices (Part 2 of 2)

Issue	Affected Devices	Planned Fix
XAUI State Machine Failure—Channel 0 Shifted by One Cycle Channel 0 data is shifted by one cycle with respect to Channels 1, 2, and 3.	EP2AGX125 ES	Production devices
High I/O Pin Leakage Current All I/O pins have higher leakage than the published *Device Datasheet for Arria II Devices* chapter, version 1.2 specifications.	EP2AGX125 ES	Production devices
Error Detection CRC Feature When enabled, the Error Detection CRC feature may cause the MLAB RAM blocks to operate incorrectly.	EP2AGX125 ES	EP2AGX125 production devices
M9K RAM Block Lock-Up The M9K RAM blocks may lock up due to a glitchy non-PLL clock.	EP2AGX125 ES	EP2AGX125 production devices
Automatic Clock Switchover The automatic clock switchover feature may not operate correctly.	EP2AGX125 ES	None
Remote System Upgrade The remote system upgrade feature fails when loading an invalid configuration image.	All Arria II GX (ES and Production) Devices	Software fix

EDCRC False Error

The error detection cyclic redundancy check (CRC) (single event upset [SEU] detection) feature may falsely assert the `CRC_ERROR` signal when no SEU event has occurred. This happens because the configuration RAM is incorrectly read for the EDCRC checks. In this scenario, the configuration RAM data and the functionality of the device are not affected.

- If EDCRC is not critical to your system, turn it off.
- If EDCRC is required, insert a soft IP in your design.

For more support and to request the soft IP, file a service request using mySupport.

PLL phasedone Signal Stuck at Low

In some cases, the Arria II GX PLL blocks exhibit the `phasedone` signal stuck at low during the PLL dynamic phase shift. When the PLL `phasedone` signal is stuck at low, the intended phase shift does not happen. You can recover from the PLL `phasedone` signal being stuck at low by resetting the PLL or by restarting the phase shift operation by asserting the `phasestep` signal.

Solution

To resolve the PLL `phasedone` signal stuck at low issue, the Altera® PLL megafunction is enhanced to automatically restart the phase shift operation internally in the Altera PLL megafunction whenever the PLL `phasedone` signal is stuck at low. Restarting the phase shift operation compensates for the missing phase shift operation and also recovers the `phasedone` signal.

This Altera PLL megafunction solution will be implemented in the Quartus II software version 12.0 and later. Altera recommends upgrading to the latest Quartus II software, regenerating the PLL megafunction, and recompiling your design.

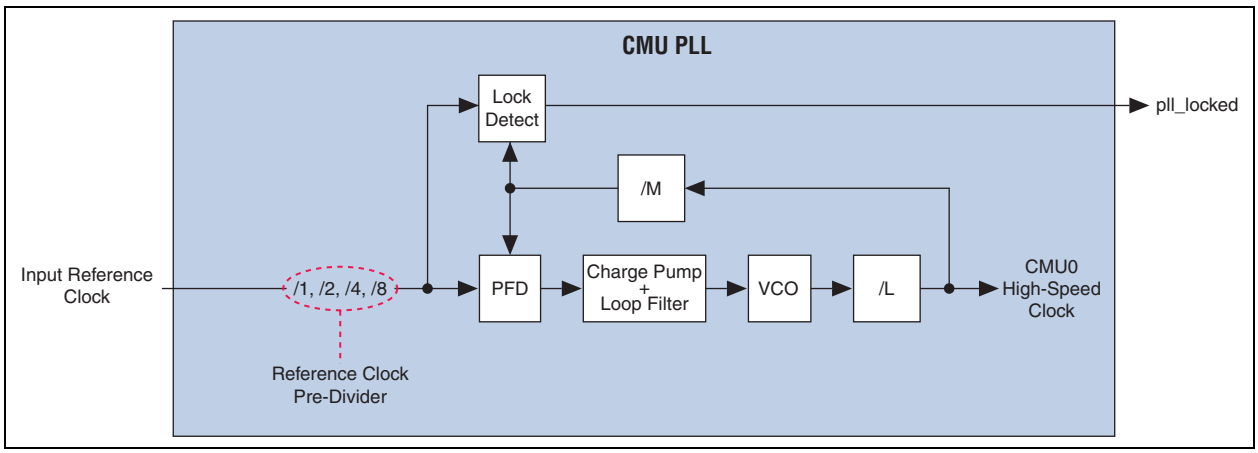
Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.1 SP1 to upgrade the PLL megafunction with the solution. To download and install the Quartus II software patch, refer to the PLL Phasedone Stuck at Low Solution.

If you need additional support, file a service request using mySupport.

Transmitter PLL Lock (pll_locked) Status Signal

The transmitter phase-locked loop (PLL) lock status signal (`pll_locked`) does not de-assert when the `pll_powerdown` signal is asserted in configurations that use the reference clock pre-divider of 2, 4, or 8. Figure 1 shows the reference clock pre-divider inside transmitter PLLs. This issue impacts the `pll_locked` status signal in the clock multiplier unit (CMU) PLL.

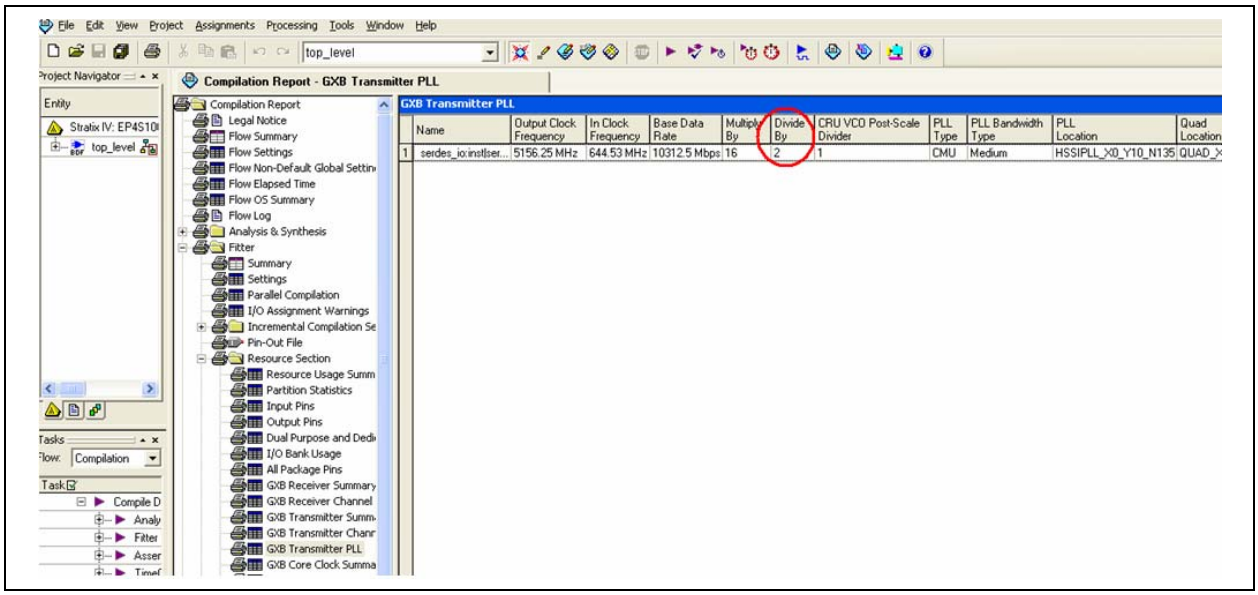
Figure 1. Reference Clock Pre-Dividers in Transmitter PLLs



Designs that implement the recommended transceiver reset sequence described in the *Reset Control and Power Down in Arria II Devices* chapter in volume 2 of the *Arria II Device Handbook* could potentially see a link failure after coming out of reset.

You can determine if the Transmitter PLL in your design uses a reference clock pre-divider of 2, 4, or 8 by referring to the Quartus II software Compilation Report. Figure 2 shows an example of the "GXB Transmitter PLL" report, which you find in the "Resources Section" under "Fitter" in the Compilation Report. If the value in the "Divide By" column reads 2, 4, or 8, your design is impacted by the `pll_locked` status signal issue.

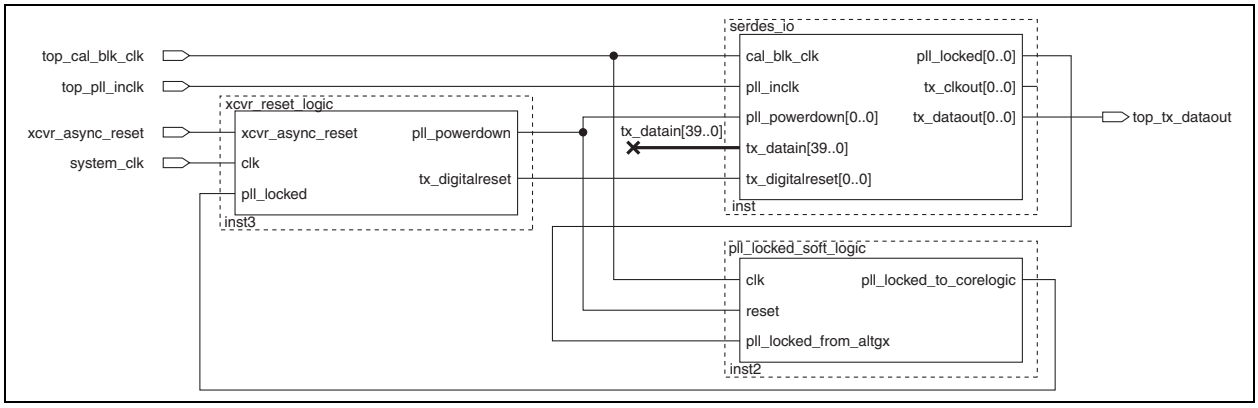
Figure 2. Determining Reference Clock Pre-Divider Value in the Compilation Report



Workaround

If the `pll_locked` issue impacts your design, instantiate and connect the `pll_locked_soft_logic` module, as shown in Figure 3. You must use the `pll_locked_to_corelogic` output from this module in the transceiver reset logic and any user logic that relies on the transmitter PLL lock status signal.

Figure 3. Instantiating and Connecting the pll_locked_soft_logic Module



Click `pll_locked_soft_logic` to obtain the module.

Use the calibration block clock (`cal_blk_clk`) for the `pll_locked_soft_logic` module. The `cal_blk_clk` frequency specification ranges from 10 MHz to 125 MHz. Depending on your `cal_blk_clk` frequency, set the parameter `p_delay_counter` in the `pll_locked_soft_logic` so that the delay is equal to 100 µs (worst-case transmitter PLL lock time).

Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode

If your application uses dynamic reconfiguration to change the transceiver channel between PCIe mode and any other transceiver mode, the transceiver may not be initialized correctly, resulting in receiver bit errors.

This problem only affects dynamic reconfiguration between PCIe mode and any other transceiver mode. Dynamic reconfiguration between any transceiver modes other than PCIe mode is not affected.

Workaround

- If you see bit errors, apply the reset sequence described in the Reset Sequence Solution.
- If you need additional support, file a service request at Altera's mysupport.

Quartus II Software Incorrect Setting for the Transceiver CDR in All Modes Except PCIe Mode

The Quartus II software versions up to and including 10.0 SP1 incorrectly set the clock and data recovery (CDR) unit when the transceiver channel is configured in any mode except PCIe mode and the CDR is configured in automatic lock mode.

When there are no data transitions on the transceiver data inputs for an extended period of time (in the ms range), the CDR may keep the `rx_freqlocked` signal asserted. The CDR does not return to the lock-to-reference state and incorrect data may be recovered.

The transceiver channels configured in PCIe mode are NOT affected by this issue.

Solution

This issue is fixed in the Quartus II software versions 10.1 and later. Altera recommends upgrading to the latest Quartus II software and recompiling your design. For complete details of the solution, refer to the Transceiver CDR Solution.

Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.0 SP1.

- To download and install the patch, refer to the Transceiver CDR Solution.

If your transceiver channels are configured to use `rx_signaldetect` with the CDR in automatic lock mode, you must apply the reset sequence described in the Transceiver CDR Solution.

If you need additional support, file a service request at Altera's mysupport.

External Memory Interface DLL Frequency Range Update

The Arria II GX delay-locked loop (DLL) range has been updated in the Quartus II software version 10.0 SP1 and later. Table 2 lists the updated DLL frequency ranges.

Table 2. Arria II GX DLL Frequency Range

Frequency Mode	Frequency Range (MHz)		
	C4	I3, C5, I5	C6
0	90–140	90–130	90–110
1	110–180	110–170	110–150
2	140–220	140–210	140–180
3	170–270	170–260	170–220
4	220–340	220–310	220–270
5	270–410	270–380	270–320
6	320–450	320–410	320–370

Table 3 lists the conditions and designs that are affected by these changes. Designs that fall into these categories must be recompiled in the Quartus II software version 10.0 SP1 and later. For example, a DDR2 SDRAM ALTMEMPHY design with a memory clock running within the 150 MHz to 170 MHz frequency range requires recompilation. All designs using the ALTDLL megafunction require recompilation regardless of the frequency and memory standard.

Table 3. Recompilation Condition *(1)*

Megafunction/ IP Core	Memory Standard	Memory Clock Frequency Range				
		100 MHz to 120 MHz	150 MHz to 170 MHz	180 MHz to 201 MHz	220 MHz to 250 MHz	270 MHz to 300 MHz
ALTMEMPHY	DDR2 SDRAM	No	Yes	Yes	Yes	Yes
	DDR SDRAM	Yes	Yes	Yes	No	No
UniPHY	QDRII/II+ SRAM	Yes	Yes	Yes	Yes	No
ALTDLL	All Conditions					

Note to Table 3:

(1) : "Yes" - Recompilation is needed

If any invalid DLL configuration critical warning appears after recompilation in the Quartus II software version 10.0 SP1 and later, as shown in Example 1, you must regenerate the megafunction or the IP core and recompile the design.

Example 1. Invalid DLL Configuration Critical Warning

```
Critical Warning: DLL atom
"ddr2_230:ddr2_230_inst|ddr2_230_controller_phy:ddr2_230_controller_phy_inst|
ddr2_230_phy:ddr2_230_phy_inst|ddr2_230_phy_alt_mem_phy:ddr2_230_phy_alt
_mem_phy_inst|ddr2_230_phy_alt_mem_phy_clk_reset:clk|dll" is using a clock
period of 4.35 ns, which is outside the valid range for its configuration mode. When
the delay buffer mode is "LOW" and the delay chain length is "8", the valid range is
from 4.55 ns to 5.88 ns.
```

Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block

The Quartus II software versions 9.1, 9.1 SP1, and 9.1 SP2 incorrectly allow logical channel 0 to be placed in any physical channel for x1 and x4 PCIe Gen1 interfaces with the hard IP block. For correct operation with the hard IP block, logical channel 0 must be placed in physical channel 0.

This issue is fixed in the Quartus II software version 10.0; however, Altera recommends upgrading to the Quartus II software version 10.0 SP1. If you have already designed or fabricated your boards using the incorrect mapping, file a service request using mysupport.altera.com to remedy this problem.

High I/O Pin Leakage Current

I/O pins on Arria II ES devices have a higher leakage current than what is specified in the Arria II GX Data Sheet version 1.2. For Arria II GX ES device I/O pin leakage current for all I/O pins, refer to Table 4.

Table 4. I/O Pin Leakage Current for Arria II GX ES Devices

Symbol	Description	Conditions	Min	Type	Max	Unit
I_I	Input pin	V_I = 0V to $V_{CCIOMAX}$	-80	—	80	µA
I_{OZ}	Tri-stated I/O Pin	V_O = 0V to $V_{CCIOMAX}$	-80	—	80	µA

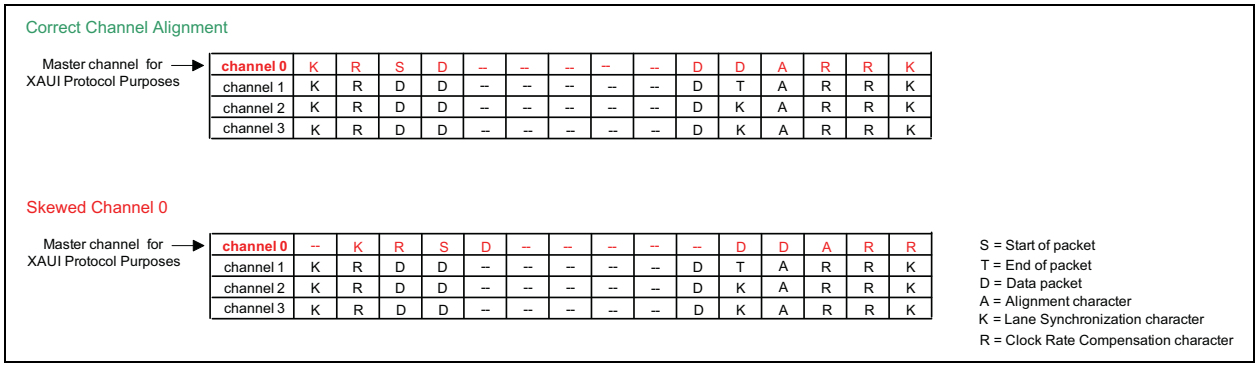
All Arria II GX production devices will have a lower leakage current. For production device specifications, refer to the *Device Datasheet for Arria II GX Devices* chapter in volume 3 of the *Arria II GX Device Handbook*.

XAUI State Machine Failure—Channel 0 Shifted by One Cycle

In XAUI functional mode, the data out of the channel 0 Rate Match FIFO may be shifted by one byte with respect to the data of the other three channels. This causes incorrect idle ordered set conversion, resulting in incorrect received parallel data. This issue happens only during initialization or receiver channel reset (assertion of `rx_analogreset` or `rx_digitalreset`).

Figure 4 shows the channel skew.

Figure 4. Rate Matcher FIFO Skew



Workaround

Altera provides a soft IP solution and associated documentation, available for download at: www.altera.com/patches/xaui-softip/xaui-softip-fix-reva.zip. This soft IP should be integrated into the XAUI receiver data path. This issue is fixed in production devices.

Error Detection CRC Feature

The Error Detection CRC feature is typically used to detect single event upsets (SEUs). When enabled, the Error Detection CRC feature may cause the memory logic array block (MLAB) RAM to operate incorrectly in Arria II GX ES devices. Only write operations in the MLAB RAM blocks are affected.

The Error Detection CRC feature and CRC error flag operate correctly. FPGA configuration bits are not affected by this issue.

If you do not use Error Detection CRC, no action is required. The MLAB RAM blocks will operate correctly.

If you enable Error Detection CRC, disabling the Error Detection CRC resolves the problem.

Also, using M9K RAM blocks or Logic Cells (LCs) instead of MLAB RAM blocks resolves the problem.

This issue will be fixed in production devices.

M9K RAM Block Lock-Up

The M9K RAM blocks can lock up if the read clock glitches when `rden=1`, which can occur if the clock source is not from a PLL. In this state, a RAM block no longer responds to read or write operations and requires an FPGA reconfiguration to restore operation. The issue occurs in the Read Timer Trigger circuitry, where a glitchy non-PLL clock may inadvertently freeze the Read Timer Trigger circuitry, locking the RAM block in its last operation. All RAM block modes are affected. MLABs are not affected.

Workarounds

The workarounds for this issue are to add clock-enable logic, an internal PLL, or clock generation logic (for example, a clock divider). You can add clock-enable logic (internal or external) to disable the RAM block operation until the clock is stable. You can also gate the clock internally or externally. If your FPGA resources permit, use an internal PLL or clock generation logic to ensure a stable clock source at the RAM block input.

This issue will be fixed in production devices.

Automatic Clock Switchover

The automatic clock switchover feature may fail to operate correctly on Arria II GX devices when the two clocks are running at different frequencies. If both clocks are running at the same frequency, there is no impact to your design. The following modes are affected:

- Automatic
- Automatic with manual override

You may observe two possible issues:

- Switchover from `inclk0` to `inclk1`, even though `inclk0` is active (and vice-versa)
- `clkbad[0,1]` status signals may glitch, even if the input clocks are active

Manual clock switchover mode operates correctly and is not affected by this issue.

There is no planned fix for this issue.

Remote System Upgrade

The remote system upgrade feature does not operate correctly when you initiate a reconfiguration cycle that goes from a factory configuration image to an invalid application configuration image. In this scenario, the Arria II GX device fails to revert back to the factory configuration image after a configuration error is detected while loading the invalid application configuration image. The failure is indicated by a continuous toggling of the `nSTATUS` pin.

In correct operation, the Arria II GX device reverts back to the factory configuration image after a configuration error is detected with the invalid configuration image.

An invalid application configuration image is classified as one of the following:

- A partially programmed application image
- A blank application image
- An application image assigned with a wrong start address

The remote system upgrade feature works correctly with all other reconfiguration trigger conditions.

This issue is addressed by enabling the Reconfig POF Checking feature in the updated ALTREMOTE_UPDATE megafunction and is available in the Quartus II software version 9.1 and later.

For more information about how to enable the Reconfig POF Checking feature, refer to *AN 603: Active Serial Remote System Upgrade Reference Design*.

Document Revision History

Table 5 lists the revision history for this errata sheet.

Table 5. Document Revision History

Date	Version	Changes
April 2013	3.7	■ Updated the "XAUI State Machine Failure—Channel 0 Shifted by One Cycle" section, per FogBugz #25367. ■ Minor text edits.
April 2013	3.6	Added the "EDCRC False Error" section.
June 2012	3.5	Added the "PLL phasedone Signal Stuck at Low" section.
September 2011	3.4	■ Updated the "Remote System Upgrade" section. ■ Minor text edits.
February 2011	3.3	Added the "Transmitter PLL Lock (pll_locked) Status Signal" section.
November 2010	3.2	■ Added the "Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode" and "Quartus II Software Incorrect Setting for the Transceiver CDR in All Modes Except PCIe Mode" sections. ■ Minor text edits.
October 2010	3.1	Added the "External Memory Interface DLL Frequency Range Update" section.
September 2010	3.0	■ Added the "Quartus II Mapping Issue with PCI Express (PCIe) Interfaces Using the Hard IP Block" section. ■ Applied the new document template.
August 2009	2.0	Added "High I/O Pin Leakage Current" and "XAUI State Machine Failure—Channel 0 Shifted by One Cycle" sections.
June 2009	1.0	Initial release.

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