Panasonic

AN32180A

http://www.semicon.panasonic.co.jp/en/

4 x 4 Dots Matrix LED Driver LSI

FEATURES

- 4 × 4 LED Matrix Driver (Total LED that can be driven = 16)
- LED Selectable Maximum Current
- LED Music Synchronizing Function
- I^2C interface (Standard Mode, Fast Mode and Fast Mode Plus) (4 Slave address selectable)
- 16 pin Plastic Quad Flat Non-leaded Package (QFN Type)

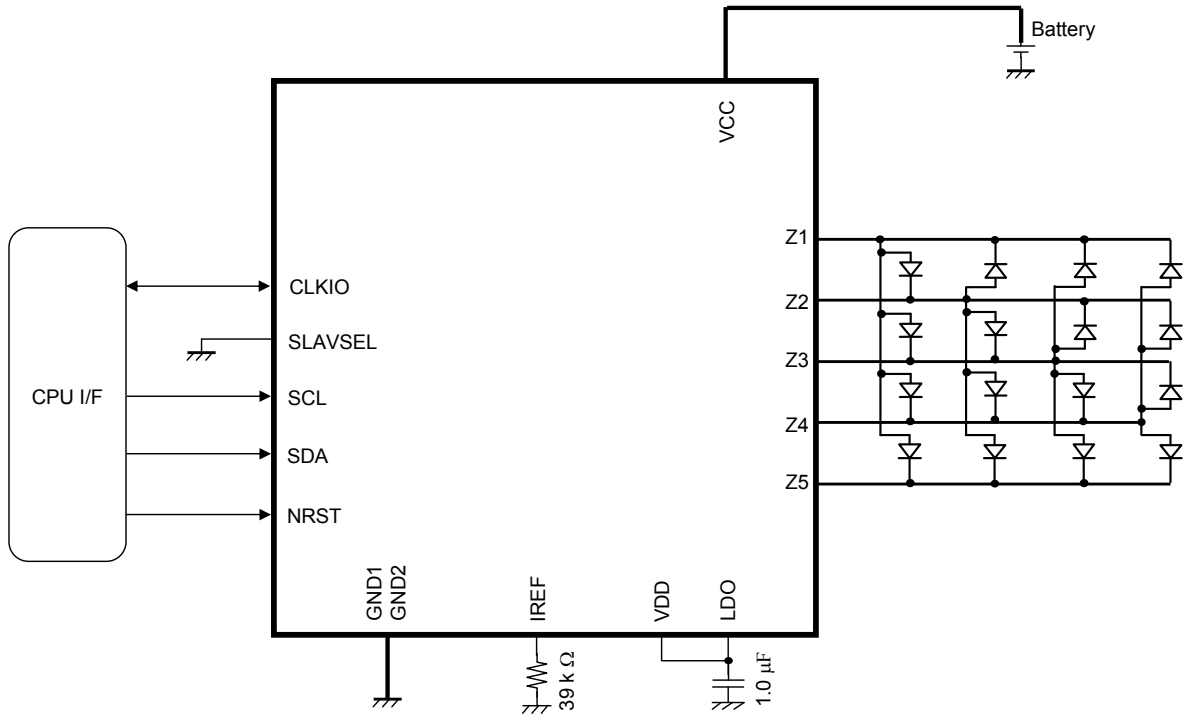
DESCRIPTION

AN32180A is a 16 Dots Matrix LED Driver.
It can drive up to 4 channels of RGB LEDs.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note)
This application circuit is an example. The operation of the mass production set is not guaranteed. Customers shall perform enough evaluation and verification on the design of mass production set. Customers shall be fully responsible for the incorporation of the above application circuit and information in the design of the equipment.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VCC_{MAX}	6.0	V	*1
	VDD_{MAX}	6.0	V	*1
Operating ambience temperature	T_{opr}	– 30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	SLAVSEL, SCL, SDA, CLKIO, NRST	– 0.3 to 6.0	V	—
Output Voltage Range	IREF, LDO, CLKIO, Z1, Z2, Z3, Z4, Z5	– 0.3 to 6.0	V	—
ESD	HBM	2.0	kV	—

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: VCC_{MAX} = VCC, VDD_{MAX} = VDD.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for operating ambient temperature, operating junction temperature and storage temperature, all ratings are for Ta = 25°C.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
16 pin Plastic Quad Flat Non-leaded package (QFN Type)	189.2 °C /W	0.529 W	0.212 W

Note) For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VCC	3.1	5.0	5.5	V	—
	VDD	1.7	5.0	5.5	V	—
Input Voltage Range	SLAVSEL, SCL, SDA, CLKIO	– 0.3	—	VDD + 0.3	V	*1
	NRST	– 0.3	—	VCC + 0.3	V	*1
Output Voltage Range	IREF, LDO, CLKIO, Z1, Z2, Z3, Z4, Z5	– 0.3	—	VCC + 0.3	V	*1

Note) Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for GND.
VCC is voltage for VCC. VDD is voltage for VDD.
Do not apply external currents or voltages to any pin not specifically mentioned.
*1 : (VCC + 0.3) V must not exceed 6 V. (VDD + 0.3) V must not exceed 6 V.

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ELECTRICAL CHARACTERISTICS

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Circuit Current							
Circuit Current (1) OFF Mode	ICC1	NRST = 0 V	—	0	1	µA	—
Circuit Current (2) OFF Mode	ICC2	NRST = High	—	250	500	µA	—
Internal Oscillator							
Oscillation Frequency	FDC1	VCC = 3.6 V	1.92	2.40	2.88	MHz	—
SCAN Switch							
Switch On Resistance	RSCAN	VCC = 3.6 V $I_{Z1\sim Z4}$ = – 20 mA	—	1.5	3	Ω	—
Constant Voltage Source (LDO)							
Output voltage (1)	VL1	I_{LDO} = – 10 µA	2.75	2.85	2.95	V	—
Output voltage (2)	VL2	I_{LDO} = – 15 mA	2.75	2.85	2.95	V	—
CLKIO							
High Level Input Voltage Range	VIH1	High Level Acknowledged Voltage (At External CLK Input Mode)	0.7 × VDD	—	VDD + 0.3	V	—
Low Level Input Voltage Range	VIL1	Low Level Acknowledged Voltage (At External CLK Input Mode)	– 0.3	—	0.3 × VDD	V	—
High Level Output Voltage	VOH1	I_{CLKIO} = – 1 mA (At Internal CLK Output Mode)	0.8 × VDD	—	VDD + 0.3	V	—
Low Level Output Voltage	VOL1	I_{CLKIO} = 1 mA (At Internal CLK Output Mode)	– 0.3	—	0.2 × VDD	V	—
High Level input Current	IIH1	VCC = 5.5 V V_{CLKIO} = 5.5 V	– 1	0	1	µA	—
Low Level input Current	IIL1	VCC = 5.5 V V_{CLKIO} = 0 V	– 1	0	1	µA	—

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ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Constant Current Source (Matrix LED)							
Output Current (1)	IMX1	LED Current Setting = 20.2 mA IMAX = [011], BRTXX = [1010] $V_{Z1\sim Z5}$ = 1 V	19.2	20.2	21.2	mA	*1
DAC Current Step	DACSTEP	DAC Constant Current Mode LED Current Setting = 20.2 mA IMAX = [011], BRTXX = [1010] $V_{Z1\sim Z5}$ = 1 V, IDAC1 = $I_{Z1\sim Z5}$ LED Current Setting = 22 mA IMAX = [011], BRTXX = [1011] $V_{Z1\sim Z5}$ = 1 V, IDAC2 = $I_{Z1\sim Z5}$ DACSTEP = IDAC2 – IDAC1	0	2	4	mA	—
OFF Mode Leak Current1	IMXOFF1	VCC = 5.5 V, VDD = 5.5 V OFF Mode $V_{Z1\sim Z5}$ = 5.5 V	– 1	—	1	µA	—
OFF Mode Leak Current2	IMXOFF2	VCC = 5.5 V, VDD = 5.5 V OFF Mode $V_{Z1\sim Z5}$ = 0 V	– 1	—	1	µA	—
Channel Difference	IMXCH	LED Current Setting = 20.2 mA IMAX = [011], BRTXX = [1010] Difference of Z1 to 5 current from the average current value	– 5	—	5	%	—
Voltage at which LED driver can keep constant current value							
LED Driver Voltage	VLD2	LED Current Setting = 20.2 mA IMAX = [011], BRTXX = [1010] Voltage at which LED Current change within ± 5 % compared with LED Current of pin voltage = 0.5 V.	0.4	—	—	V	—

Note) * 1: This is allowable value when recommended parts (ERJ2RHD393X) are used for the terminal IREF.

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ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SLAVSEL							
High Level Input Voltage Range	VIH2	High Level Acknowledged Voltage	0.7 × VDD	—	VDD + 0.3	V	—
Low Level Input Voltage Range	VIL2	Low Level Acknowledged Voltage	– 0.3	—	0.3 × VDD	V	—
High Level Input Current	IIH2	VCC = 5.5 V $V_{SLAVSEL}$ = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	IIL2	VCC = 5.5 V $V_{SLAVSEL}$ = 0 V	– 1	0	1	µA	—
NRST							
High Level Input Voltage Range	VIH3	High Level Acknowledged Voltage	1.5	—	VCC + 0.3	V	—
Low Level Input Voltage Range	VIL3	Low Level Acknowledged Voltage	– 0.3	—	0.6	V	—
High Level Input Current	IIH3	VCC = 5.5 V V_{NRST} = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	IIL3	VCC = 5.5 V V_{NRST} = 0 V	– 1	0	1	µA	—
I²C bus (Internal I/O stage characteristics)							
Low-level input voltage	V_{IL}	Voltage which recognized that SDA and SCL are Low-level	– 0.5	—	0.3 × VDD	V	*2
High-level input voltage	V_{IH}	Voltage which recognized that SDA and SCL are High-level	0.7 × VDD	—	VDD_{MAX} + 0.5	V	*2
Low-level output voltage 1	V_{OL1}	VDD > 2 V I_{SDA} = 3 mA	0	—	0.4	V	—
Low-level output voltage 2	V_{OL2}	VDD < 2 V I_{SDA} = 3 mA	0	—	0.2 × VDD	V	—
Low-level output current	I_{OL}	V_{SDA} = 0.4 V	20	—	—	mA	—
Input current each I/O pin	I_i	VCC = 5.5 V, VDD = 5.5 V V_{SCL}, V_{SDA} = 0.1 VDD_{MAX} to 0.9 VDD_{MAX}	– 10	0	10	µA	—
SCL clock frequency	f_{SCL}	—	0	—	1000	kHz	—

Note) VDD_{max} refers to the maximum operating supply voltage of VDD.

*2 : The input threshold voltage of I²C bus (Vth) is linked to VDD (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not VDD, the threshold voltage (Vth) is fixed to ((VDD / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value (V_{ILMAX}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (VDD).

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ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TSD (Thermal shutdown protection circuit)							
Detection temperature	Tdet	Temperature which Constant current circuit, and Matrix SW turn off.	—	150	—	°C	*3 *4
Constant Voltage Source (LDO)							
Ripple rejection ratio (1)	PSL11	VCC = 3.6 V + 0.3 V [p-p] f = 1 kHz I_{LDO} = – 15 mA PSL11 = 20 log (acV_{LDO} / 0.3)	—	– 50	—	dB	*4
Ripple rejection ratio (2)	PSL12	VCC = 3.6 V + 0.3 V[p-p] f = 10 kHz I_{LDO} = – 15 mA PSL12 = 20 log (acV_{LDO} / 0.3)	—	– 40	—	dB	*4
Short-circuit protection current	IPT1	V_{LDO} = 0 V	—	40	—	mA	*4
I²C bus (Internal I/O stage characteristics) (Continued)							
Hysteresis of Schmitt trigger input 1	V_{hys1}	VDD > 2 V, Hysteresis of SDA, SCL	0.05 × VDD	—	—	V	*5 *6
Hysteresis of Schmitt trigger input 2	V_{hys2}	VDD < 2 V, Hysteresis of SDA, SCL	0.1 × VDD	—	—	V	*5 *6
Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	Bus capacitance : 10 pF to 550 pF $I_P \leq 20$ mA (V_{OLmax} = 0.4 V) I_P : Max. sink current	—	—	120	ns	*5 *6
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	—	0	—	50	ns	*5 *6
Capacitance for each I/O pin	C_i	—	—	—	10	pF	*5 *6

Note) *3 : Constant current circuit, and Matrix SW turn off and IC reset when TSD operates.
*4 : Typical Design Value
*5 : The timing of Fast-mode Plus devices in I²C-bus is specified in Page.10. All values referred to V_{IHMIN} and V_{ILMAX} level.
*6 : These are values checked by design but not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Bus line specifications) (Continue)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA.}$	0.26	—	—	µs	*5 *6
Low period of the SCL clock	t_{LOW}	—	0.5	—	—	µs	*5 *6
High period of the SCL clock	t_{HIGH}	—	0.26	—	—	µs	*5 *6
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.26	—	—	µs	*5 *6
Data hold time	$t_{HD:DAT}$	—	0	—	—	µs	*5 *6
Data set-up time	$t_{SU:DAT}$	—	50	—	—	ns	*5 *6
Rise time of both SDA and SCL signals	t_r	—	—	—	120	ns	*5 *6
Fall time of both SDA and SCL signals	t_f	—	—	—	120	ns	*5 *6
Set-up time of STOP condition	$t_{SU:STO}$	—	0.26	—	—	µs	*5 *6
Bus free time between STOP and START condition	t_{BUF}	—	0.5	—	—	µs	*5 *6
Capacitive load for each bus line	C_b	—	—	—	550	pF	*5 *6
Data valid time	$t_{VD:DAT}$	—	—	—	0.45	µs	*5 *6
Data valid acknowledge	$t_{VD:ACK}$	—	—	—	0.45	µs	*5 *6
Noise margin at the Low-level for each connected device	V_{nL}	—	0.1 × VDD	—	—	V	*5 *6
Noise margin at the High-level for each connected device	V_{nH}	—	0.2 × VDD	—	—	V	*5 *6

Note) *5 : The timing of Fast-mode Plus devices in I²C-bus is specified in Page.10. All values referred to V_{IHMIN} and V_{ILMAX} level.
*6 : These are values checked by design but not production tested.

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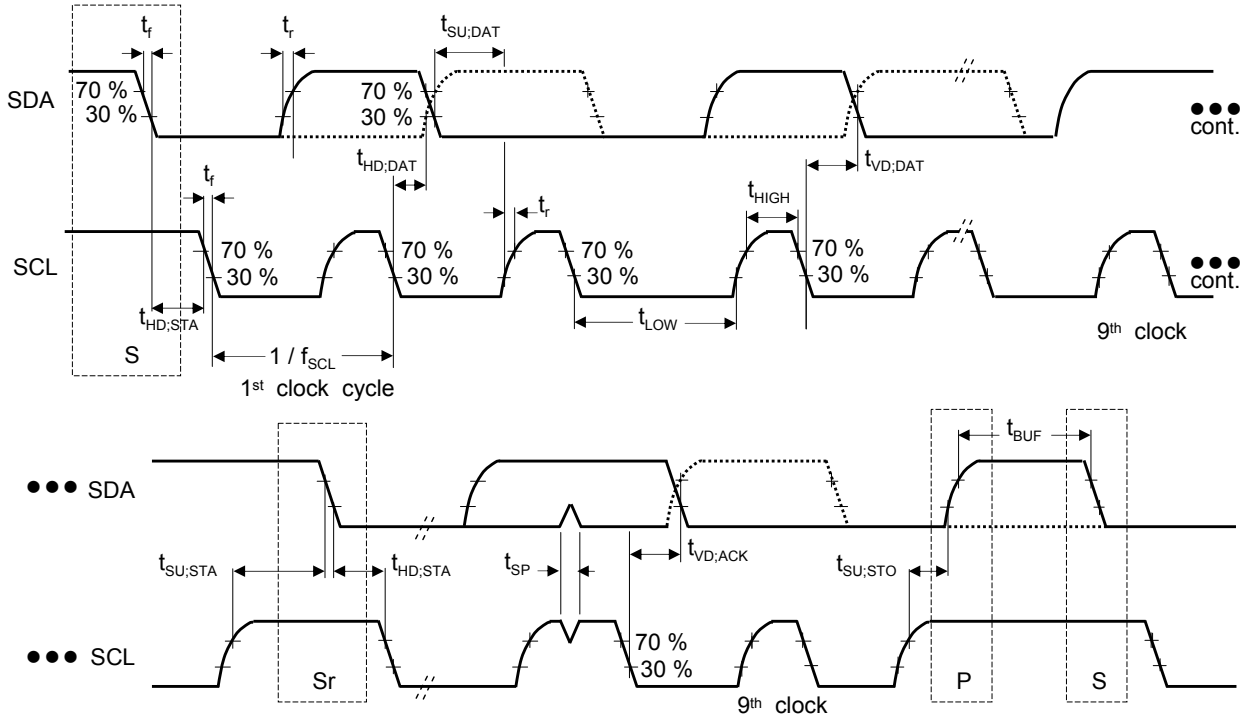
ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned



V_{ILMAX} = 0.3 V_{DD}

V_{IHMIN} = 0.7 V_{DD}

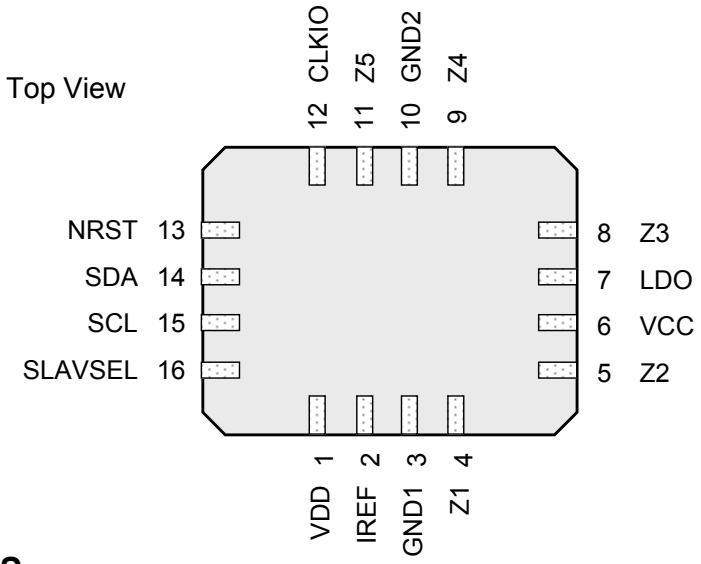
S : START condition

Sr : Repeat START condition

P : STOP condition

Establ ished : 2 0 1-0 7-2 9
Revised : 2 0 1-0 3-2 2

PIN CONFIGURATION



PIN FUNCTIONS

Pin No.	Pin name	Type	Description	Pin processing at unused
1	VDD	Power supply	Power supply pin for I²C interface	(Required pin)
2	IREF	Output	Resistor connection pin for constant current setup	(Required pin)
3 10	GND1 GND2	Ground	Ground pin	(Required pin)
4	Z1	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
5	Z2	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
6	VCC	Power supply	Power supply pin for matrix driver and Internal reference circuit	Battery or External power supply
7	LDO	Output	LDO output pin	(Required pin)
8	Z3	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
9	Z4	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
11	Z5	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
12	CLKIO	Input/Output	Reference clock input output / Music Input pin	Open
13	NRST	Input	Reset input pin	(Required pin)
14	SDA	Input/Output	Data input / output pin for I²C interface	(Required pin)
15	SCL	Input	Clock input pin for I²C interface	(Required pin)
16	SLAVSEL	Input	Slave address selection pin for I²C interface	(Required pin)

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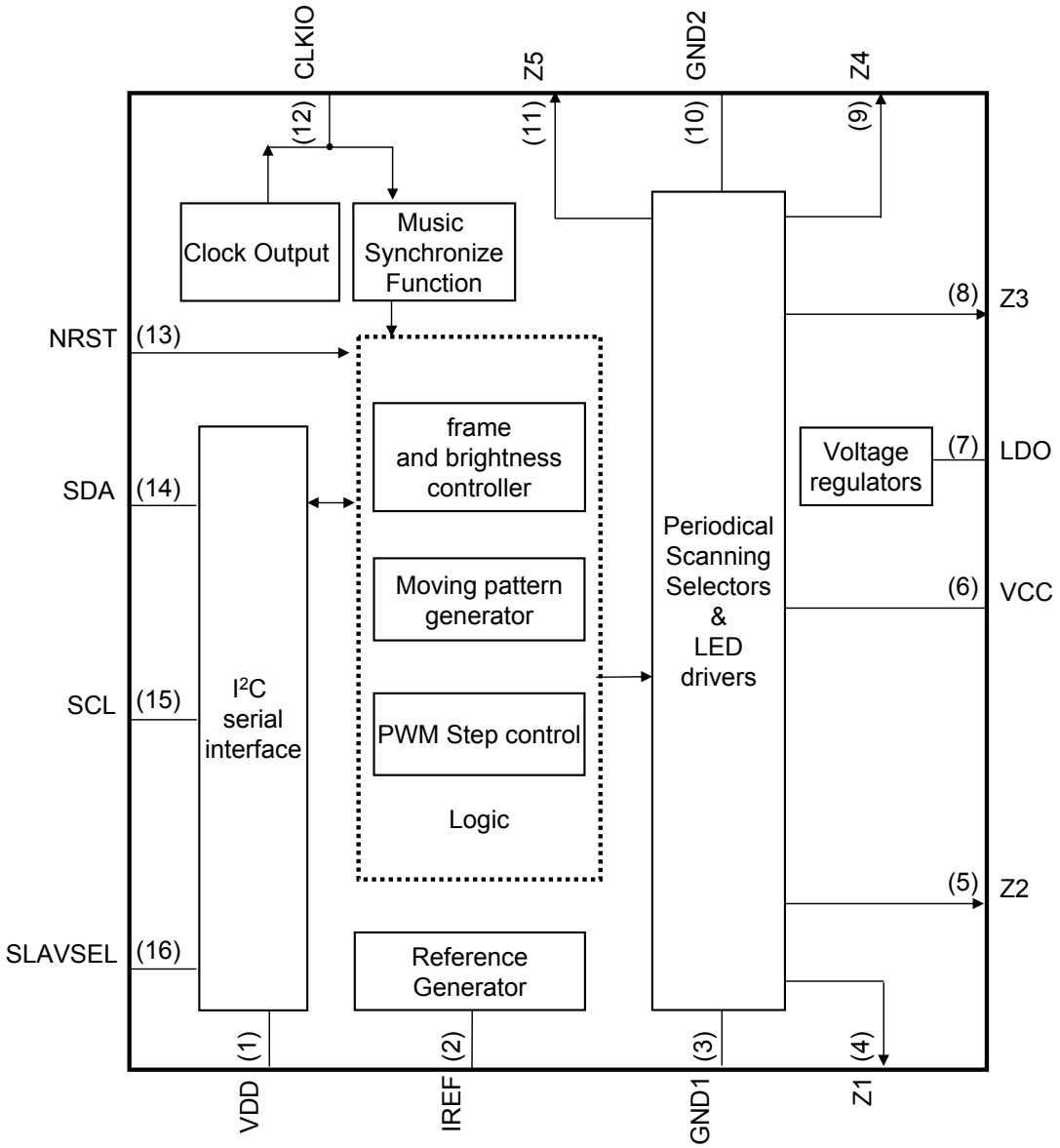
FUNCTIONAL BLOCK DIAGRAM



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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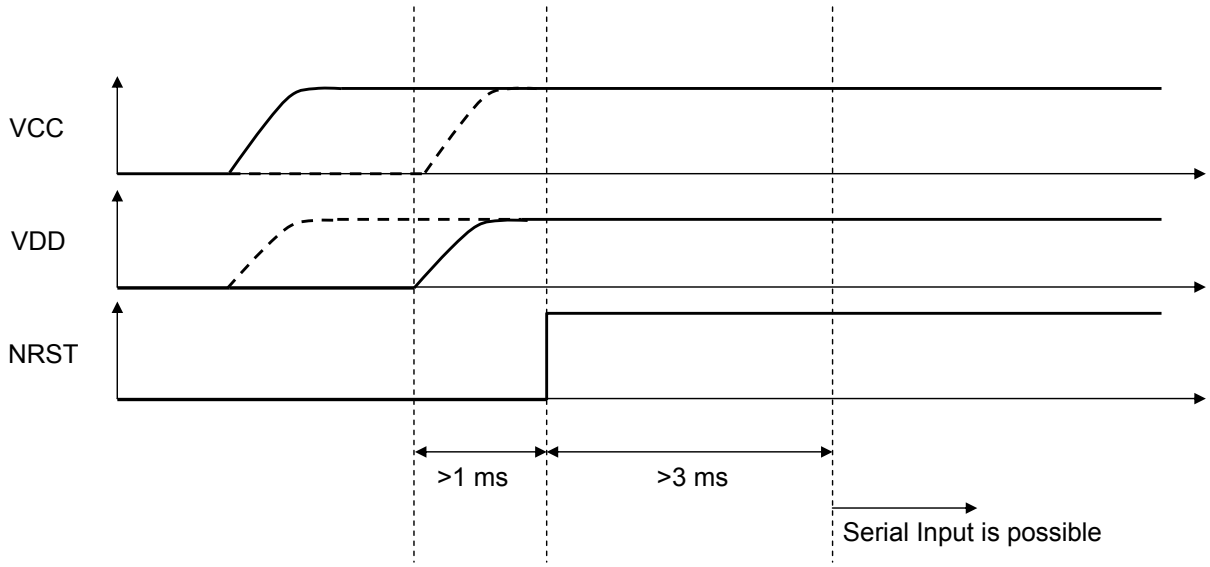
OPERATION

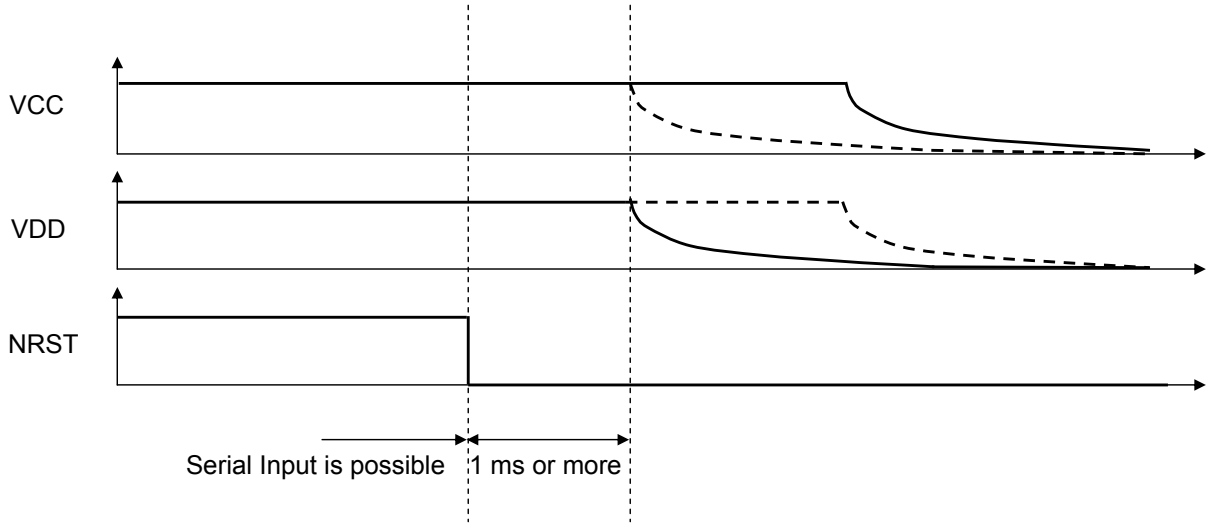
1. Power Supply Sequence

Power ON



Note) For the Startup Timing of VCC and VDD, it is possible to be changed.

Power OFF



Note) For the Shut down Timing of VCC and VDD, it is possible to be changed.

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OPERATION (continued)

2. Register Map

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
01h	RST	00h	R/W	--	--	--	--	--	--	RAMRST	SRST
02h	POWERCNT	00h	R/W		--	--	--	--	--	--	OSCEN
03h	reserved	--	--	--	--	--	--	--	--	--	--
04h	OPTION	00h	R/W	--	--	--	--	ZPDEN	MLDACT	CLKOUT	EXTCLK
05h	MTXON	1Eh	R/W	--	--	--	IMAX Reserved	IMAX[2:0]			MTXON
06h	PWMEN1	00h	R/W	PWMB4	PWMB3	PWMB2	PWMB1	PWMA4	PWMA3	PWMA2	PWMA1
07h	PWMEN2	00h	R/W	PWMD4	PWMD3	PWMD2	PWMD1	PWMC4	PWMC3	PWMC2	PWMC1
08h	MDLEN1	00h	R/W	MLDB4	MLDB3	MLDB2	MLDB1	MLDA4	MLDA3	MLDA2	MLDA1
09h	MDLEN2	00h	R/W	MLDD4	MLDD3	MLDD2	MLDD1	MLDC4	MLDC3	MLDC2	MLDC1
0Ah	MDLMODE2	00h	R/W	--	GRP_ALL	GRP8_1	GRP8_0	GRP4_3	GRP4_2	GRP4_1	GRP4_0
0Bh	MLDCOM	03h	R/W	--	--	--	--	--	MLDCOM[2:0]		
0Ch	THOLD	00h	R/W	THOLD[7:0]							
0Dh	XCONST	00h	R/W	--	--	--	X5	X4	X3	X2	X1
0Eh	YCONST	00h	R/W	Y4	Y3	Y2	Y1	Y4MSK	Y3MSK	Y2MSK	Y1MSK
0Fh	SLPTIME	00h	R/W	--	SCANSET[1:0]		FADTIM	SLOPEEXTL[1:0]		SLOPEEXTH[1:0]	

Note) "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used.
For data bits indicated by "--" in other registers except for "reversed" registers, will return "zero" value if these bits are read.
Writing to these bits will be ignored. IMAX Reserved will give default value [1].

OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
10h	DTA1	00h	R/W	DTA1[7:0]							
11h	DTA2	00h	R/W	DTA2[7:0]							
12h	DTA3	00h	R/W	DTA3[7:0]							
13h	DTA4	00h	R/W	DTA4[7:0]							
14h	DTB1	00h	R/W	DTB1[7:0]							
15h	DTB2	00h	R/W	DTB2[7:0]							
16h	DTB3	00h	R/W	DTB3[7:0]							
17h	DTB4	00h	R/W	DTB4[7:0]							
18h	DTC1	00h	R/W	DTC1[7:0]							
19h	DTC2	00h	R/W	DTC2[7:0]							
1Ah	DTC3	00h	R/W	DTC3[7:0]							
1Bh	DTC4	00h	R/W	DTC4[7:0]							
1Ch	DTD1	00h	R/W	DTD1[7:0]							
1Dh	DTD2	00h	R/W	DTD2[7:0]							
1Eh	DTD3	00h	R/W	DTD3[7:0]							
1Fh	DTD4	00h	R/W	DTD4[7:0]							
20h	A1	00h	R/W	BRTA1[3:0]				--	SDTA1[2:0]		
21h	A2	00h	R/W	BRTA2[3:0]				--	SDTA2[2:0]		
22h	A3	00h	R/W	BRTA3[3:0]				--	SDTA3[2:0]		
23h	A4	00h	R/W	BRTA4[3:0]				--	SDTA4[2:0]		
24h	B1	00h	R/W	BRTB1[3:0]				--	SDTB1[2:0]		
25h	B2	00h	R/W	BRTB2[3:0]				--	SDTB2[2:0]		
26h	B3	00h	R/W	BRTB3[3:0]				--	SDTB3[2:0]		
27h	B4	00h	R/W	BRTB4[3:0]				--	SDTB4[2:0]		
28h	C1	00h	R/W	BRTC1[3:0]				--	SDTC1[2:0]		
29h	C2	00h	R/W	BRTC2[3:0]				--	SDTC2[2:0]		
2Ah	C3	00h	R/W	BRTC3[3:0]				--	SDTC3[2:0]		
2Bh	C4	00h	R/W	BRTC4[3:0]				--	SDTC4[2:0]		
2Ch	D1	00h	R/W	BRTD1[3:0]				--	SDTD1[2:0]		
2Dh	D2	00h	R/W	BRTD2[3:0]				--	SDTD2[2:0]		
2Eh	D3	00h	R/W	BRTD3[3:0]				--	SDTD3[2:0]		
2Fh	D4	00h	R/W	BRTD3[3:0]				--	SDTD4[2:0]		

Note) Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

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OPERATION (continued)

3. Register map Detailed Explanation

Register Name		RST							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
01h	R/W	--	--	--	--	--	--	RAMRST	SRST
Default	00h	0	0	0	0	0	0	0	0

D1 : RAMRST RAM reset
[0] : RAM can be overwritten (default)
[1] : Clear all PWM duty setting and intensity setting

D0 : SRST Soft reset control
[0] : Reset release state (default)
[1] : Reset reset

• This register will auto-return to zero when written with "High" logic value.

Register Name		POWERCNT							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
02h	R/W	--	--	--	--	--	--	--	OSCEN
Default	00h	0	0	0	0	0	0	0	0

D0 : OSCEN Internal oscillator ON/OFF bit
[0] : Internal oscillator OFF (default)
[1] : Internal oscillator ON

• Oscillator will auto turn ON if any of the LED drivers are enabled (MTXON = 1) even if this bit is [0].

Established : 2011-07-29
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		OPTION							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
04h	R/W	--	--	--	--	ZPDEN	MLDACT	CLKOUT	EXTCLK
Default	00h	0	0	0	0	0	0	0	0

D3 : ZPDEN Ghost Image Prevention Enable
[0] : Turn off ghost image prevention (default)
[1] : Turn on ghost image prevention

D2 : MLDACT External Melody Input Selection
[0] : Turn off melody mode (default)
[1] : Turn on melody mode

D1 : CLKOUT Internal clock output enable
[0] : Internal clock is not output from CLKOUT (default)
[1] : Internal clock is output from CLKOUT

D0 : EXTCLK Internal/external synchronous clock selection
[0] : Internal clock operation (default)
[1] : External clock operation

- Ghost Image Prevention may not remove the ghost image perfectly. It depends on the LED color combination and LED connection method. Please refer to Page.46 for details.
  Please refer to Page.47 for details especially when this LSI is used for RGB driver.
- For D2, D1 and D0 cannot be set to High at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

Register Name		MTXON							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
05h	R/W	--	--	--	IMAX Reserved	IMAX[2:0]			MTXON
Default	1Eh	0	0	0	1	1	1	1	0

D3-1 : IMAX Maximum current setup selection

[000] : 7.5 mA	[100] : 37.5 mA
[001] : 15 mA	[101] : 45 mA
[010] : 22.5 mA	[110] : 52.5 mA
[011] : 30 mA	[111] : 60 mA (default)

D0 : MTXON LED Matrix Set up ON/OFF control
[0] : OFF (default)
[1] : ON

- For better accuracy, it is advisable to set IMAX at 30 mA (IMAX = 011). The brightness can be adjusted lower by using brightness register (BRT*[3:0] (register #20h to #2Fh)) or PWM register (DT*[7:0] (register #10h to #1Fh)).

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		PWMEN1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
06h	R/W	PWMB4	PWMB3	PWMB2	PWMB1	PWMA4	PWMA3	PWMA2	PWMA1
Default	00h	0	0	0	0	0	0	0	0

D7 : PWMB4 B4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D6 : PWMB3 B3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D5 : PWMB2 B2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D4 : PWMB1 B1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D3 : PWMA4 A4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D2 : PWMA3 A3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D1 : PWMA2 A2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D0 : PWMA1 A1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		PWMEN2							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
07h	R/W	PWMD4	PWMD3	PWMD2	PWMD1	PWMC4	PWMC3	PWMC2	PWMC1
Default	00h	0	0	0	0	0	0	0	0

D7 : PWMD4 D4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D6 : PWMD3 D3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D5 : PWMD2 D2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D4 : PWMD1 D1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D3 : PWMC4 C4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D2 : PWMC3 C3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D1 : PWMC2 C2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D0 : PWMC1 C1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MDLEN1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
08h	R/W	MLDB4	MLDB3	MLDB2	MLDB1	MLDA4	MLDA3	MLDA2	MLDA1
Default	00h	0	0	0	0	0	0	0	0

D7 : MLDB4 B4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D6 : MLDB3 B3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D5 : MLDB2 B2 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D4 : MLDB1 B1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D3 : MLDA4 A4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D2 : MLDA3 A3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D1 : MLDA2 A2 Melody mode enable
[0] : Not PWM mode (default)
[1] : Melody mode

D0 : MLDA1 A1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MDLEN2							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
09h	R/W	MLDD4	MLDD3	MLDD2	MLDD1	MLDC4	MLDC3	MLDC2	MLDC1
Default	00h	0	0	0	0	0	0	0	0

D7 : MLDD4 D4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D6 : MLDD3 D3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D5 : MLDD2 D2 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D4 : MLDD1 D1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D3 : MLDC4 C4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D2 : MLDC3 C3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D1 : MLDC2 C2 Melody mode enable
[0] : Not PWM mode (default)
[1] : Melody mode

D0 : MLDC1 C1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MDLMODE2							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	R/W	--	GRP_ALL	GRP8_1	GRP8_0	GRP4_3	GRP4_2	GRP4_1	GRP4_0
Default	00h	0	0	0	0	0	0	0	0

D6 : GRP_ALL All LED blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode
(D1→C1→B1→A1→D2→C2→B2→A2→D3→C3→B3→A3→D4→C4→B4→A4)

D5 : GRP8_1 Column 3 and Column 4 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D3→C3→B3→A3→D4→C4→B4→A4)

D4 : GRP8_0 Column 1 and Column 2 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D1→C1→B1→A1→D2→C2→B2→A2)

D3 : GRP4_3 Column 4 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D4→C4→B4→A4)

D2 : GRP4_2 Column 3 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D3→C3→B3→A3)

D1 : GRP4_1 Column 2 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D2→C2→B2→A2)

D0 : GRP4_0 Column 1 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D1→C1→B1→A1)

A1	A2	A3	A4
B1	B2	B3	B4
C1	C2	C3	C4
D1	D2	D3	D4

GRP_ALL	GRP8_0	GRP4_0	MLDA1	Melody Modes
0	0	0	0	Normal mode
1	x	x	x	Bar meter mode of all LED
0	1	x	x	Bar meter mode of Column 1 and Column 2
0	0	1	x	Bar meter mode of Column 1
0	0	0	1	Melody mode of A1

• During Bar Meter Mode, auto threshold detection should be used. This LSI does not support Bar Meter Mode with fixed threshold setting.

Established : 2011-07-29
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MLDCOM							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Bh	R/W	--	--	--	--	--	MLDCOM[2:0]		
Default	03h	0	0	0	0	0	0	1	1

D2-0 : MLDCOM LED Turn on time compensation in melody mode

[000] : 0 s
[001] : 0.86 µs
[010] : 1.72 µs
[011] : 2.58 µs (default)
[100] : 3.44 µs
[101] : 4.30 µs
[110] : 5.17 µs
[111] : 6.03 µs

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		THOLD							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	R/W	THOLD[7:0]							
Default	00h	0	0	0	0	0	0	0	0

D7 : THOLD[7] Threshold 8 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 8 is used. (Threshold 8 is about 1.93 V)

D6 : THOLD[6] Threshold 7 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 7 is used. (Threshold 7 is about 1.80 V)

D5 : THOLD[5] Threshold 6 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 6 is used. (Threshold 6 is about 1.67 V)

D4 : THOLD[4] Threshold 5 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 5 is used. (Threshold 5 is about 1.55 V)

D3 : THOLD[3] Threshold 4 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 4 is used. (Threshold 4 is about 1.42 V)

D2 : THOLD[2] Threshold 3 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 3 is used. (Threshold 3 is about 1.30 V)

D1 : THOLD[1] Threshold 2 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 2 is used. (Threshold 2 is about 1.17 V)

D0 : THOLD[0] Threshold 1 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 1 is used. (Threshold 1 is about 1.04 V)

- When all bits are set zero, threshold is in auto-detection mode (default)
- Do not set more than 1 register bit to logic "High" value at the same time.
- If 2 bits are set to "High" at the same time, system will only recognize the first "High" bit threshold that is set.

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		XCONST							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	R/W	--	--	--	X5	X4	X3	X2	X1
Default	00h	0	0	0	0	0	0	0	0

D4 : X5 Z5 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z5 is fixed as constant current mode. The LED D1's current setting is used.

D3 : X4 Z4 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z4 is fixed as constant current mode. The LED A4's current setting is used.

D2 : X3 Z3 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z3 is fixed as constant current mode. The LED A3's current setting is used.

D1 : X2 Z2 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z2 is fixed as constant current mode. The LED A2's current setting is used.

D0 : X1 Z1 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z1 is fixed as constant current mode. The LED A1's current setting is used.

• Please refer to Page.30 for details.

Established : 2011-07-29
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		YCONST							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Eh	R/W	Y4	Y3	Y2	Y1	Y4MSK	Y3MSK	Y2MSK	Y1MSK
Default	00h	0	0	0	0	0	0	0	0

D7 : Y4 Z4 output is fixed to High (VCC level).
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z4 turns on (VCC level).

D6 : Y3 Z3 output is fixed to High (VCC level).
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z3 turns on (VCC level).

D5 : Y2 Z2 output is fixed High (VCC level).
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z2 turns on (VCC level).

D4 : Y1 Y1CNT is fixed to High (VCC level).
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z1 turns on (VCC level).

D3 : Y4MSK Z4 output is fixed to OFF.
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z4 turns off.

D2 : Y3MSK Z3 output is fixed to OFF.
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z3 turns off.

D1 : Y2MSK Z2 output is fixed to OFF.
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z2 turns off.

D0 : Y1MSK Z1 output is fixed to OFF.
[0] : Normal matrix operation (default)
[1] : Switch between VCC and Z1 turns off.

• Please refer to Page.30 for details.

Established : 2011-07-29
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		SLPTIME							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Fh	R/W	--	SCANSET[1:0]		FADTIM	SLOPEEXTL[1:0]		SLOPEEXTH[1:0]	
Default	60h	0	1	1	0	0	0	0	0

D6-5 : SCANSET Scan number control.
[00] : Only scan the first column.
[01] : Only scan the first 2 column.
[10] : Only scan the first 3 column.
[11] : Scan all column (default)

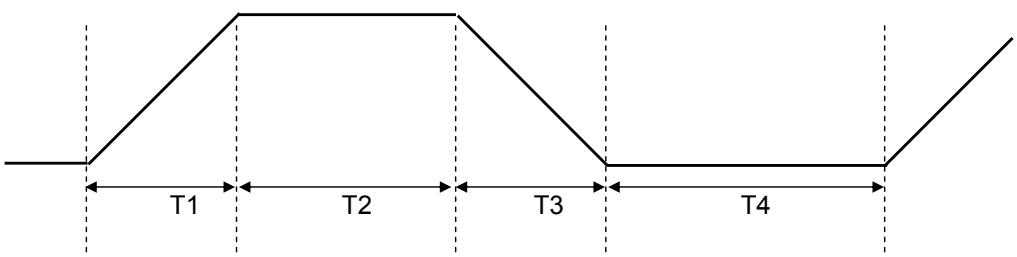
D4 : FADTIM Fade out time control.
[0] : T3 = T1 (default)
[1] : T3 = T1 × 2

• This bit also affect in PWM fade out mode. Fade out time becomes 2 times of fade in time when FADTIM = 1.

D3-2 : SLOPEEXTL T4 time extent control.
[00] : T4 = T1 (default)
[01] : T4 = T1 × 0.25
[10] : T4 = T1 × 0.5
[11] : T4 = T1 × 2

D1-0 : SLOPEEXTH T2 time extent control.
[00] : T2 = T1 (default)
[01] : T2 = T1 × 0.25
[10] : T2 = T1 × 0.5
[11] : T2 = T1 × 2

• T1 time is controlled by the register #20h to #2Fh.



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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		DTA1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
10h	R/W	DTA1[7:0]							
Default	00h	0	0	0	0	0	0	0	0

D7-0 : DTA1 A1 PWM duty control.
[0000_0000] : 0%. (default)
[0000_0001] : 0.39%. (1/256)
[0000_0010] : 0.78%. (2/256)
[0000_0011] : 1.17%. (3/256)
…
[1111_1100] : 98.8%. (253/256)
[1111_1110] : 99.2%. (254/256)
[1111_1111] : 99.6%. (255/256)

- This duty setting is only effective when PWMA1 is High.
- The definition for register addresses #11h to #1Fh is the same as address #10h.

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		A1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
20h	R/W	BRTA1[3:0]				--	SDTA1[2:0]		
Default	00h	0	0	0	0	0	0	0	0

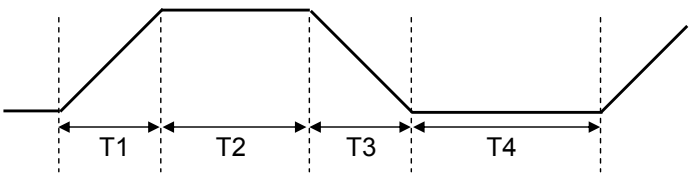
D7-4 : BRTA1 Luminance set up of LED A1 (in case of IMAX [2:0] == [011])

[0000] : 0 mA (default)
[0001] : 2 mA
[0010] : 4 mA
[0011] : 6 mA
[0100] : 8 mA
[0101] : 10 mA
[0110] : 12 mA
[0111] : 14 mA
[1000] : 16 mA
[1001] : 18 mA
[1010] : 20 mA
[1011] : 22 mA
[1100] : 24 mA
[1101] : 26 mA
[1110] : 28 mA
[1111] : 30 mA

D2-0 : SDTA1 (SCANSET == [11], default setting)

(1) Firefly Operation (PWMA1 == 0)

[000] : Constant current mode (default)
[001] : 0.22 s
[010] : 0.44 s
[011] : 0.88 s
[100] : 1.32 s
[101] : 1.76 s
[110] : 2.2 s
[111] : 2.64 s



(2) PWM Fade-in/out Operation (PWMA1 == 1)

[000] : Instant change mode (default)
[001] : 1.72 ms
[010] : 3.44 ms
[011] : 6.89 ms
[100] : 10.34 ms
[101] : 13.79 ms
[110] : 17.3 ms
[111] : 20.7 ms

- In case of PWM duty change from 0 to 255, the longest time is 255 × 20.7 ms = 5.2785 s.
- T1 time is also controlled by SCANSET in register #0Fh. The calculation method is as follow:
  SCANSET == 00 : T1 = 0.25 × T_default
  SCANSET == 01 : T1 = 0.5 × T_default
  SCANSET == 10 : T1 = 0.75 × T_default
- The definition for register addresses #21h to #2Fh is the same as address #20h.

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OPERATION (continued)

4. Operation Mode priority

MTXON	X*	Y*MSK	Y*	PWM*	SDT*	Operation Mode
0	x	x	x	x	x	OFF
1	1	x	x	x	x	Z* constant current mode
1	0	1	x	x	x	Switch between VCC and Z* turns off
1	0	0	1	x	x	Switch between VCC and Z4 turns on (VCC level).
1	0	0	0	1	x	PWM mode
1	0	0	0	0	!=0	Firefly mode
1	0	0	0	0	0	Constant current mode

• * for X*, PWM*, SDT* == 1 ~ 5, * for Y*MSK, Y* == 1 ~ 4.

Established : 2011-07-29
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OPERATION (continued)

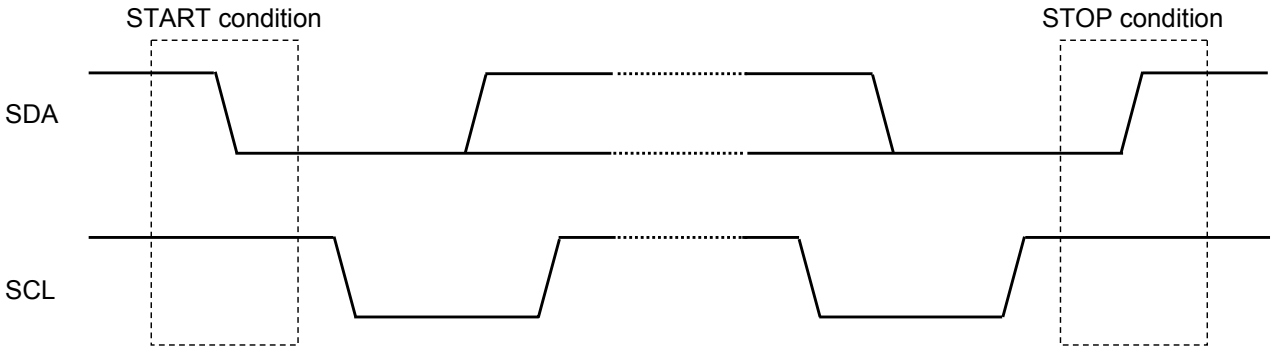
5. I²C Bus Interface

5.1 Basic Rules

- This LSI, I²C-bus, is designed to correspond to the Standard-mode (100 kbps), Fast-mode(400 kbps) and Fast-mode plus (1 000 kbps) devices in the version 2.1 of NXP's specification. However, it does not correspond to the H_S-mode (to 3.4 Mbps).
- This LSI will operate as a slave device in the I²C-bus system. This LSI will not operate as a master device.
- The program operation check of this LSI has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this LSI to the CBUS receiver also has not been checked. Please confirm with our company if it will be used in these mode systems.
- The I²C is the brand of NXP.

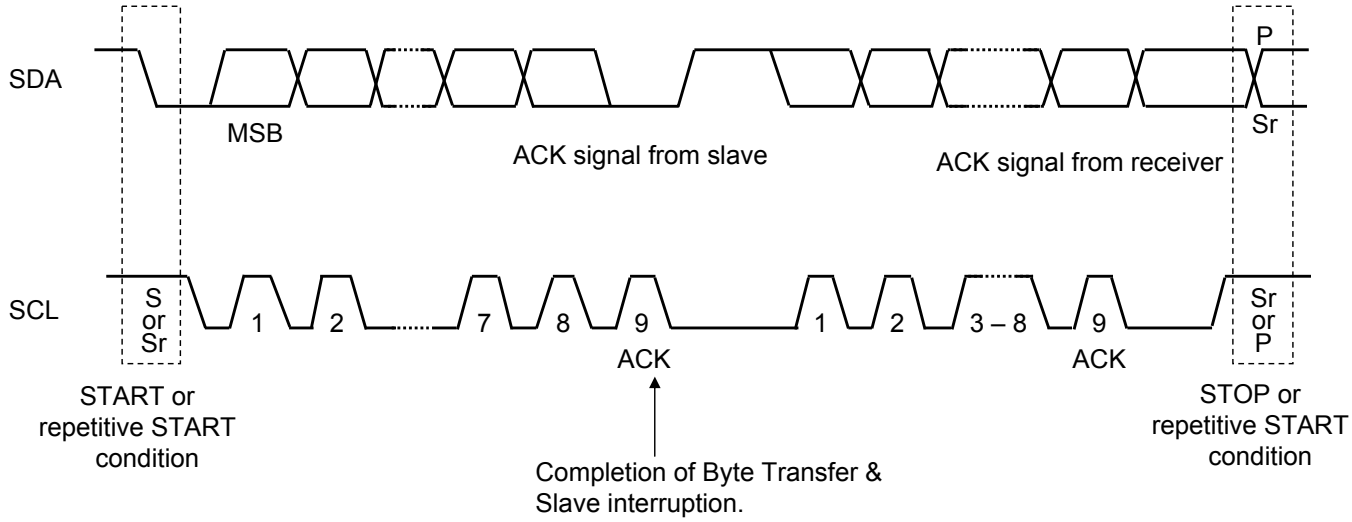
5.2 START and STOP conditions

When SDA signal changes from "High" to "Low" while SCL is "High" will trigger START condition. Whereas, STOP condition will be triggered when SDA signal changes from "Low" to "High" while SCL is "High".
START condition and STOP condition are always formed by the master. After the START condition occurs, the bus becomes busy state. After STOP condition occurs, the bus becomes free again.



5.3 Data Transfer

Length of each byte output to SDA line is always 8 bits. There is no limitation in the number of bytes that can be transmitted at 1 time. Many bytes can be sent. The acknowledge bit is necessary for each byte.
Data is sequentially transmitted from most significant bit (MSB).



Established : 2011-07-29
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OPERATION (continued)

5. I²C Bus Interface (continued)

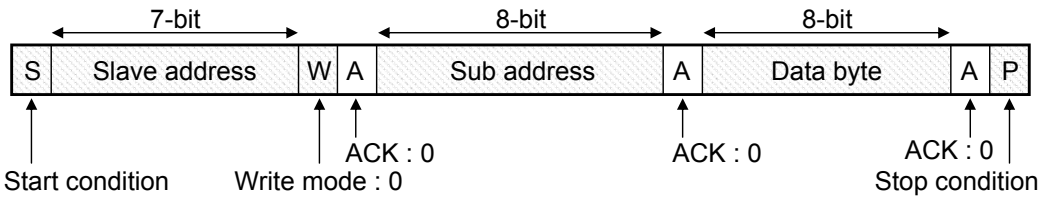
5.4 I²C Interface - Data Format

In this LSI, 4 different Slave address can be changed by selecting SLAVSEL ("Low" or "High" or "SCL" or "SDI").
The slave addresses of this LSI are as follow:

SLAVSEL	Slave address
Low	1010 000X
High	1010 001X
SCL	1010 010X
SDI	1010 011X

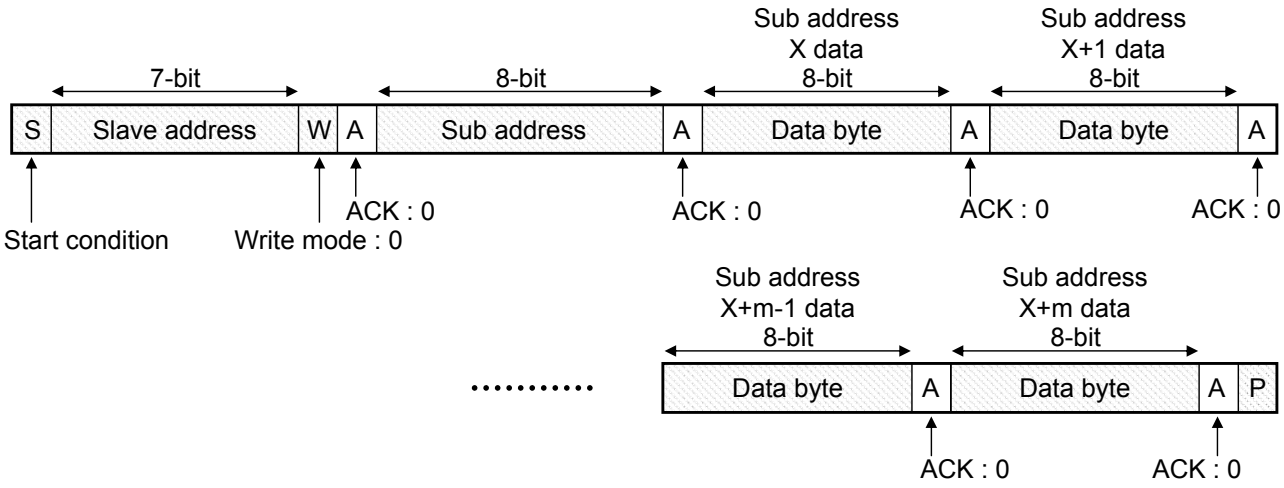
Write mode

Sub address is not incremented automatically.
The next data byte is written in the same Sub address by transmitting data byte continuously.



Write mode (Auto increment mode)

Data byte can be written in Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



: Data transmission from Master

: Data transmission from Slave

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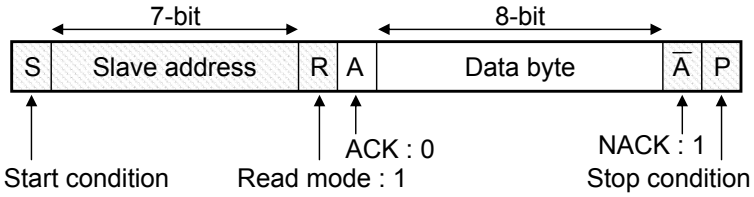
OPERATION (continued)

5. I²C Bus Interface (continued)

5.4 I²C Interface - Data Format (continued)

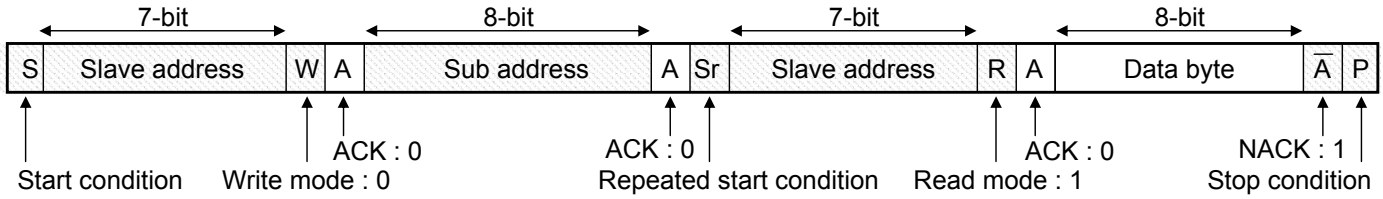
Read mode (in case Sub address is not specified)

When Sub address 8 bit is not specified and data is read, this LSI allows to read the value of adjacent Sub address specified in the last Write mode.
The next data byte reads the same Sub address by transmitting data byte continuously.



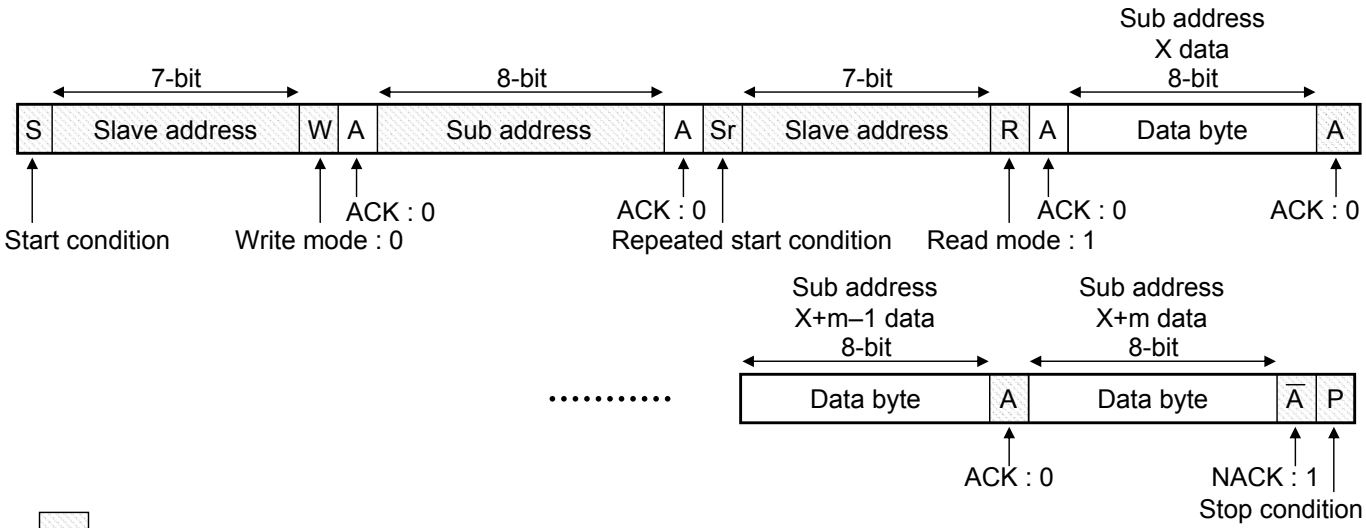
Read mode (in case Sub address is specified)

Sub address is not incremented automatically.
The next data byte reads the same Sub address by transmitting data byte continuously.



Read mode (Auto increment mode)

It is possible to read data byte in continuous Sub address by transmitting data byte continuously.
Sub address is incremented automatically.



: Data transmission from Master

: Data transmission from Slave

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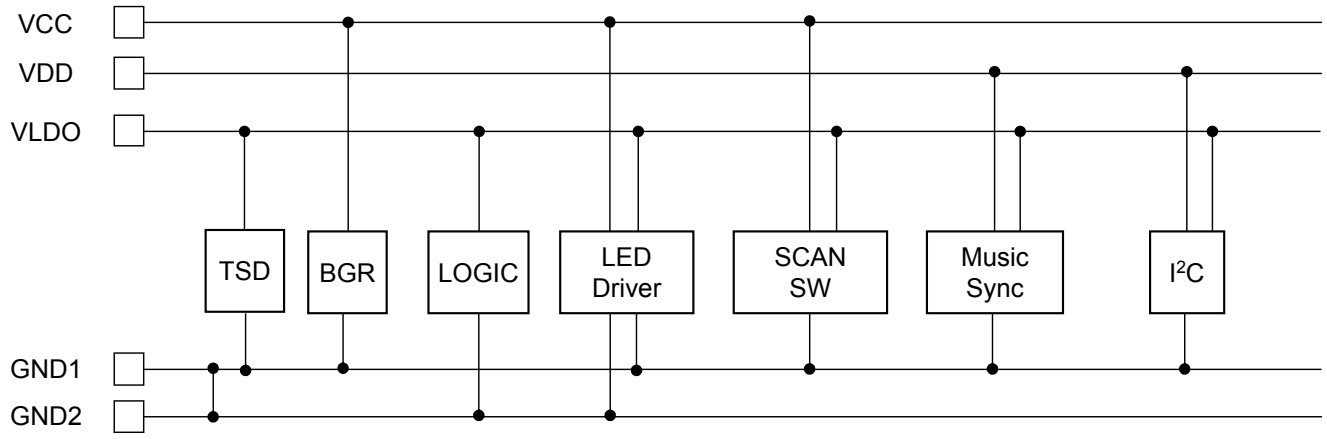
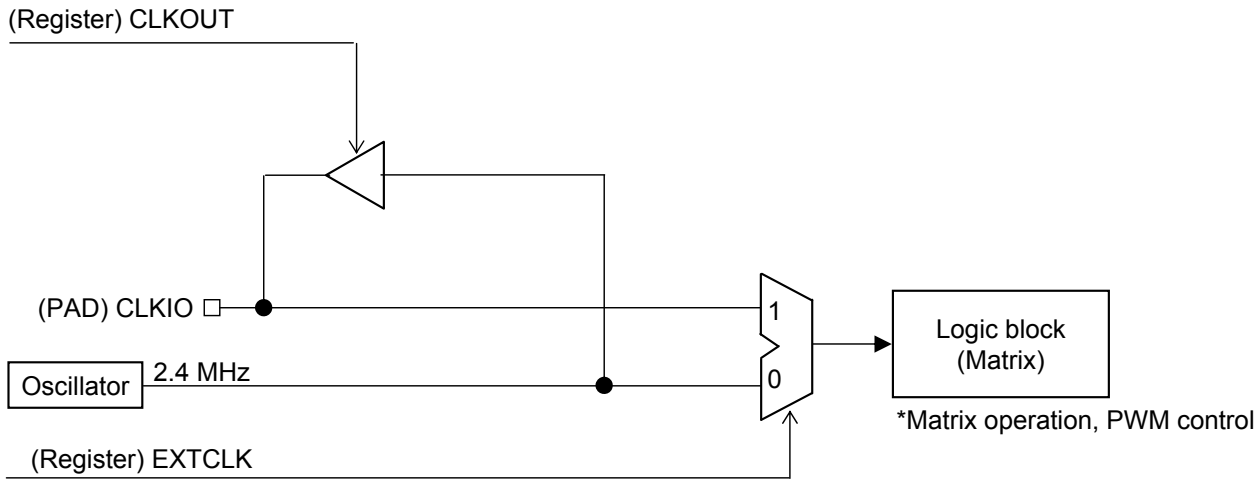
OPERATION (continued)

6. Signal distribution diagram

6.1 Distribution diagram of power supply



6.2 Distribution diagram of control / clock system



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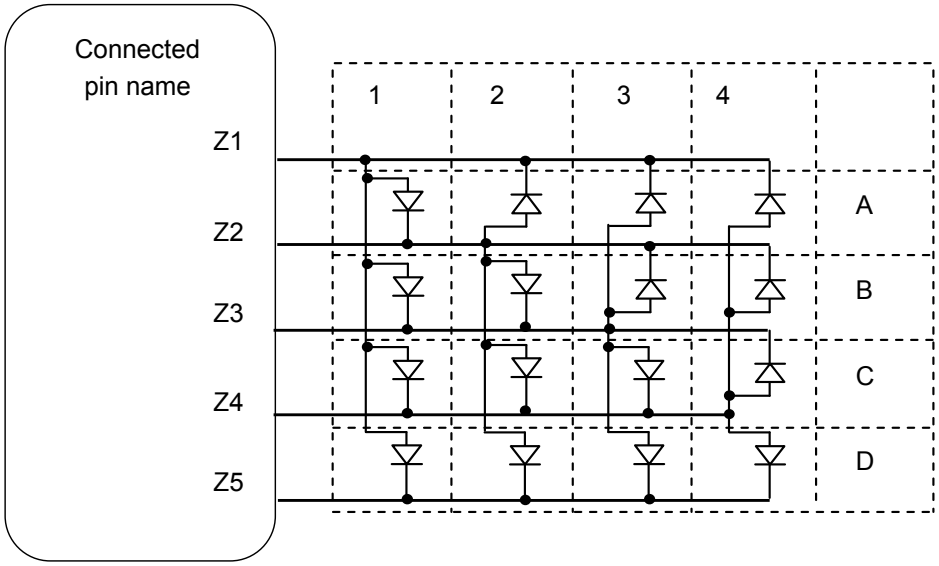
OPERATION (continued)

7. Block Configuration of Matrix LED

7.1 Matrix LED descriptions, Matrix LED's numbers

LED matrix driver circuit individually drives LED of 4 × 4 matrix. In total, the LSI can drive and light up 16 LED.
In this specification, LED's number controlled by each pin corresponds as follows.
The internal logic circuit is operated by using an internal clock or the external clock input to the terminal CLKIO.



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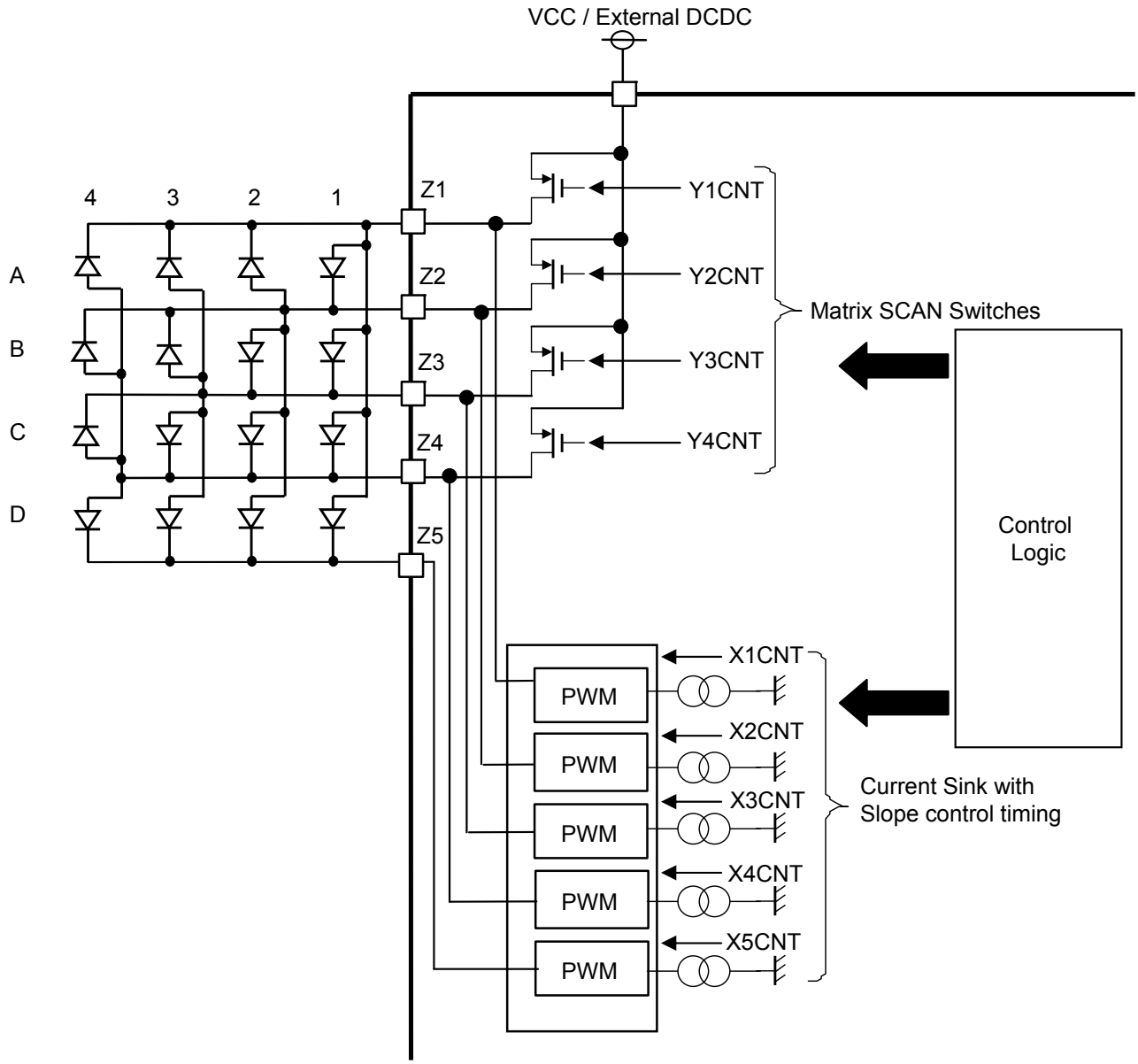
OPERATION (continued)

7. Block Configuration of Matrix LED (continued)

7.2 Driver Configuration

- Actual driver configuration is shown in the following figure.
- The anodes and cathode of each LED are connected to different Z pin as shown in figure below.
- Z5 pin consists of only Current Sink and Slope control timing driver. Thus, LED anode are not to be connected to Z5 pin.
- Please do not remove any of the LED inside the matrix if it is not used. If LED are to be removed, it is advised to remove the entire row (e.g: all LED in row A) instead of removing only 1 LED. If only one LED in the row is removed instead of the whole row, user needs to avoid using LED whose reverse breakdown voltage is lower than the operating VCC level.
- Internal control logic according to user register settings is used to control Y1 to Y4CNT(PMOS ON/Off Scan Switches) as well as X1 to X5CNT (Current sink value as well as PWM/Slope timing for lighting effects)



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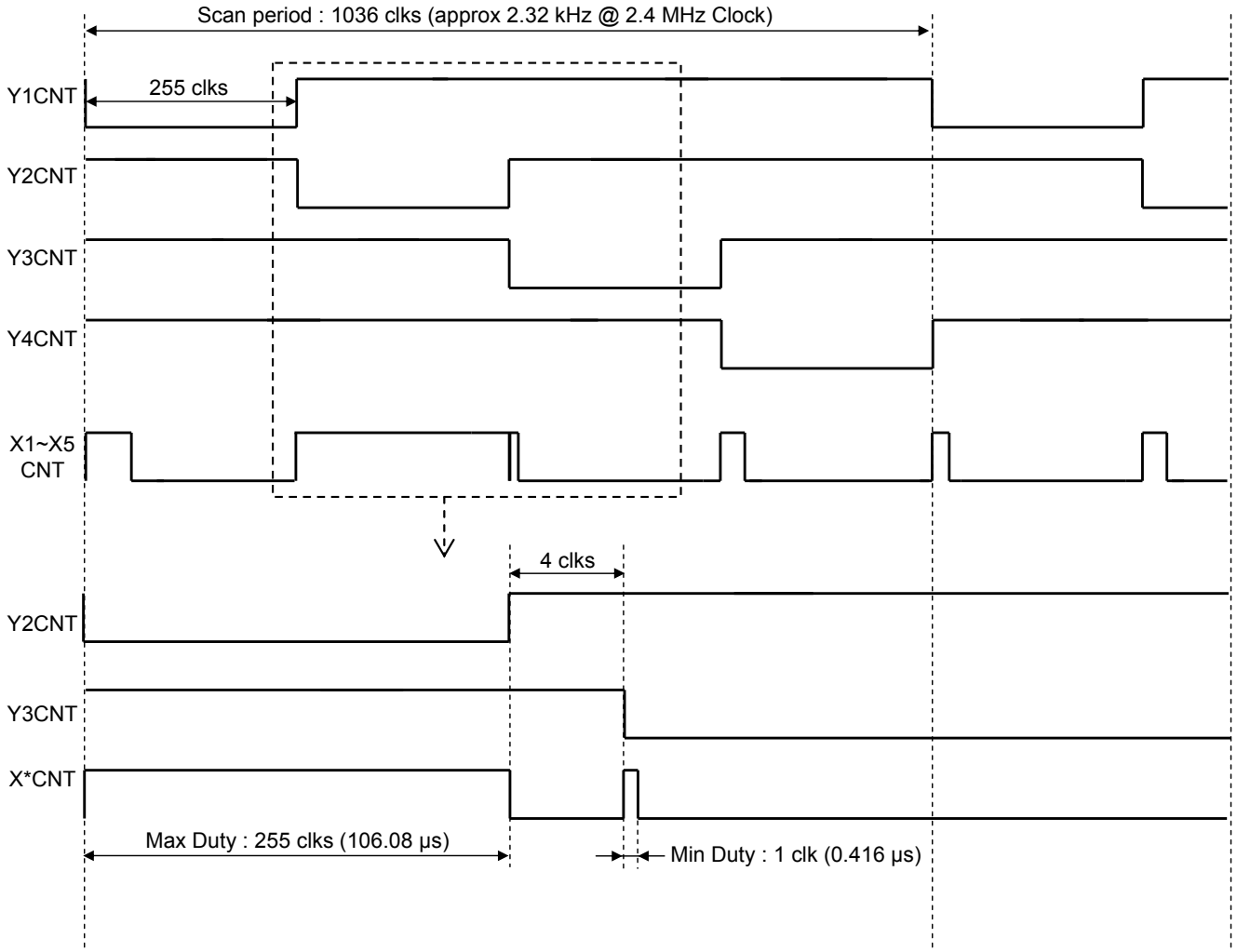
OPERATION (continued)

7. Block Configuration of Matrix LED (continued)

7.3 Timing Chart when in operation

- The figure below shows a timing chart when in operation.
- Timing can be controlled according to the external clock frequency input to CLKIO pin.
- In default condition, it is controlled by internal 2.4 MHz clock.
- Y1 to Y4CNT are scan timing which is turned on one at a time. The ON period of each pin is constant 255 clks (106.08 µs) and includes the interval of 4 clks (1.664 µs).
- 16 LED (4 × 4 matrix) are controlled by X1 to X5CNT according to below figure.
- When Yx = Xx = Low, the actual waveform of Zx is set to Hi-Z.



- Duty can be set using register DT*[7:0] from registers #10h to #1Fh. Additional brightness control is provided through register BRT*[3:0] (registers #20h to #2Fh).

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OPERATION (continued)

8. LED Driver Block Function

Functions Table for LED Driver

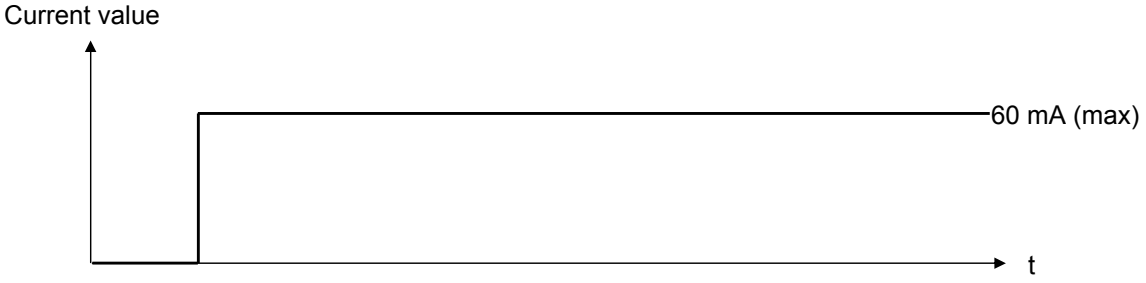
No.	Features	Setting Range
1	Constant current mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step
2	PWM mode and Fade-in/out mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Adjustable detention Time for each step : (1.72 ms to 20.7 ms / step)
3	Firefly mode	Fixed Current at 100% Duty IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Adjustable detention Time for each step : (0.22 s to 2.64 s / step)
4	Melody mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Each LED can synchronize with Music Input from CLKIO pin
5	Bar Meter Mode	IMAX Setting : 7.5 mA to 60 mA (max) DAC Current Step (Brightness) : 0.5 mA to 4 mA (max) step Group LED can synchronize with Music Input from CLKIO pin Bar Meter Mode has more priority than Melody mode.

8.1 Constant Current Mode

Maximum current setting value can be set up as 60 mA using register IMAX[2:0] (register 05h). Brightness can be set through the register BRT*[3:0] (register #20h to #2Fh) for individual LED.

Example)

E.g. If user sets register IMAX[2:0] (#05h) = 011 and BRT*[3:0] = 1111, the current will be 30 mA.
E.g. If user sets register IMAX[2:0] (#05h) = 111 and BRT*[3:0] = 1111, the current will be 60 mA.
E.g. If user sets register IMAX[2:0] (#05h) = 111 and BRT*[3:0] = 0111, the current will be 28 mA.



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OPERATION (continued)

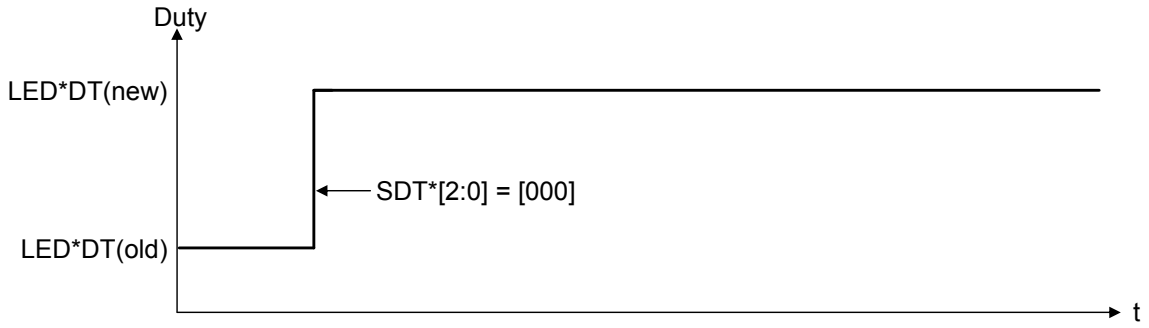
8. LED Driver Block Function (continued)

8.2 PWM Mode and Fade-in/out Mode

This operation is characterized by PWM signal having variable duty depending on register DT*[7:0] (registers #10h to #1Fh). However, any changes in duty is not instantaneous, but rather it will step to the new duty at time determined by register SDT*[2:0].

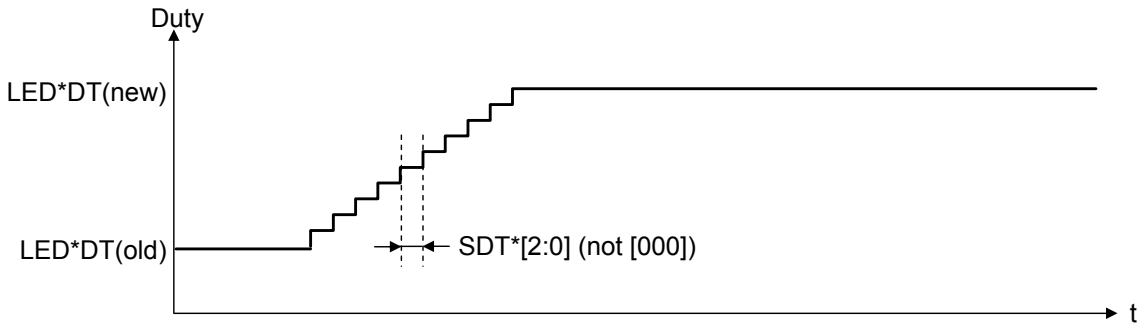
Example)

Case 1 : LED*DT(new) > LED*DT(old) (PWM Mode without Fade in/out control)



In Case 1, PWM duty has been changed from low to high duty. But the register SDT*[2:0] setting is [000] indicating that there is no Fade in/out control. Therefore, PWM duty changes instantaneously. Users can see that LED becomes brighter instantaneously once PWM duty has been changed.

Case 2 : LED*DT(new) > LED*DT(old) (PWM Mode with Fade in control)



In Case 2, PWM duty has also been changed from low to high duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 2. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade in control. Users can see that LED becomes brighter slowly according to the timing set in register SDT*[2:0].

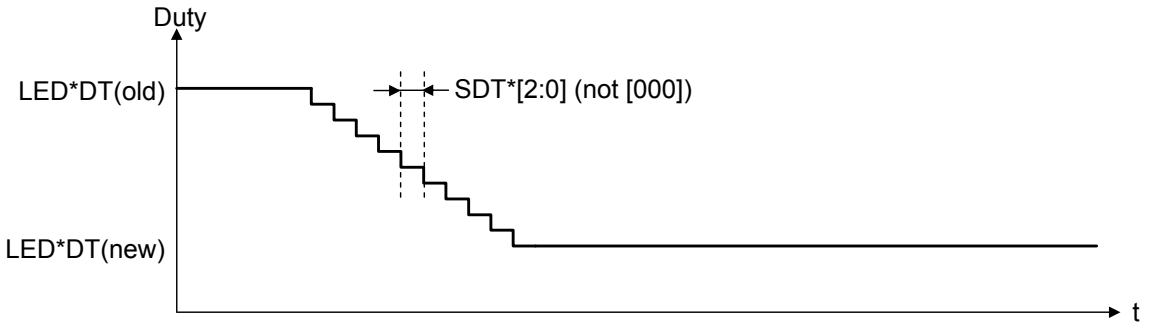
OPERATION (continued)

8. LED Driver Block Function (continued)

8.2 PWM Mode and Fade-in/out Mode (continued)

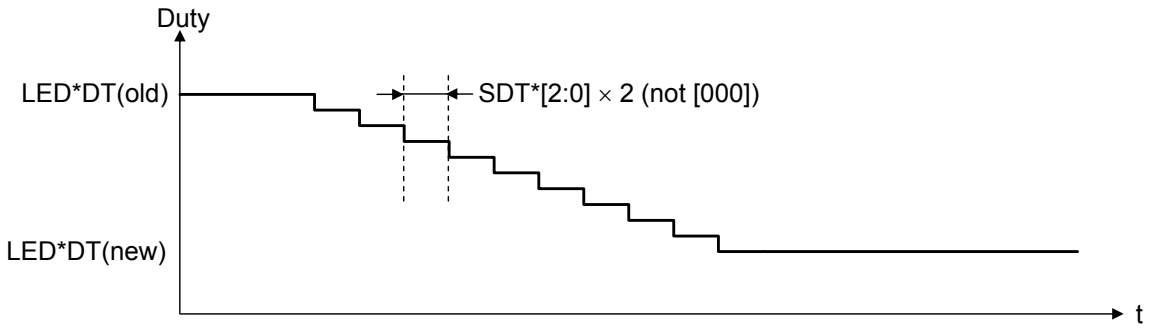
Example) (continued)

Case 3 : LED*DT(new) < LED*DT(old), FADTIM = 0 (PWM Mode with Fade out control)



In Case 3, PWM duty has been changed from high to low duty. Unlike in case 1, the register SDT*[2:0] setting is not [000] in case 3. Therefore, PWM duty has changed according to the register SDT*[2:0] setting. This is called PWM mode with Fade out control. Users can see that LED becomes dimmer slowly according to the timing set in register SDT*[2:0].

Case 4 : LED*DT(new) < LED*DT(old), FADTIM = 1 (PWM Mode with Fade out control)



In Case 4, PWM duty has also been changed from high to low duty. Unlike in case 3, the register FADTIM is not [0]. Again, the register SDT*[2:0] setting is also not [000] in case 4. PWM duty has changed according to the register SDT*[2:0] setting. Users can see that LED becomes dimmer slowly. It is slower than Case3 as FADTIM register is high (2 times slower than Case 3 Fade out control).

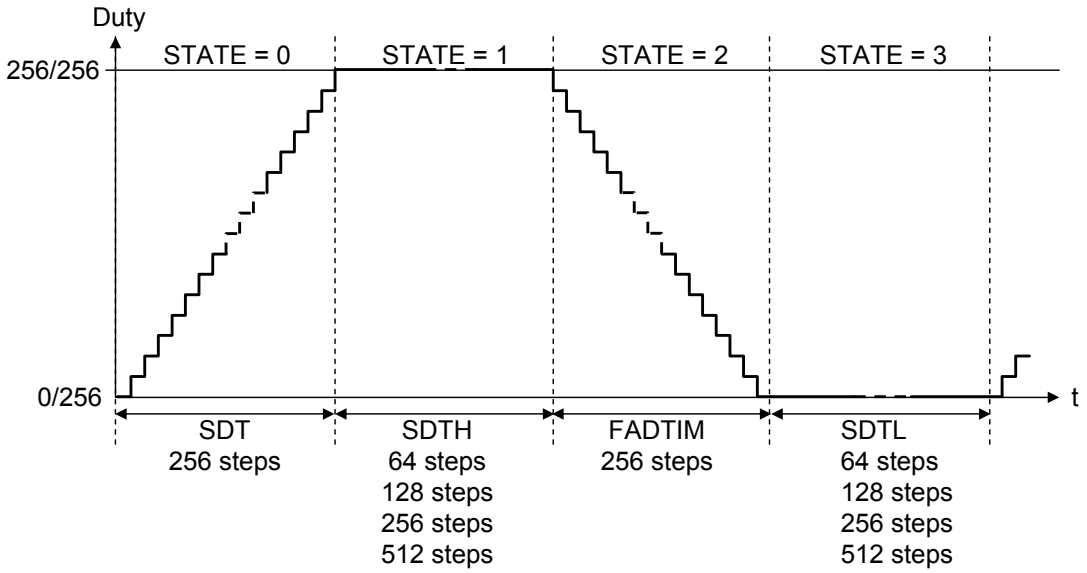
DT*[7:0] is set through register #10h to #1Fh. FADTIM is set through register #0Fh. SDT*[2:0] is set through register #20h to #2Fh.

OPERATION (continued)

8. LED Driver Block Function (continued)

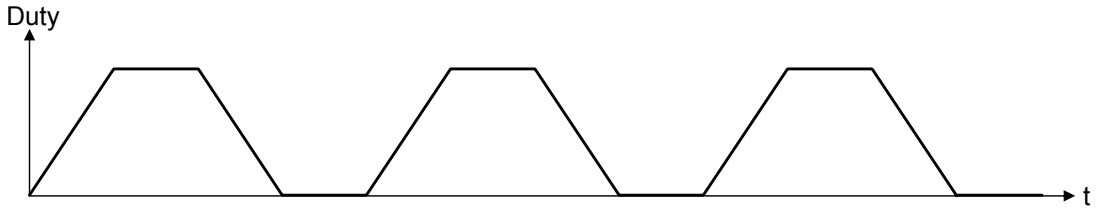
8.3 Firefly Control

This operation is characterized by PWM signal cycling from minimum to maximum duty and vice versa with auto repeat function at time step determined by register SDT*[2:0]. Unlike PWM Fade in/out mode, firefly is auto repeat and thus creating LED blinking function effect.

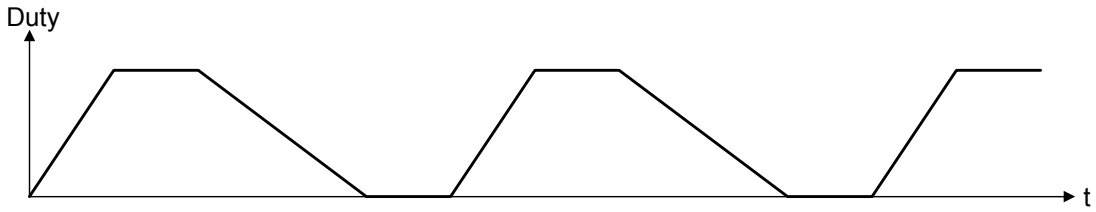


Example)

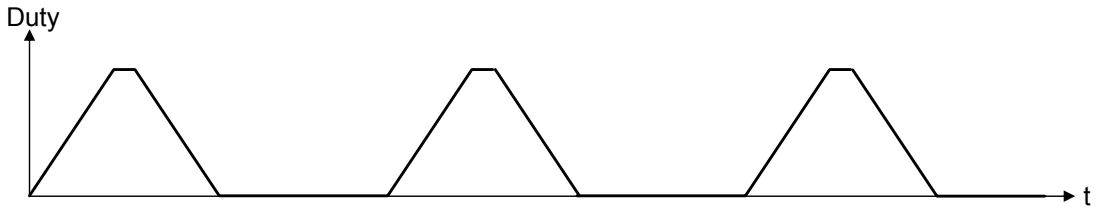
Example 1 : SDTH = 00 (SDT × 1), SDTL = 00 (SDT × 1), FADTIM = 0



Example 2 : SDTH = 00 (SDT × 1), SDTL = 00 (SDT × 1), FADTIM = 1 (SDT × 2)



Example 3 : SDTH = 01 (SDT × 0.25), SDTL = 11 (SDT × 2), FADTIM = 0



The SDTH is controlled by SLOPEEXTH[1:0] register, SDTL is controlled by SLOPEEXTL[1:0] register. All these registers, SLOPEEXTH[1:0], SLOPEEXTL[1:0] and FADTIM can be set through register #0Fh. SDT*[2:0] registers are set individually through register #20h to #2Fh. All other combinations of SDTH, SDTL and FADTIM is possible.

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OPERATION (continued)

8. LED Driver Block Function (continued)

8.4 Melody Mode Explanation

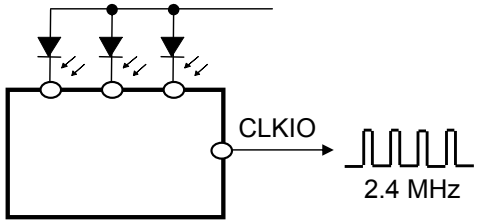
Melody mode is to synchronize LED to external music signal. Melody mode can be set through register MLDACT from register 04h. Each of the 16 LED matrix can be individually enabled for external music synchronization through register data (address #08h to #09h when register address 04h is set as data 04h).

External Music Signal can be injected from CLKIO pin. CLKIO pin serve as both input and output. CLKIO pin can output internal oscillator frequency by using CLKOUT register (register 04h).

CLKIO pin can be used as input for external signal by using EXTCLK register (register 04h). External clock frequency is typically 2.4 MHz. It is advisable to use external clock frequency from 1.2 MHz to 4.8 MHz.

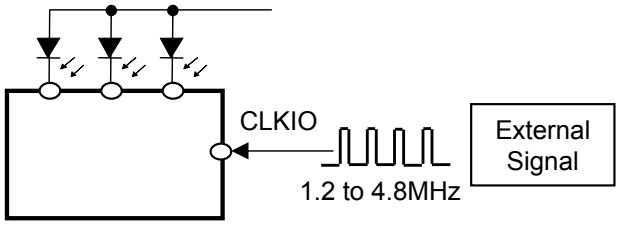
Please do not set MLDACT, EXTCLK and CLKOUT register to "High" at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

Case 1 : CLKIO as output pin



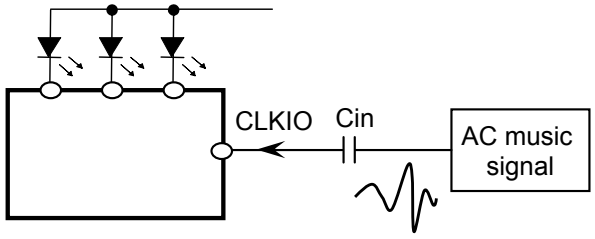
CLKIO output internal frequency by using CLKOUT register

Case 2 : CLKIO as input for external clock



CLKIO uses as external input by using EXTCLK register

Case 3 : CLKIO as input for music signal during melody mode



CLKIO uses as music input when melody mode is enabled by register MLDACT from register 04h.

Note : If input CLKIO voltage is higher than VDD, there will be back flow current to VDD. It can be calculated as below :

$$I_{BackFlow} = \frac{(V_{CLKIO} - 0.7\ V - VDD)}{393\ k\Omega}$$

Note : Cin can be calculated as below : In case of that the applicable music frequency is 20 Hz.

$$Cin >= \frac{1}{(20\ Hz) \times 2 \times 3.14 \times 175\ k\Omega} = 45.5\ nF$$

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OPERATION (continued)

8. LED Driver Block Function (continued)

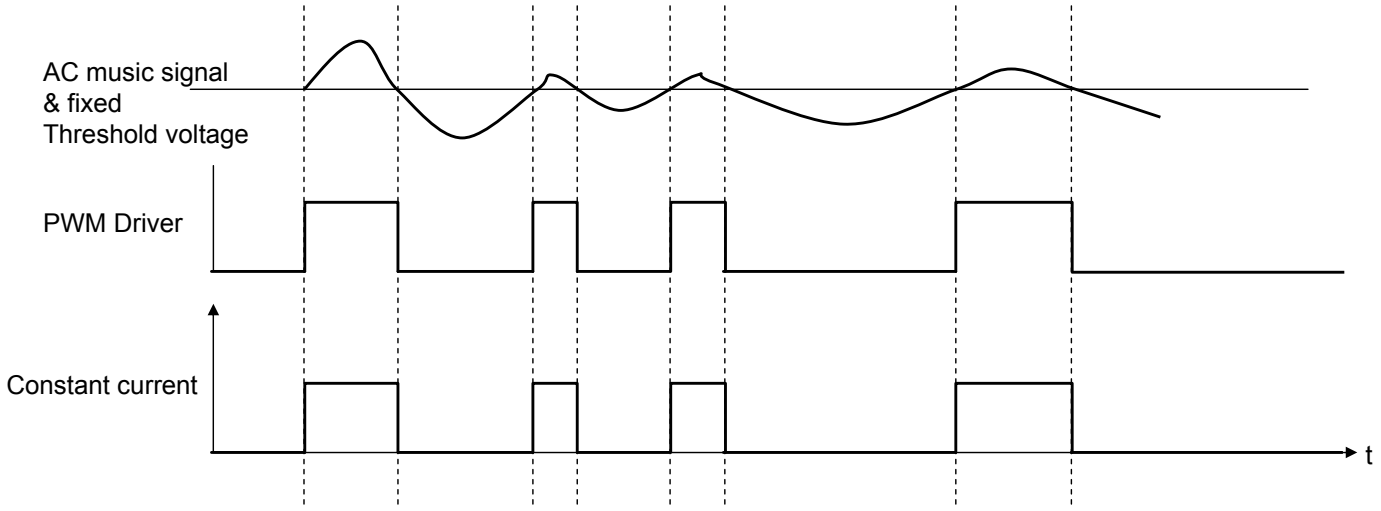
8.4 Melody Mode Explanation (continued)

AC music signal input from CLKIO pin will be compared with internal threshold setting. Based on the comparison of music signal and threshold voltage, PWM driver control will change and control the LED ON/OFF. Therefore, LED light on/off control will synchronize with music tempo while LED brightness will synchronize with music loudness. There are two threshold mode, one is “auto threshold” and the other is “fixed threshold mode”.

There are 8 threshold voltage levels in this LSI as defined in the register 0Ch (THOLD[7:0]). Auto threshold mode means that the 8 threshold voltages will be scanned automatically from the lowest to highest threshold voltages at a fixed frequency higher than audio frequency. Input music signal will be compared with these scanning threshold voltages to control PWM Driver in order to have music synchronization effects. This mode allows user to easily use music synchronize function without having the trouble of manually setting the detection threshold. When melody mode is enabled, auto threshold mode will be the default mode.

Fixed threshold mode means that the threshold voltage is fixed at one threshold level. It can be set using register 0Ch (THOLD[7:0]). Input music signal will be compared with this fixed threshold voltage set by the user. During fixed threshold mode, do not set more than 1 register bit to logic "High" value at the same time. If user set more register bits to logic "High" after setting 1 register bit to "High", system will only recognise the first "High" bit threshold that is set. In this mode, user can have the flexibility to configure different threshold voltage levels to achieve the desired LED music synchronizing visual effect according to the system music input level.

It is also advised that AC music signal peak to peak voltage to be at least 0.35 V and not more than 2.8 V.



Example of Fixed threshold mode

• Brightness Compensation in Melody Mode

Additional brightness compensation in melody mode can be achieved by increasing or decreasing the turning on period of LED. Using brightness compensation register #0Bh, LED turning on period can be controlled and LED can become brighter or dimmer.

This additional brightness compensation will be effective only in auto threshold mode. If fixed threshold mode is used, this register will not be able to control LED brightness.

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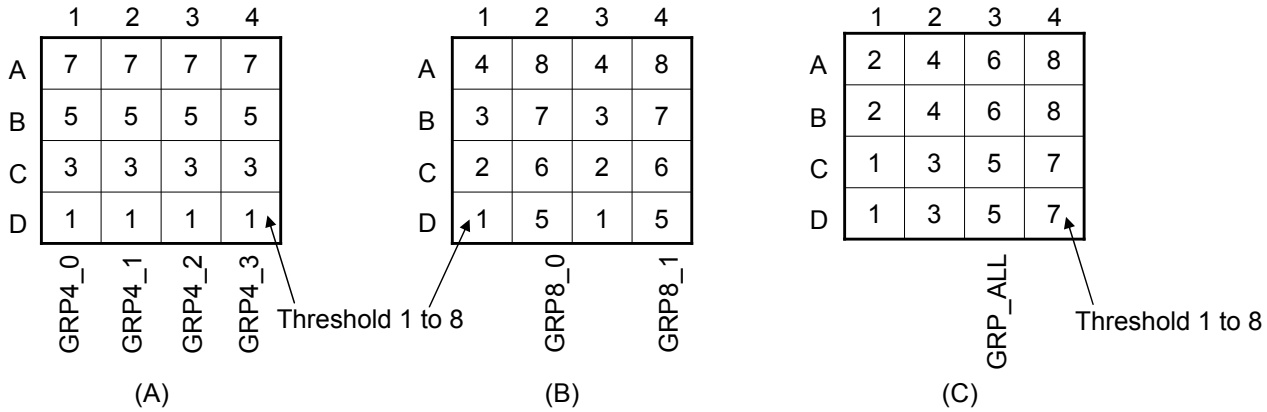
OPERATION (continued)

8. LED Driver Block Function (continued)

8.5 Bar Meter Mode Explanation

Bar Meter Mode operation is another method of external melody mode wherein a group of LEDs are used instead of individual LED. Bar Meter Mode has higher priority than individual LED melody mode.



In the above diagram (A), column 1 = group4_0, column 2 = group4_1, column 3 = group4_2 and column 4 = group4_3.
Each group can be enabled through register GRP4_0, 4_1, 4_2, 4_3 (address #0Ah). The LED in the all groups will be synchronized to threshold signals as follow:

Threshold Signal	Bar Meter Mode Group LED ON	
Threshold 1	Row's	D
Threshold 3	Row's	C, D
Threshold 5	Row's	B, C, D
Threshold 7	Row's	A, B, C, D

In the above diagram (B), another pattern of grouping is shown. Column 1 & 2 = group8_0 and Column 3 & 4 = group8_1.
Each group can be enable through register GRP8_0 & GRP8_1 (address #0Ah). The LED in the all groups will be synchronized to threshold signals as follow:

Threshold Signal	Bar Meter Mode Group LED ON	
Threshold 1	LED	D1, D3
Threshold 2	LED	C1, C3, D1, D3
Threshold 3	LED	B1, B3 , C1, C3, D1, D3
Threshold 4	LED	A1, A3, B1, B3, C1, C3, D1, D3
Threshold 5	LED	D2, D4, A1, A3, B1, B3, C1, C3, D1, D3
Threshold 6	LED	C2, C4, D2, D4, A1, A3, B1, B3, C1, C3, D1, D3
Threshold 7	LED	B2, B4, C2, C4, D2, D4, A1, A3, B1, B3, C1, C3, D1, D3
Threshold 8	LED	A2, A4, B2, B4, C2, C4, D2, D4, A1, A3, B1, B3, C1, C3, D1, D3

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OPERATION (continued)

8. LED Driver Block Function (continued)

8.5 Bar Meter Mode Explanation (continued)

In the above diagram (C), another pattern of grouping is shown. The whole 4 × 4 matrix is grouped. It can be enable through register GRP_ALL (address #0Ah). The LED in the all groups will be synchronized to threshold signals as follow:

Threshold Signal	Bar Meter Mode Group LED ON	
Threshold 1	LED	C1, D1
Threshold 2	LED	A1, B1, C1, D1
Threshold 3	LED	C2, D2, A1, B1, C1, D1
Threshold 4	LED	A2, B2, C2, D2, A1, B1, C1, D1
Threshold 5	LED	C3, D3, A2, B2, C2, D2, A1, B1, C1, D1
Threshold 6	LED	A3, B3, C3, D3, A2, B2, C2, D2, A1, B1, C1, D1
Threshold 7	LED	C4, D4, A3, B3, C3, D3, A2, B2, C2, D2, A1, B1, C1, D1
Threshold 8	LED	A4, B4, C4, D4, A3, B3, C3, D3, A2, B2, C2, D2, A1, B1, C1, D1

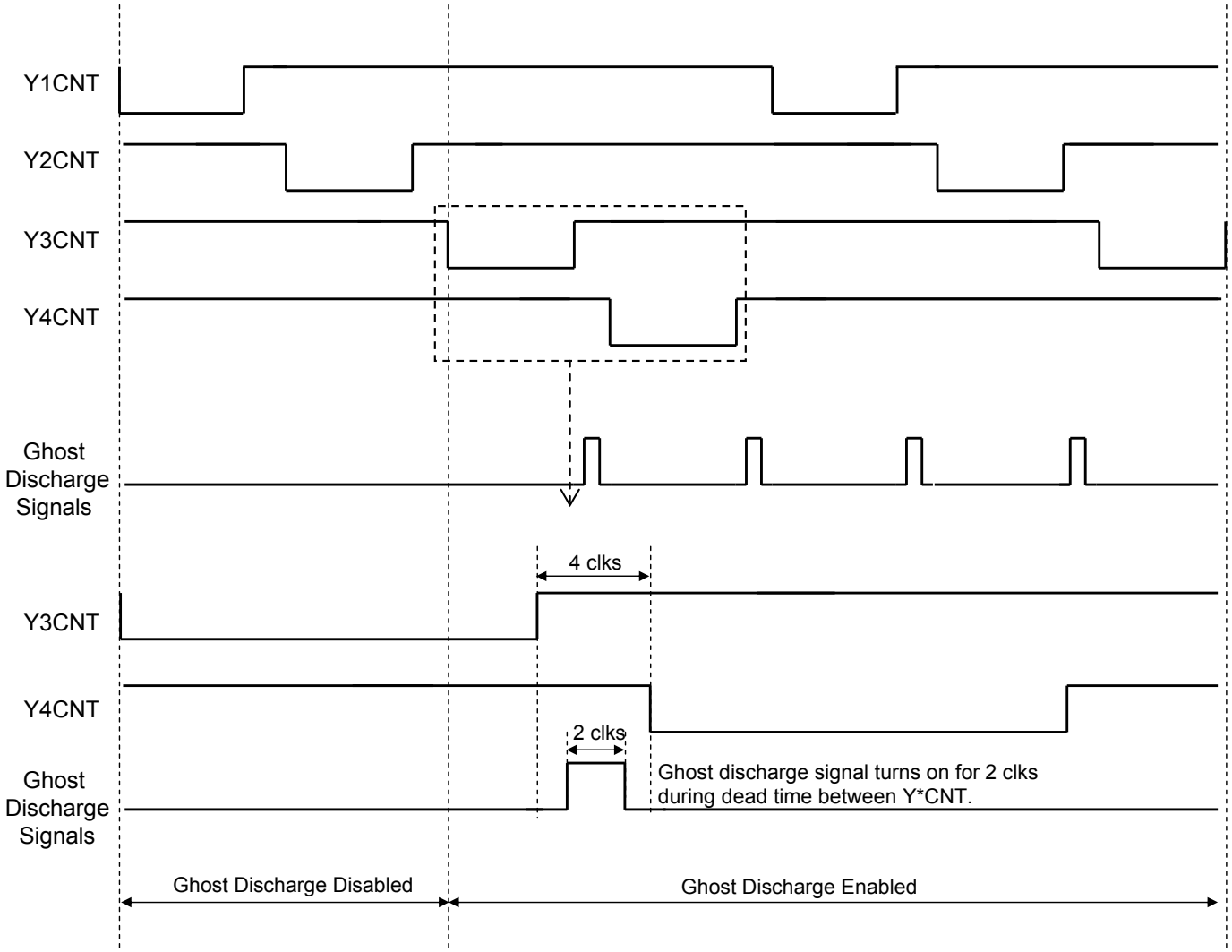
Note : During Bar Meter mode, auto threshold detection should be used. This LSI does not support Bar Meter Mode with fixed threshold setting. It is also recommended not to use other modes together with Bar Meter Mode.

OPERATION (continued)

9. Ghost Image Prevention Function

Ghost images sometimes appear during LED matrix mode operation. Very dim light can appear in some LED even during OFF condition. This is called Ghost Image. In this LSI, Ghost Image Prevention Function is included to prevent Ghost Image. Ghost Image Prevention Function can be enabled through register ZPDEN (register 04h).

• Ghost Image Prevention may not remove the ghost image perfectly. It depends on the LED color combination and LED connection method.



During normal operation, ghost discharge signal will be always low. When ghost image prevention function is enabled through register 04h, ghost discharge signal will turn on for 2 clks cycle during 4 clks dead time between each YCNT. During on period of 2 clks cycle, output Z pin will be forced to half of VCC.

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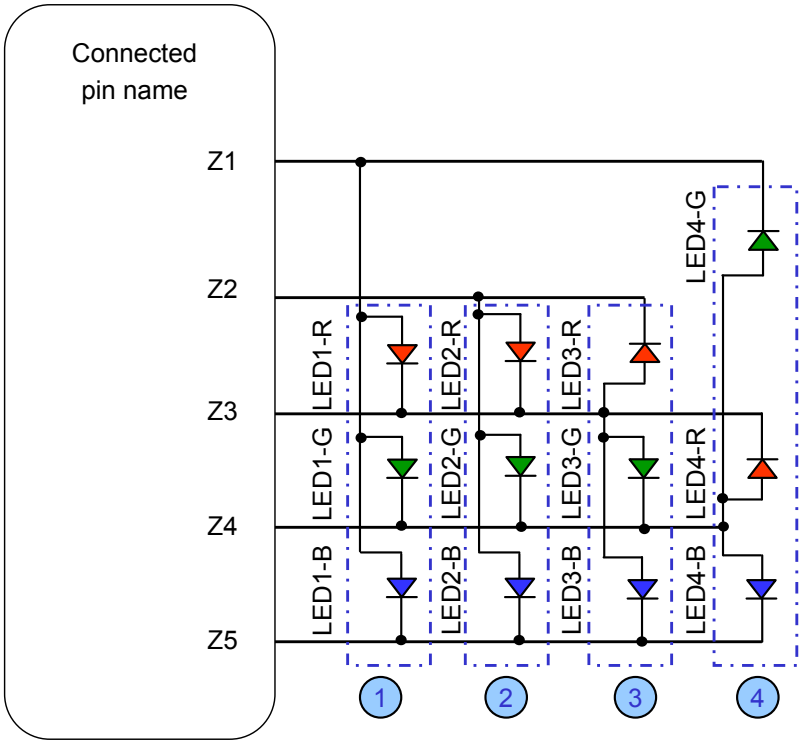
OPERATION (continued)

9. Ghost Image Prevention Function (continued)

To minimize ghost image, it is recommended to use LED with same forward voltage drop in LED panel. If user wants to use LED with different forward voltage drop in LED panel (e.g. RGB LED in LED panel), it is recommended that all the cathodes of LED connected to the same pin must have same forward voltage drop. (i.e. same colour LED sharing the same cathode). A recommended RGB LED connection to minimize ghost image is shown in diagram below.



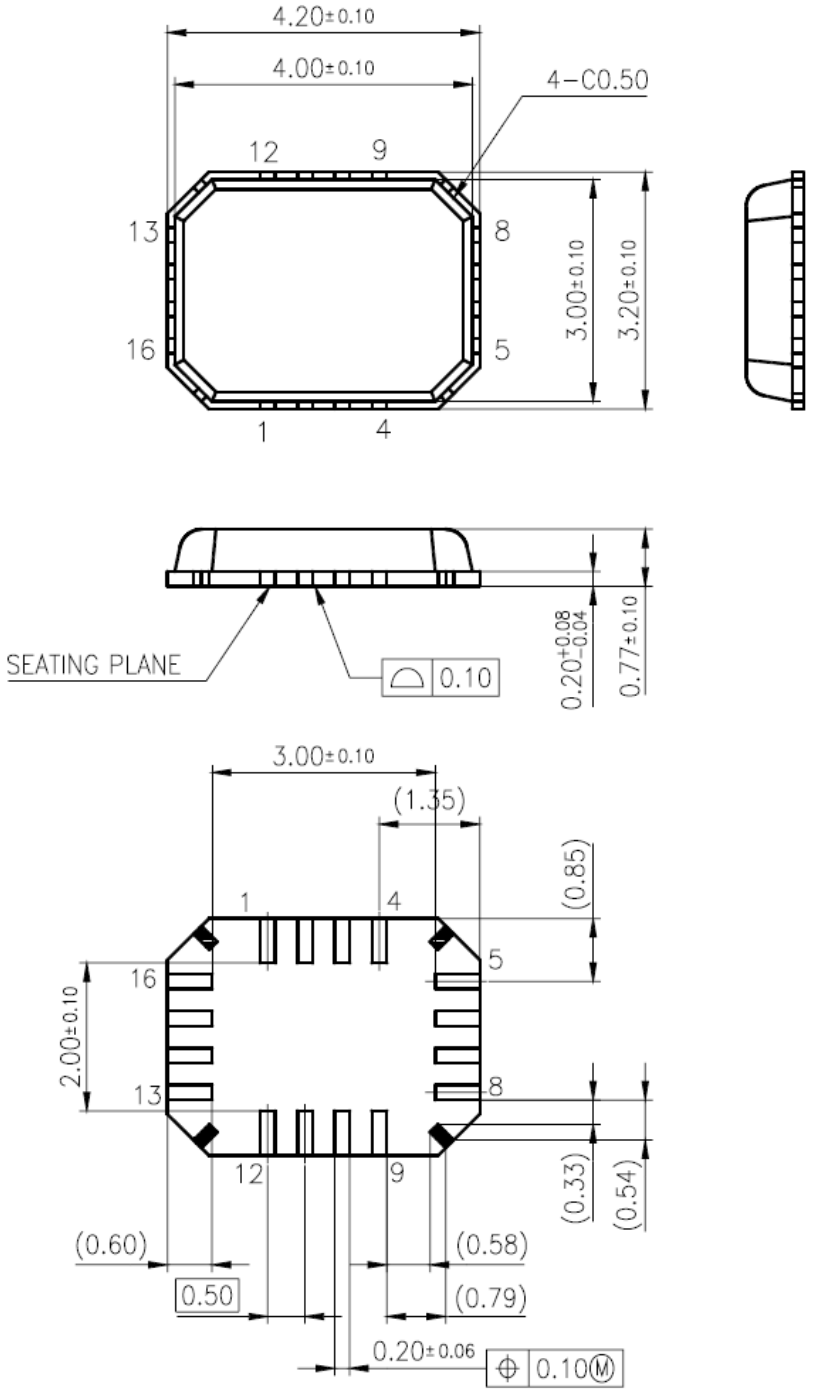
Example of RGB LED connection

Established : 2011-07-29
Revised : 2013-03-22

PACKAGE INFORMATION (Reference Data)

Package Code : ＊QFN016-P-0304C

Unit:mm



Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	Pd Plating

Established : 2011-07-29
Revised : 2013-03-22

IMPORTANT NOTICE

1. When using the LSI for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this LSI, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This LSI is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the LSI being used for any special application, unless our company agrees to the use of such special application.
4. This LSI is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the LSI being used in automotive application, unless our company agrees to such application in this book.
5. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our LSI being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
9. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply..
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.

Established : 2011-07-29
Revised : 2013-03-22

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com