TPD4E1U06 Quad-Channel, High-Speed ESD Protection Device

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±15 kV Contact Discharge
  - ±15 kV Air-Gap Discharge
- IO Capacitance 0.8 pF (Typical)
- DC Breakdown Voltage 6.5 V (Minimum)
- Ultra Low Leakage Current 10 nA (Maximum)
- Low ESD Clamping Voltage
- Industrial Temperature Range: –40°C to 125°C
- Small, Easy-to-Route DCK, and DBV Package

2 Applications

- USB 2.0
- Ethernet
- HDMI Control Lines
- MIPI Bus
- LVDS
- SATA

3 Description

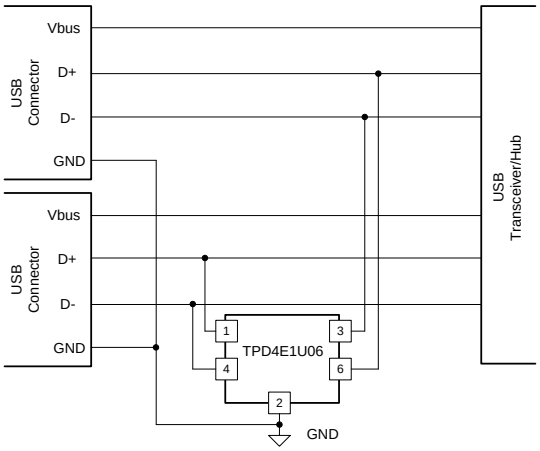
The TPD4E1U06 is a quad channel unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode with ultra low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. Its 0.8-pF line capacitance makes it suitable for a wide range of applications. Typical application areas include HDMI, USB2.0, MHL, and DisplayPort.

Device Information(1)

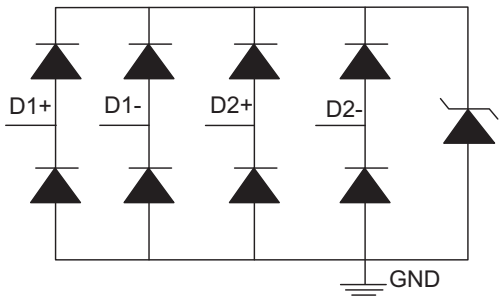
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E1U06	SOT (6)	2.00 mm × 1.25 mm
		2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Circuit Schematic Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

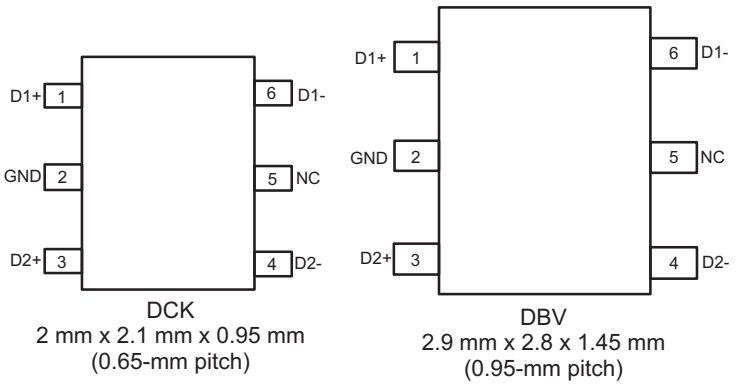
Changes from Revision B (February 2013) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (December 2012) to Revision B — **Page**

- Added C_{CROSS} data for DBV package ... 5

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION	USAGE
NAME	NO.			
D1+	1	I/O	ESD protected channel	Connect to data line as close to the connector as possible
D1–	6	I/O		
D2–	4	I/O		
D2+	3	I/O		
NC	5	I/O	No connect	Can be left floating, grounded, or connected to VCC
GND	2	GND	Ground	Connect to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Operating temperature range	–40	125	°C
I_{PP}, peak pulse current (tp = 8/20 µs)		3	A
P_{PP}, peak pulse power (tp = 8/20 µs)		45	W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	115	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	–4	4	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	–1.5	1.5	
		IEC 61000-4-2 contact ESD	–15	15	kV
		IEC 61000-4-2 air-gap ESD	–15	15	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	5.5	V
T_A	Operating free-air temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPD4E1U06		UNIT
		DBV	DCK	
		6 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.3	274.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	166.1	113.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	68.4	76.7	
ψ_{JT}	Junction-to-top characterization parameter	57.3	3.6	
ψ_{JB}	Junction-to-board characterization parameter	67.9	75.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} = 10 µA				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, tp = 8/20 µs, from I/O to GND(1)			11		V
		I_{PP} = 3A, tp = 8/20 µs, from I/O to GND(1)			15		V
R_{DYN}	Dynamic resistance	Pin x to GND Pin(2)			1.0		Ω
		GND to Pin x			0.6		
C_L	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V, 25 °C			0.8	1	pF
C_{CROSS}	Channel to channel input capacitance	Pin 2 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins	DCK package		0.006	0.015	pF
			DBV package		0.01	0.025	
$\Delta C_{IO-TO-GND}$	Variation of channel input capacitance	Pin 2 = 0V , f = 1 MHz, V_{BIAS} = 2.5 V, channel_x pin to gnd – channel_y pin to gnd			0.025	0.07	pF
V_{BR}	Break-down voltage, IO to GND	I_{IO} = 1 mA		6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V			1	10	nA

(1) Non-repetitive current pulse 8/20 us exponentially decaying waveform according to IEC61000-4-5
(2) Extraction of RDYN using least squares fit of TLP characteristics between I=10A and I=20A

6.6 Typical Characteristics

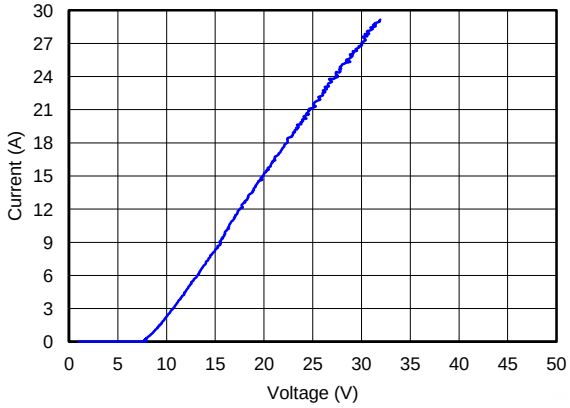


Figure 1. TLP, Data to GND

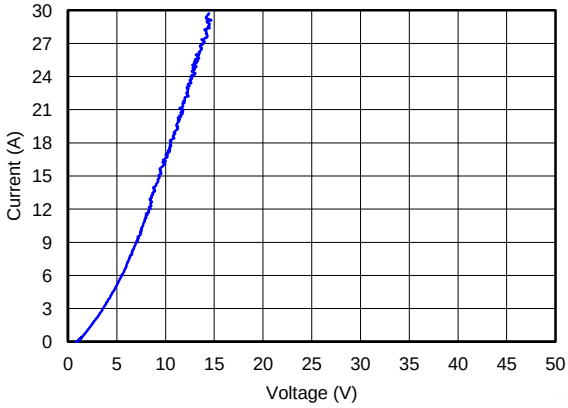


Figure 2. TLP, GND to Data

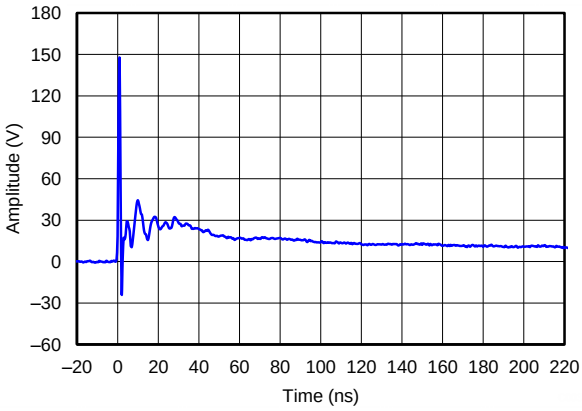


Figure 3. IEC 61000-4-2 Clamping Voltage, +8kV Contact

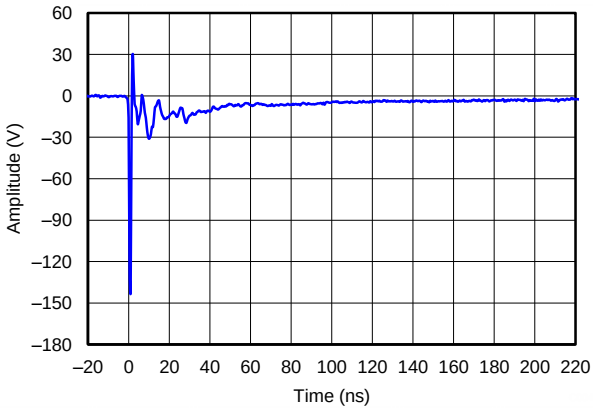


Figure 4. IEC 61000-4-2 Clamping Voltage, –8kV Contact

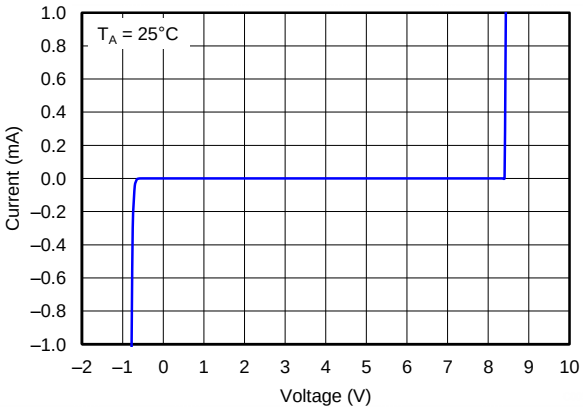


Figure 5. Diode Curve

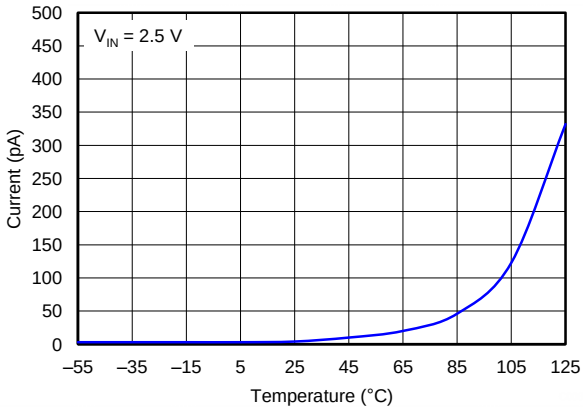


Figure 6. I_{LEAK} vs. Temperature

Typical Characteristics (continued)

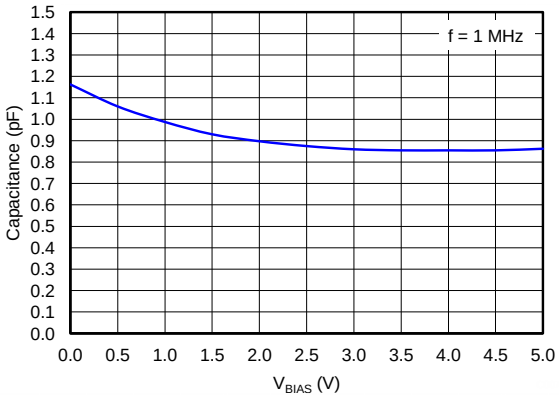


Figure 7. Capacitance Across V_{BIAS}

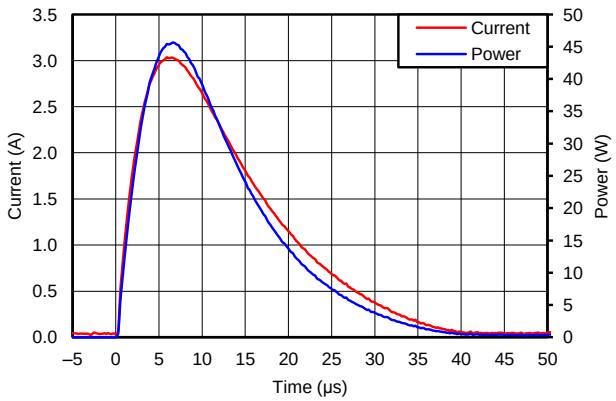


Figure 8. Surge Curve (tp = 8/20 µs), Pin IO to GND

7 Detailed Description

7.1 Overview

The TPD4E1U06 is a quad channel unidirectional TVS ESD protection diode with ultra low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. Typical application areas include HDMI, USB2.0, MHL, and DisplayPort. Its 0.8-pF line capacitance makes it suitable for a wide range of applications.

7.2 Functional Block Diagram

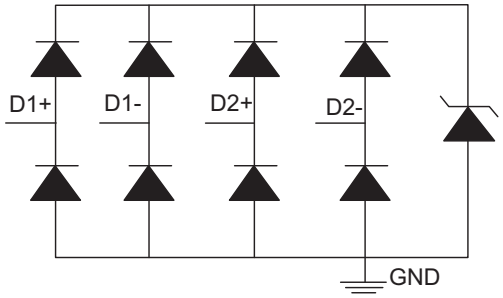


Figure 9. Circuit Schematic Diagram

7.3 Feature Description

7.3.1 IEC 61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±15-kV contact and air. An ESD/surge clamp diverts the current to ground.

7.3.2 IO Capacitance

The capacitance between each I/O pin to ground is 0.8 pF.

7.3.3 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

7.3.4 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Max) with a bias of 2.5 V.

7.3.5 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 11 V (I_{PP} = 1 A).

7.3.6 Industrial Temperature Range

This device features an industrial operating range of –40°C to 125°C.

7.3.7 Small, Easy-to-route Packages

The layout of this device makes it simple to add protection to the design. Industry standard packages allow for easy additions to the board and easy layout.

7.4 Device Functional Modes

TPD4E1U06 is a passive integrated circuit that triggers when voltages are above V_{BR} or below the forward diode drop. During ESD events, voltages as high as ±15 kV can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E1U06 (usually within 10's of nano-seconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD4E1U06 is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

For this design example, one TPD4E1U06 device is being used in a dual USB 2.0 application. This will provide a complete port protection scheme.

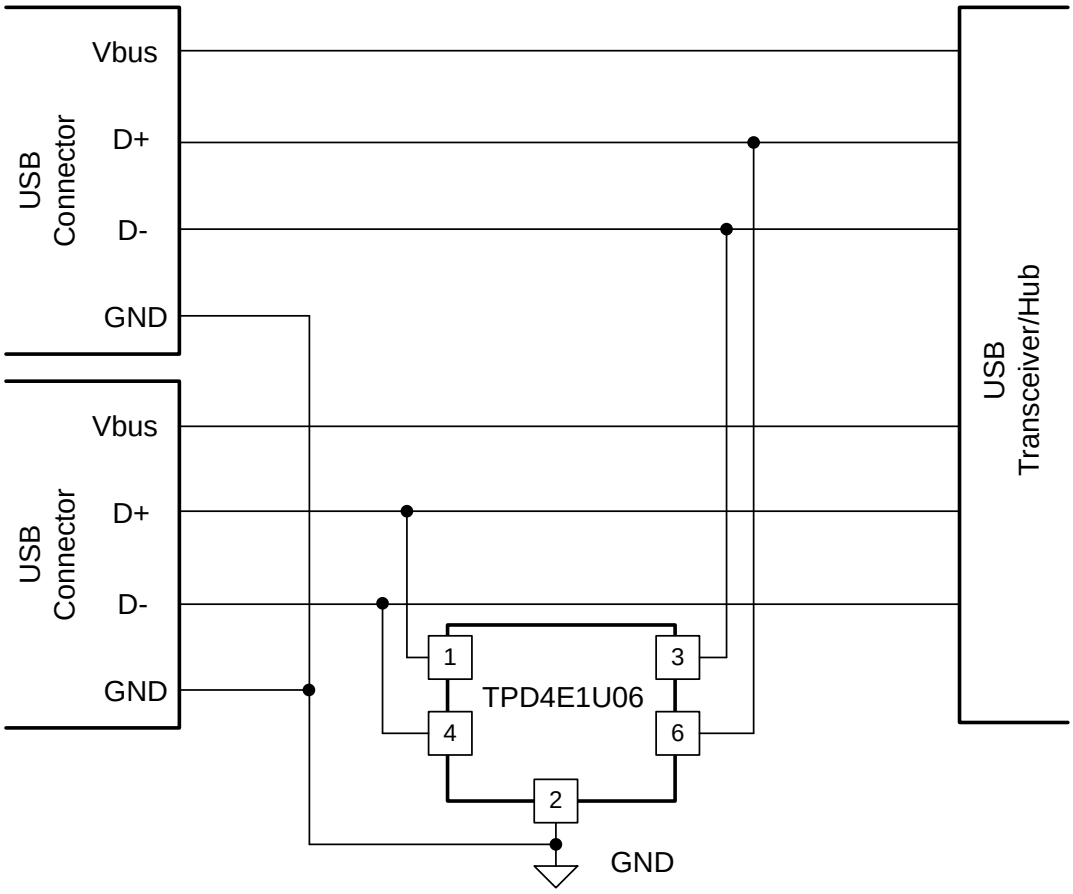


Figure 10. Dual USB 2.0 Application

Typical Application (continued)

8.2.1 Design Requirements

Given the USB 2.0 application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on Pins 1, 3, 4, or 6	0 V to 5 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range on Pins 1, 3, 4, or 6

TPD4E1U06 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels will protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

8.2.2.2 Operating Frequency

The TPD4E1U06 has a capacitance of 0.8 pF (typical), supporting USB 2.0 data rates.

8.2.3 Application Curve

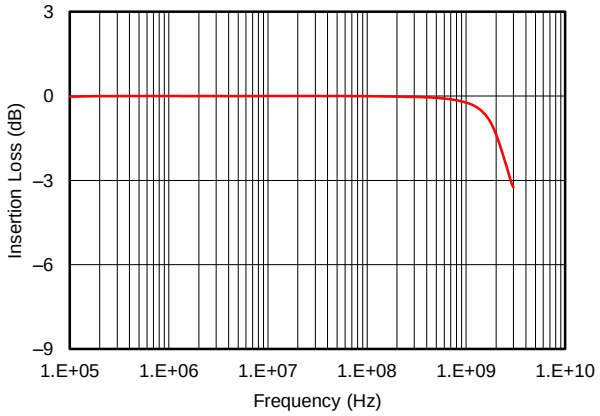


Figure 11. Insertion Loss Graph

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (0 to 5.5 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

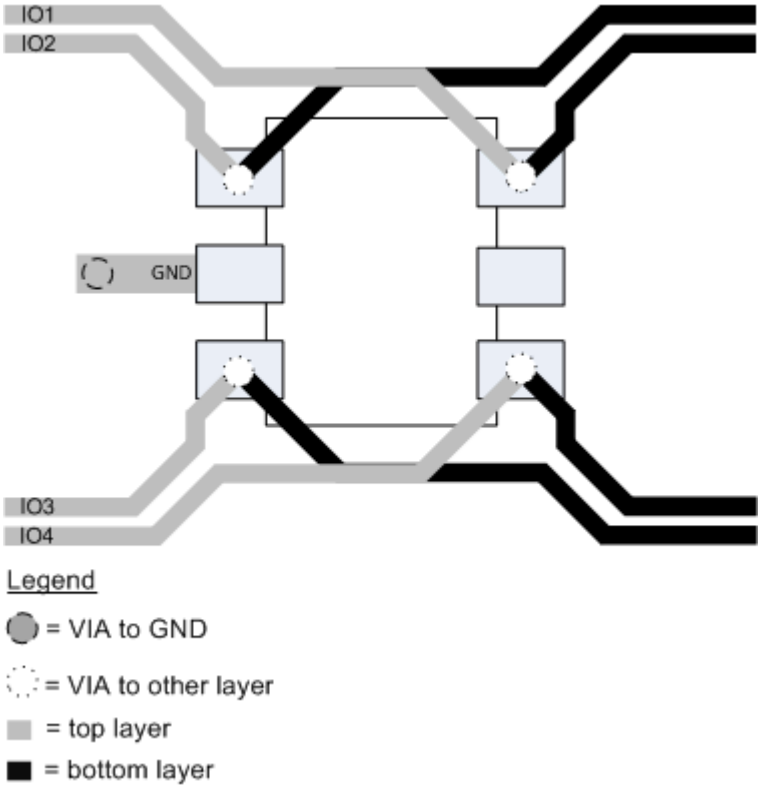


Figure 12. PCB Layout Recommendation

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E1U06DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	NG4	Samples
TPD4E1U06DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BP6 ~ BP8 ~ BPI)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

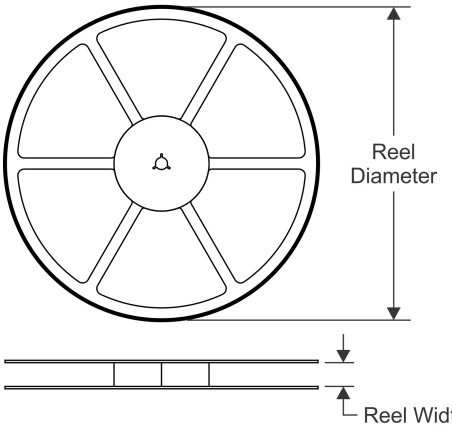
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

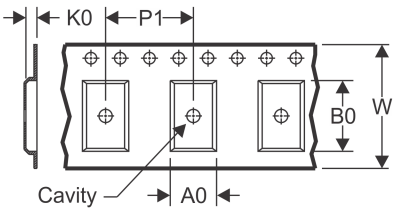
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

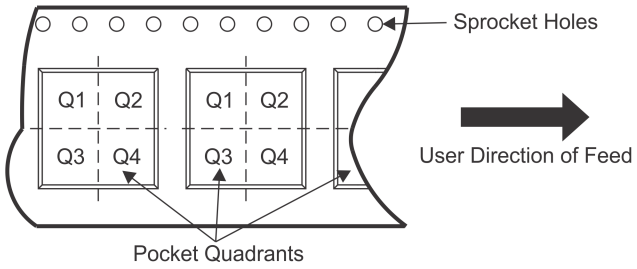


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

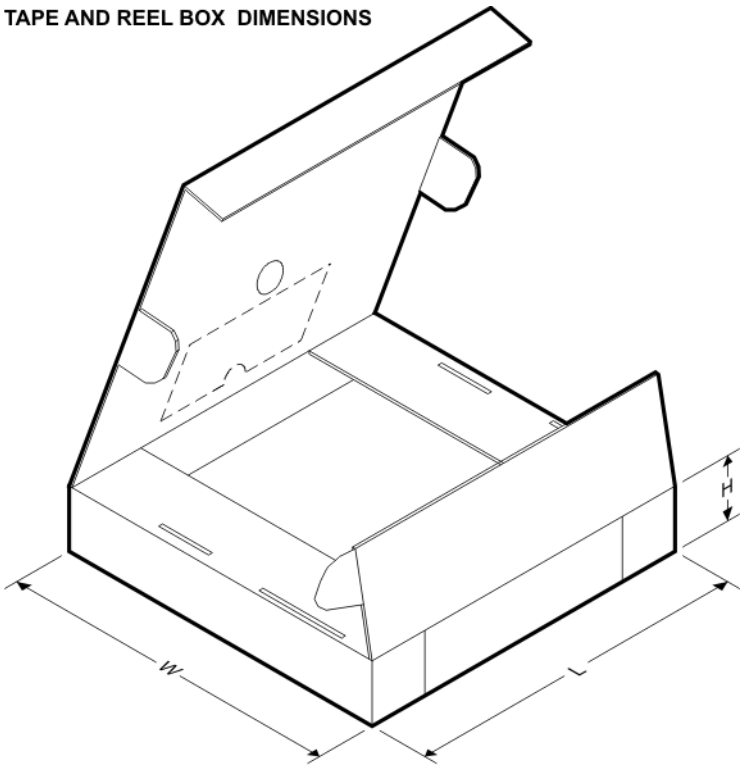
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E1U06DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

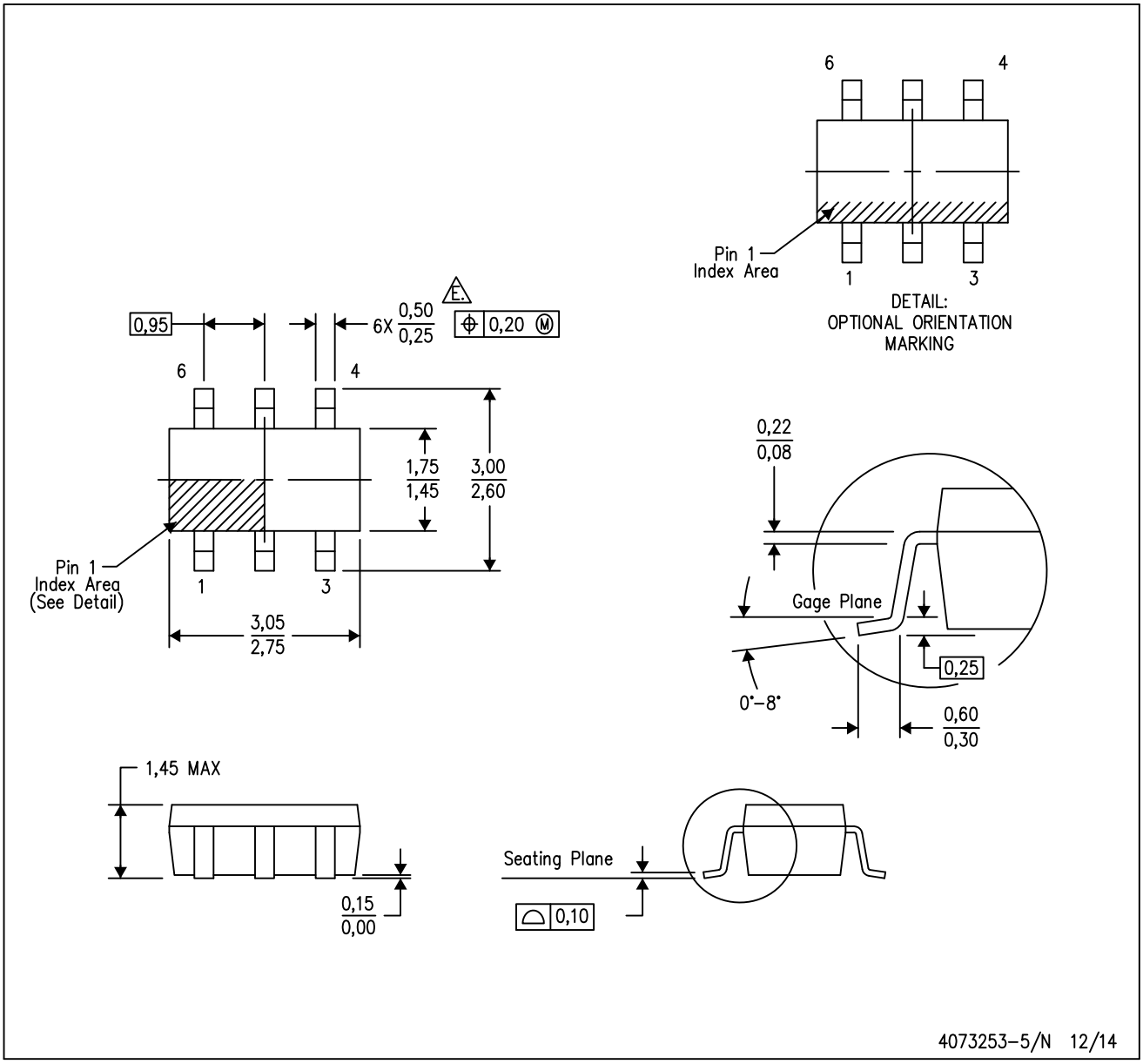
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

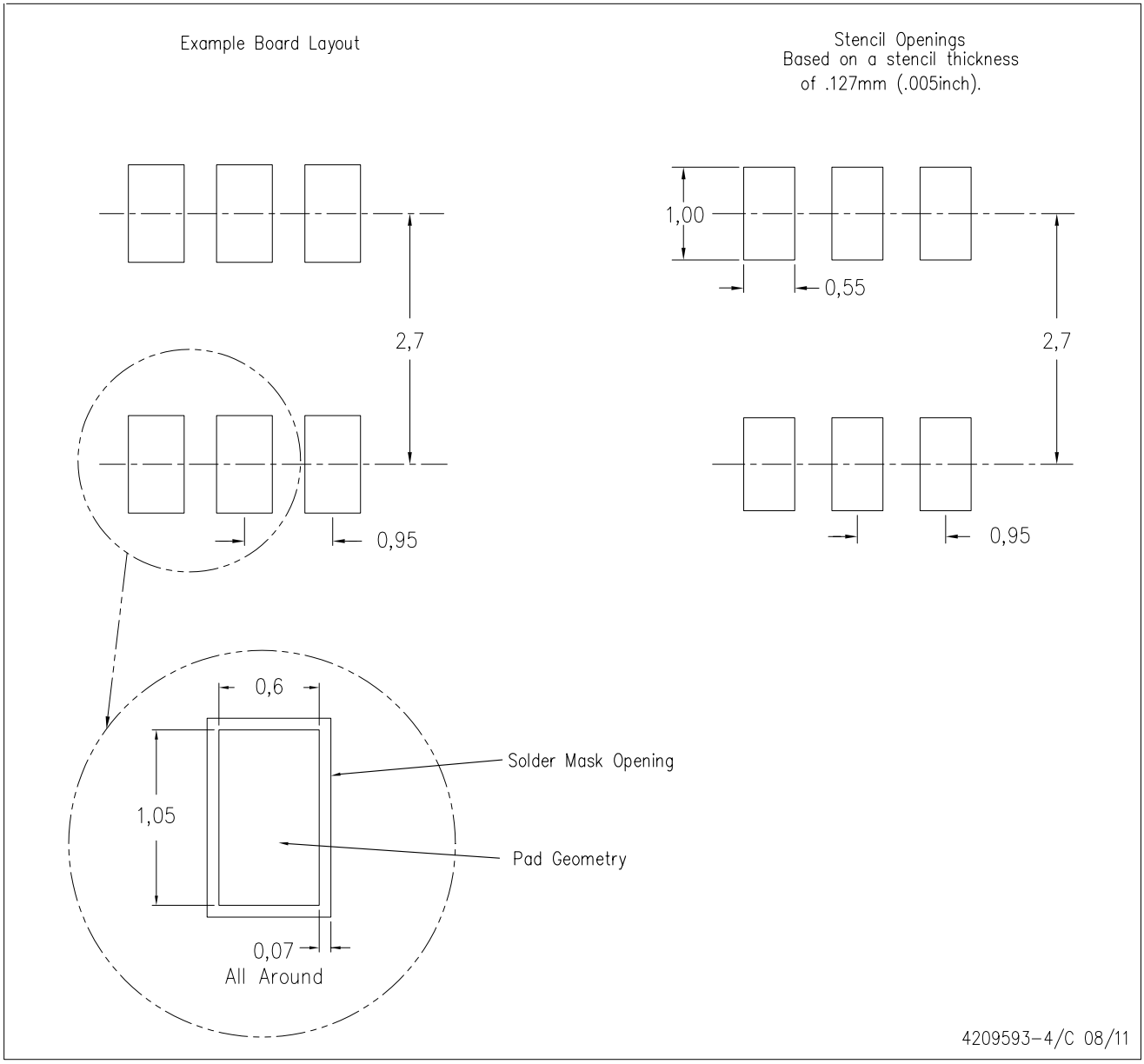
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E1U06DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



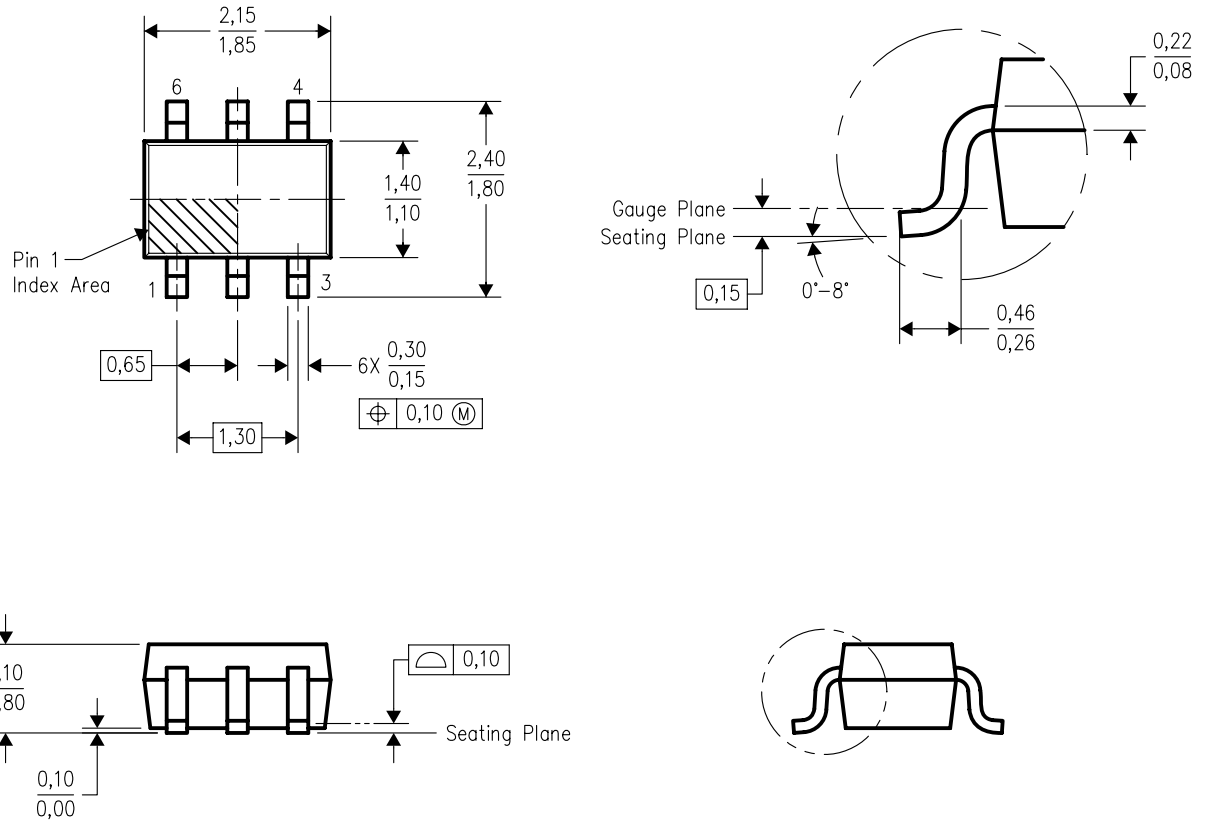
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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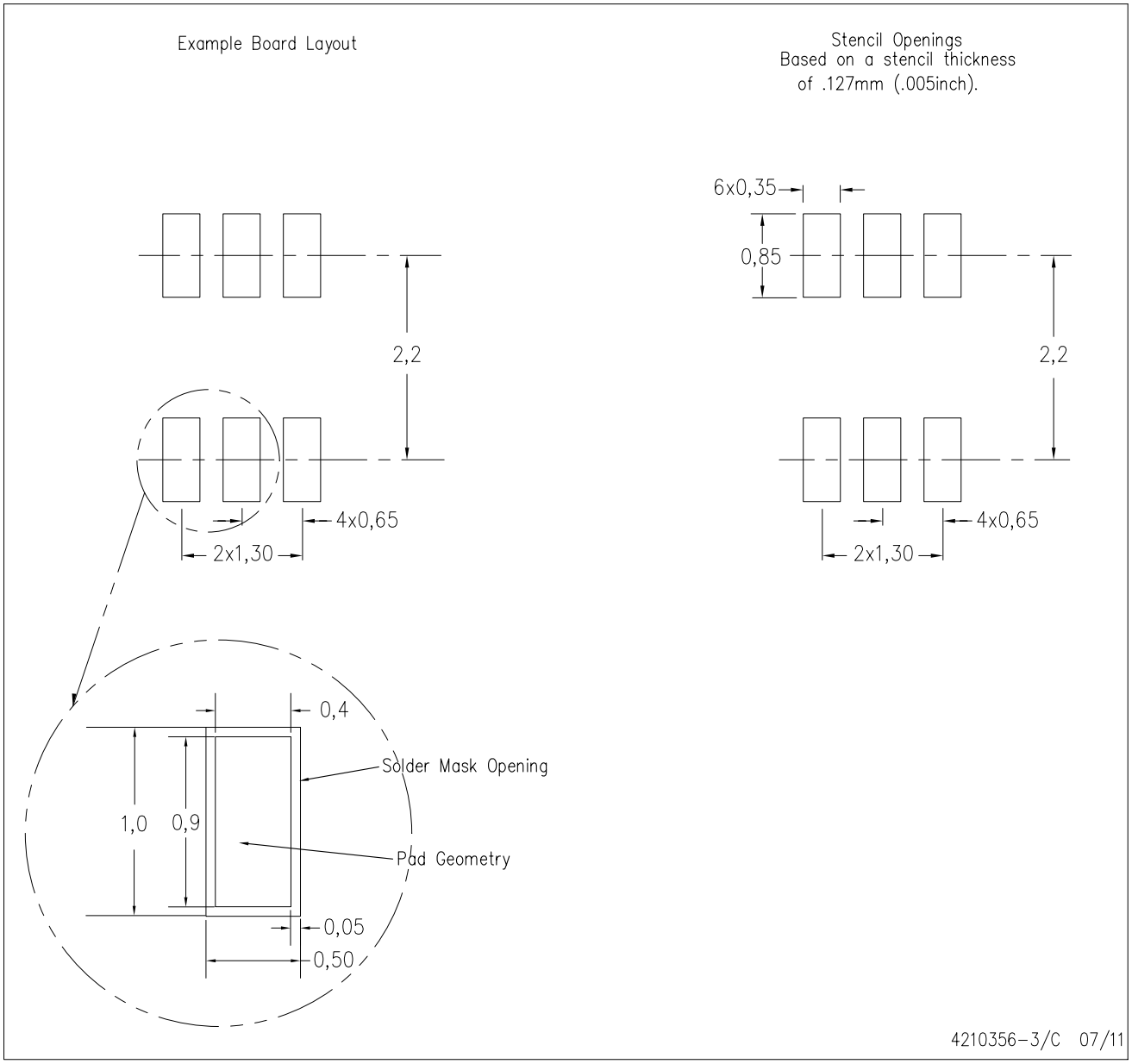
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



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E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE

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