

DATA SHEET

74ABT162245A

74ABTH162245A

16-Bit bus transceiver with 30Ω series
termination resistors (3-State)

Product specification
Supersedes data of 1996 Nov 20
IC23 Data Handbook

1998 Feb 25

16-bit bus transceiver with 30Ω series termination resistors (3-State)

74ABT162245A
74ABTH162245A

FEATURES

- 16-bit bidirectional bus interface
- Power-up 3-State
- Multiple V_{CC} and GND pins minimize switching noise
- 3-State buffers
- Output capability: +12mA/−32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same part as 74ABT16245A-1
- 74ABTH162245A incorporates bus hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT162245A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT162245A device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two Output Enable ($1\overline{OE}$, $2\overline{OE}$) inputs for easy cascading and two Direction ($1DIR$, $2DIR$) inputs for direction control.

The 74ABT162245A is designed with 30 ohm series resistance in both the upper and lower output structures on both A and B ports. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receiver/transmitters.

The 74ABT162245A is the same as the 74ABT16245A-1. The part number has been changed to reflect industry standards

Two options are available, 74ABT162245A which does not have the bus hold feature and the 74ABTH162245A which incorporates the bus hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	$C_L = 50\text{pF}$; $V_{CC} = 5\text{V}$	2.0 3.0	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	3	pF
$C_{I/O}$	I/O pin capacitance	$V_O = 0\text{V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	300	nA
I_{CCL}		Outputs Low; $V_{CC} = 5.5\text{V}$	10	mA

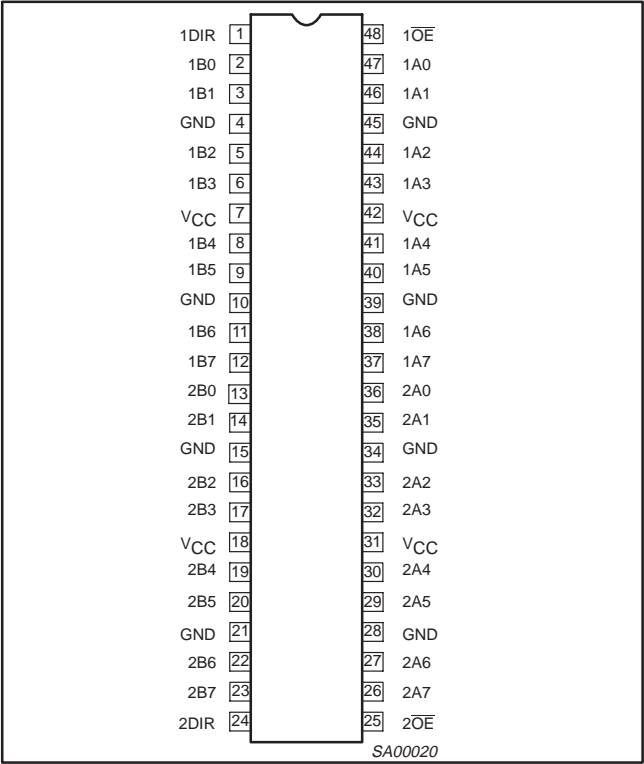
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	−40°C to +85°C	74ABT162245A DL	BT162245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABT162245A DGG	BT162245A DGG	SOT362-1
48-Pin Plastic SSOP Type III	−40°C to +85°C	74ABTH162245A DL	BH162245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74ABTH162245A DGG	BH162245A DGG	SOT362-1

16-bit bus transceiver with 30Ω series termination resistors (3-State)

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74ABTH162245A

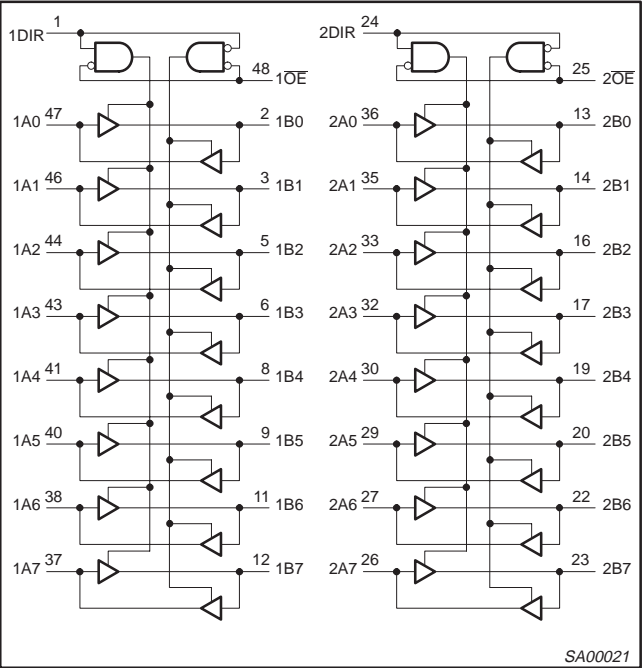
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
1DIR, 2DIR	1, 24	Direction control inputs (Active-High)
1A0 – 1A7, 2A0 – 2A7	47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	Data inputs/outputs (A side)
1B0 – 1B7, 2B0 – 2B7	2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	Data inputs/outputs (B side)
1OE, 2OE	48, 25	Output enables
GND	4, 10, 15, 21, 28, 34, 39, 45	Ground (0V)
VCC	7, 18, 31, 42	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

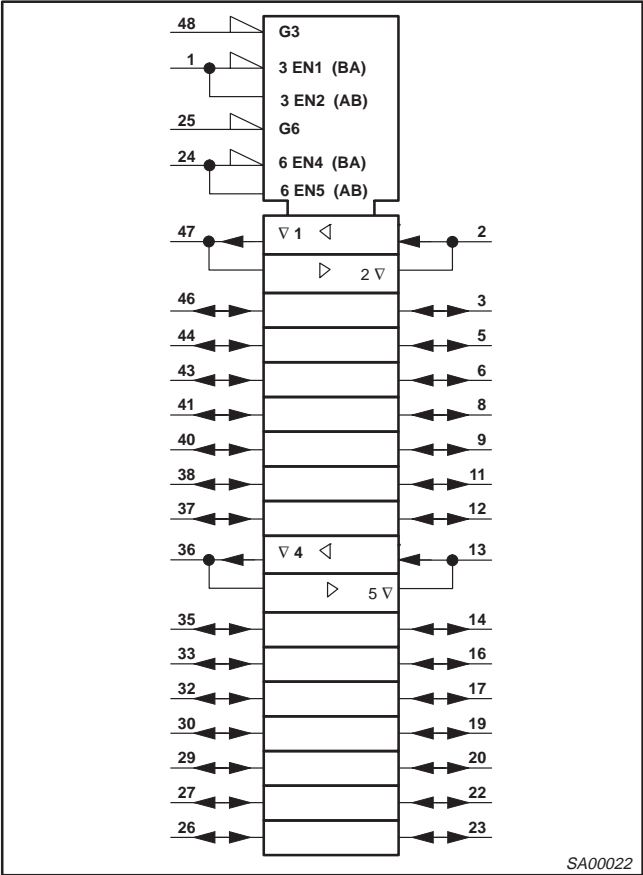
INPUTS		INPUTS/OUTPUTS	
nOE	nDIR	nAx	nBx
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = D0n't care
Z = High impedance "off" state

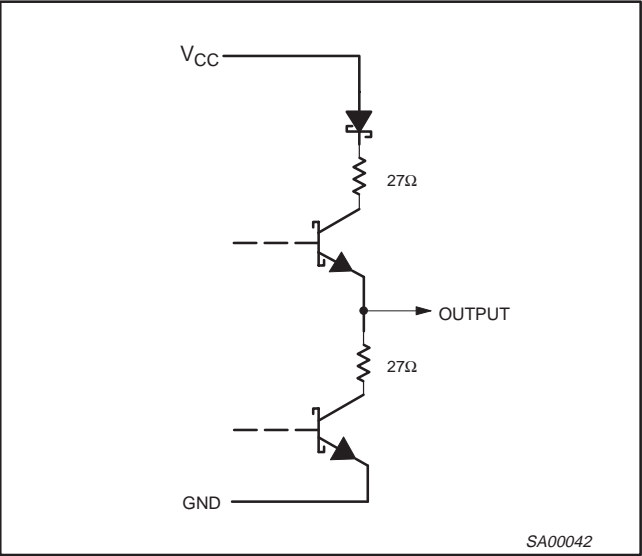
16-bit bus transceiver with 30Ω series termination resistors (3-State)

74ABT162245A
74ABTH162245A

LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC OF EACH OUTPUT



16-bit bus transceiver with 30Ω series termination resistors (3-State)

74ABT162245A
74ABTH162245A

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage ³		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

16-bit bus transceiver with 30Ω series termination resistors (3-State)

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
				Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = −18mA			−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}		2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}		3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}		2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 8mA; V _I = V _{IL} or V _{IH}			0.46	0.65		0.65	V
	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 12mA; V _I = V _{IL} or V _{IH}			0.50	0.80		0.80	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V	Control pins		±0.01	±1.0		±1.0	μA
I _{HOLD}	Bus hold current A and B inputs ⁴ 74ABTH162245A	V _{CC} = 4.5V; V _I = 0.8V		50			50		μA
		V _{CC} = 5.5V; V _I = 2.0V		−75			−75		
		V _{CC} = 5.5V; V _I = 0 to 5.5V		±500					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V			±5.0	±100		±100	μA
I _{PU} /I _{PD}	Power-up/down 3-State output current ³	V _{CC} = 2.0V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care			±5.0	±50		±50	μA
I _{IH} +I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 5.5V; V _I = V _{IL} or V _{IH}			0.5	10		10	μA
I _{IL} +I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.0V; V _I = V _{IL} or V _{IH}			−0.5	−10		−10	μA
I _{CEX}	Output high leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}			5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V		−50	−92	−180	−50	−180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}			0.3	0.70		0.70	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}			10	19		19	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}			0.3	0.70		0.70	mA
ΔI _{CC}	Additional supply current per input pin ²	Outputs enabled, one data input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V			400	700		700	μA
		Outputs 3-State, one data input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V 74ABT162245A			1.0	50		50	μA
		Outputs 3-State, one data input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V 74ABTH162245A			100	250		250	μA
		Control pins, outputs disabled, one enable input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V			400	700		700	μA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5 ±10% a transition time of up to 100 μsec is permitted.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

16-bit bus transceiver with 30Ω series termination resistors (3-State)

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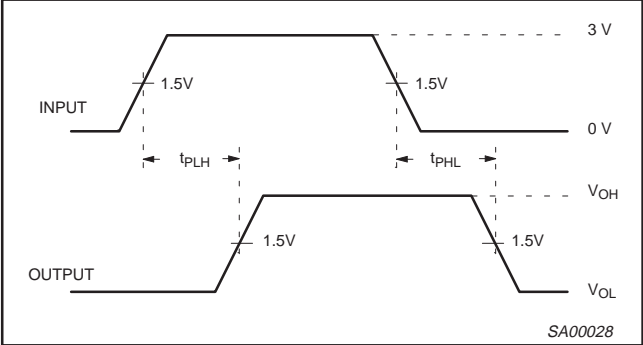
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

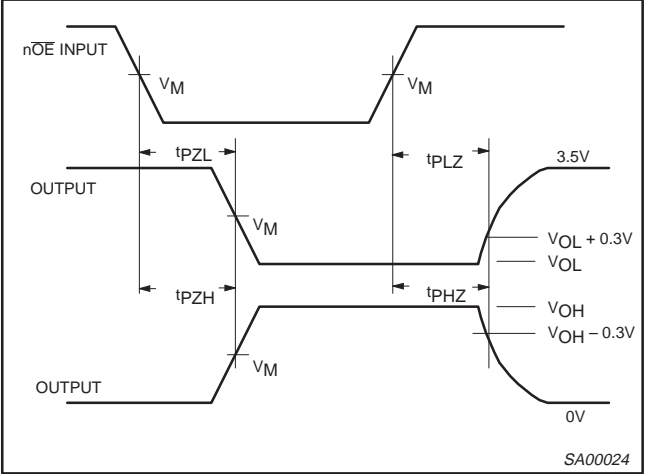
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40°C to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.0 1.5	2.0 3.0	3.3 4.5	1.0 1.5	3.5 4.9	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 2.0	3.1 5.0	4.3 6.1	1.5 2.0	5.0 7.0	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.7 1.5	3.5 3.2	4.8 4.5	1.7 1.5	5.4 4.9	ns

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Input to Output Propagation Delays

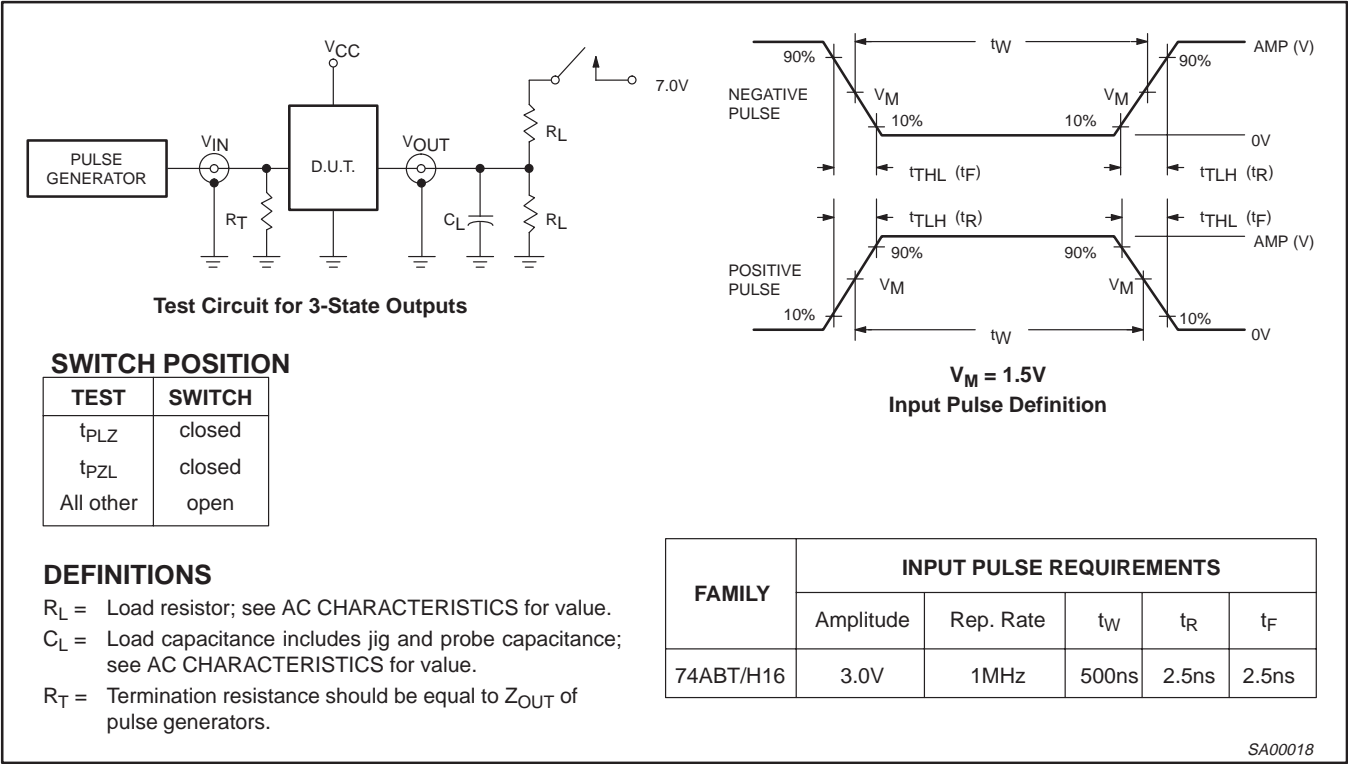


Waveform 2. 3-State Output Enable and Disable Times

16-bit bus transceiver with 30Ω series termination resistors (3-State)

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TEST CIRCUIT AND WAVEFORMS

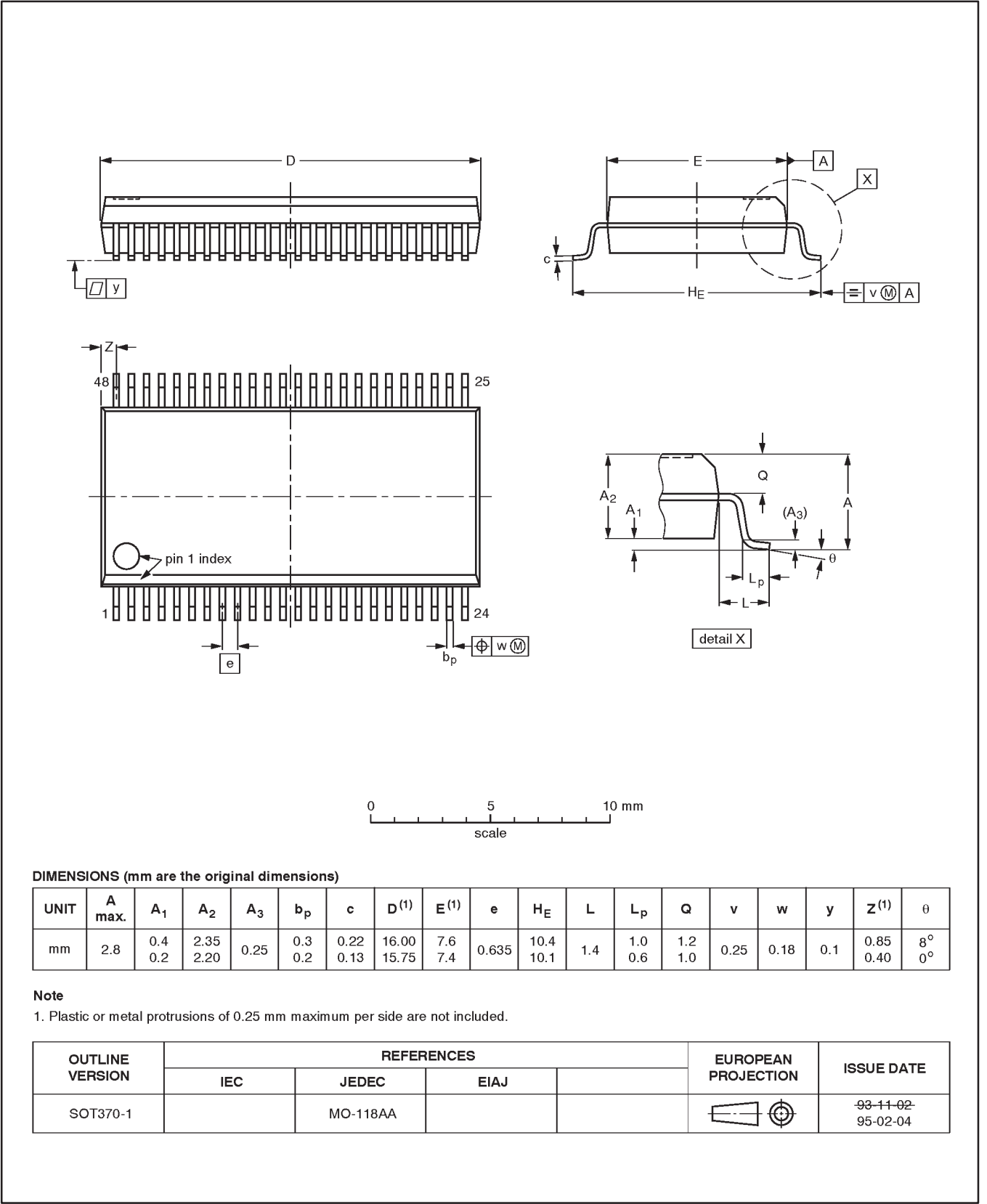


16-Bit bus transceiver with 30Ω series termination resistors (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



74ABT162245A
74ABTH162245A

SOT362-1



16-Bit bus transceiver with 30 Ω series termination
resistors (3-State)

74ABT162245A
74ABTH162245A

NOTES

16-Bit bus transceiver with 30Ω series termination resistors (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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