

# 74LVT574, 74LVTH574

## Low Voltage Octal D-Type Flip-Flop with 3-STATE Outputs

### Features

- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH574), also available without bushold feature (74LVT574)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink  $-32\text{mA}/+64\text{mA}$
- Functionally compatible with the 74 series 574
- Latch-up performance exceeds 500mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V

### General Description

The LVT574 and LVTH574 are high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops.

The LVTH574 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal flip-flops are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT574 and LVTH574 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

### Ordering Information

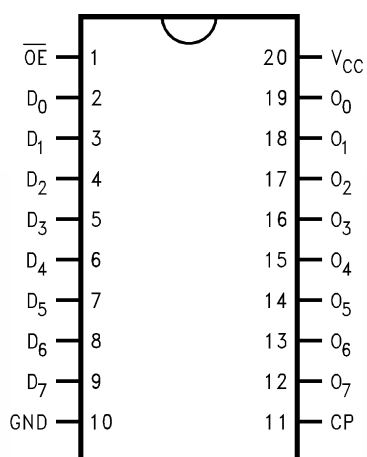
Order Number	Package Number	Package Description
74LVT574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVT574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVT574MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LVT574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH574MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LVTH574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagram



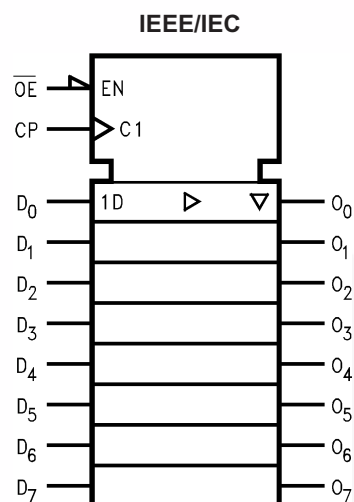
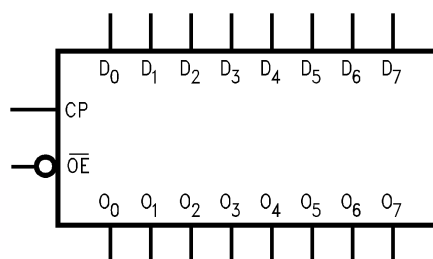
## Pin Description

Pin Names	Description
D <sub>0</sub> –D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O <sub>0</sub> –O <sub>7</sub>	3-STATE Outputs

## Functional Description

The LVT574 and LVTH574 consist of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Logic Symbols



## Truth Table

Inputs			Outputs
D <sub>n</sub>	CP	$\overline{OE}$	O <sub>n</sub>
H	↗	L	H
L	↗	L	L
X	L	L	O <sub>o</sub>
X	X	H	Z

H = HIGH Voltage Level

L = LOW Voltage Level

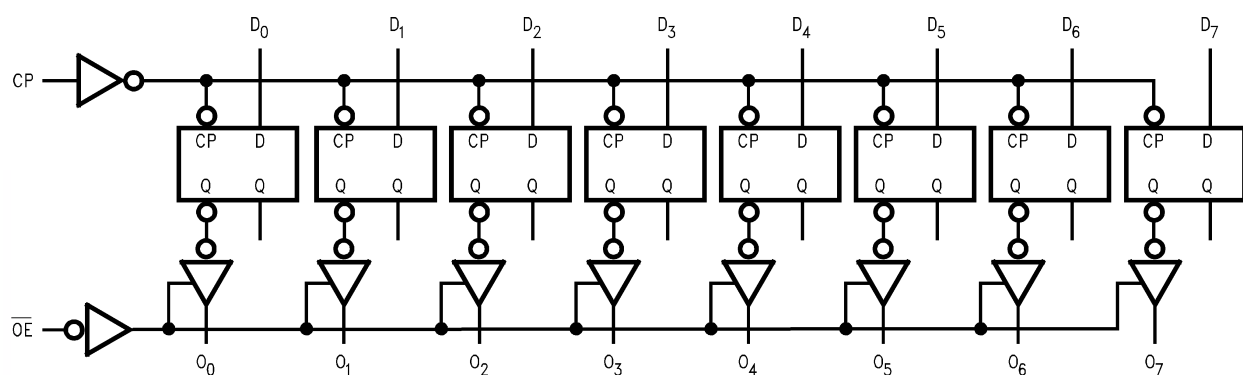
X = Immaterial

Z = High Impedance

↗ = LOW-to-HIGH Transition

O<sub>o</sub> = Previous O<sub>o</sub> before HIGH to LOW of CP

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	−0.5V to +4.6V
$V_I$	DC Input Voltage	−0.5V to +7.0V
$V_O$	DC Output Voltage Output in 3-STATE	−0.5V to +7.0V
	Output in HIGH or LOW State <sup>(1)</sup>	−0.5V to +7.0V
$I_{IK}$	DC Input Diode Current, $V_I < GND$	−50mA
$I_{OK}$	DC Output Diode Current, $V_O < GND$	−50mA
$I_O$	DC Output Current, $V_O > V_{CC}$ Output at HIGH State	64mA
	Output at LOW State	128mA
$I_{CC}$	DC Supply Current per Supply Pin	±64mA
$I_{GND}$	DC Ground Current per Ground Pin	±128mA
$T_{STG}$	Storage Temperature	−65°C to +150°C

### Note:

1.  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage	2.7	3.6	V
$V_I$	Input Voltage	0	5.5	V
$I_{OH}$	HIGH-Level Output Current		−32	mA
$I_{OL}$	LOW-Level Output Current		64	mA
$T_A$	Free-Air Operating Temperature	−40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = -40°C to +85°C			Units
				Min.	Typ. <sup>(2)</sup>	Max.	
V <sub>IK</sub>	Input Clamp Diode Voltage	2.7	I <sub>I</sub> = -18mA			-1.2	V
V <sub>IH</sub>	Input HIGH Voltage	2.7–3.6	V <sub>O</sub> ≤ 0.1V or	2.0			V
V <sub>IL</sub>	Input LOW Voltage	2.7–3.6	V <sub>O</sub> ≥ V <sub>CC</sub> - 0.1V			0.8	V
V <sub>OH</sub>	Output HIGH Voltage	2.7–3.6	I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2			V
		2.7	I <sub>OH</sub> = -8mA	2.4			
		3.0	I <sub>OH</sub> = -32mA	2.0			
V <sub>OL</sub>	Output LOW Voltage	2.7	I <sub>OL</sub> = 100μA			0.2	V
			I <sub>OL</sub> = 24mA			0.5	
		3.0	I <sub>OL</sub> = 16mA			0.4	
			I <sub>OL</sub> = 32mA			0.5	
			I <sub>OL</sub> = 64mA			0.55	
I <sub>I(HOLD)</sub> <sup>(3)</sup>	Bushold Input Minimum Drive	3.0	V <sub>I</sub> = 0.8V	75			μA
			V <sub>I</sub> = 2.0V	-75			
I <sub>I(OD)</sub> <sup>(3)</sup>	Bushold Input Over-Drive Current to Change State	3.0	<sup>(4)</sup>	500			μA
			<sup>(5)</sup>	-500			
I <sub>I</sub>	Input Current	3.6	V <sub>I</sub> = 5.5V			10	μA
		Control Pins	V <sub>I</sub> = 0V or V <sub>CC</sub>			±1	
		Data Pins	V <sub>I</sub> = 0V			-5	
			V <sub>I</sub> = V <sub>CC</sub>			1	
I <sub>OFF</sub>	Power Off Leakage Current	0	0V ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V			±100	μA
I <sub>PU/PD</sub>	Power up/down 3-STATE Output Current	0–1.5	V <sub>O</sub> = 0.5V to 3.0V, V <sub>I</sub> = GND or V <sub>CC</sub>			±100	μA
I <sub>OZL</sub>	3-STATE Output Leakage Current	3.6	V <sub>O</sub> = 0.5V			-5	μA
I <sub>OZH</sub>	3-STATE Output Leakage Current	3.6	V <sub>O</sub> = 3.0V			5	μA
I <sub>OZH</sub> <sup>+</sup>	3-STATE Output Leakage Current	3.6	V <sub>CC</sub> < V <sub>O</sub> ≤ 5.5V			10	μA
I <sub>CCH</sub>	Power Supply Current	3.6	Outputs HIGH			0.19	mA
I <sub>CCL</sub>	Power Supply Current	3.6	Outputs LOW			5	mA
I <sub>CCZ</sub>	Power Supply Current	3.6	Outputs Disabled			0.19	mA
I <sub>CCZ</sub> <sup>+</sup>	Power Supply Current	3.6	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled			0.19	mA
ΔI <sub>CC</sub>	Increase in Power Supply Current <sup>(6)</sup>	3.6	One Input at V <sub>CC</sub> - 0.6V, Other Inputs at V <sub>CC</sub> or GND			0.2	mA

## Notes:

2. All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

3. Applies to bushold versions only (74LVTH574).

4. An external driver must source at least the specified current to switch from LOW-to-HIGH.

5. An external driver must sink at least the specified current to switch from HIGH-to-LOW.

6. This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

**Dynamic Switching Characteristics<sup>(7)</sup>**

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C			Units
			C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	Min.	Typ.	Max.	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3	<sup>(8)</sup>		0.8		V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3	<sup>(8)</sup>		−0.8		V

**Notes:**

7. Characterized in SOIC package. Guaranteed parameter, but not tested.

8. Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output under test held LOW.

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = −40°C to +85°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω					Units
		V <sub>CC</sub> = 3.3V ± 0.3V			V <sub>CC</sub> = 2.7V		
		Min.	Typ. <sup>(9)</sup>	Max.	Min.	Max.	
f <sub>MAX</sub>	Maximum Clock Frequency	150			150		MHz
t <sub>PHL</sub>	Propagation Delay, CP to O <sub>n</sub>	1.8		4.6	1.8	5.3	ns
t <sub>PLH</sub>		1.8		4.5	1.8	5.3	
t <sub>PZL</sub>	Output Enable Time	1.5		5.2	1.5	6.1	ns
t <sub>PZH</sub>		1.5		4.8	1.5	5.9	
t <sub>PLZ</sub>	Output Disable Time	2.0		4.4	2.0	4.4	ns
t <sub>PHZ</sub>		2.0		4.8	2.0	5.1	
t <sub>S</sub>	Setup Time	2.0			2.4		ns
t <sub>H</sub>	Hold Time	0.3			0.0		ns
t <sub>W</sub>	Pulse Width	3.3			3.3		ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew <sup>(10)</sup>			1.0		1.0	ns

**Notes:**

9. All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

10. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Capacitance<sup>(11)</sup>**

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	4	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.0V, V <sub>O</sub> = 0V or V <sub>CC</sub>	6	pF

**Note:**

11. Capacitance is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

## Physical Dimensions

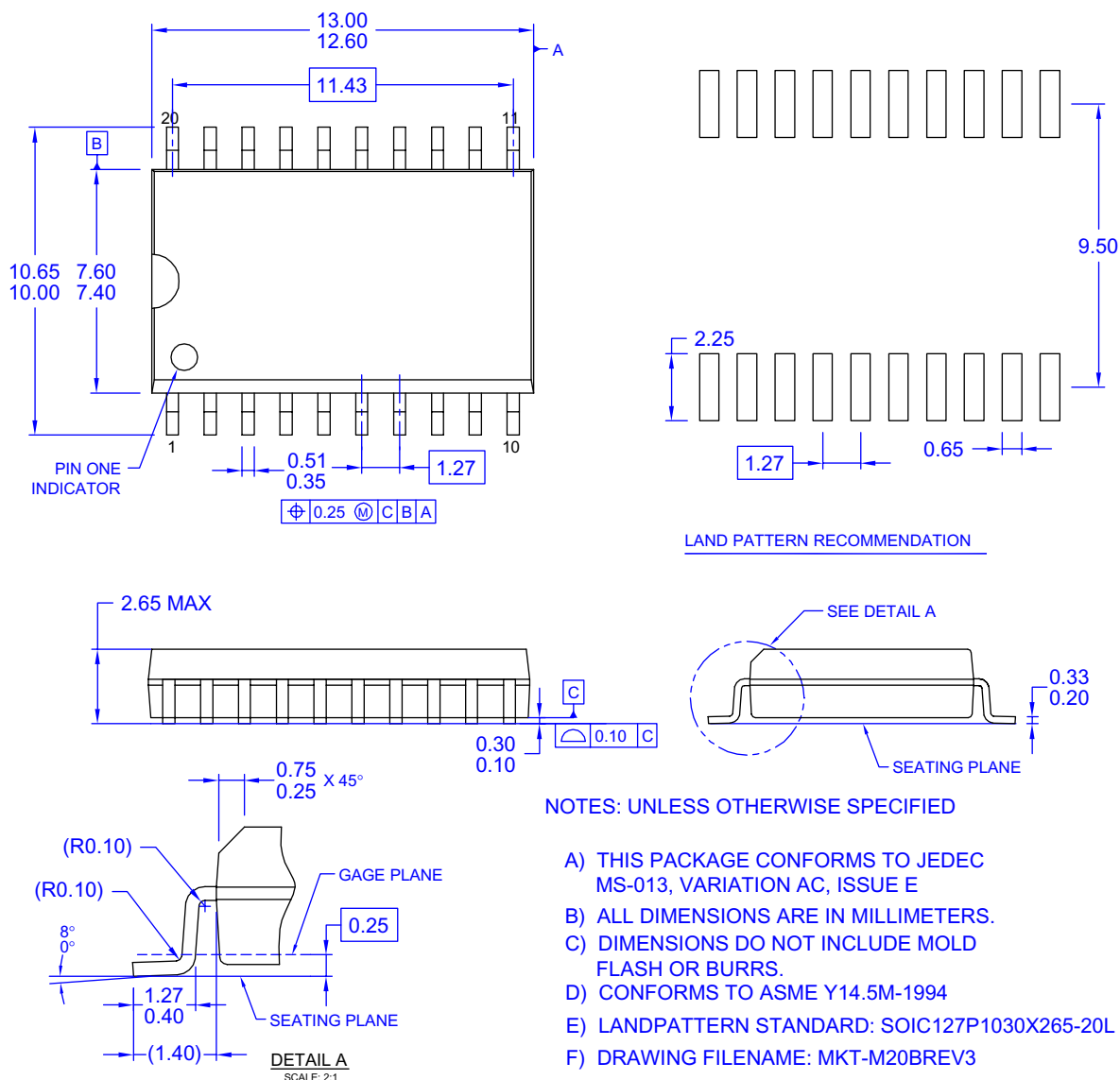


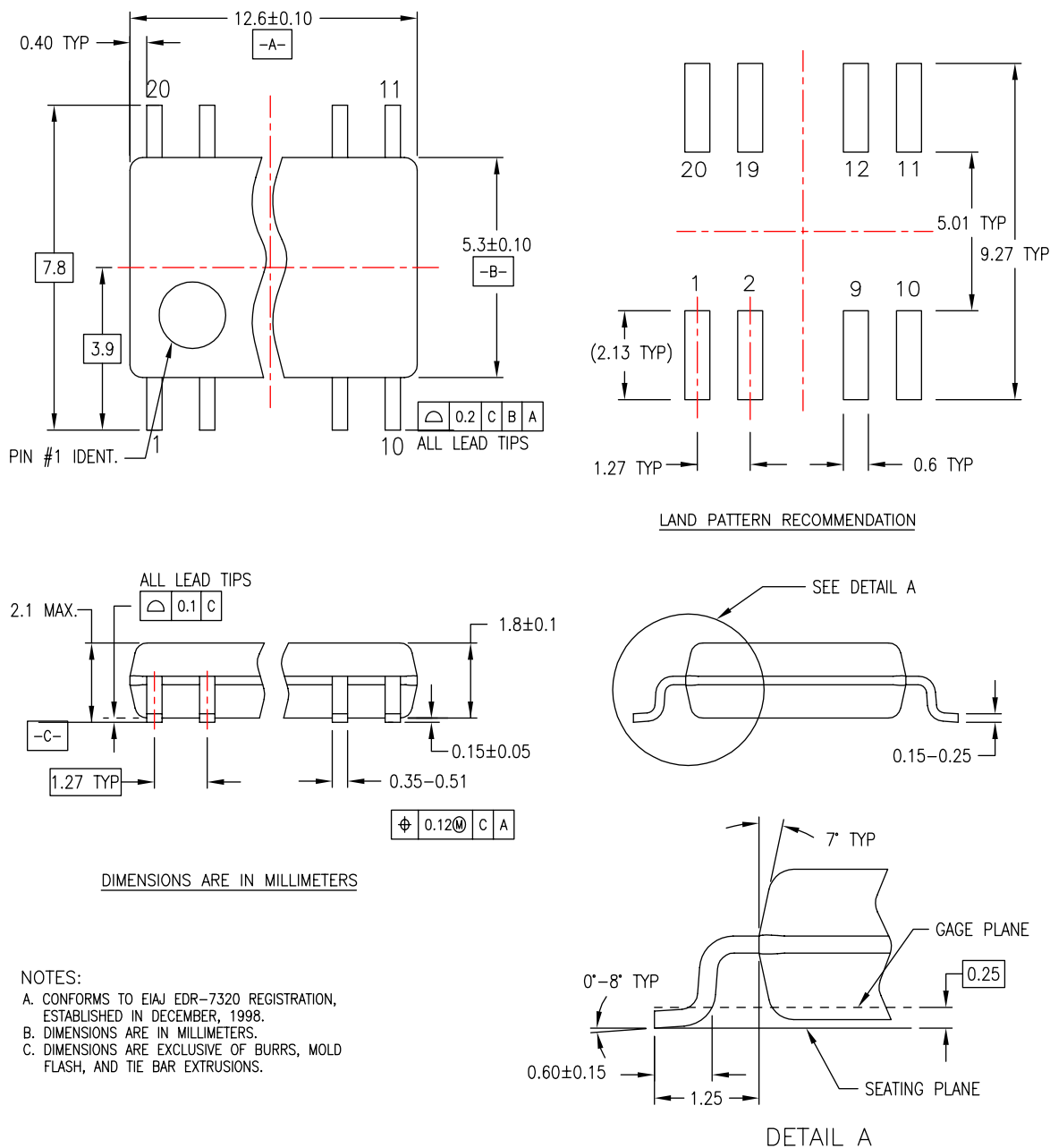
Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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# Physical Dimensions (Continued)



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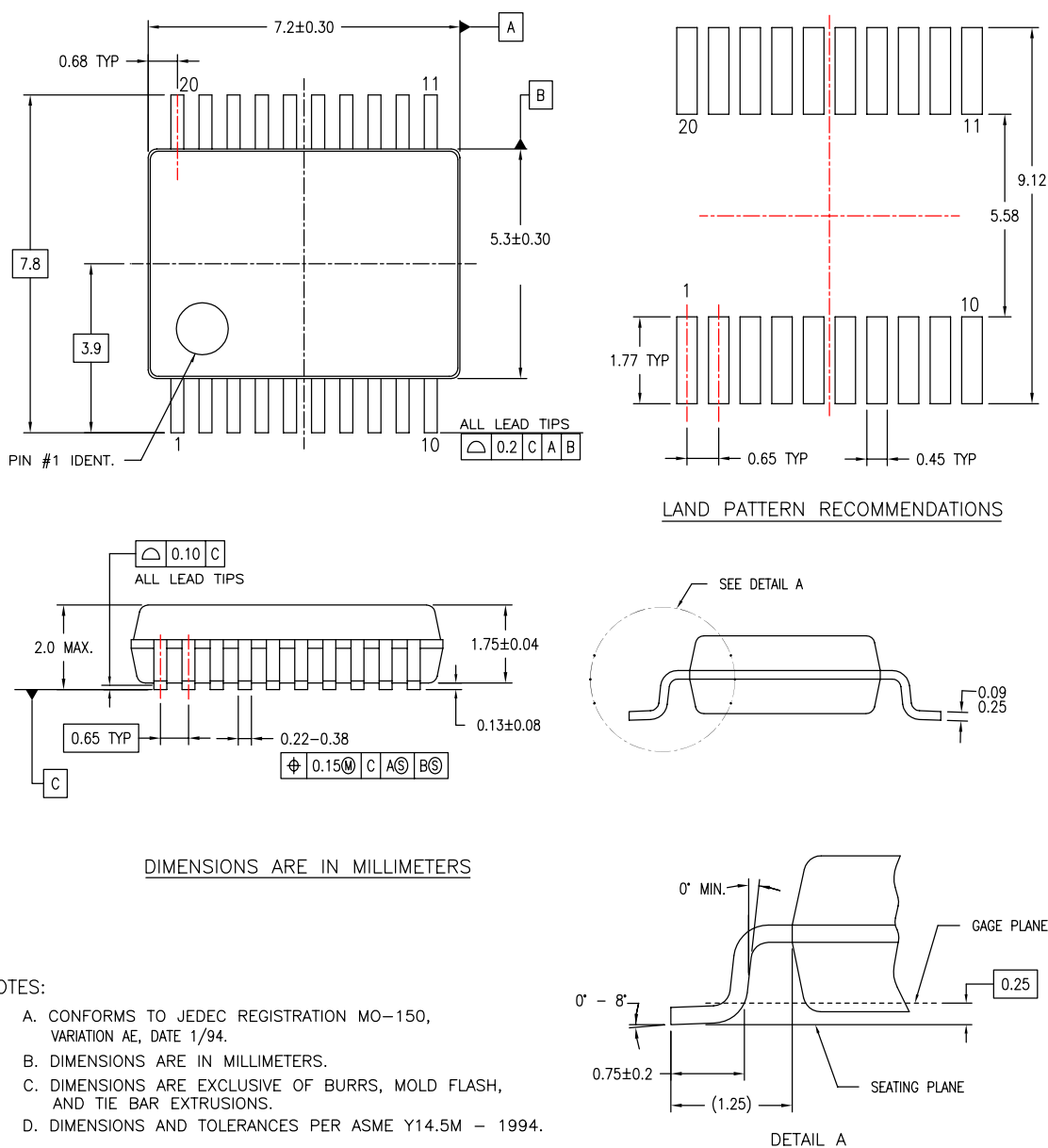
**Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**

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# Physical Dimensions (Continued)



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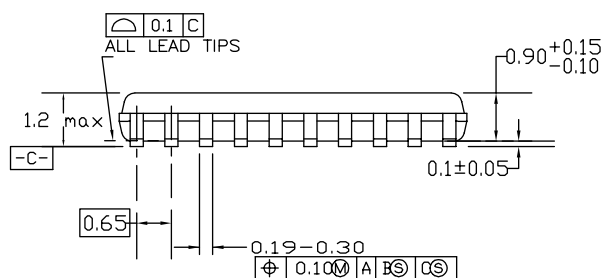
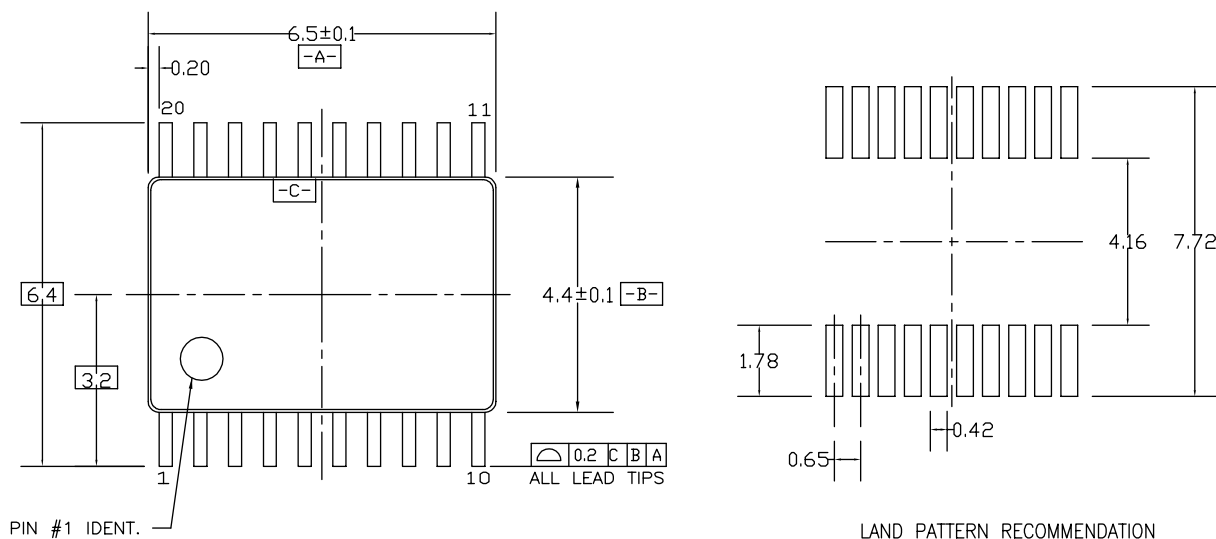
**Figure 3. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide**

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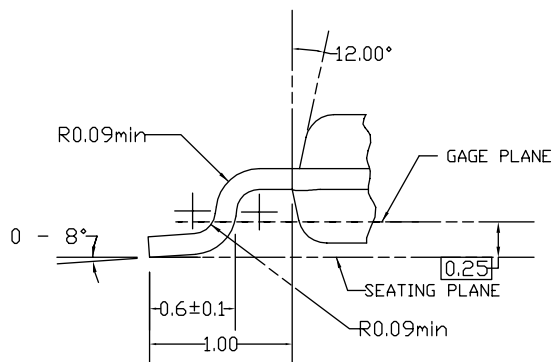
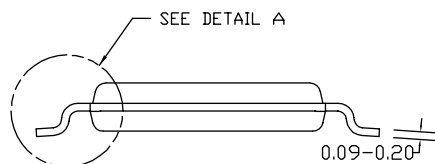
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# Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

## NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

Figure 4. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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

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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I33

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