![Texas Instruments]

PCF8575

SCPS121E −JANUARY 2005−REVISED JANUARY 2015

PCF8575 Remote16-BIT I²C AND SMBus I/O Expander with Interrupt Output

1 Features

- I²C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Low Standby-Current Consumption of 10 µA Max
- Compatible With Most Microcontrollers
- 400-kHz Fast I²C Bus
- Address by Three Hardware Address Pins for Use of up to Eight Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Current Source to V_{CC} for Actively Driving a High at the Output
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

2 Applications

- Telecom Shelters: Filter Units
- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics
- Industrial Automation
- Products with GPIO-Limited Processors

3 Description

This 16-bit I/O expander for the two-line bidirectional bus (I²C) is designed for 2.5-V to 5.5-V V_{CC} operation.

The PCF8575 device provides general-purpose remote I/O expansion for most microcontroller families by way of the I²C interface [serial clock (SCL), serial data (SDA)].

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07–P00, P17–P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V_{CC} is active.

Device Information[(1)]

PART NUMBER	PACKAGE (PIN)	BODY SIZE
PCF8575	SSOP (24)	8.20 mm × 5.30 mm
	QSOP (24)	8.65 mm × 3.90 mm
	TVSOP (24)	5.00 mm × 4.50 mm
	SOIC (24)	15.40 mm × 7.50 mm
	TSSOP (24)	7.80 mm × 4.40 mm
	QFN (24)	4.00 mm × 4.00 mm

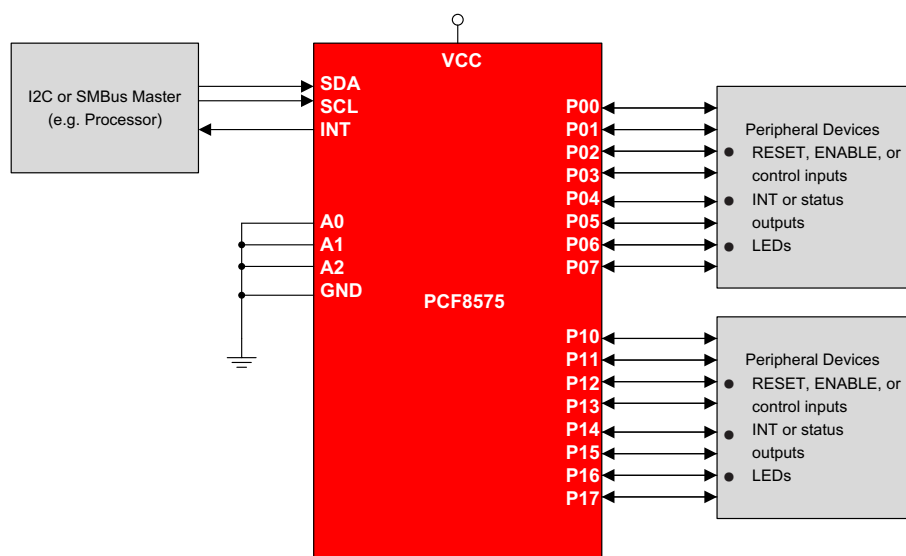(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

Changes from Revision D (April 2007) to Revision E   **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted *Ordering Information* table. 1

Product Folder Links: *PCF8575*

5 Pin Configurations and Functions

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)

```
        ┌──────┐
 INT  [ 1     24 ] V_CC
 A1   [ 2     23 ] SDA
 A2   [ 3     22 ] SCL
 P00  [ 4     21 ] A0
 P01  [ 5     20 ] P17
 P02  [ 6     19 ] P16
 P03  [ 7     18 ] P15
 P04  [ 8     17 ] P14
 P05  [ 9     16 ] P13
 P06  [ 10    15 ] P12
 P07  [ 11    14 ] P11
 GND  [ 12    13 ] P10
        └──────┘
```

RGE PACKAGE
(TOP VIEW)

```
         A2  A1  INT V_CC SDA SCL
         24  23  22  21  20  19
       ┌───────────────────────┐
 P00  1│                       │18  A0
 P01  2│                       │17  P17
 P03  3│                       │16  P16
 P03  4│                       │15  P15
 P04  5│                       │14  P14
 P05  6│                       │13  P13
       └───────────────────────┘
         7   8   9  10  11  12
        P06 P07 GND P10 P11 P12
```
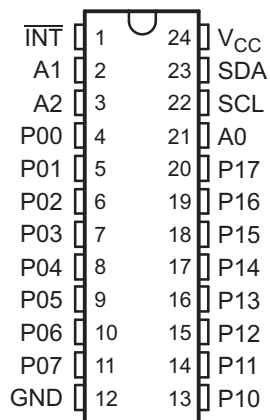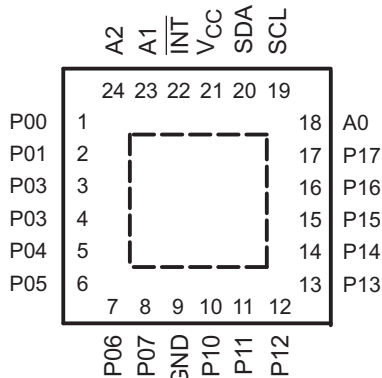
Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DB, DBQ, DGV, DW, AND PW	RGE		
A0	21	18	I	Address input 0. Connect directly to V_{CC} or ground. Pullup resistors are not needed.
A1	2	23	I	Address input 1. Connect directly to V_{CC} or ground. Pullup resistors are not needed.
A2	3	24	I	Address input 2. Connect directly to V_{CC} or ground. Pullup resistors are not needed.
$\overline{INT}$	1	22	O	Interrupt output. Connect to V_{CC} through a pullup resistor.
P00	4	1	I/O	P-port input/output. Push-pull design structure.
P01	5	2	I/O	P-port input/output. Push-pull design structure.
P02	6	3	I/O	P-port input/output. Push-pull design structure.
P03	7	4	I/O	P-port input/output. Push-pull design structure.
P04	8	5	I/O	P-port input/output. Push-pull design structure.
P05	9	6	I/O	P-port input/output. Push-pull design structure.
P06	10	7	I/O	P-port input/output. Push-pull design structure.
P07	11	8	I/O	P-port input/output. Push-pull design structure.
GND	12	9	—	Ground
P10	13	10	I/O	P-port input/output. Push-pull design structure.
P11	14	11	I/O	P-port input/output. Push-pull design structure.
P12	15	12	I/O	P-port input/output. Push-pull design structure.
P13	16	13	I/O	P-port input/output. Push-pull design structure.
P14	17	14	I/O	P-port input/output. Push-pull design structure.
P15	18	15	I/O	P-port input/output. Push-pull design structure.
P16	19	16	I/O	P-port input/output. Push-pull design structure.
P17	20	17	I/O	P-port input/output. Push-pull design structure.
SCL	22	19	I	Serial clock line. Connect to V_{CC} through a pullup resistor
SDA	23	20	I/O	Serial data line. Connect to V_{CC} through a pullup resistor.
V_{CC}	24	21	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range[2]		–0.5	$V_{CC} + 0.5$	V
V_O	Output voltage range[2]		–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{OK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		–20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–4	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	1000	

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.5	5.5	V
V_{IH}	High-level input voltage	$0.7 \times V_{CC}$	$V_{CC} + 0.5$	V
V_{IL}	Low-level input voltage	–0.5	$0.3 \times V_{CC}$	V
I_{OH}	P-port high-level output current		–1	mA
I_{OHT}	P-port transient pullup current		–10	mA
I_{OL}	P-port low-level output current		25	mA
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		PCF8575						UNIT
		DB	DBQ	DGV	DW	PW	RGE	
		24 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63	61	86	46	88	53	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

Product Folder Links: *PCF8575*

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA	2.5 V to 5.5 V	−1.2			V
V_{POR}	Power-on reset voltage [2]	$V_I = V_{CC}$ or GND, $I_O = 0$	V_{POR}		1.2	1.8	V
I_{OH}	P port	$V_O = $ GND	2.5 V to 5.5 V	−30		−300	µA
I_{OHT}	P-port transient pullup current	High during ACK, $V_{OH} = $ GND	2.5 V	−0.5	−1		mA
I_{OL}	SDA	$V_{OL} = 0.4$ V	2.5 V to 5.5 V	3			mA
	P port	$V_{OL} = 0.4$ V		5	15		
		$V_{OL} = 1$ V		10	25		
	$\overline{INT}$	$V_{OL} = 0.4$ V		1.6			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.5 V to 5.5 V			±5	µA
	A0, A1, A2					±1	
I_{IHL}	P port	$V_I \geq V_{CC}$ or $V_I \leq $ GND	2.5 V to 5.5 V			±400	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, $f_{scl} = 400$ kHz	5.5 V		100	200	µA
			3.6 V		30	75	
			2.7 V		20	50	
	Standby mode	$V_I = V_{CC}$ or GND, $I_O = 0$, $f_{scl} = 0$ kHz	5.5 V		2.5	10	
			3.6 V		2.5	10	
			2.7 V		2.5	10	
ΔI_{CC}	Supply current increase	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND	2.5 V to 5.5 V			200	µA
C_I	SCL	$V_I = V_{CC}$ or GND	2.5 V to 5.5 V		3	7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.5 V to 5.5 V		3	7	pF
	P port				4	10	

(1)   All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and $T_A = 25$°C.
(2)   The power-on reset circuit resets the I²C bus logic with $V_{CC} < V_{POR}$ and sets all I/Os to logic high (with current source to V_{CC}).

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 12)

			MIN	MAX	UNIT
f_{scl}	I²C clock frequency			400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial data setup time		100		ns
t_{sdh}	I²C serial data hold time		0		ns
t_{icr}	I²C input rise time		$20 + 0.1C_b$ [1]	300	ns
t_{icf}	I²C input fall time		$20 + 0.1C_b$ [1]	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3		µs
t_{sts}	I²C start or repeated Start condition setup		0.6		µs
t_{sth}	I²C start or repeated Start condition hold		0.6		µs
t_{sps}	I²C Stop condition setup		0.6		µs
t_{vd}	Valid-data time	SCL low to SDA output valid		1.2	µs
C_b	I²C bus capacitive load			400	pF

(1) $C_b = $ total bus capacitance of one bus line in pF

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 13 and Figure 14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	µs
t_{pv}	Output data valid	SCL	P port		4	µs
t_{su}	Input data setup time	P port	SCL	0		µs
t_{h}	Input data hold time	P port	SCL	4		µs

6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)
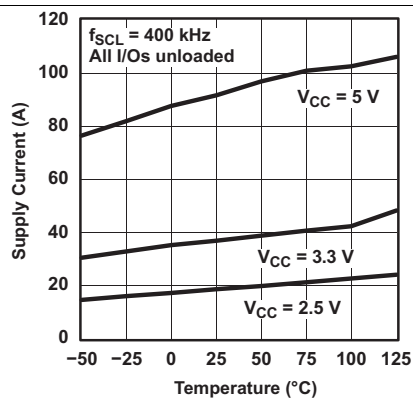
Figure 1. Supply Current vs Temperature
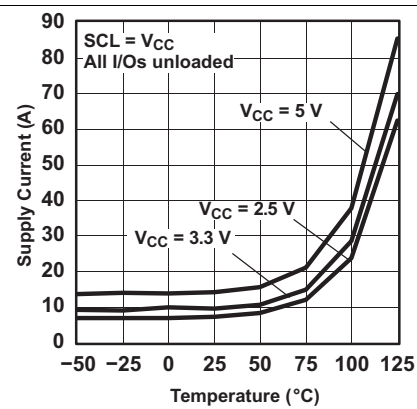
Figure 2. Standby Supply Current vs Temperature
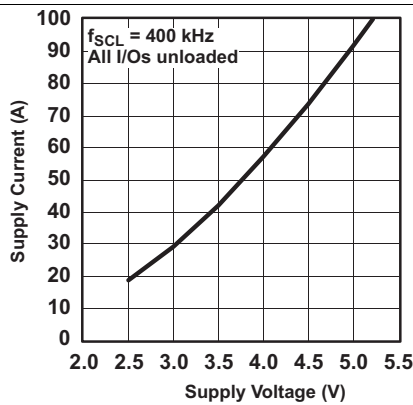
Figure 3. Supply Current vs Supply Voltage
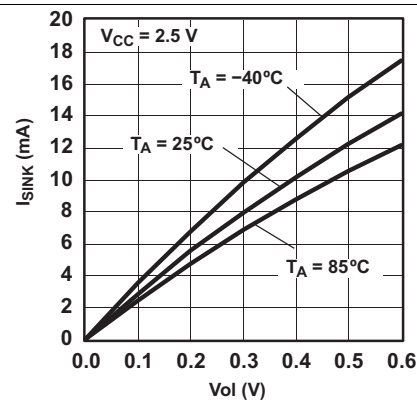
Figure 4. I/O Sink Current vs Output Low Voltage

Product Folder Links: *PCF8575*

Typical Characteristics (continued)

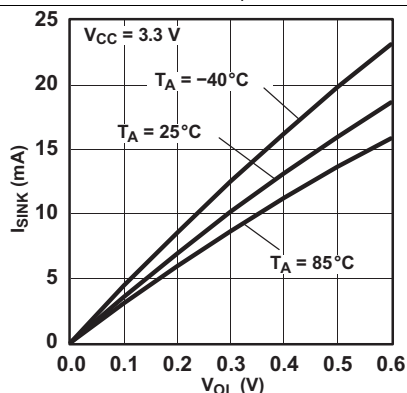T_A = 25°C (unless otherwise noted)

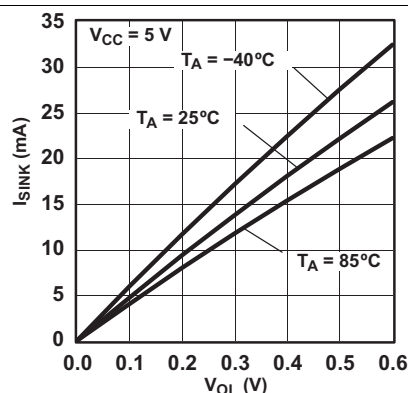**Figure 5. I/O Sink Current vs Output Low Voltage**

Figure 6. I/O Sink Current vs Output Low Voltage
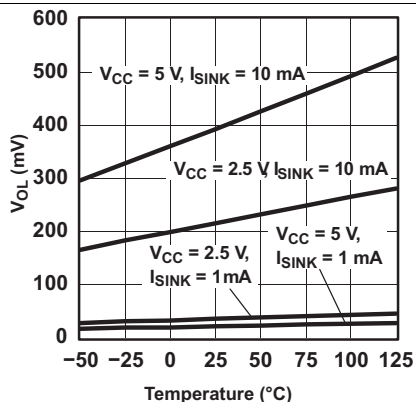

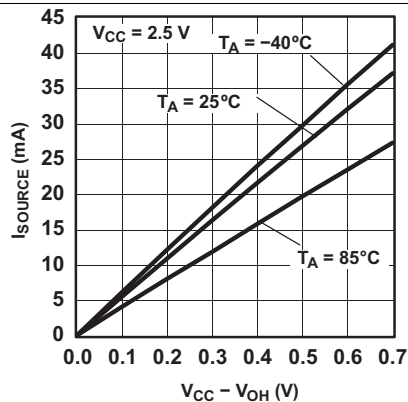**Figure 7. I/O Output Low Voltage vs Temperature**

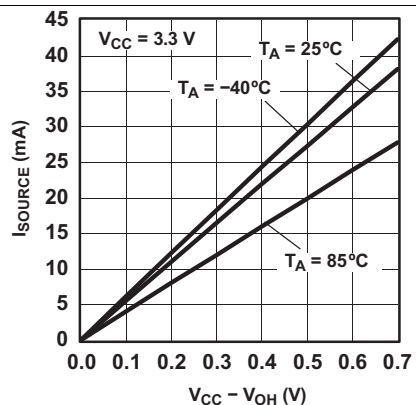**Figure 8. I/O Source Current vs Output High Voltage**
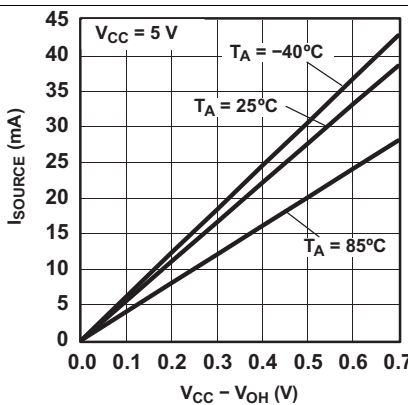

Figure 9. I/O Source Current vs Output High Voltage

Figure 10. I/O Source Current vs Output High Voltage

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)
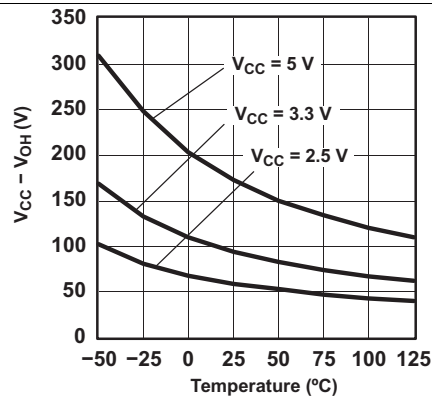
Figure 11. I/O High Voltage vs Temperature

Product Folder Links: *PCF8575*

7 Parameter Measurement Information

SDA LOAD CONFIGURATION

VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

Figure 12. I^2C Interface Load Circuit and Voltage Waveforms

Product Folder Links: *PCF8575*

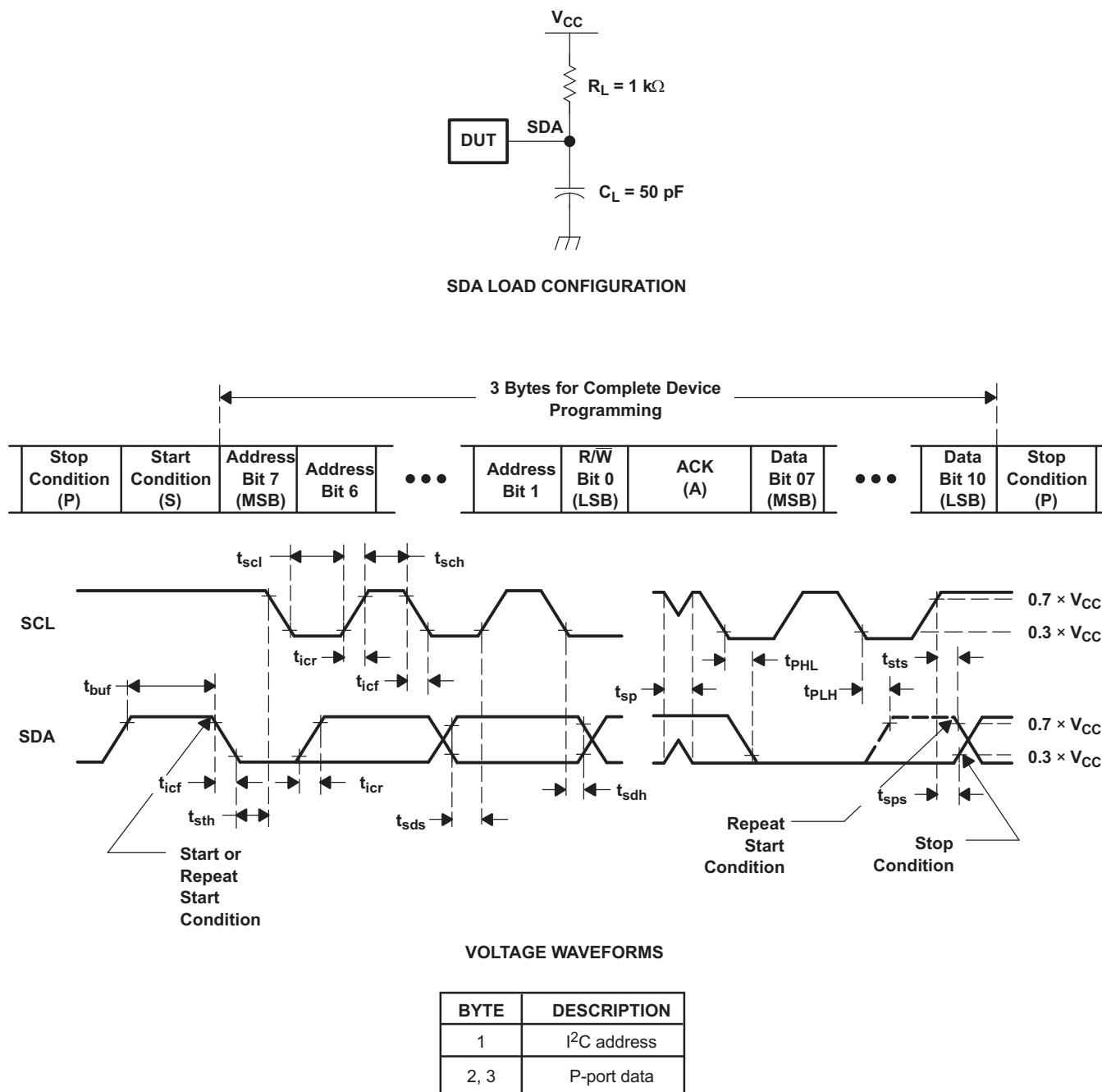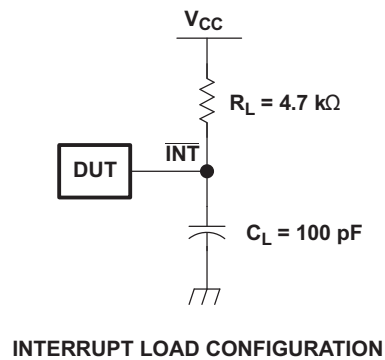## Parameter Measurement Information (continued)
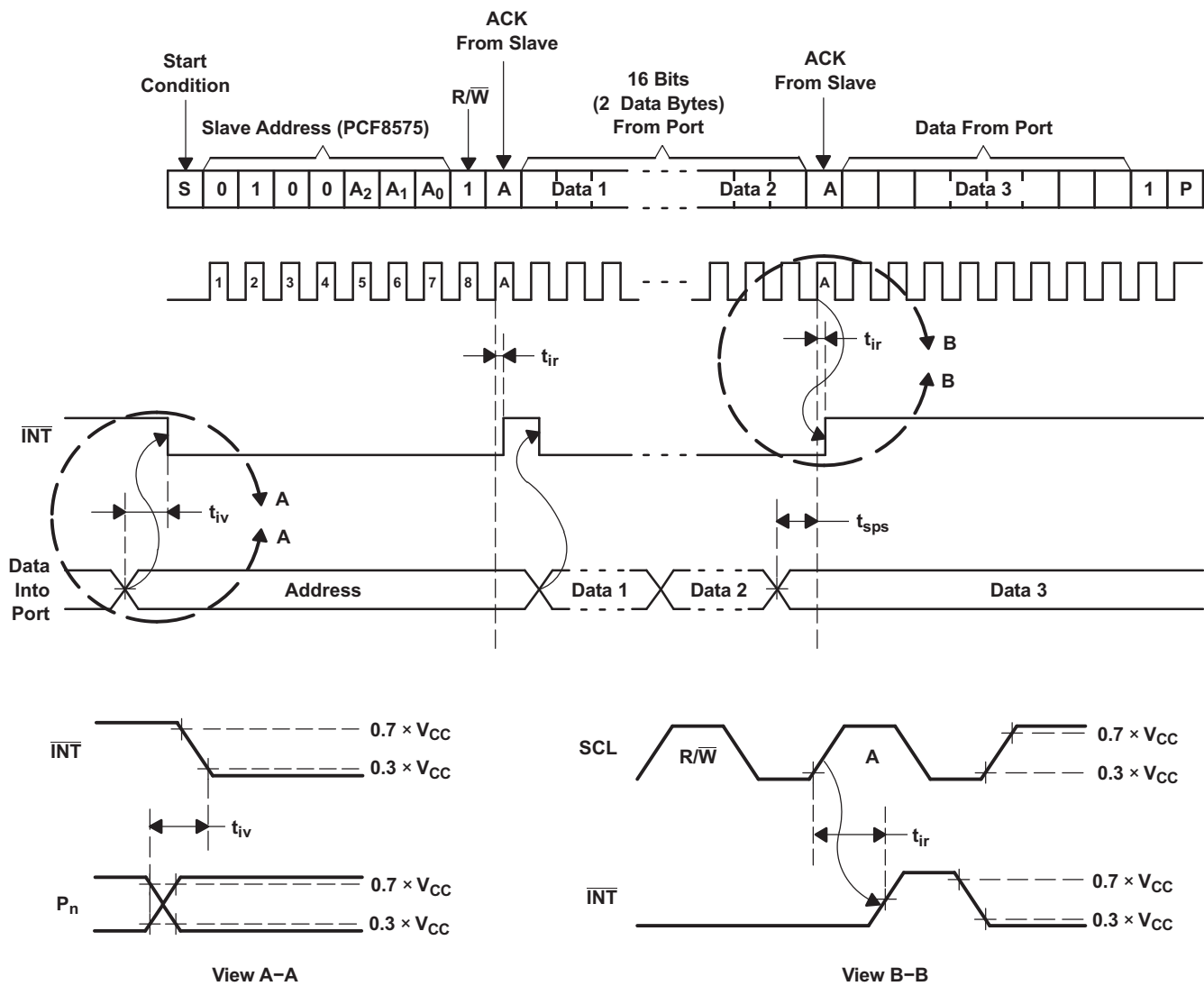

INTERRUPT LOAD CONFIGURATION

Figure 13. Interrupt Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

SDA LOAD CONFIGURATION

INTERRUPT LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION

Write-Mode Timing (R/$\overline{W}$ = 0)

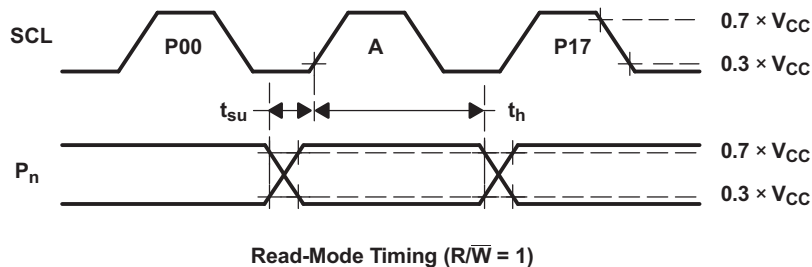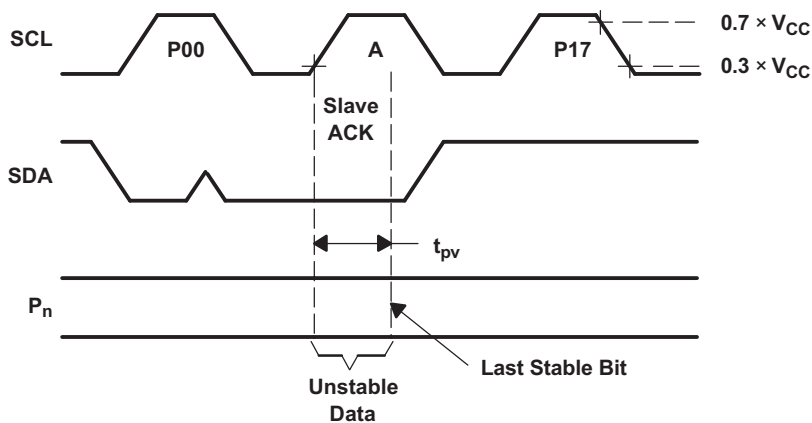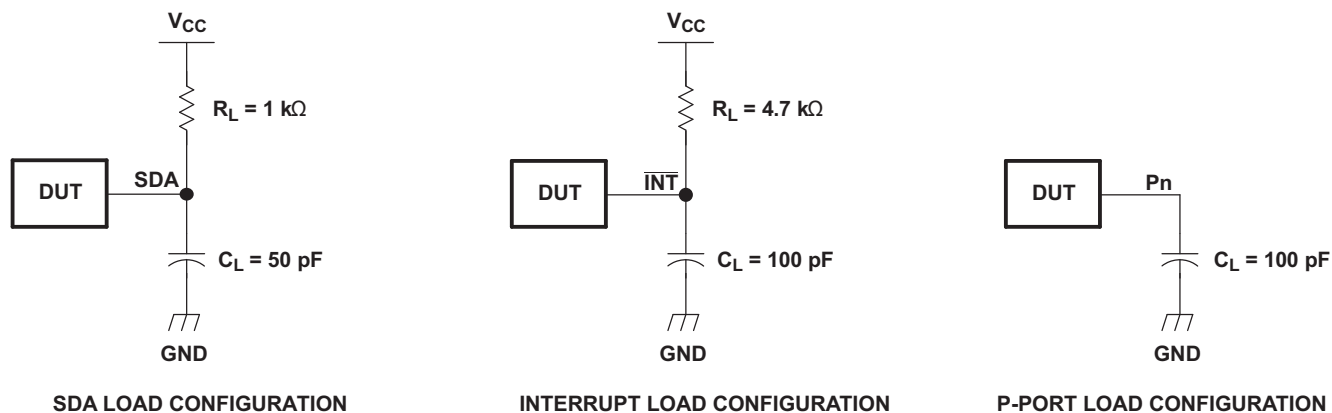Read-Mode Timing (R/$\overline{W}$ = 1)

Figure 14. P-Port Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The PCF8575 provides general-purpose remote I/O expansion for most microcontroller families via the I^{2}C interface serial clock (SCL) and serial data (SDA).

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07–P00, P17–P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source (I$_{OH}$) to V$_{CC}$ is active. An additional strong pullup to V$_{CC}$ (I$_{OHT}$) allows fast-rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs. After power on, as all the I/Os are set high, all of them can be used as inputs. Any change in setting of the I/Os as either input or outputs can be done with the write mode. If a high is applied externally to an I/O that has been written earlier to low, a large current (I$_{OL}$) will flow to GND.

The PCF8575 provides an open-drain interrupt ($\overline{INT}$) output, which can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t$_{iv}$, the signal $\overline{INT}$ is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting, or data is read from or written to the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal or in the write mode at the ACK bit after the falling edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short), due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit. This device does not have internal configuration or status registers. Instead, read or write to the device I/Os directly after sending the device address (see Figure 18 and Figure 19).

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports, without having to communicate via the I^{2}C bus. Thus, the PCF8575 can remain a simple slave device.

Every data transmission to or from the PCF8575 must consist of an even number of bytes. The first data byte in every pair refers to port 0 (P07–P00), and the second data byte in every pair refers to port 1 (P17–P10). To write to the ports (output mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 0. The PCF8575 acknowledges, and the master sends the first data byte for P07–P00. After the first data byte is acknowledged by the PCF8575, the second data byte (P17–P10) is sent by the master. Once again, the PCF8575 acknowledges the receipt of the data, after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten. When the PCF8575 receives the pairs of data bytes, the first byte is referred to as P07–P00 and the second byte as P17–P10. The third byte is referred to as P07–P00, the fourth byte as P17–P10, and so on.

Before reading from the PCF8575, all ports desired as input should be set to logic 1. To read from the ports (input mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 1. The data bytes that follow on the SDA are the values on the ports. If the data on the input port changes faster than the master can read, this data may be lost.

When power is applied to V$_{CC}$, an internal power-on reset holds the PCF8575 in a reset state until V$_{CC}$ has reached V$_{POR}$. At that time, the reset condition is released, and the device I^{2}C-bus state machine initializes the bus to its default state.

The hardware pins (A0, A1, and A2) are used to program and vary the fixed I^{2}C address and allow up to eight devices to share the same I^{2}C bus or SMBus. The fixed I^{2}C address of the PCF8575 is the same as the PCF8575C, PCF8574, PCA9535, and PCA9555, allowing up to eight of these devices, in any combination, to share the same I^{2}C bus or SMBus.

8.2 Functional Block Diagram

8.2.1 Logic Diagram (Positive Logic)
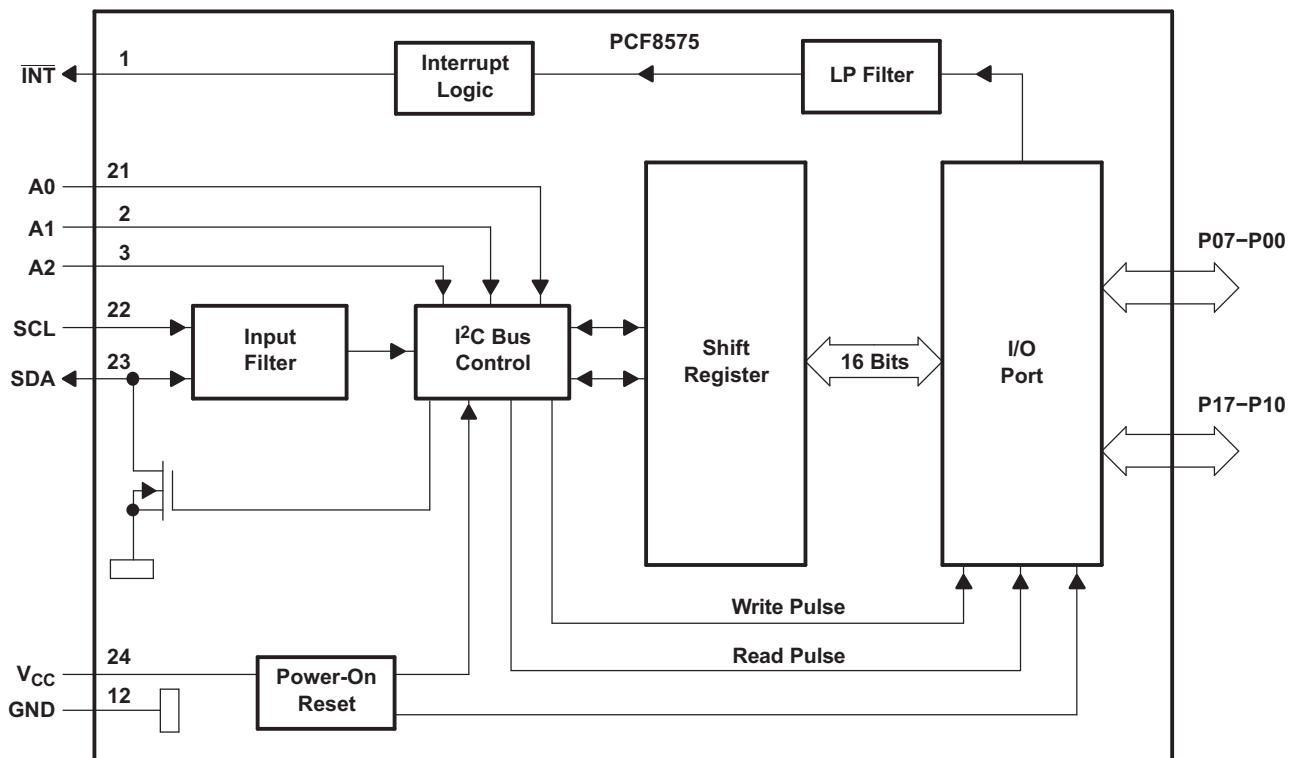
8.2.2 Simplified Schematic Diagram of Each P-Port Input/Output
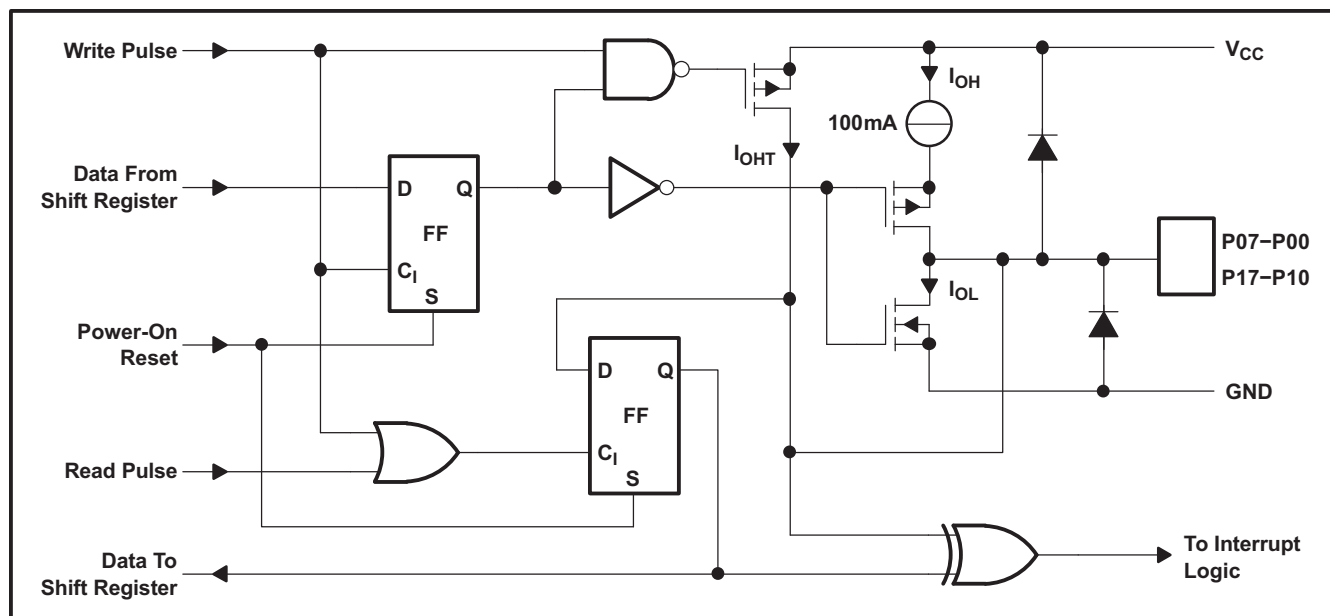
8.3 Feature Description

8.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 15). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A2–A0) of the slave device must not be changed between the Start and Stop conditions.

The data byte follows the address ACK. If the R/$\overline{W}$ bit is high, the data from this device are the values read from the P port. If the R/$\overline{W}$ bit is low, the data are from the master, to be output to the P port. The data byte is followed by an ACK sent from this device. If other data bytes are sent from the master, following the ACK, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (t_{pv}) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 16).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 15).

The number of data bytes transferred between the Start and Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 17). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.
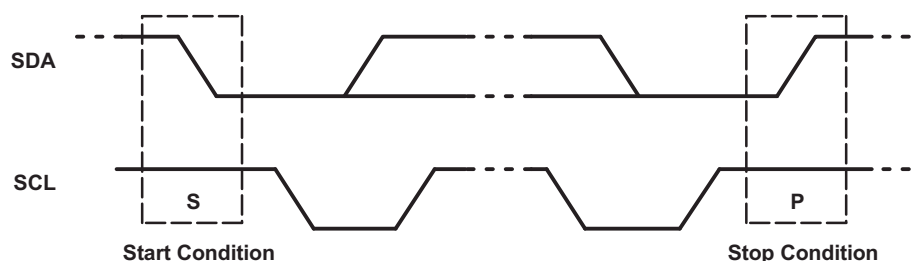
Figure 15. Definition of Start and Stop Conditions

Feature Description (continued)
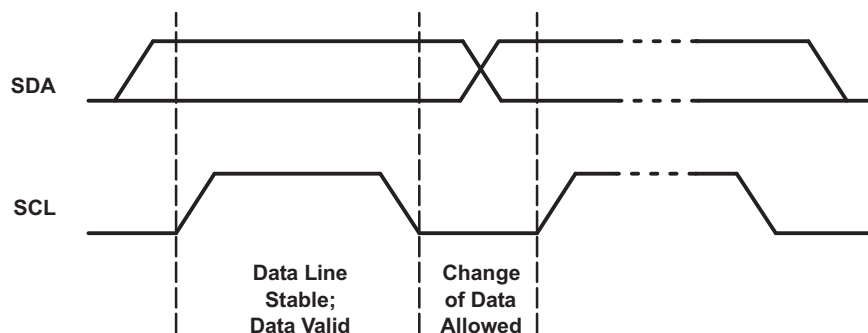
Figure 16. Bit Transfer
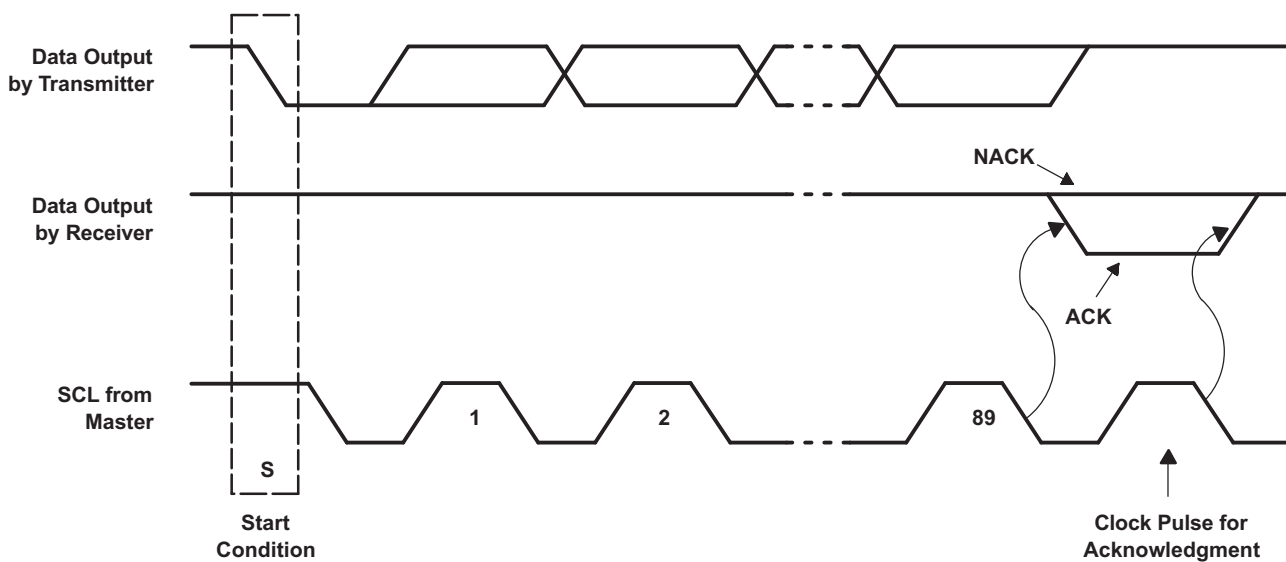
Figure 17. Acknowledgment on I²C Bus

8.3.2 Interface Definition

BYTE	BIT							
	7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
I²C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

8.3.3 Address Reference

INPUTS			I²C BUS SLAVE 8-BIT READ ADDRESS	I²C BUS SLAVE 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	65 (decimal), 41 (hexadecimal)	64 (decimal), 40 (hexadecimal)
L	L	H	67 (decimal), 43 (hexadecimal)	66 (decimal), 42 (hexadecimal)
L	H	L	69 (decimal), 45 (hexadecimal)	68 (decimal), 44 (hexadecimal)
L	H	H	71 (decimal), 47 (hexadecimal)	70 (decimal), 46 (hexadecimal)
H	L	L	73 (decimal), 49 (hexadecimal)	72 (decimal), 48 (hexadecimal)
H	L	H	75 (decimal), 4B (hexadecimal)	74 (decimal), 4A (hexadecimal)
H	H	L	77 (decimal), 4D (hexadecimal)	76 (decimal), 4C (hexadecimal)
H	H	H	79 (decimal), 4F (hexadecimal)	78 (decimal), 4E (hexadecimal)

8.4 Device Functional Modes

Figure 18 and Figure 19 show the address and timing diagrams for the write and read modes, respectively.

Integral Multiples of Two Bytes
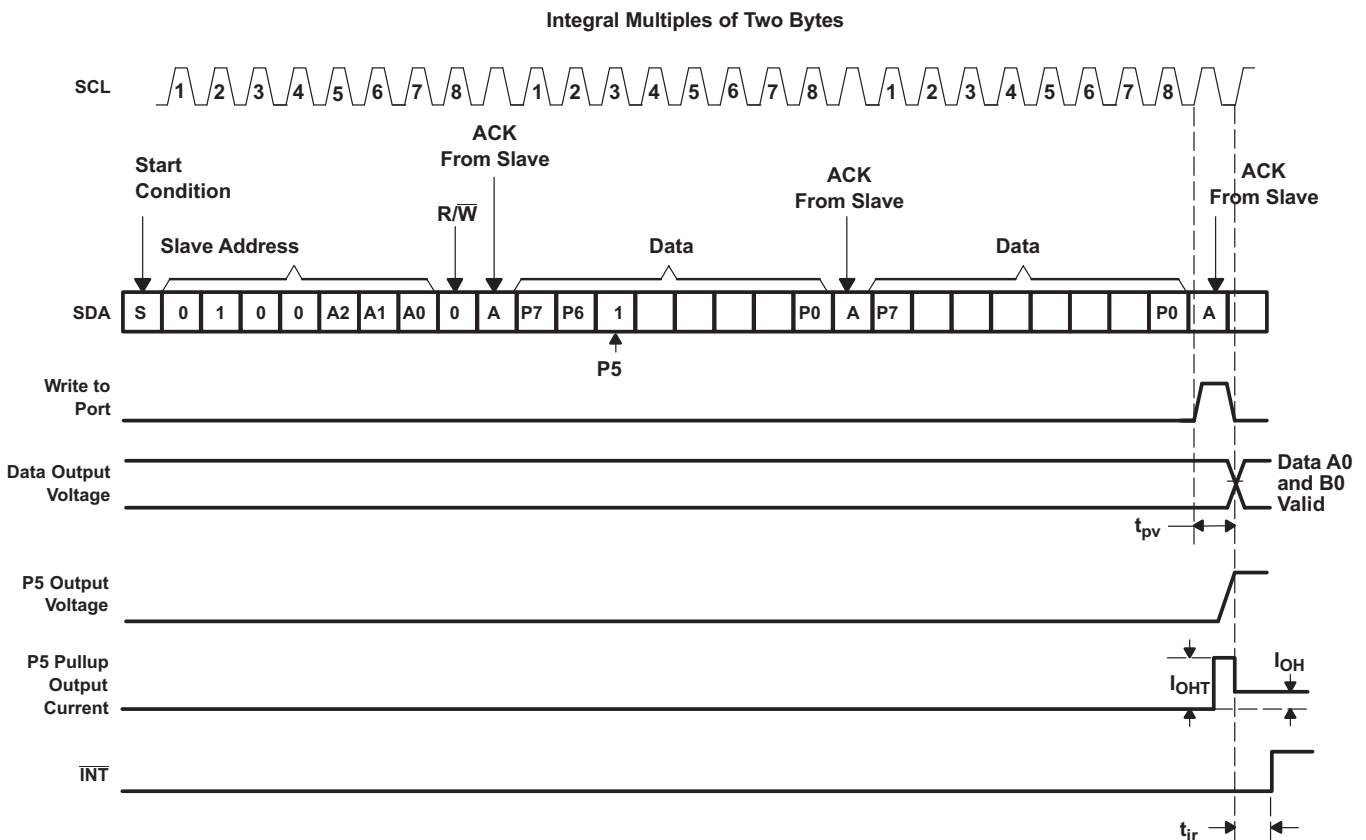
Figure 18. Write Mode (Output)

Product Folder Links: PCF8575

Device Functional Modes (continued)
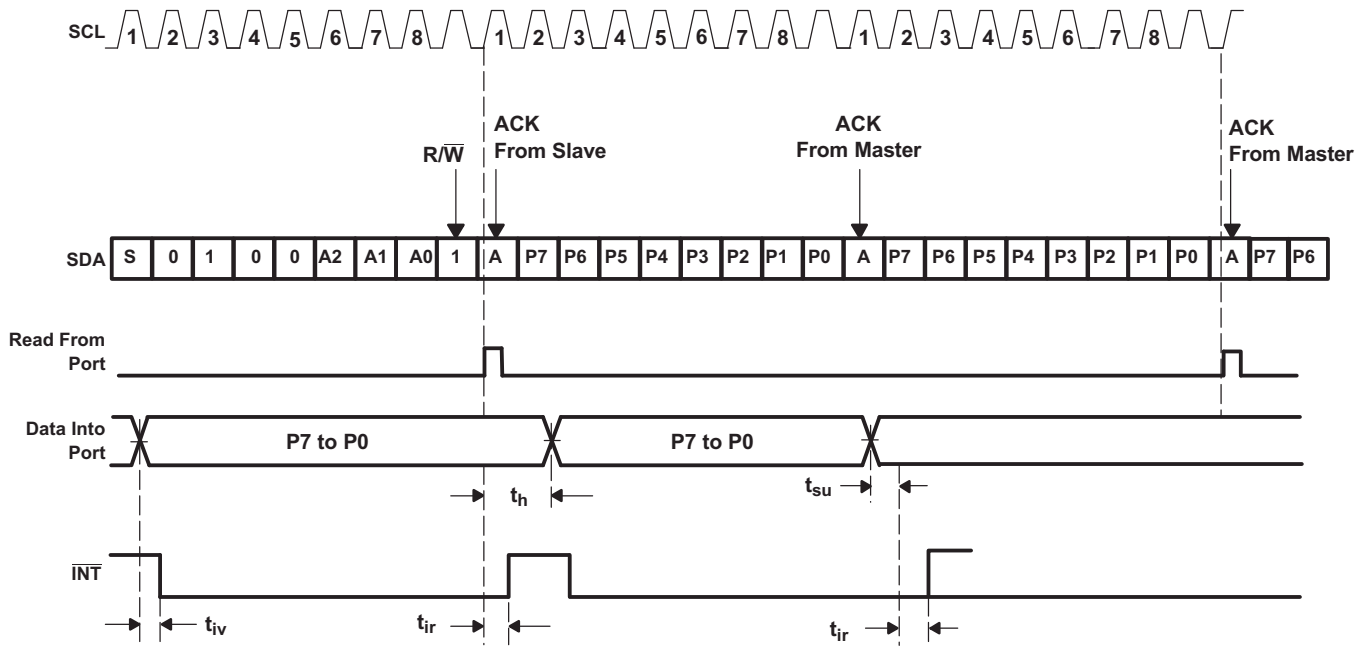
Figure 19. Read Mode (Input)

9 Application and Implementation

9.1 Application Information

Figure 20 shows an application in which PCF8575 can be used.

9.2 Typical Application

Figure 20. Application Schematic
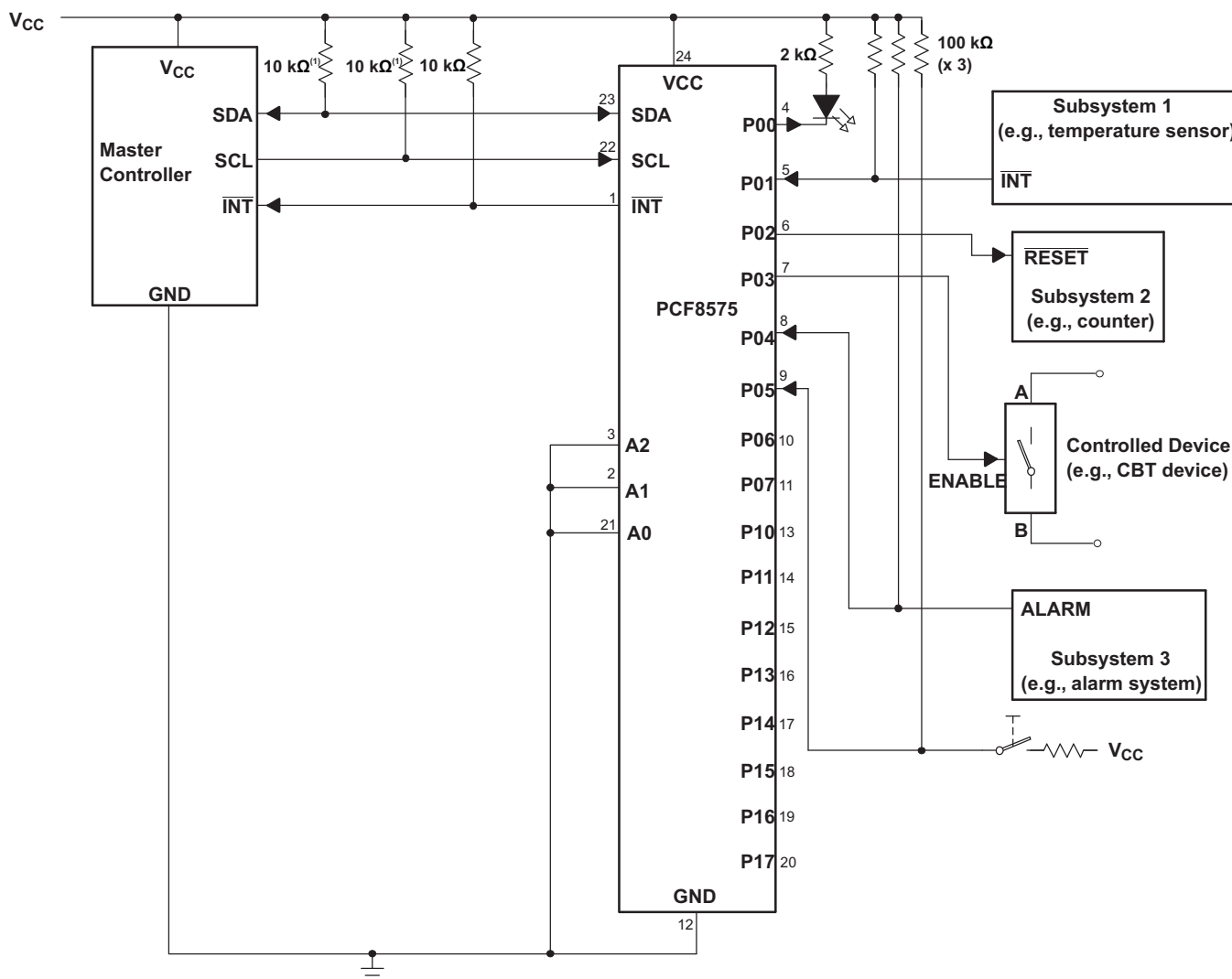
(1) The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that could be powered on while VCC is powered off, then the supply current, ICC, will increase as a result.

A. Device address is configured as 0100000 for this example.

B. P0, P2, and P3 are configured as outputs.

C. P1, P4, and P5 are configured as inputs.

D. P6 and P7 are not used and must be configured as outputs.

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 20. For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC}. The LED is a diode, with threshold voltage V_T, and when a P-port is configured as an input the LED will be off but V_I is a V_T drop below V_{CC}.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. Figure 21 shows a high-value resistor in parallel with the LED. Figure 22 shows V_{CC} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.
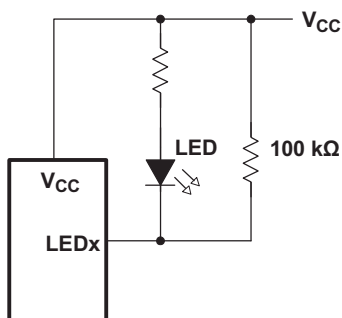
Figure 21. High-Value Resistor in Parallel With LED
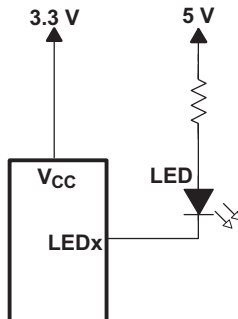
Figure 22. Device Supplied by a Lower Voltage

Typical Application (continued)

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I²C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}}$$

(1)

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b}$$

(2)

The maximum bus capacitance for an I²C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8575, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

9.2.3 Application Curves

Standard-mode
(f_{SCL}= 100 kHz, t_r = 1 µs)

Fast-mode
(f_{SCL}= 400 kHz, t_r= 300 ns)

Figure 23. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)

V_{OL} = 0.2*V_{CC}, I_{OL} = 2 mA
when V_{CC} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA
when V_{CC} > 2 V

Figure 24. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

Product Folder Links: *PCF8575*
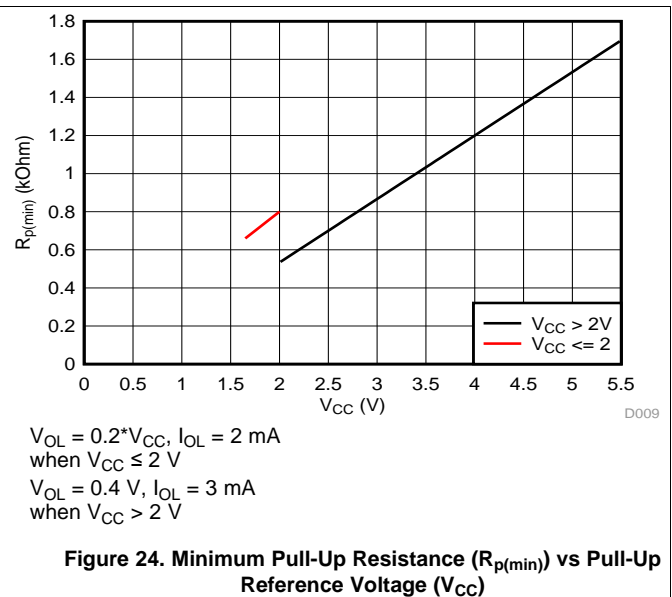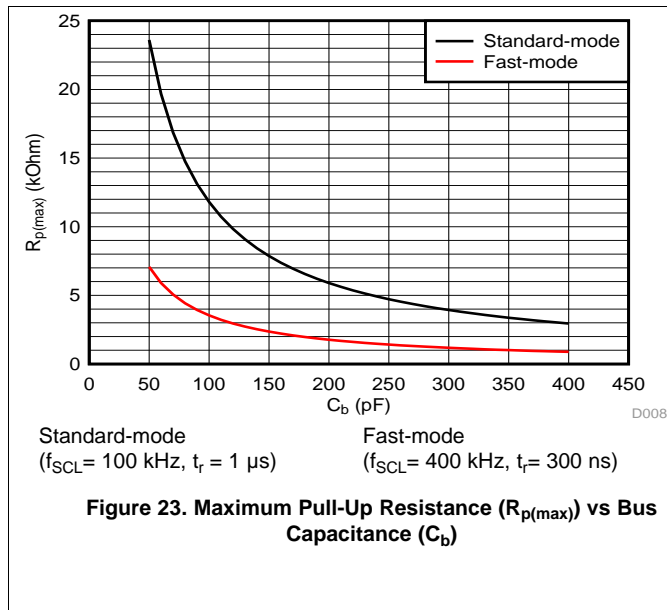
10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCF8575 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 25 and Figure 26.
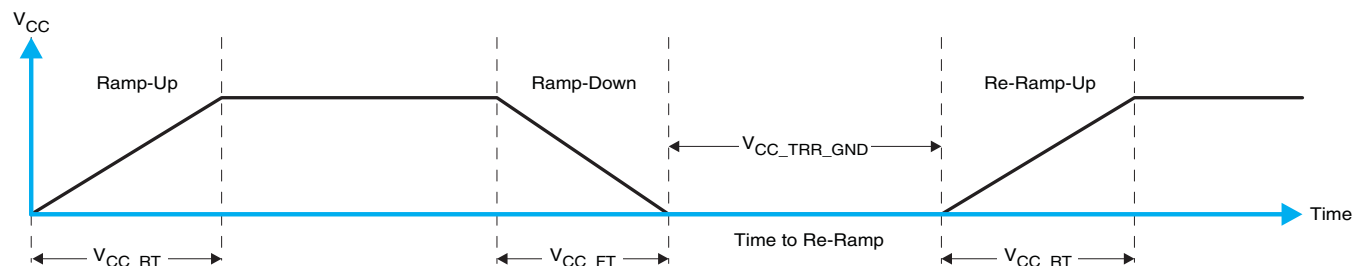
Figure 25. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}
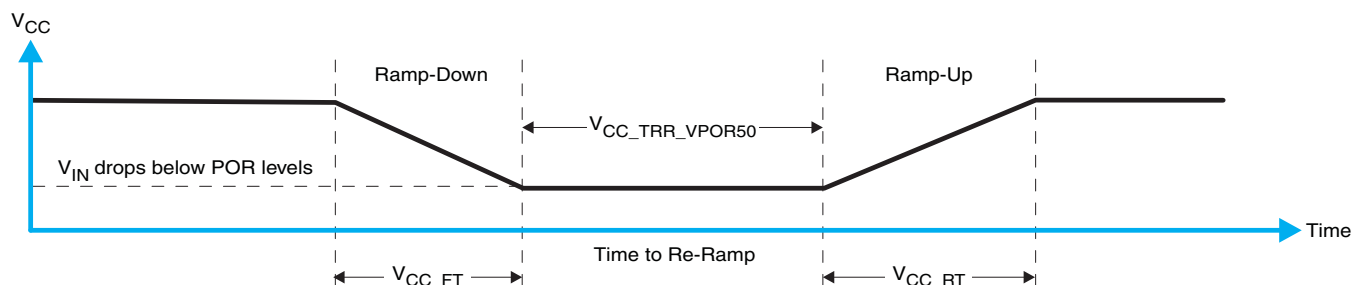
Figure 26. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 1 specifies the performance of the power-on reset feature for PCF8575 for both types of power-on reset.

Table 1. Recommended Supply Sequencing and Ramp Rates[1]

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 25	1		100	ms
V_{CC_RT}	Rise rate	See Figure 25	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See Figure 25	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} − 50 mV)	See Figure 26	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 μs	See Figure 27			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See Figure 27				μs
V_{PORF}	Voltage trip point of POR on falling V_{CC}			0.767	1.144	V
V_{PORR}	Voltage trip point of POR on fising V_{CC}			1.033	1.428	V

(1) T_A = −40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 27 and Table 1 provide more information on how to measure these specifications.
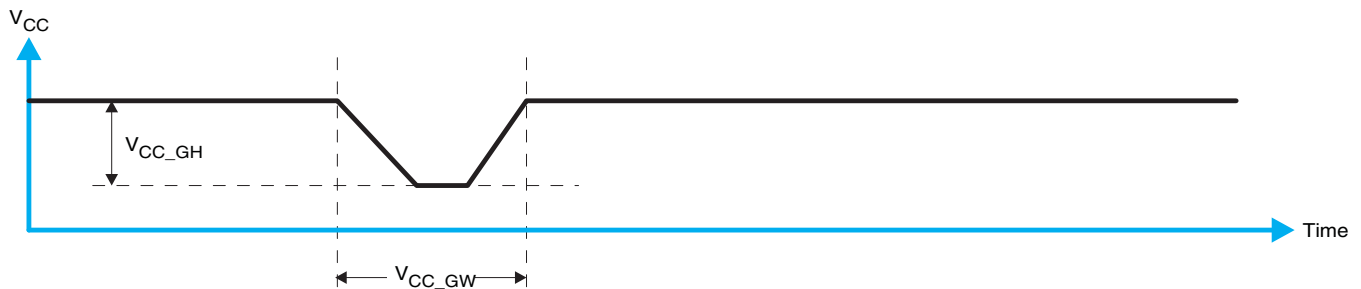
Figure 27. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 28 and Table 1 provide more details on this specification.
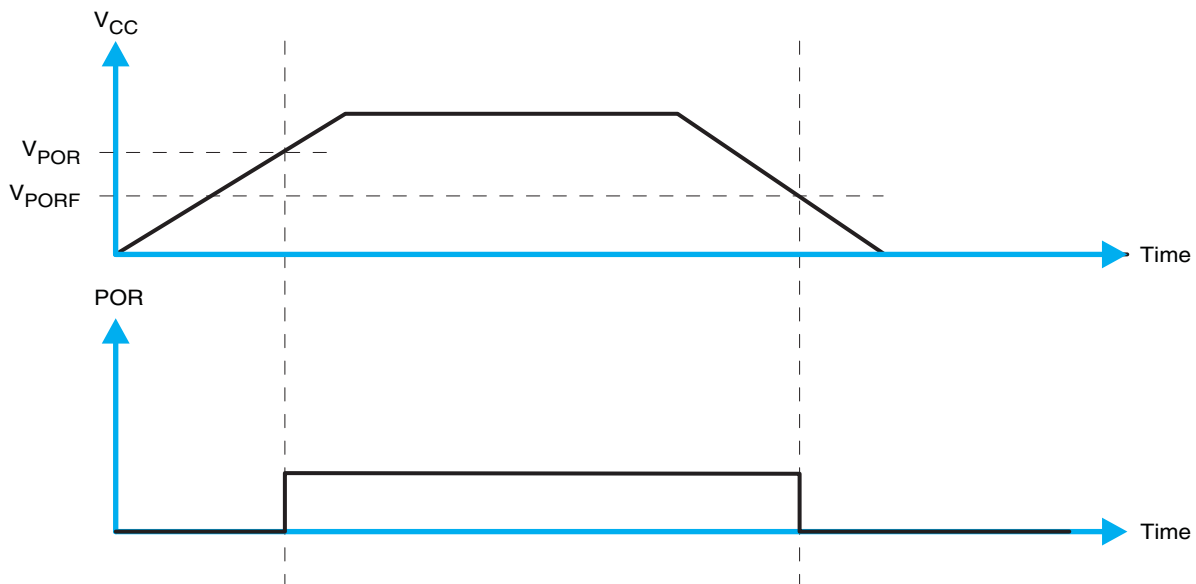
Figure 28. V_{POR}

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCF8575 device, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^{2}C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8575 as possible. These best practices are shown in Figure 29.

For the layout example provided in Figure 29, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 29.

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Product Folder Links: *PCF8575*

11.2 Layout Example
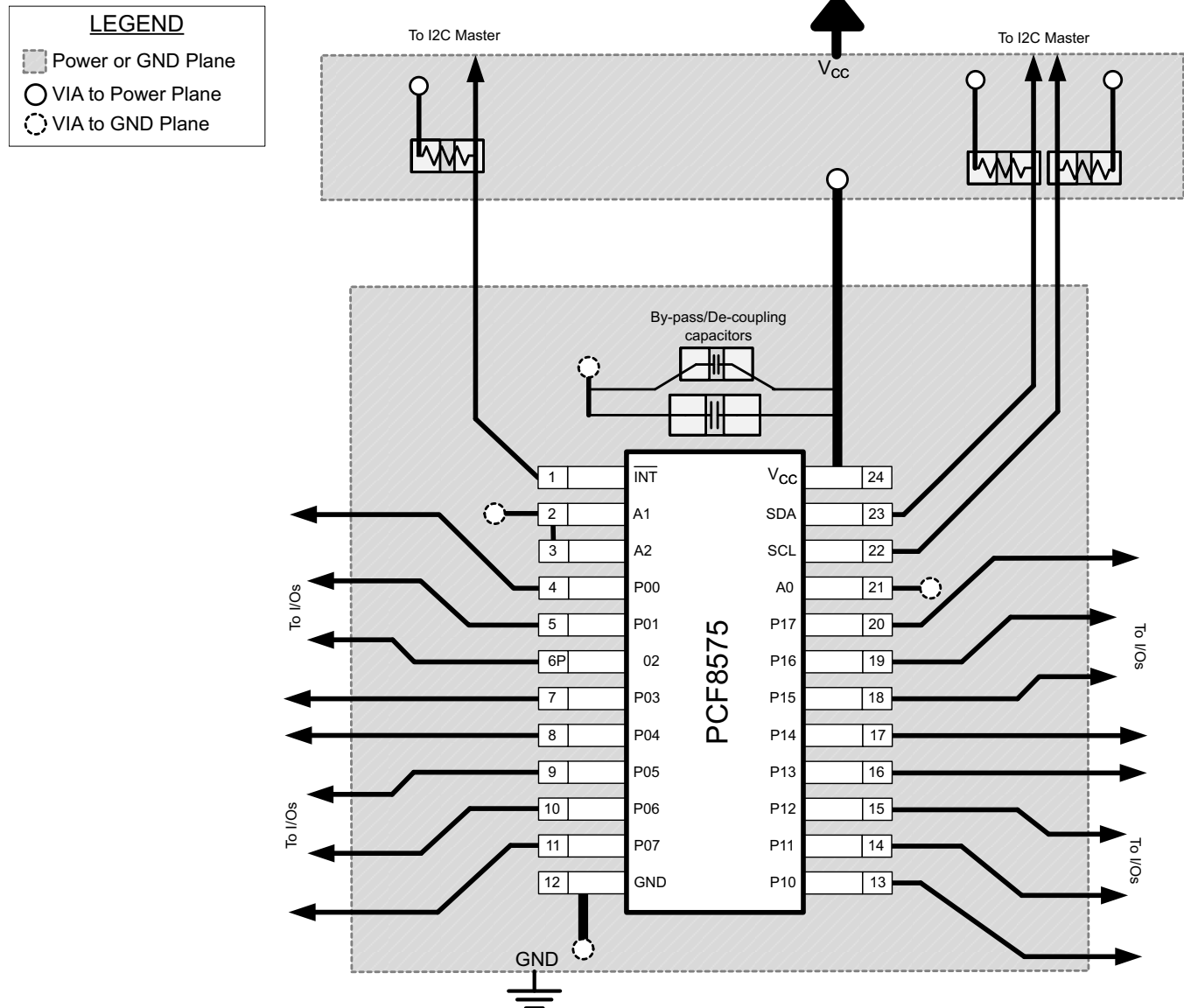
Figure 29. Layout Example for PCF8575

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Product Folder Links: *PCF8575*

12   Device and Documentation Support

12.1   Trademarks

All trademarks are the property of their respective owners.

12.2   Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3   Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

13   Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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14-Sep-2014

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8575DB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCF8575	Samples
PCF8575DBQRE4	ACTIVE	SSOP	DBQ	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575DBQRG4	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCF8575	Samples
PCF8575DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575DBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575DBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575DGVRE4	ACTIVE	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575	Samples
PCF8575DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575	Samples
PCF8575DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575	Samples
PCF8575DWRG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8575PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575PWRG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF575	Samples
PCF8575RGERG4	ACTIVE	VQFN	RGE	24		TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCF8575DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCF8575DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCF8575DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCF8575DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCF8575PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCF8575RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCF8575DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
PCF8575DBR	SSOP	DB	24	2000	367.0	367.0	38.0
PCF8575DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
PCF8575DWR	SOIC	DW	24	2000	367.0	367.0	45.0
PCF8575PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
PCF8575RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

$\dfrac{0.614\ (15,60)}{0.598\ (15,20)}$

24   13

$\dfrac{0.419\ (10,63)}{0.393\ (9,97)}$

$\dfrac{0.299\ (7,60)}{0.291\ (7,40)}$

1   12

Pin 1
Index Area

0.050 (1,27)

$\dfrac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\dfrac{0.012\ (0,30)}{0.004\ (0,10)}$

$\dfrac{0.013\ (0,33)}{0.008\ (0,20)}$

⌂ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

$\dfrac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−5/G 01/11
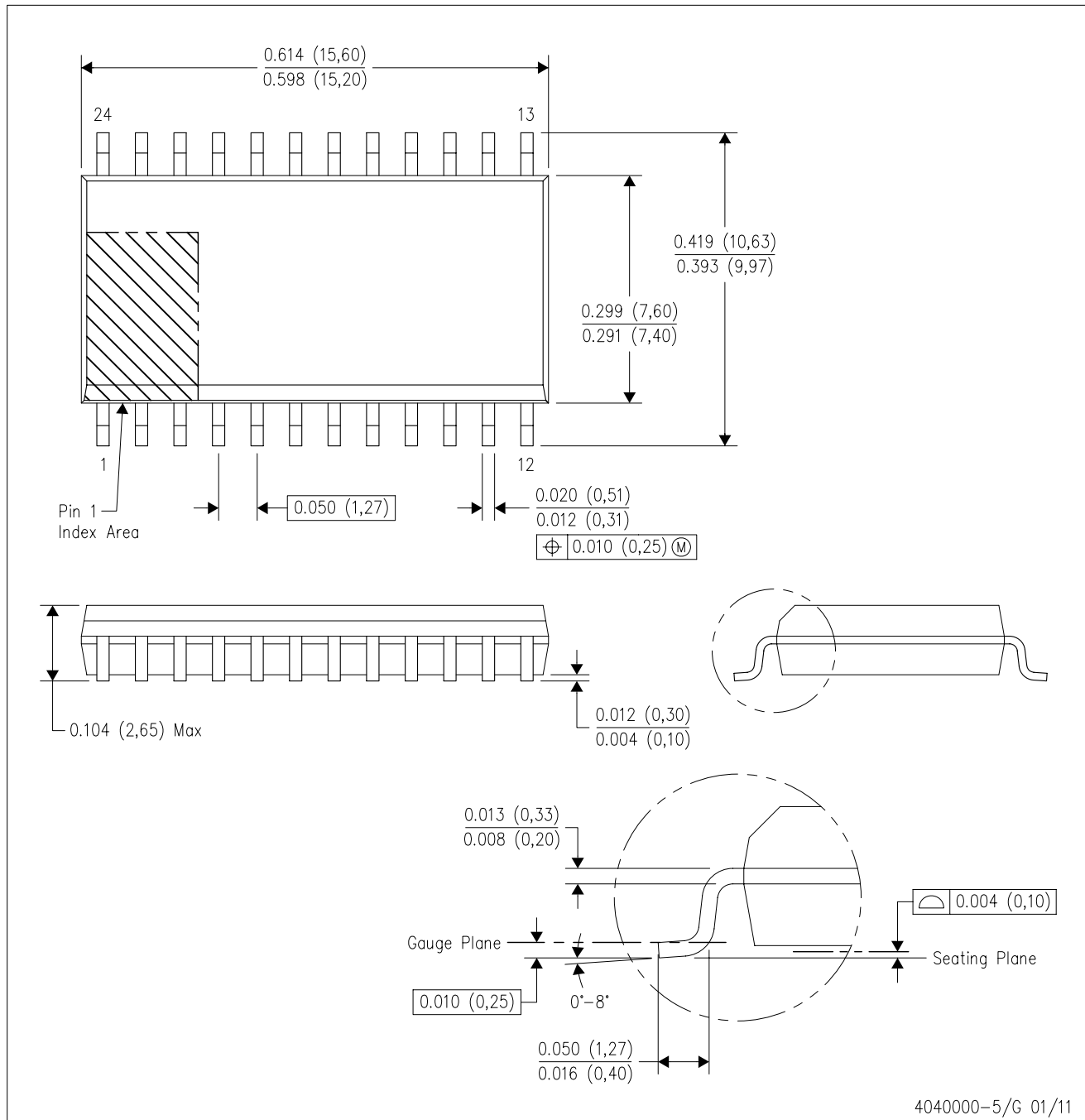
NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AD.

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DBQ (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE

$\frac{0.344\ (8,75)}{0.337\ (8,55)}$

24   13

$\frac{0.244\ (6,20)}{0.228\ (5,80)}$

$\frac{0.157\ (4,00)}{0.150\ (3,80)}$

Pin 1
Index Area

1   12

0.025 (0,635)

$\frac{0.012\ (0,30)}{0.008\ (0,20)}$

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

$\frac{0.010\ (0,25)}{0.004\ (0,10)}$

$\frac{0.010\ (0,25)}{0.005\ (0,13)}$

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

$\frac{0.035\ (0,89)}{0.016\ (0,40)}$

4073301−4/H   10/2008

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
         D.   Falls within JEDEC MO−137 variation AE.

DBQ (R−PDSO−G24)   PLASTIC SMALL OUTLINE PACKAGE
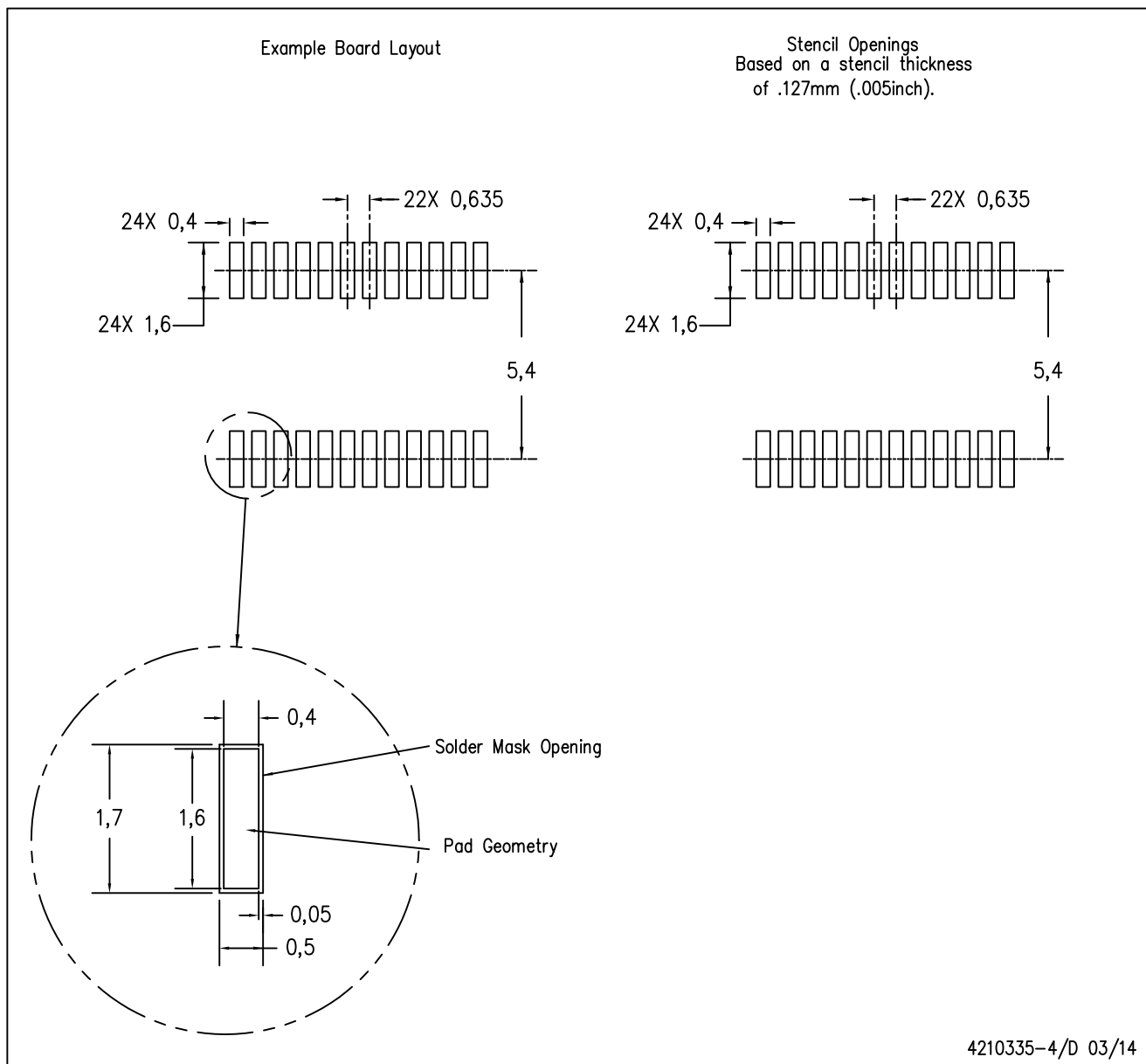
Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

24X 0,4

22X 0,635

24X 1,6

5,4

24X 0,4

22X 0,635

24X 1,6

5,4

0,4

Solder Mask Opening

1,7   1,6

Pad Geometry

0,05

0,5

4210335−4/D 03/14

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

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PW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

24   13

Ⓓ 4,50   6,60
   4,30   6,20

1   12

7,90
7,70

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌀ 0,10

4040064−6/G 02/11
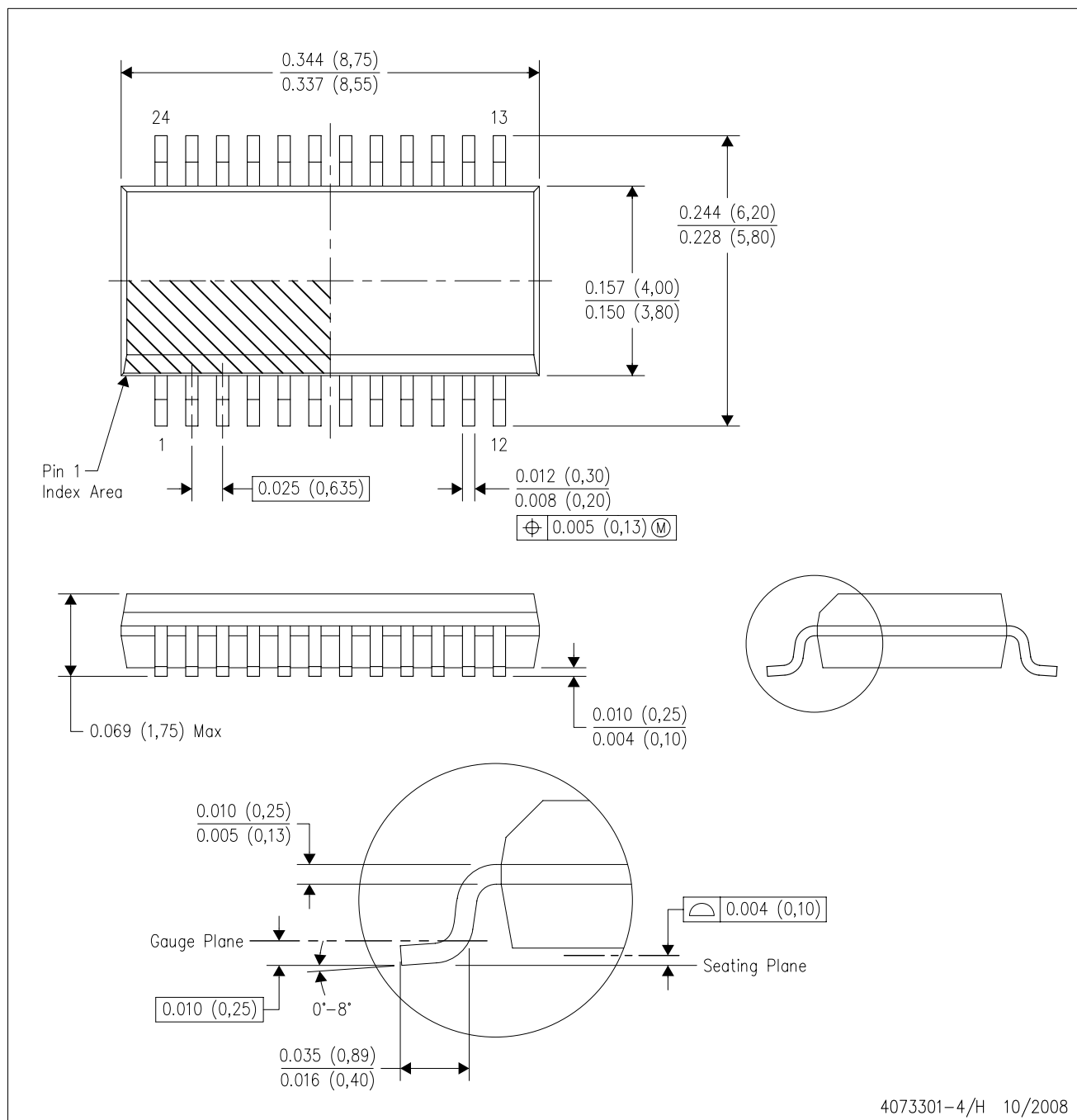
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153
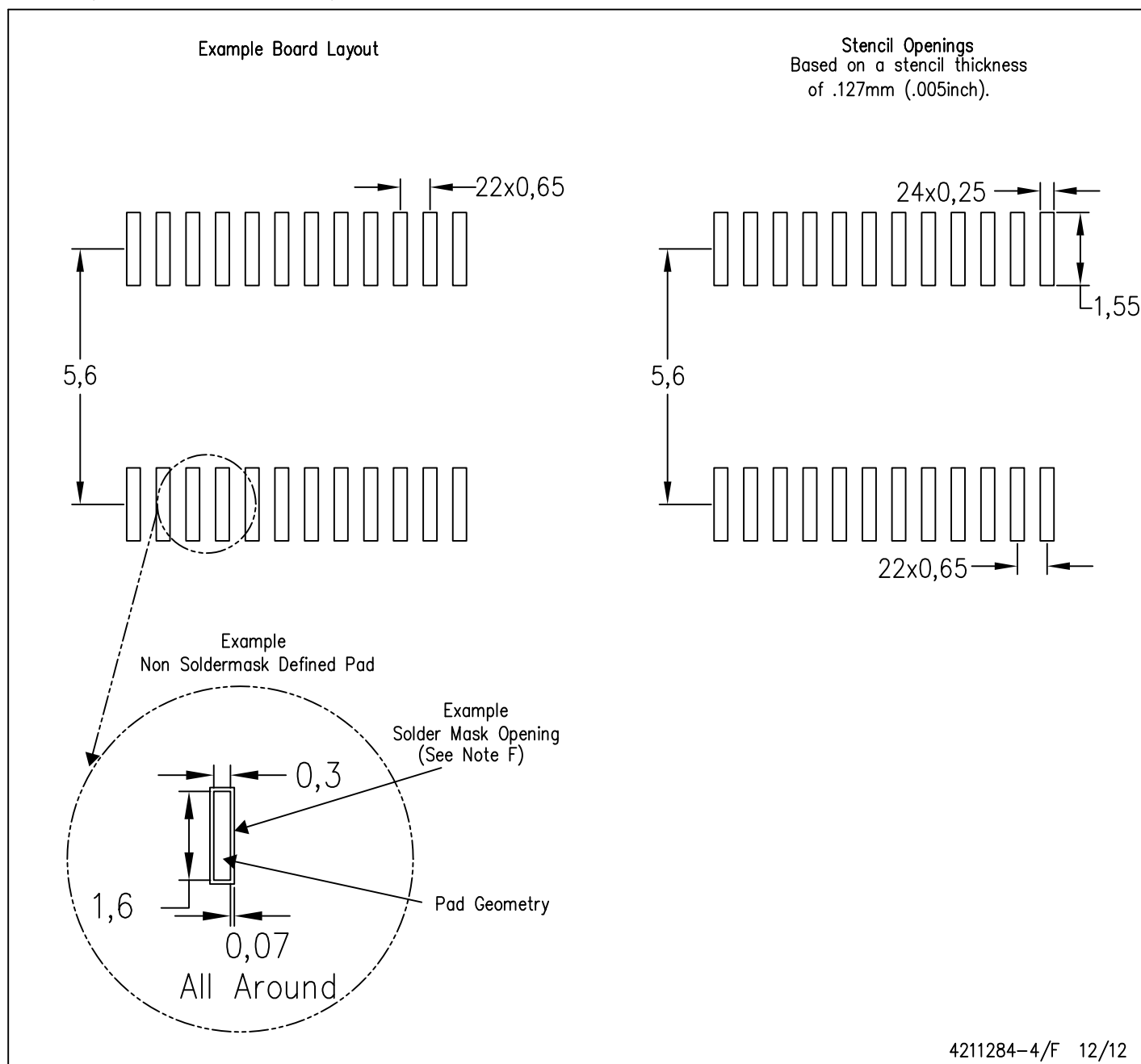
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PW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

22x0,65

24x0,25

1,55

5,6

5,6

22x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−4/F 12/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate design.
        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
        E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01
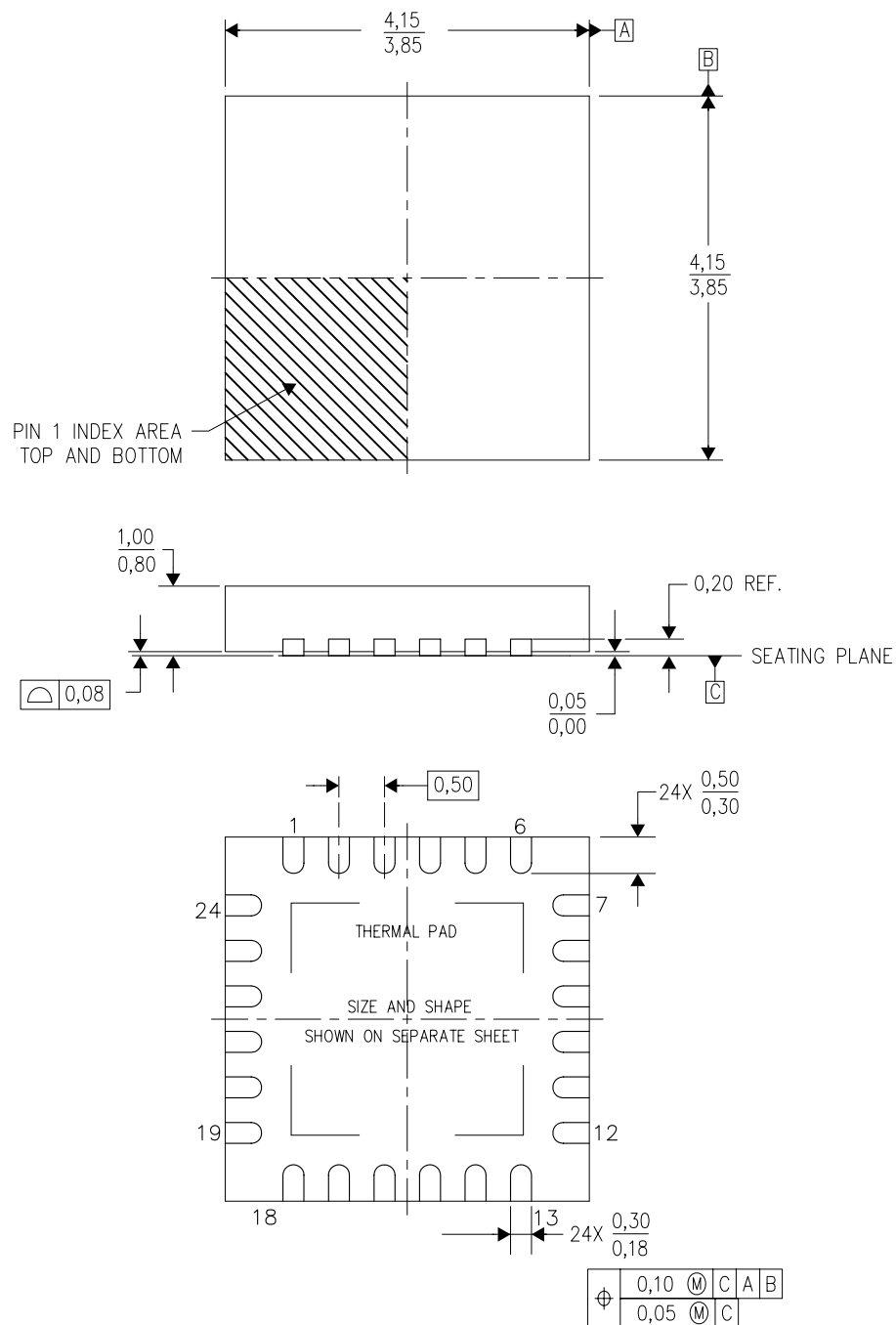
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

$\dfrac{4,15}{3,85}$ A

B

$\dfrac{4,15}{3,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\dfrac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

C

0,08

$\dfrac{0,05}{0,00}$

0,50

24X $\dfrac{0,50}{0,30}$

1   6

24   7

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

19   12

18   13   24X $\dfrac{0,30}{0,18}$

| ⊕ | 0,10 Ⓜ | C | A | B |
| | 0,05 Ⓜ | C | | |

4204104/G 07/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Quad Flatpack, No−Leads (QFN) package configuration.
        D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
        E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
        F. Falls within JEDEC MO−220.

TEXAS INSTRUMENTS
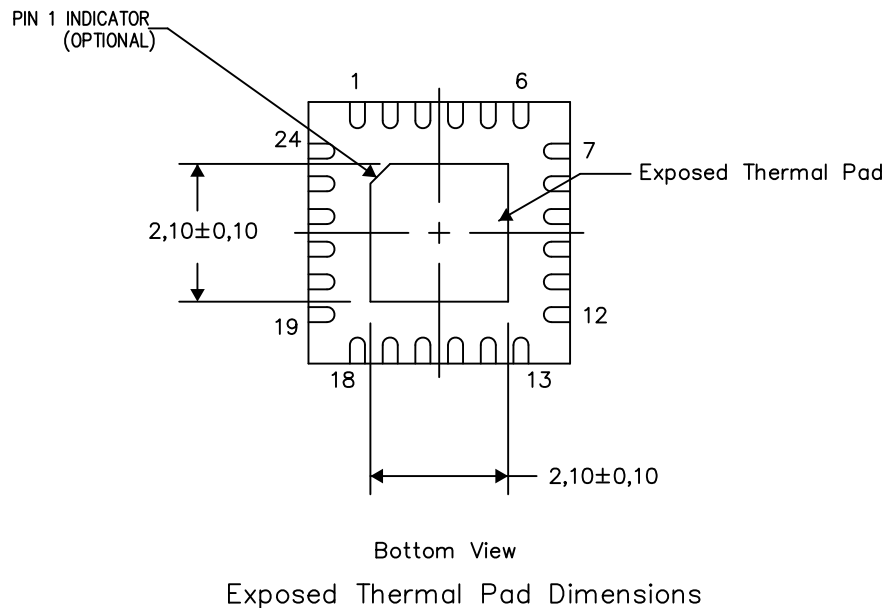www.ti.com

RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
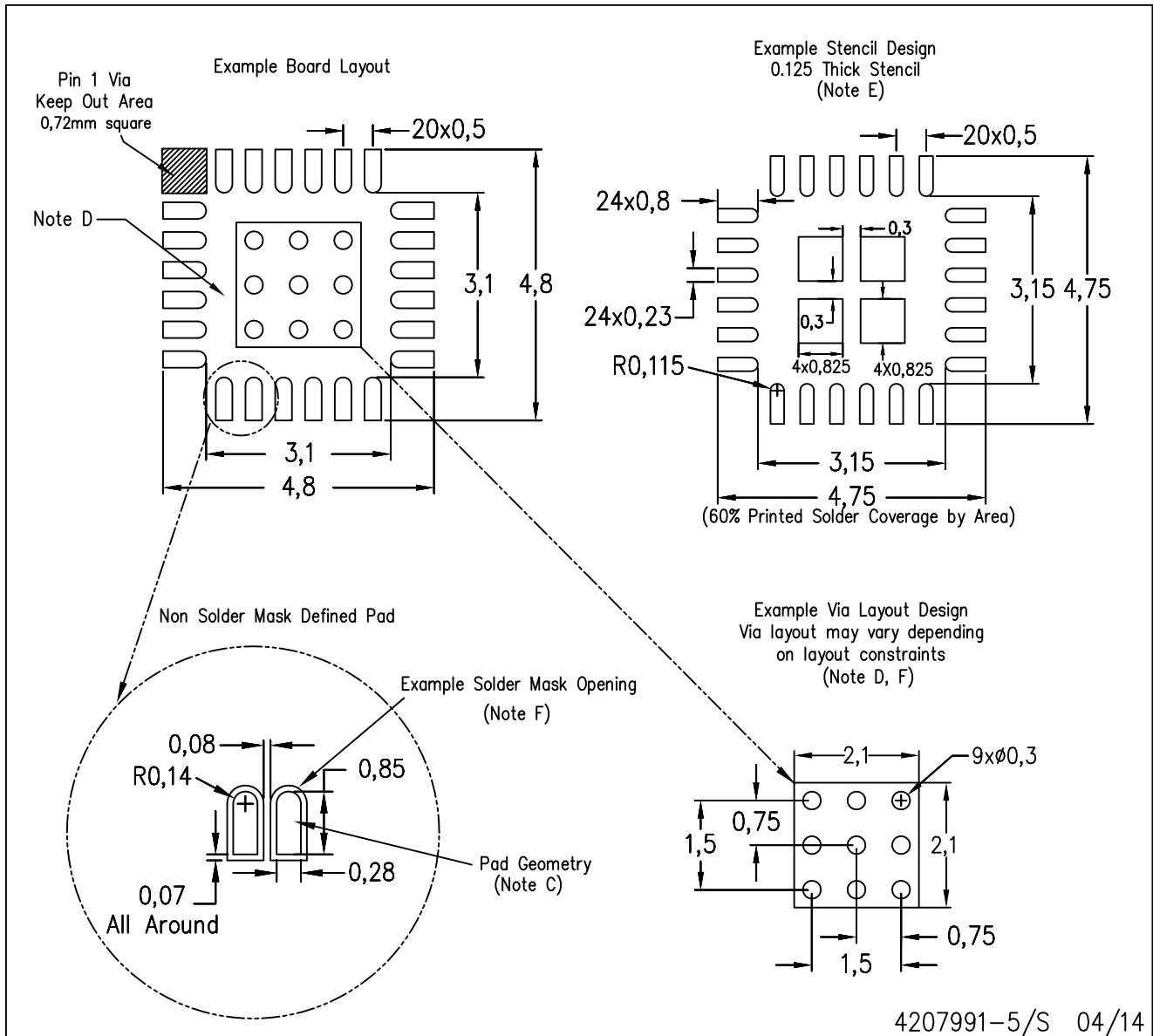(OPTIONAL)

1   6

24   7   Exposed Thermal Pad

2,10±0,10

19   12

18   13

2,10±0,10

Bottom View

Exposed Thermal Pad Dimensions

4206344−6/AH 08/14

NOTES: A. All linear dimensions are in millimeters

RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

Pin 1 Via
Keep Out Area
0,72mm square

Example Board Layout

20x0,5

Note D

3,1   4,8

3,1

4,8

Example Stencil Design
0.125 Thick Stencil
(Note E)

20x0,5

24x0,8

0,3

24x0,23

0,3

R0,115

4x0,825   4X0,825

3,15   4,75

3,15

4,75
(60% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07
All Around

0,28

Pad Geometry
(Note C)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

2,1   9xØ0,3

0,75

1,5   2,1

0,75

1,5

4207991−5/S   04/14

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
              Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout. These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design
              considerations.
         F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
              recommendations for vias placed in the thermal pad.

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