Si4022 Universal ISM Band FSK Transmitter

DESCRIPTION

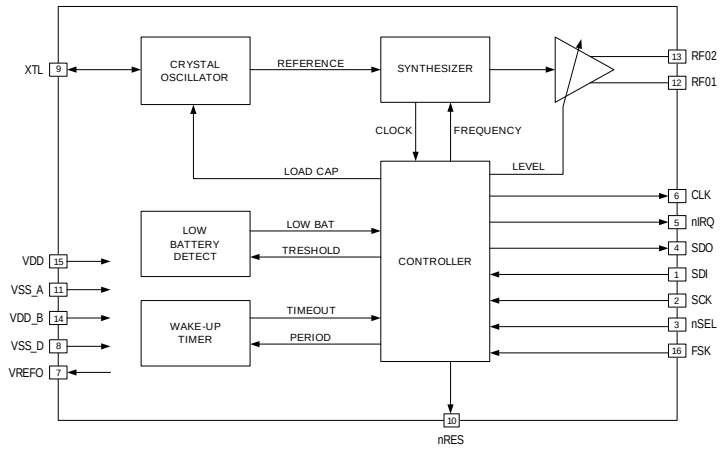
Integration's Si4022 is a single chip, low power, multi-channel FSK transmitter designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the bands at 868 and 915 MHz. Used in conjunction with Integration's FSK receivers, it is a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering is needed for operation.

The transmitter has a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency-hopping, bypassing multipath fading and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. In addition, highly stable and accurate FSK modulation is accomplished by direct closed-loop modulation with bit rates up to 115.2 kbps.

The integrated power amplifier of the transmitter has an open-collector differential output and can directly drive a loop antenna with programmable output level, no additional matching network is required. An automatic antenna tuning circuit is built in to avoid both costly trimming procedures and de-tuning due to the "hand effect".

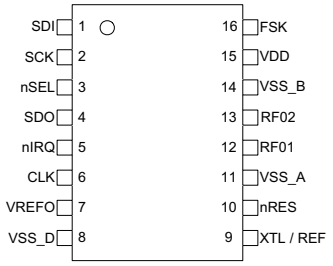
For battery-operated applications the device supports various power saving modes with wake-up interrupt generation options based on a low battery voltage detector and a sleep timer. Several additional features ease system design. Power-on reset and clock signals are provided to the microcontroller. An on-chip baud rate generator and a data FIFO are available. The transmitter is programmed and controlled via an SPI compatible interface.

FUNCTIONAL BLOCK DIAGRAM



Si4022

PIN ASSIGNMENT



This document refers to Si4022-IC Rev A0.
See www.silabs.com/integration for any applicable errata. See back page for ordering information.

FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- Stable and accurate FSK modulation with programmable deviation
- Programmable PLL loop bandwidth
- Direct loop antenna drive
- Automatic antenna tuning circuit
- Programmable output power level
- SPI bus for interfacing with microcontroller
- Clock and reset signals for microcontroller
- 64 bit TX data FIFO
- Integrated programmable crystal load capacitor
- Standard 10 MHz crystal reference
- Power-saving modes
- Multiple event handling options for wake-up activation
- Wake-up timer
- Low battery detection
- 2.2 to 3.8 V supply voltage
- Low power consumption
- Low standby current (typ. 0.3 µA)

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED FEATURE-LEVEL DESCRIPTION

The Si4022 FSK transmitter is designed to cover the unlicensed frequency bands at 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows the usage of multiple channels in any of the bands. The FSK deviation is selectable (from 20 to 160 kHz with 20 kHz increments) to accommodate various bandwidth, data rate and crystal tolerance requirements, and it is also highly accurate due to the direct closed-loop modulation of the PLL. The transmitted digital data can be sent asynchronously through the FSK pin or over the control interface using the appropriate command.

The RF VCO in the PLL performs automatic calibration, which requires only a few microseconds. To ensure proper operation in the programmed frequency band, the RF VCO is automatically calibrated upon activation of the synthesizer.

RF Power Amplifier (PA)

The power amplifier has an open-collector differential output and can directly drive a loop antenna with a programmable output power level. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and the so-called "hand effect."

Crystal Oscillator and Microcontroller Clock Output

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet. The transmitter can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. In normal operation it is divided from the reference 10 MHz. During sleep mode a low frequency (typical 32 kHz) output clock signal can be switched on.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the *Power Management Command,* the chip provides a certain number (default is 128) of further clock pulses ("clock tail") for the microcontroller to let it go to idle or sleep mode.

Low Battery Voltage Detector

The low battery detector circuit monitors periodically (typ. 8 ms) the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer

The wake-up timer has very low current consumption (4 µA max) and can be programmed from 1 ms to several hours.

It calibrates itself to the crystal oscillator at every startup and then at every 40 seconds with an accuracy of ±0.5%. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing. The periodic autocalibration feature can be turned off.

Event Handling

In order to minimize current consumption, the transmitter supports the sleep mode. Switching between the various modes is controlled by the appropriate bits in the *Power Management Command* (page 11).

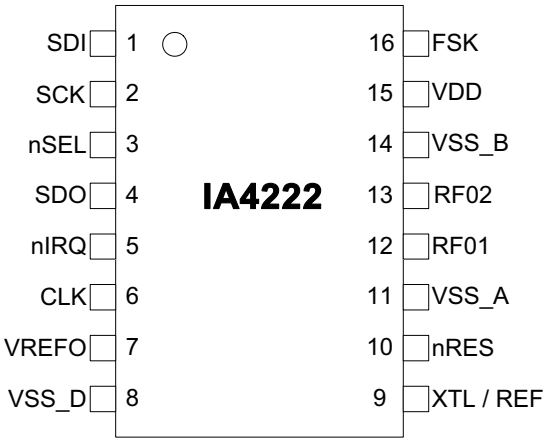
Si4022 generates an interrupt signal on several events (wake-up timer timeout, low supply voltage detection, on-chip FIFO almost empty). This signal can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the output power. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the transmitter.

PIN DEFINITION

Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



Pin	Name	Function	Type	Description
1	SDI	SDI	DI	Serial control / data input
2	SCK	SCK	DI	Serial interface clock input
3	nSEL	nSEL	DI	Chip (interface) select input (active low)
4	SDO	SDO	DO	Serial status data output
5	nIRQ	nIRQ	DO	Interrupt request output (active low)
6	CLK	CLK	DO	Clock output for the microcontroller
7	VREFO	VREFO	AO	Voltage reference output
8	VSS_D	VSS_D	S	Negative supply voltage (digital)
9	XTL / REF	XTL	AIO	Crystal connection (other terminal of crystal to VSS)
		REF	DI	External reference input
10	nRES	nRES	DO	Reset output (active low)
11	VSS_A	VSS_A	S	Negative supply voltage (analog)
12	RFO1	RFO1	AO	RF differential signal output (open collector)
13	RFO2	RFO2	AO	RF differential signal output (open collector)
14	VSS_B	VSS_B	S	Negative supply voltage (bulk)
15	VDD	VDD	S	Positive supply voltage
16	FSK	FSK	DI	Data input for asynchronous modulation

GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin	-0.5	V_{dd}+0.5	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	°C
T_{ld}	Lead temperature (soldering, max 10 s)		260	°C

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	3.8	V
T_{op}	Ambient operating temperature	-40	+85	°C

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions: T_{op} = 27 °C; V_{dd} = V_{oc} = 2.7 V)

DC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
$I_{dd,TX0}$	Supply current	868 MHz band, P_{out} = 0dBm 915 MHz band, P_{out} = 0dBm		14 15		mA
$I_{dd,TXmax}$	Supply current	868 MHz band, P_{out} = P_{max} 915 MHz band, P_{out} = P_{max}		23 24		mA
I_{pd}	Standby current (Note 1)	all blocks disabled		1		µA
I_{lb}	Low battery voltage detector and wake-up timer current				5	µA
I_x	Idle current	crystal oscillator is ON		0.5		mA
V_{lb}	Low battery detection threshold	programmable in 0.1 V steps	2.0		3.5	V
V_{lba}	Low battery detection accuracy			± 0.05		V
V_{POR}	V_{dd} threshold required to generate a POR			1.5		V
$V_{POR,hyst}$	POR hysteresis	larger glithches on the V_{dd} generate a POR even above the threshold V_{POR}		0.6		V
SR_{Vdd}	V_{dd} slew rate	for proper POR generation	0.1			V/ms

Note 1: Using a CR2032 battery (225 mAh capacity), the expected battery life is greater than 2 years using a 60-second wake-up period for sending 100 bytes packets in length at 19.2 kbps with +6 dBm output power in the 915 MHz band.

DC Characteristics (continued)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
V_{il}	Digital input low level				$0.3*V_{dd}$	V
V_{ih}	Digital input high level		$0.7*V_{dd}$			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	$V_{ih} = V_{dd}$, V_{dd} = 3.8 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

AC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{LO}	Transmitter frequency	868 MHz band, 20 kHz resolution 915 MHz band, 20 kHz resolution	801.92 881.92		878.06 958.06	MHz
f_{ref}	PLL reference frequency	(Note 1)	9	10	11	MHz
f_{res}	PLL frequency resolution			20		kHz
t_{lock}	PLL lock time	Frequency error < 1kHz after 1 MHz step		30		µs
t_{sp}	PLL startup time	Initial calibration after power-up with running crystal oscillator			500	µs
C_{xl}	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance +/- 10%	8.5		16	pF
t_{POR}	Internal POR pulse width (Note 2)	After V_{dd} has reached 90% of final value		50	100	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ω		2	5	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 40 seconds (Note 3)	0.995	1	1.005	ms
$t_{wake-up}$	Programmable wake-up time		1		$8.4*10^6$	ms

Note 1: Using anything but a 10 MHz crystal is allowed but not recommended because all crystal-referred timing and frequency parameters will change accordingly.

Note 2: No command are accepted by the chip during this period.

Note 3: Autocalibration can be turned off.

AC Characteristics (continued)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
BR	FSK bit rate	(Note 4)			115.2	kbps
I_{out}	Open collector output current	Adjustable in 8 steps	0.5		6	mA
P_{max}	Available output power	With optimal antenna impedance (Note 5)		6		dBm
P_{out}	Typical output power	Adjustable in 8 steps (3 dB/step)	P_{max} - 21		P_{max}	dBm
P_{sp}	Spurious emission	Out of band, EIRP (Note 6)			-52	dBm
C_{out}	Output capacitance	Set by the automatic antenna tuning circuit	1.6	2.2	2.8	pF
Q_{out}	Quality factor of the output capacitance		16	18	22	
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier (Note 4)		-85 -105		dBc/Hz
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns
$t_{r, f, ckout}$	Clock output rise/fall time	10 pF pure capacitive load			15	ns
$f_{ckout, slow}$	Slow clock frequency	Tolerance +/- 1 kHz		32		kHz

Setting (bw1, bw0)	Max. datarate [kbps]	Phase noise at 1 MHz offset [dBc/Hz]	PLL bandwidth
00	19.2	-112	15 kHz
01	38.4	-110	30 kHz
10	64	-107	60 kHz (POR default)
11	115.2	-102	120 kHz

Band	$Y_{antenna}$ [S]	$Z_{antenna}$ [Ω]	$L_{antenna}$ [nH]
868 MHz	1.35E-3 – j1.2E-2	9 + j82	15.2
915 MHz	1.45E-3 – j1.3E-2	8.7 + j77	13.6

Note 4: The maximum FSK bitrate and the output phase noise are dependent on the PLL settings (with the *Extended Features Command*).

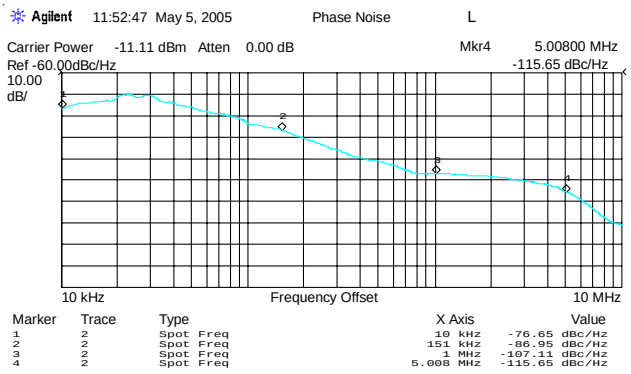
Note 5: Optimal antenna / admittance / inductance for the Si4022

Note 6: With selective resonant antennas (see: Application Notes available from http://www.silabs.com/integration).

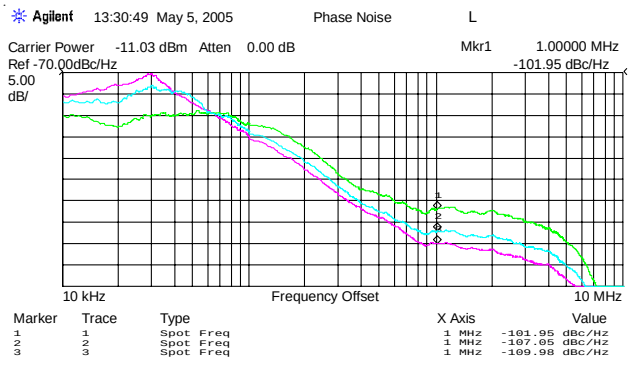
TYPICAL PERFORMANCE DATA

Phase noise measurements in the 868 MHz ISM band

50% Charge pump current setting (Ref. level: -60 dBc/Hz, 10 dB/div)



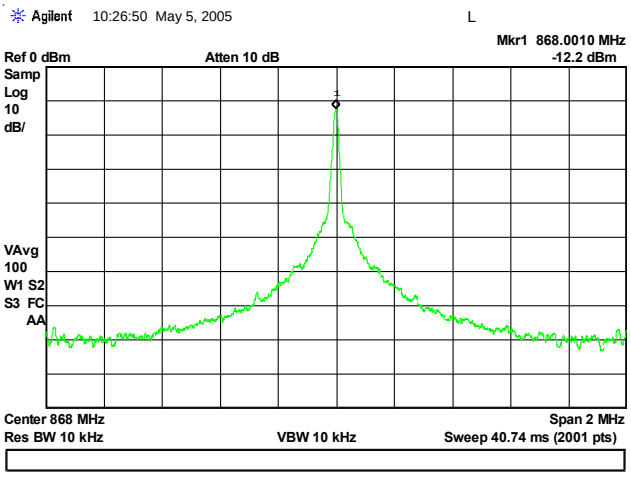
100, 50, 33% Charge pump current settings (Ref. level: -70 dBc/Hz, 5 dB/div)



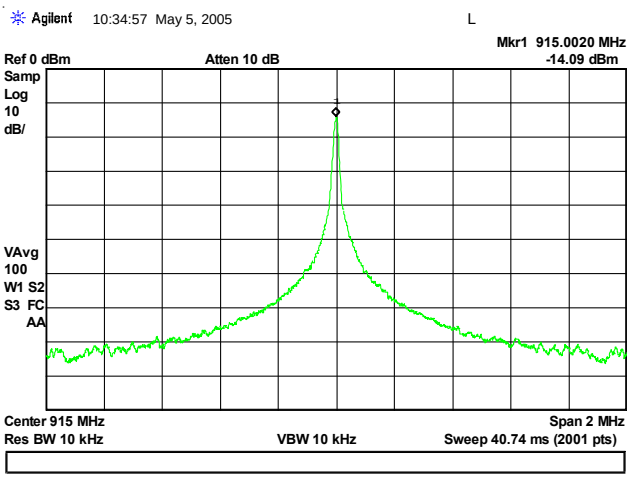
Unmodulated RF Spectrum

The output spectrum is measured at different frequencies. The output is loaded with 50 Ohm through a matching network.

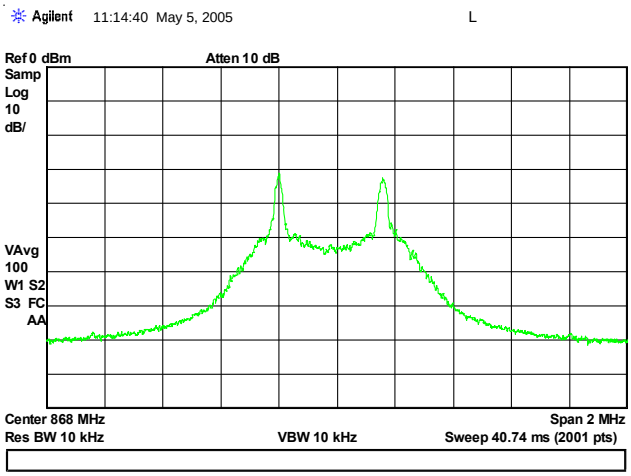
At 868 MHz



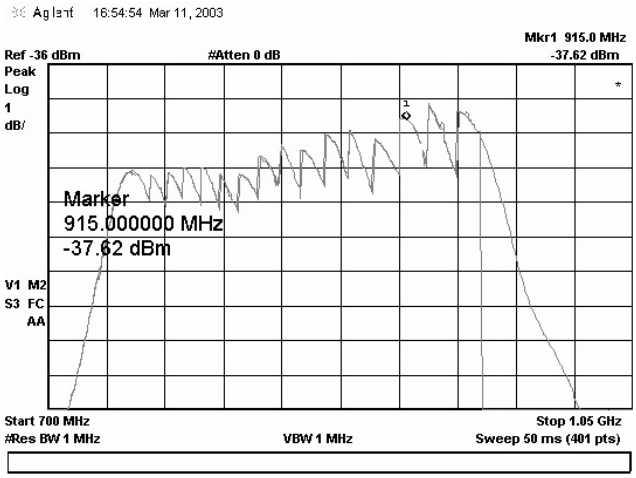
At 915 MHz



At 868 MHz with
180 kHz Deviation at 9.6 kbps



Antenna Tuning Characteristics
750–970 MHz



The antenna tuning characteristics was recorded in “max-hold” state of the spectrum analyzer. During the measurement, the transmitters were forced to change frequencies by forcing an external reference signal to the XTL pin. While the carrier was changing the antenna tuning circuit switched trough all the available states of the tuning circuit. The graph clearly demonstrates that while the complete output circuit had about a 40 MHz bandwidth, the tuning allows operating in a 220 MHz band. In other words the tuning circuit can compensate for 25% variation in the resonant frequency due to any process or manufacturing spread.

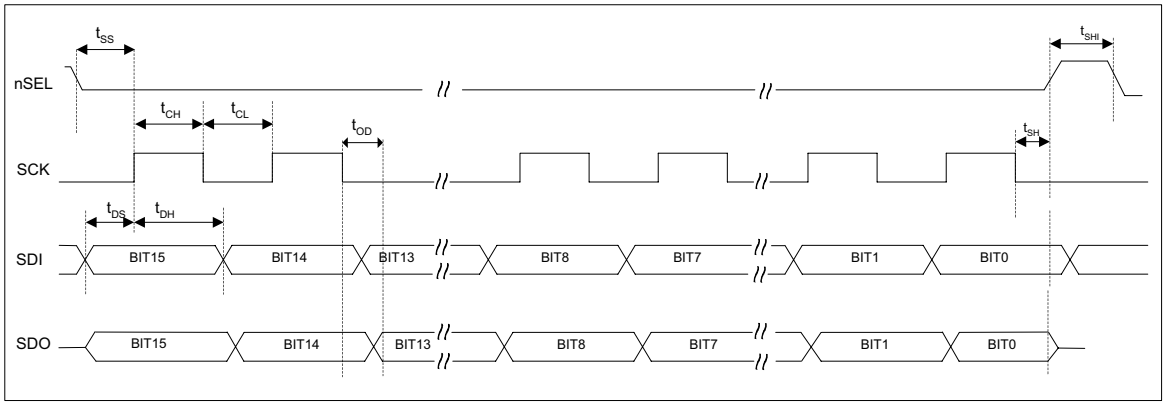
CONTROL INTERFACE

Commands to the transmitters are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8 (except for the *Transmitter FIFO Write Command*). All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control and command registers.

Timing Specification

Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram



Control Commands

Control Word	Related Parameters/Functions
Configuration Setting Command	frequency band and deviation, output power, crystal oscillator load capacitance
Frequency Setting Command	frequency of the local oscillator
Power Managament Command	crystal oscillator, synthesizer, power amplifier, low battery detector, wake-up timer, clock output buffer
Transmitter FIFO Write Command	transmitter FIFO write
FIFO Setting Command	FIFO functions
Data Rate Command	bit rate
Low Battery and Microcontroller Clock Divider Command	LBD voltage threshold and microcontroller clock division ratio
Wake-up Timer Command	wake-up time period
Extended Wake-up Timer Command	wake-up time period finer adjustment
Extended Features Command	low frequency output clock, wake-up timer extra functions
Status Register Read Command	transmitter status read

Note: In the following tables the POR column shows the default values of the command registers after power-on.

Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	bs	p2	p1	p0	x3	x2	x1	x0	ms	m2	m1	m0	9082h

bs	Frequency Band [MHz]
0	868
1	915

p2	p1	p0	Output Power [dBm]
0	0	0	0
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-18
1	1	1	-21

The output power is given in the table as relative to the maximum available power, which depends on the actual antenna impedance. (See: Antenna Application Note available from http://www.silabs.com/integration).

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
.....				....
1	1	1	0	15.5
1	1	1	1	16.0

The resulting output frequency can be calculated as:

$$f_{out} = f_0 - (-1)^{SIGN} * (M + 1) * (20\ kHz)$$

where:

f_0 is the channel center frequency (see the next command)

M is the three bit binary number <*m2 : m0*>

SIGN = (*ms*) XOR (FSK input)

Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	AD57h

The 12-bit parameter of the *Frequency Setting Command <f11 : f0>* has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as:

$$f_0 = 8 * 10\ MHz * (C + F/4000)$$

The constant C is determined by the selected band as:

Band [MHz]	C
868	10
915	11

Power Management Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	0	0	ex	es	etr	eb	et	dc	C002h

Bit 5 <*ex*>: Enables the the crystal oscillator.

Bit 4 <*es*>: Enables the synthesizer.

Bit 3 <*etr*>: Enables the power amplifier. If the *ex* and *es* bit is not set, it switches on the crystal oscillator and the synthesizer as well.
In FIFO mode (bit *fe* is set in the *FIFO Setting Command*) setting this bit will roll out the content of the FIFO.

Bit 2 <*eb*>: Enables the low battery detector.

Bit 1 <*et*>: Enables the wake-up timer.

Bit 0 <*dc*>: Disables the clock output buffer.

Note: If faster operation is needed, then leave *ex* and *es* bit set to '1' and toggle only the *etr* bit.

Power Saving Modes

The different operating modes of the chip depend on the following control bits:

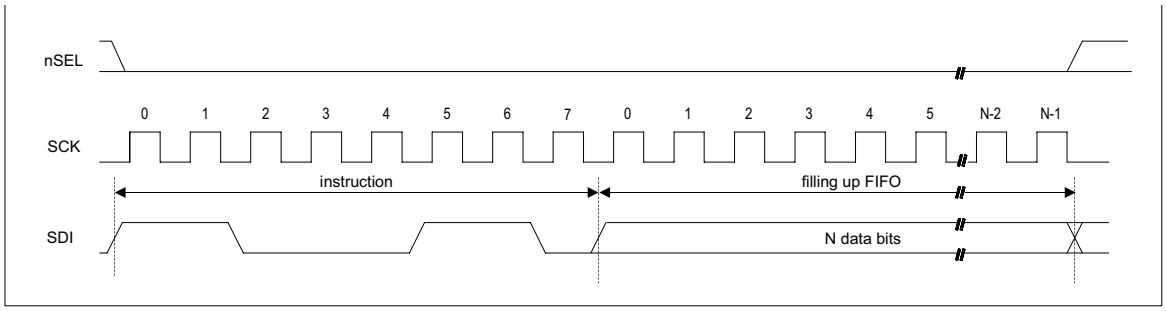
Operating Mode	eb or et	es	etr	ex
Active (transmit)	X	x	1	x
Idle	X	0	0	1
Sleep	1	0	0	0
Standby	0	0	0	0

Transmitter FIFO Write Command

Bit	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	-

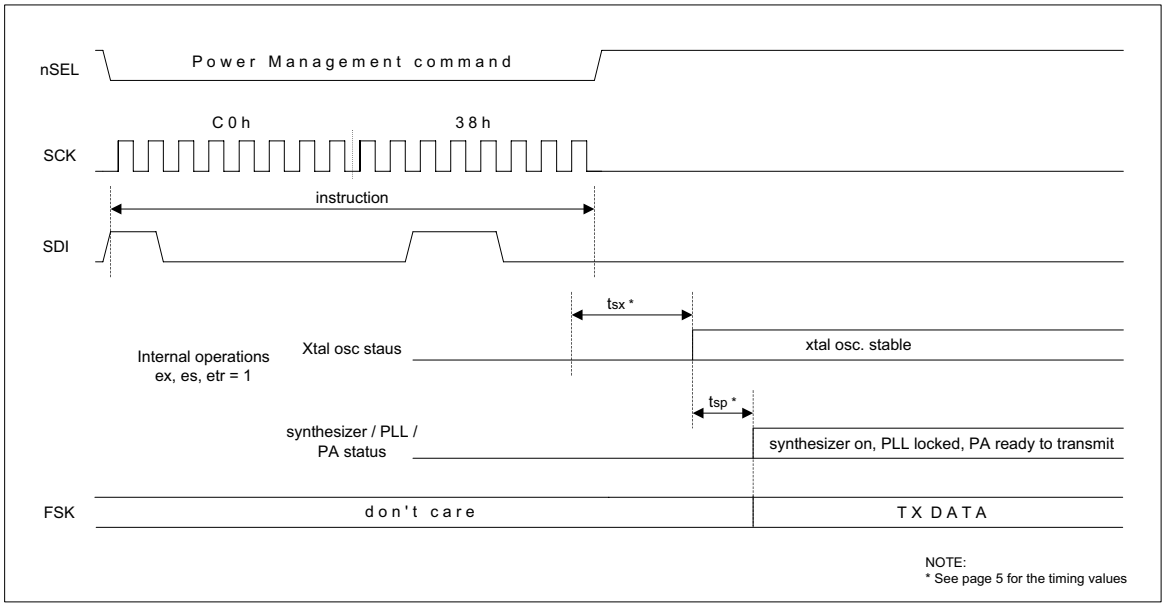
With this command, the controller can write databits to the transmitter FIFO. Bit *(fe)* must be set in the *FIFO Setting Command.*

Transmitter FIFO register write



Data Transmit Sequence Through the FSK Pin

It is possible to transmit data without the FIFO by using the FSK input pin. In that case the power amplifier should be enabled first with the *Power Management Comand.*



Note:

- If the crystal oscillator was formerly switched off (*ex*=0), the internal oscillator needs t_{sx} time, to switch on. The actual value depends on the type of quartz crystal used.
- If the synthesizer was formerly switched off (*es*=0), the internal PLL needs t_{sp} startup time. Valid data can be transmitted only when the internal locking process is finished.

FIFO Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	fe	0	f5	f4	f3	f2	f1	f0	CE00h

Bit 7 <*fe*>: Enables the 64 bit transmit FIFO. Resetting this bit clears the contents of the FIFO.

Bit 5-0 <*f5* : *f0*>: FIFO IT level. The FIFO generates IT when number of the remaining data bits in the FIFO reaches this level.

Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C813h

The bit rate of the transmitted data stream is determined by the 7-bit value R (bits *r6* to *r0*) and the 1 bit *cs*.

BR = 10 MHz / 29 / (R+1) / (*1* + *cs**7)

In the receiver set R according the next function:

R= (10 MHz / 29 /(*1* + *cs**7)/ BR) – 1

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

Low Battery and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	d2	d1	d0	elfc	t3	t2	t1	t0	C213h

The 4-bit value T of *t3-t0* determines the threshold voltage of the threshold voltage V_{lb} of the detector:

$$V_{lb} = 2.0\ V + T * 0.1\ V$$

Bit 4 <*elfc*>: Enables low frequency (32 kHz) microcontroller output clock during sleep mode.

Clock divider configuration (valid only if the crystal oscillator is on):

d2	d1	d0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	0	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by M <*m13* : *m0*> , R <*r3* : *r0*> and D <*d1* : *d0*>:

$$T_{wake\text{-}up} = M * 2^{R\text{-}D}\ ms$$

Note: • The wake-up timer generates interrupts continuously at the programmed interval while the *et* bit is set.

Extended Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	1	d1	d0	m13	m12	m11	m10	m9	m8	C300h

These bits can be used for further fine adjustment of the wake-up timer. The explanation of the bits can be found above.

Extended Features Command:

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	0	0	0	exlp	ctls	0	dcal	bw1	bw0	dsfi	ewi	B0CAh

Bit 7 <*exlp*>: Enables low power mode for the crystal oscillator.

Bit 6 <*ctls*>: Clock tail selection bit. Setting this bit selects 512 cycle long clock tail instead of the default 128.

Bit 4 <*dcal*>: Disables the wake-up timer autocalibration.

Bit 3-2 <*bw1:bw0*>: Select the bandwidth of the PLL.

bw1	bw0	PLL bandwidth
0	0	15 kHz
0	1	30 kHz
1	0	60 kHz
1	1	120 kHz

Bit 1 <*dsfi*>: Disables autosleep on FIFO interrupt if set to 1.

Bit 0 <*ewi*>: Enables the automatic wake-up on any interrupt event.

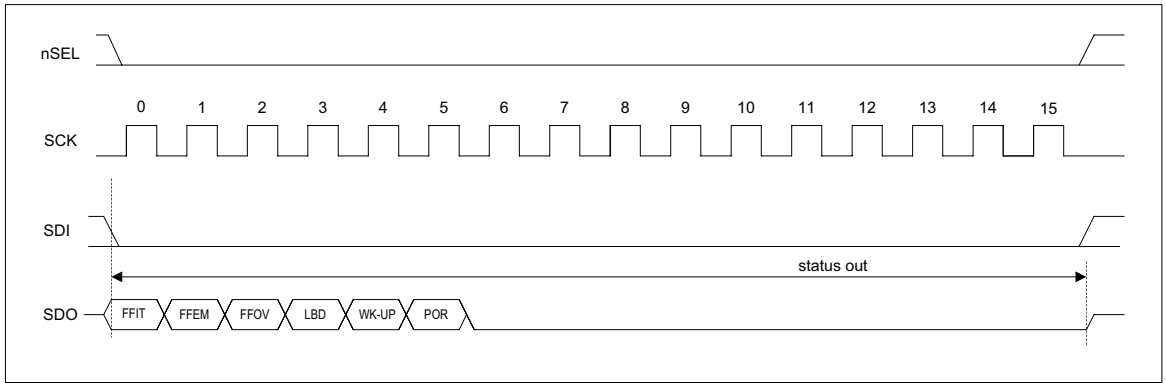
Status Register Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-

With this command, it is possible to read the status register of the chip through the SDO pin.

FFIT	The number of data bits in the FIFO has gone below the preprogrammed limit
FFEM	FIFO is empty
FFOV	FIFO overflow
LBD	Low battery detect, the power supply voltage is below the preprogrammed limit
WK-UP	Wake-up timer overflow
POR	Power-on reset

Status Register Read Sequence



Dual Clock Output

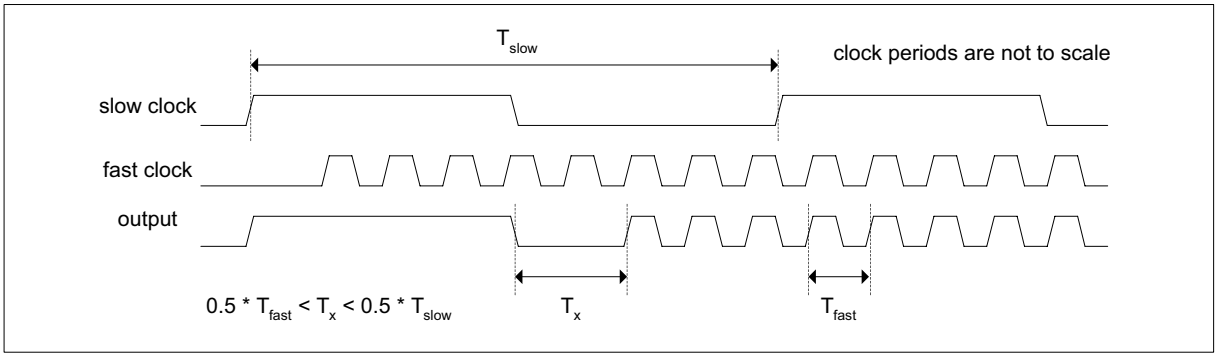
When the chip is switched into idle mode, the 10 MHz crystal oscillator starts. After oscillation ramp-up a 1 MHz clock signal is available on the CLK pin. This (fast) clock frequency can be reprogrammed during operation with the *Low Battery and Microcontroller Clock Divider Command* (page13). During startup and in sleep or standby mode (crystal oscillator disabled), the CLK output is pulled to logic low.

On the same pin a low frequency clock signal can be obtained if the *elfc* bit is set in the *Low Battery and Microcontroller Clock Divider Command*. The clock frequency is 32 kHz which is derived from the low-power RC oscillator of the wake-up timer. In order to use this slow clock the wake-up timer should be enabled by setting the *et* bit in the *Power Management Command* (page 11) even if the wake-up timer itself is not used.

Slow clock feature can be enabled by entering into sleep mode (page 11). Driving the output will increase the sleep mode supply current. Actual worst-case value can be determined when the exact load and min/max operating conditions are defined. After power-on reset the chip goes into sleep mode and the slow frequency clock appears on the CLK pin.

Switching back into fast clock mode can be done by setting the *ex* or *etr* bits in the approriate commands. It is important to leave bit *dc* in the *Power Management Command* at its default state (0) otherwise there will be no clock signal on the CLK pin.

Switching between the fast and slow clock modes is glitch-free in a sense that either state of the clock lasts for at least a half cycle of the fast clock. During switching the clock can be logic low once for an intermediate period i.e. for any time between the half cycle of the fast and the slow clock.



The clock switching synchronization circuit detects the falling edges of the clocks. One consequence is a latency of 0 to $T_{slow} + T_{fast}$ from the occurrence of a clock change request (entering into sleep mode or interrupt) until the beginning of the intermediate length (T_x) half cycle. The other is that both clocks should be up and running for the change to occur. Changing from fast to slow clock, it is automatically ensured by entering into the sleep mode in the appropriate way provided that the wake-up timer is continouosly enabled. As the crystal oscillator is normally stopped while the slow clock is used, when changing back to fast clock the crystal oscillator startup time has to pass first before the above mentioned latency period starts. The startup condition is detected internally, so no software timing is necessary.

Wake-Up Timer Calibration

By default the wake-up timer is calibrated each time it is enabled by setting the *et* bit in the *Power Management Command*. After timeout the timer can be stopped by resetting this bit otherwise it operates continuously. If the timer is programmed to run for longer periods, at approximately every 40 seconds it performs additional self-calibration.

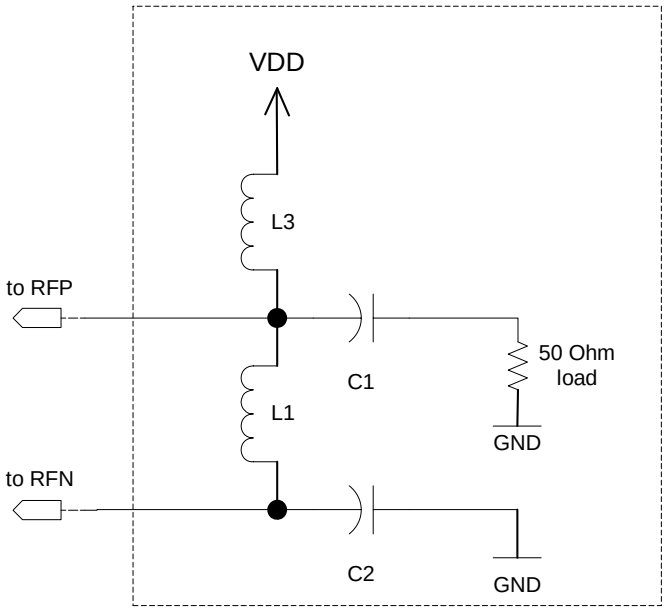
This feature can be disabled to avoid sudden changes in the actual wake-up time period. A suitable software algorithm can then compensate for the gradual shift caused by temperature change.

Bit *dcal* in the *Extended Features Command* (page 14) controls the automatic calibration feature. It is reset to 0 at power-on and the automatic calibration is enabled. This is necessary to compensate for process tolerances. After one calibration cycle further (re)calibration can be disabled by setting this bit to 1.

MATCHING NETWORK FOR A 50 OHM SINGLE ENDED OUTPUT

Matching Network Schematic

C_1 , C_2 [pF]	3.9
L_1 [nH]	6.8
L_3 [nH]	100



RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the Si4022 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 300 ohms ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup. It is recommended to keep the PCB parasitic capacitances on the XTL pin as low as possible.

The crystal frequency is used as the reference of the PLL, which generates the RF carrier frequency (f_c). Therefore f_c is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable carrier frequency error.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4 kbps

	Transmitter Deviation [+/- kHz]							
	20	**40**	**60**	**80**	**100**	**120**	**140**	**160**
868	2	12	25	30	40	50	70	80
915	2	12	20	30	40	50	60	70

Bit Rate: 9.6 kbps

	Transmitter Deviation [+/- kHz]							
	20	**40**	**60**	**80**	**100**	**120**	**140**	**160**
868	do not use	8	20	30	40	50	60	70
915	do not use	8	15	30	40	50	60	70

Bit Rate: 38.4 kbps

	Transmitter Deviation [+/- kHz]							
	20	**40**	**60**	**80**	**100**	**120**	**140**	**160**
868	do not use	do not use	10	20	30	40	50	70
915	do not use	do not use	10	20	30	40	50	60

Bit Rate: 115.2 kbps

	Transmitter Deviation [+/- kHz]							
	20	**40**	**60**	**80**	**100**	**120**	**140**	**160**
868	do not use	do not use	do not use	do not use	do not use	2	12	25
915	do not use	do not use	do not use	do not use	do not use	2	12	20

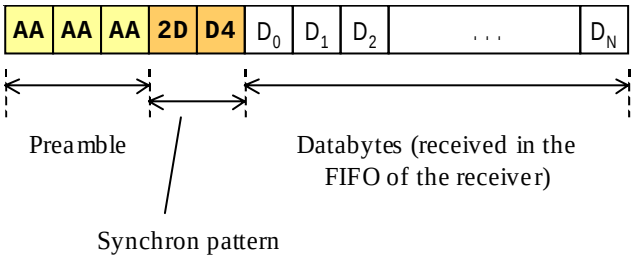
Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C_0.

Note: There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.

EXAMPLE APPLICATIONS: DATA PACKET TRANSMISSION

Data packet structure

An example data packet structure using theSi4022 –Si4022 pair for data transmission. This packet structure is an example of how to use the high efficiency FIFO mode at the receiver side:



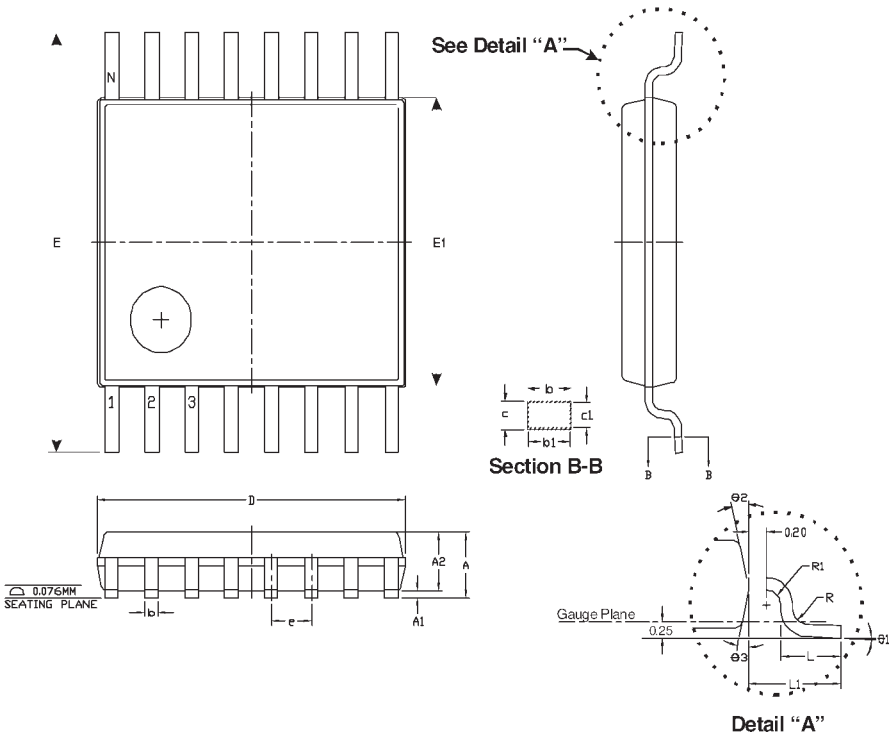
The first 3 bytes compose a 24 bit length '01' pattern to let enough time for the clock recovery of the receiver to lock. The next two bytes compose a 16 bit synchron pattern which is essential for the receiver's FIFO to find the byte synchron in the received bit stream. The synchron patters is followed by the payload. The first byte transmitted after the synchron pattern (D_0 in the picture above) will be the first received byte in the FIFO.

Important: The bytes of the data stream should follow each other continuously, otherwise the clock recovery circuit of the receiver side will be unable to track.

Further details of packet structures can be found in the IA ISM-UGSB1 software development kit manual.

PACKAGE INFORMATION

16-pin TSSOP



Symbol	Dimensions in mm			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			1,20			0,047
A1	0,05		0,15	0,002		0,006
A2	0,80	0,90	1,05	0,031	0,035	0,041
b	0,19		0,30	0,007		0,012
b1	0,19	0,22	0,25	0,007	0,009	0,010
c	0,09		0,20	0,004		0,008
c1	0,09		0,16	0,004		0,006
D	4,90	5,00	5,10	0,193	0,197	0,201
e		0.65 BSC.			0.026 BSC.	
E		6.40 BSC.			0.252 BSC.	
E1	4,30	4,40	4,50	0,169	0,173	0,177
L	0,50	0,60	0,75	0,020	0,024	0,030
L1		1.00 REF.			0.39 REF.	
R	0,09			0,004		
R1	0,09			0,004		
θ1	0		8	0		8
θ2		12 REF.			12 REF.	
θ3		12 REF.			12 REF.	

ORDERING INFORMATION

Si4022 Universal ISM Band FSK Transmitter

DESCRIPTION	ORDERING NUMBER
Si4022 16-pin TSSOP	Si4022-IC CC16 Rev A0
die	see Silicon Labs

Demo Boards and Development Kits

DESCRIPTION	ORDERING NUMBER
ISM Chipset Development Kit	IA ISM – DK3

Related Resources

DESCRIPTION	ORDERING NUMBER
Antenna Selection Guide	IA ISM – AN1
Antenna Development Guide	IA ISM – AN2
IA4322 Universal ISM Band FSK Receiver	see http://www.silabs.com/integration for details

Note: Volume orders must include chip revision to be accepted.

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