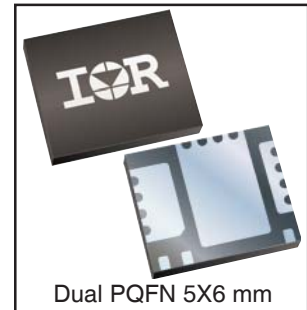
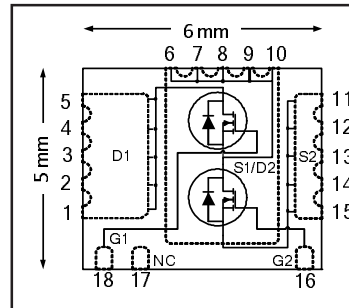


HEXFET® Power MOSFET

	Q1	Q2	
V_{DS}	30	30	V
$R_{DS(on)}$ max (@ $V_{GS} = 10V$)	8.6	3.0	mΩ
Q_g (typical)	8.3	34	nC
I_D (@ $T_A = 25^\circ C$)	13	28	A



Applications

- Control and synchronous MOSFET for buck converters

Features and Benefits

Features

Control and synchronous FET in one package
Low charge control MOSFET (8.3 nC typical)
Low $R_{DS(on)}$ synchronous MOSFET (< 3.0 mΩ)
100% Rg tested
Low Profile (≤ 0.9 mm)
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL2, Consumer Qualification

results in



Benefits

Increased power density (50% vs two PQFN 5x6)
Lower switching losses
Lower conduction losses
Increased reliability
Increased power density
Easier manufacturing
Environmentally Friendlier
Increased reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFH7911TRPbF	PQFN 5mm x 6mm	Tape and Reel	4000	
IRFH7911TR2PbF	PQFN 5mm x 6mm	Tape and Reel	400	EOL notice # 259

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V _{DS}	Drain-to-Source Voltage	30		V
V _{GS}	Gate-to-Source Voltage	± 20		
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	13	28	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	10	23	
I _{DM}	Pulsed Drain Current ①	100	230	
P _D @T _A = 25°C	Power Dissipation	2.4	3.4	W
P _D @T _A = 70°C	Power Dissipation	1.5	2.2	
	Linear Derating Factor ⑤	0.019	0.027	W/°C
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	7.7	2.5	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient ⑤	53	37	

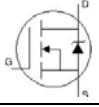
Static @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	Q1&Q2	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	Q1	—	0.021	—	V/°C	Reference to 25°C, I _D = 1mA
		Q2	—	0.022	—		
R _{DS(on)}	Static Drain-to-Source On-Resistance	Q1	—	7.2	8.6	mΩ	V _{GS} = 10V, I _D = 12A ③
			—	11.1	14.5		V _{GS} = 4.5V, I _D = 10A ③
		Q2	—	2.4	3.0		V _{GS} = 10V, I _D = 26A ③
			—	3.4	4.0		V _{GS} = 4.5V, I _D = 21A ③
V _{GS(th)}	Gate Threshold Voltage	Q1&Q2	1.35	—	2.35	V	Q1: V _{DS} = V _{GS} , I _D = 25μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	Q1	—	-6.8	—	mV/°C	Q2: V _{DS} = V _{GS} , I _D = 100μA
		Q2	—	-6.4	—		
I _{DSS}	Drain-to-Source Leakage Current	Q1&Q2	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		Q1&Q2	—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	Q1&Q2	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	Q1&Q2	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	Q1	17	—	—	S	V _{DS} = 15V, I _D = 10A
		Q2	106	—	—		V _{DS} = 15V, I _D = 21A
Q _g	Total Gate Charge	Q1	—	8.3	12	nC	Q1 V _{DS} = 15V V _{GS} = 4.5V, I _D = 10A
		Q2	—	34	51		
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	Q1	—	2.0	—		
		Q2	—	7.9	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	Q1	—	1.0	—		
		Q2	—	3.6	—		
Q _{gd}	Gate-to-Drain Charge	Q1	—	3.2	—		
		Q2	—	11	—		
Q _{godr}	Gate Charge Overdrive	Q1	—	2.1	—		
		Q2	—	12	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	Q1	—	4.2	—	nC	Q2 V _{DS} = 15V V _{GS} = 4.5V, I _D = 21A
		Q2	—	15	—		
Q _{oss}	Output Charge	Q1	—	5.0	—	nC	V _{DS} = 16V, V _{GS} = 0V
		Q2	—	19	—		
R _G	Gate Resistance	Q1	—	1.8	—	Ω	
		Q2	—	0.7	—		
t _{d(on)}	Turn-On Delay Time	Q1	—	12	—	ns	Q1 V _{DD} = 15V, V _{GS} = 4.5V I _D = 10A R _G = 1.8Ω
		Q2	—	22	—		
t _r	Rise Time	Q1	—	15	—		
		Q2	—	35	—		
t _{d(off)}	Turn-Off Delay Time	Q1	—	12	—		
		Q2	—	28	—		
t _f	Fall Time	Q1	—	5.9	—	pF	Q2 V _{DD} = 15V, V _{GS} = 4.5V I _D = 21A R _G = 1.8Ω
		Q2	—	14	—		
C _{iss}	Input Capacitance	Q1	—	1060	—		
		Q2	—	4450	—		
C _{oss}	Output Capacitance	Q1	—	230	—		
		Q2	—	850	—		
C _{rss}	Reverse Transfer Capacitance	Q1	—	110	—	pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
		Q2	—	440	—		

Avalanche Characteristics

	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	12	32	mJ
I _{AR}	Avalanche Current ①	—	10	21	A

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	Q1	—	—	3.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
		Q2	—	—	3.0		
I _{SM}	Pulsed Source Current (Body Diode) ①	Q1	—	—	100	A	T _J = 25°C, I _S = 10A, V _{GS} = 0V ③
		Q2	—	—	230		
V _{SD}	Diode Forward Voltage	Q1	—	—	1.0	V	T _J = 25°C, I _S = 21A, V _{GS} = 0V ③
		Q2	—	—	1.0		
t _{rr}	Reverse Recovery Time	Q1	—	13	20	ns	Q1 T _J = 25°C, I _F = 10A, V _{DD} = 15V, di/dt = 300A/μs ③
		Q2	—	20	29		
Q _{rr}	Reverse Recovery Charge	Q1	—	13	20	nC	Q2 T _J = 25°C, I _F = 21A, V _{DD} = 15V, di/dt = 280A/μs ③
		Q2	—	24	36		

Typical Characteristics

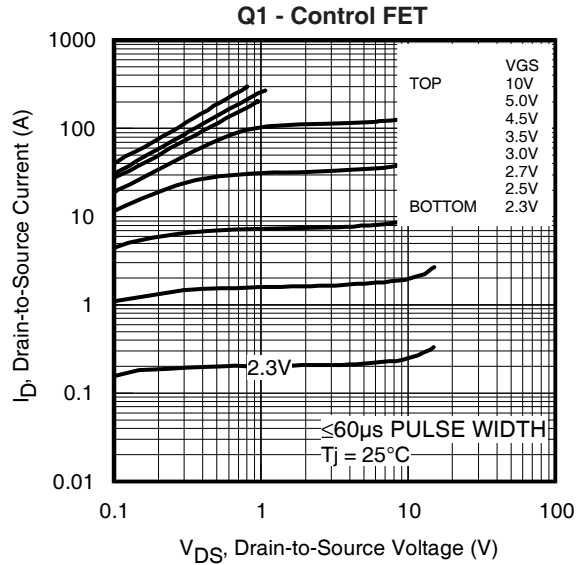


Fig 1. Typical Output Characteristics

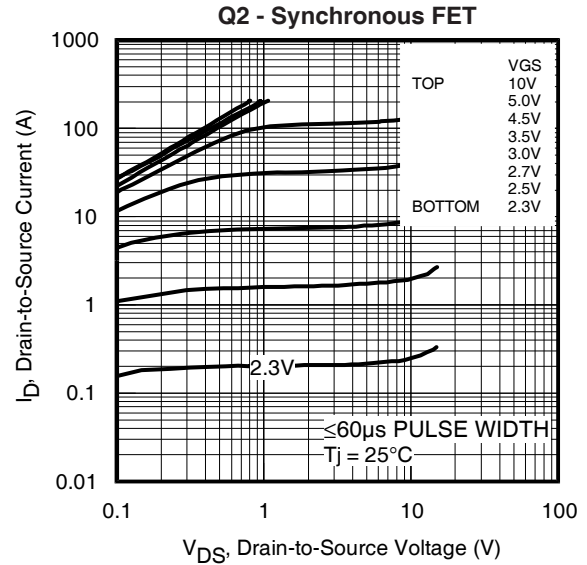


Fig 2. Typical Output Characteristics

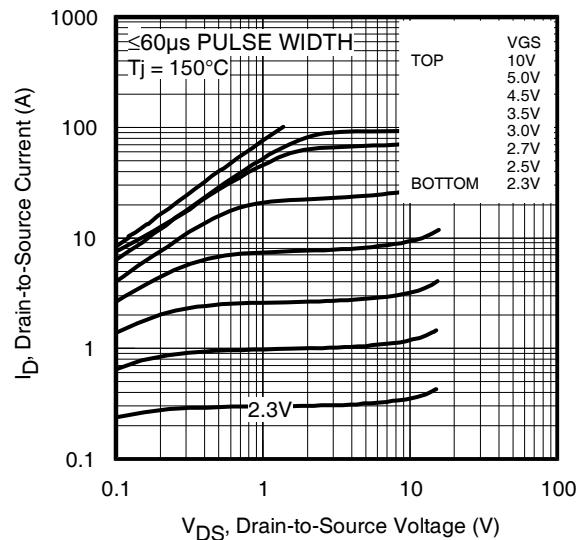


Fig 3. Typical Output Characteristics

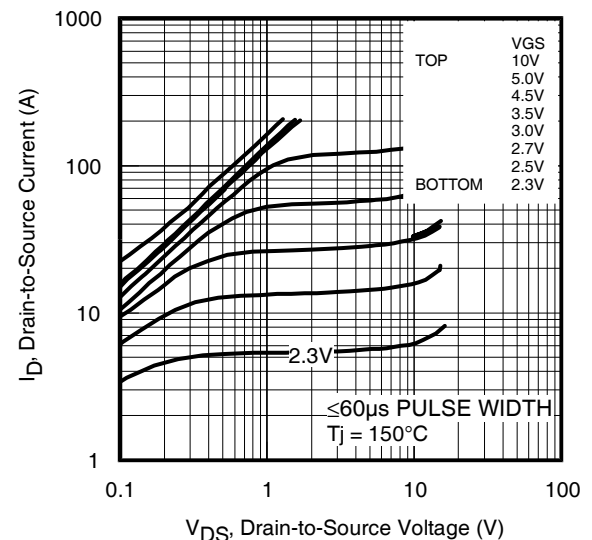


Fig 4. Typical Output Characteristics

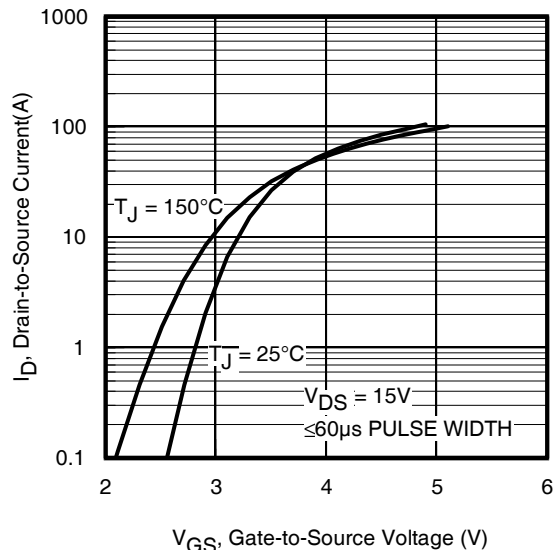


Fig 5. Typical Transfer Characteristics

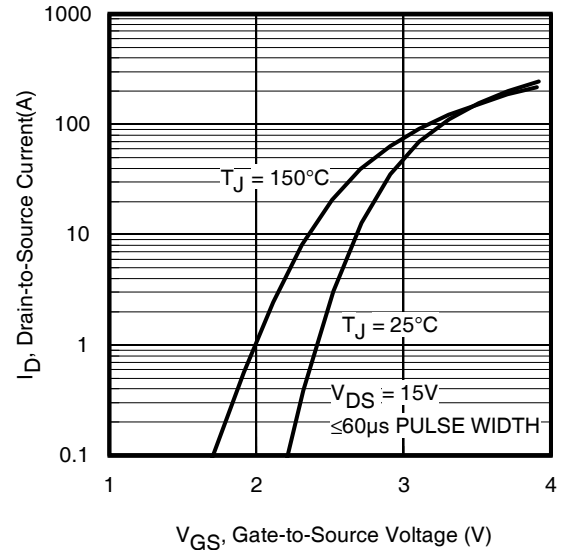
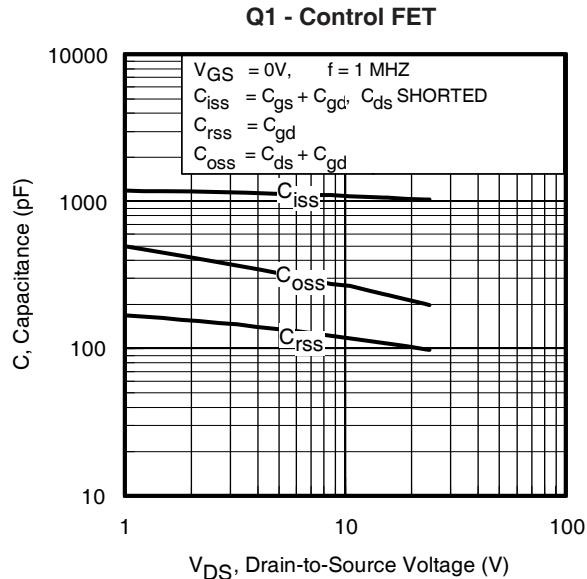
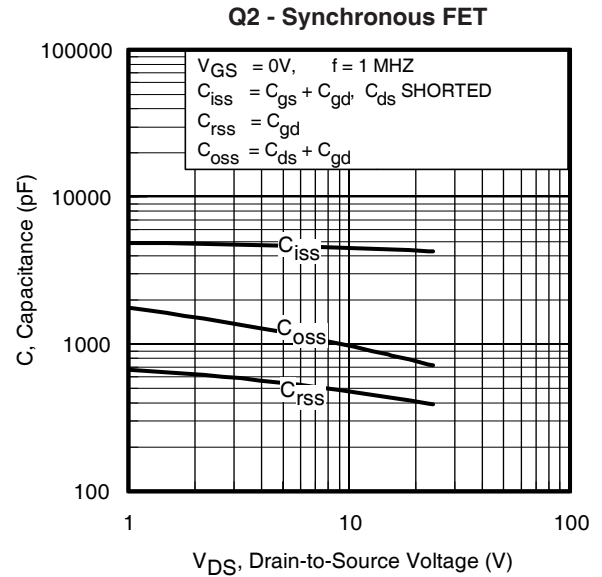
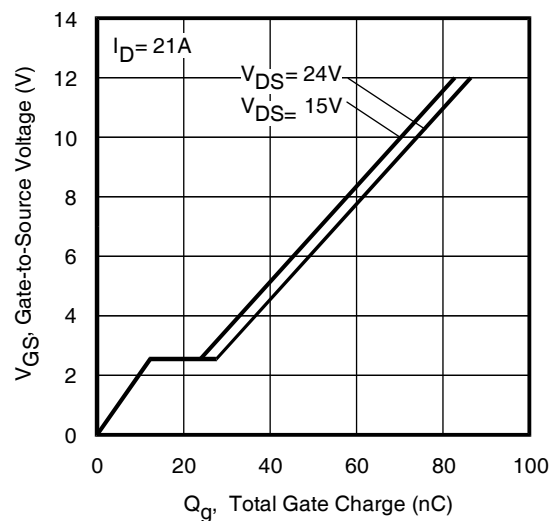
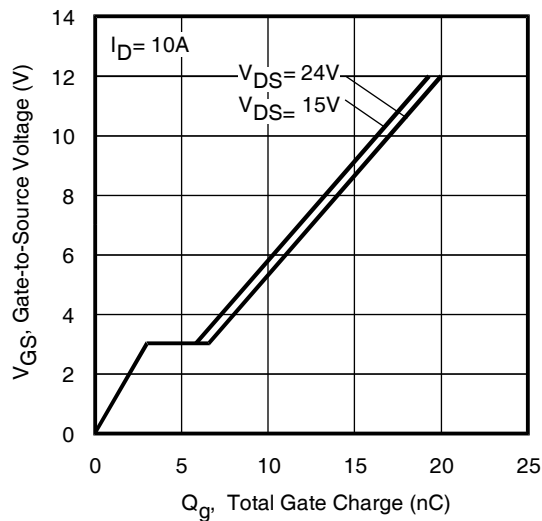
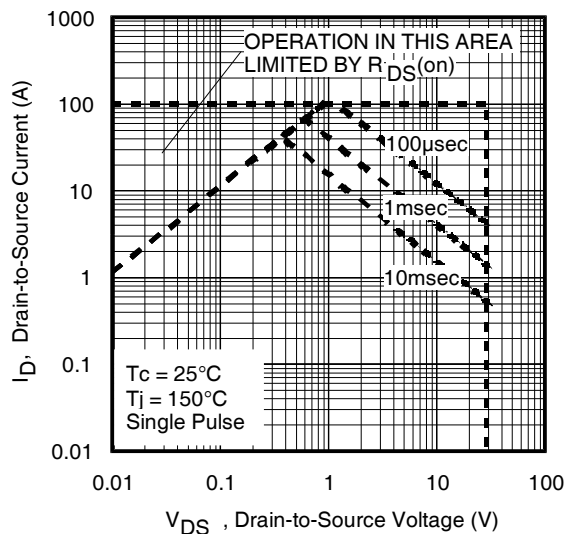
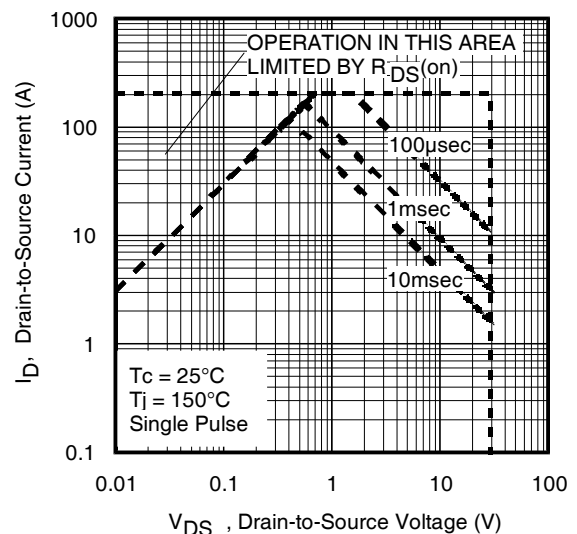
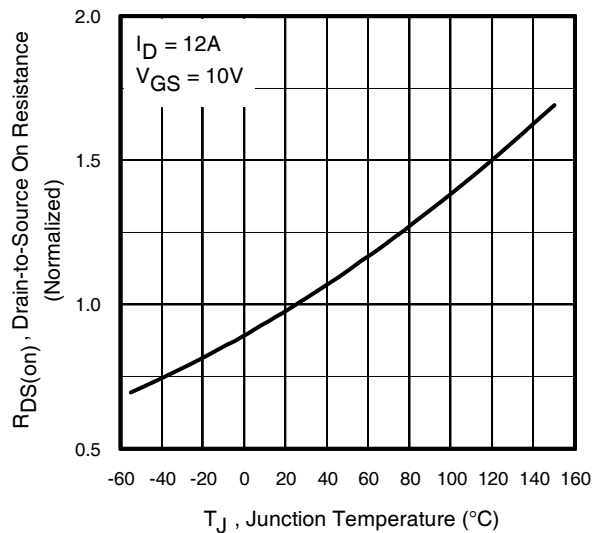


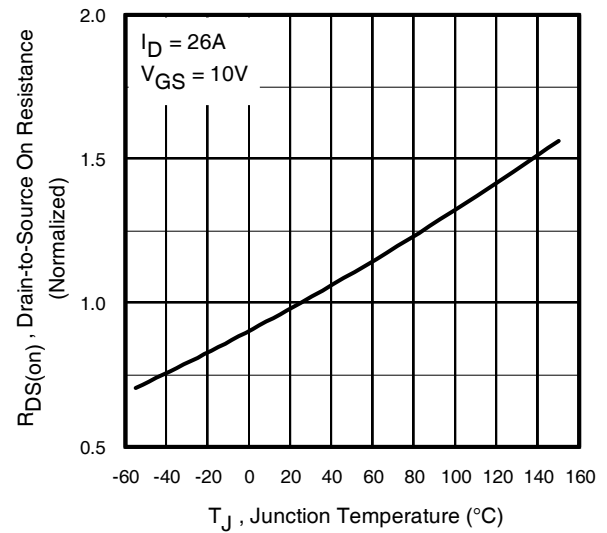
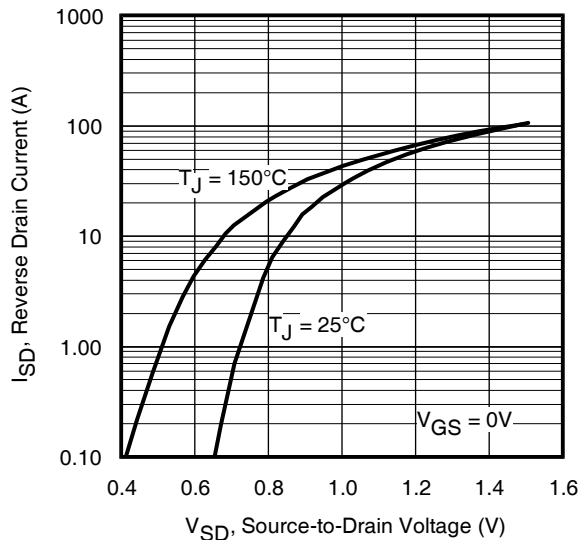
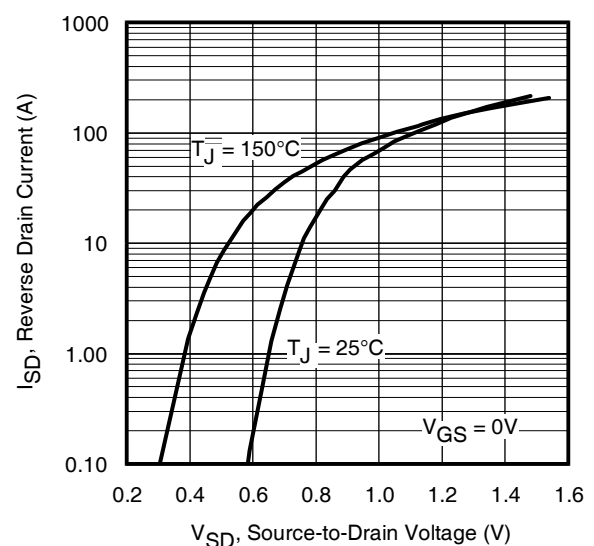
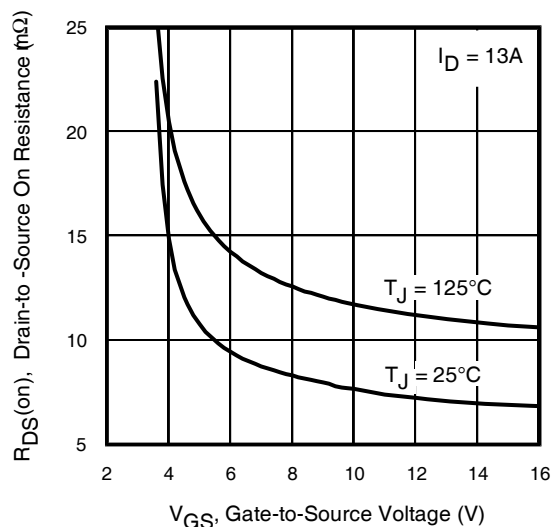
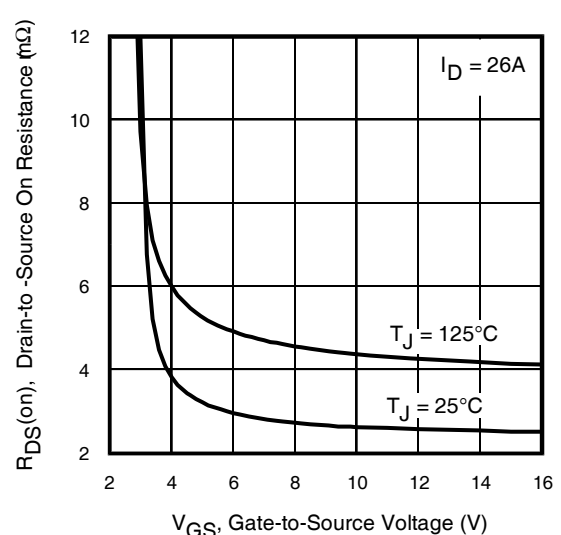
Fig 6. Typical Transfer Characteristics

Typical Characteristics

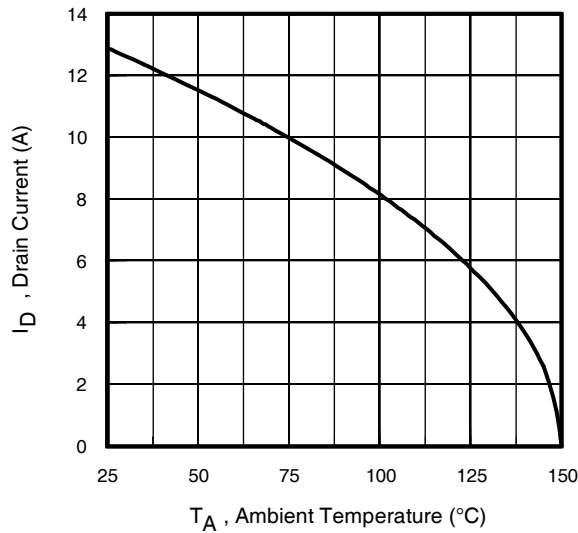

Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

Fig 11. Maximum Safe Operating Area

Fig 12. Maximum Safe Operating Area

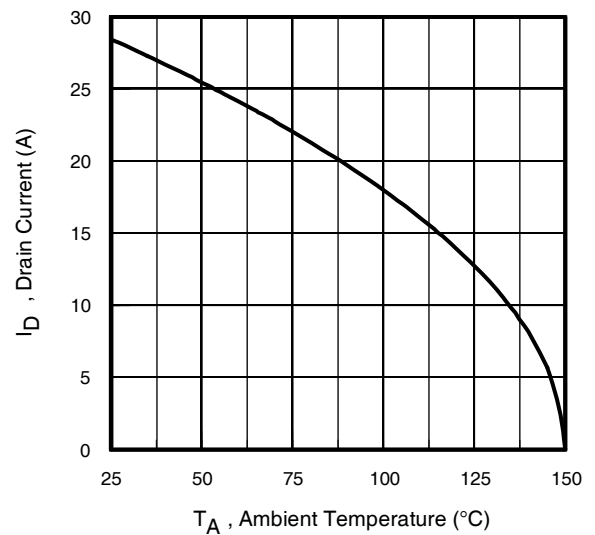
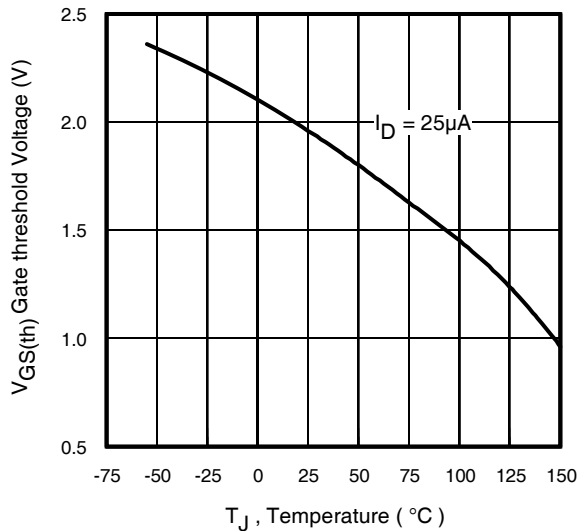
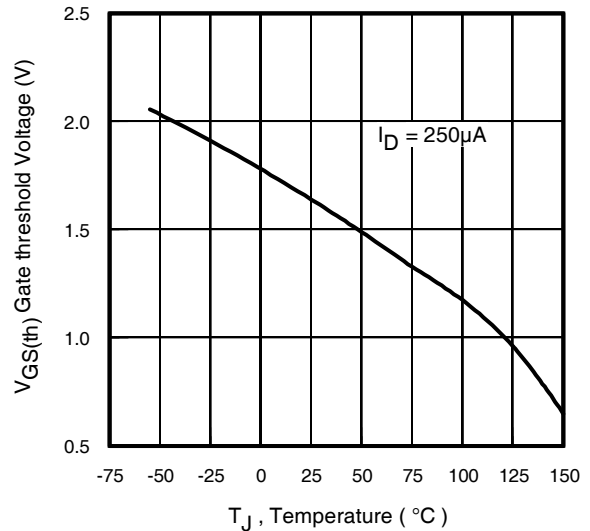
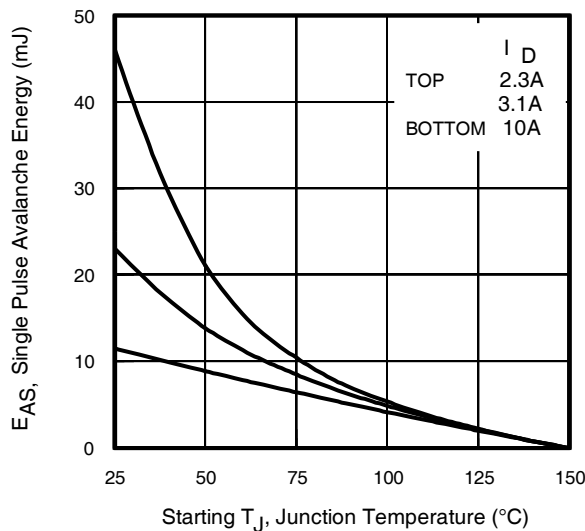
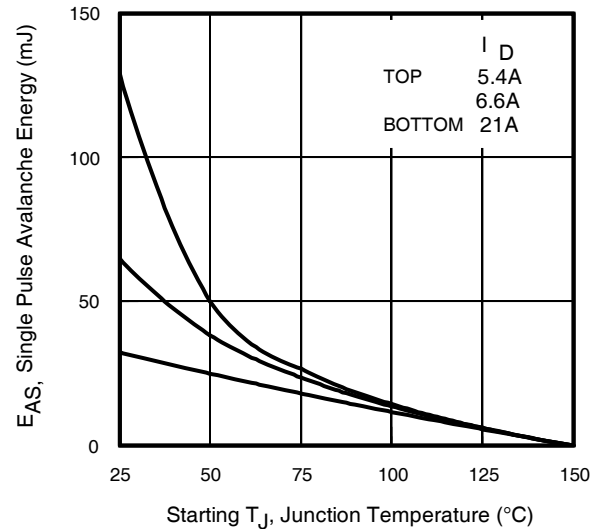
Typical Characteristics

Q1 - Control FET

Fig 13. Normalized On-Resistance vs. Temperature

Q2 - Synchronous FET

Fig 14. Normalized On-Resistance vs. Temperature

Fig 15. Typical Source-Drain Diode Forward Voltage

Fig 16. Typical Source-Drain Diode Forward Voltage

Fig 17. Typical On-Resistance vs. Gate Voltage

Fig 18. Typical On-Resistance vs. Gate Voltage

Typical Characteristics

Q1 - Control FET

Fig 19. Maximum Drain Current vs. Ambient Temp.

Q2 - Synchronous FET

Fig 20. Maximum Drain Current vs. Ambient Temp.

Fig 21. Threshold Voltage vs. Temperature

Fig 22. Threshold Voltage vs. Temperature

Fig 23. Maximum Avalanche Energy vs. Drain Current

Fig 24. Maximum Avalanche Energy vs. Drain Current

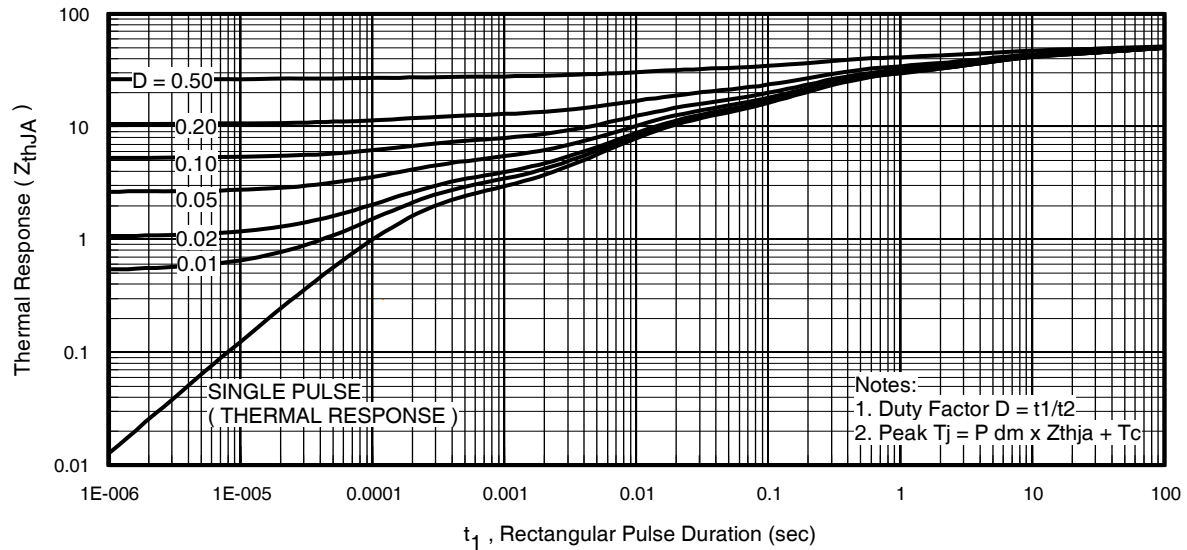


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q1)

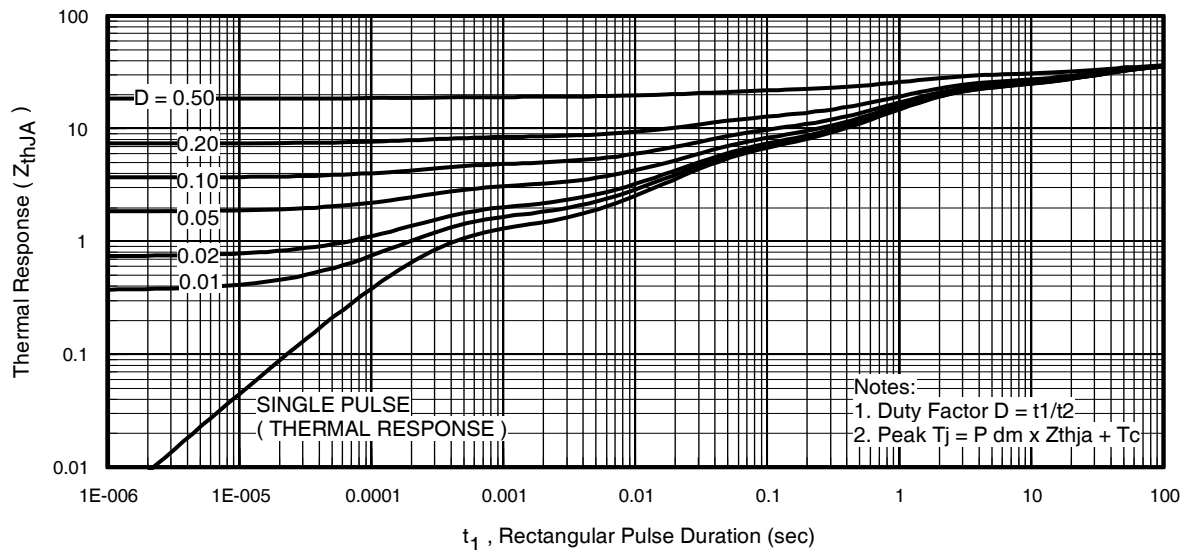
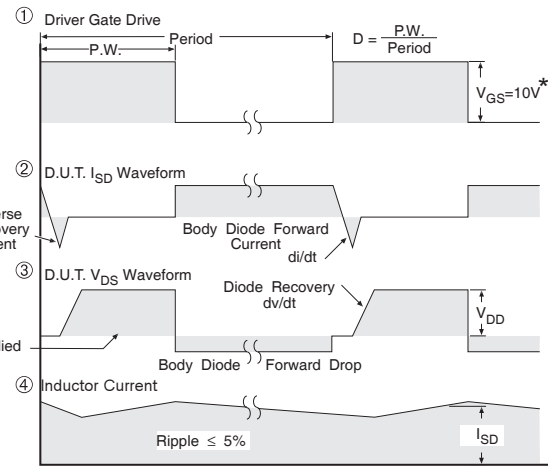
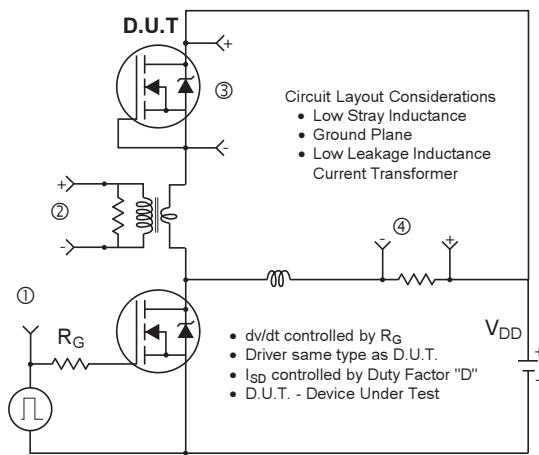


Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q2)



* $V_{GS} = 5V$ for Logic Level Devices

Fig 28. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

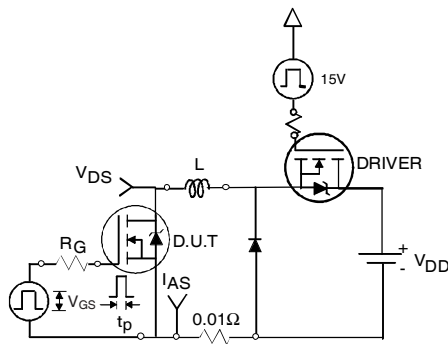


Fig 29a. Unclamped Inductive Test Circuit

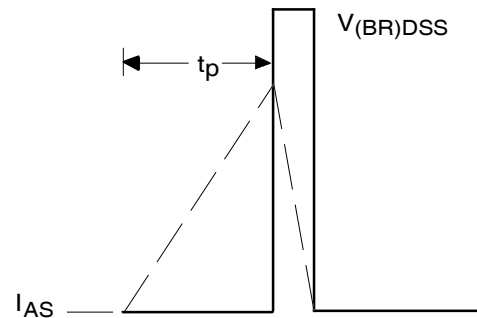


Fig 29b. Unclamped Inductive Waveforms

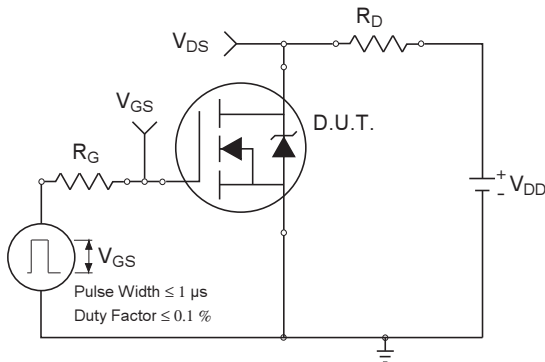


Fig 30a. Switching Time Test Circuit

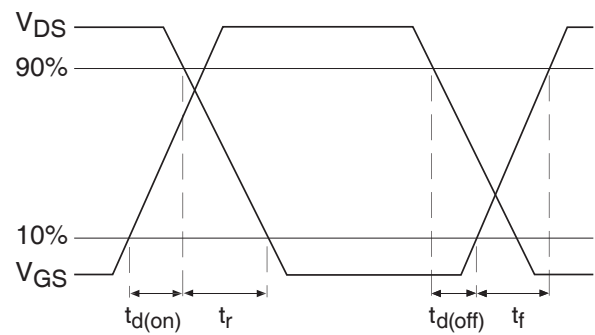


Fig 30b. Switching Time Waveforms

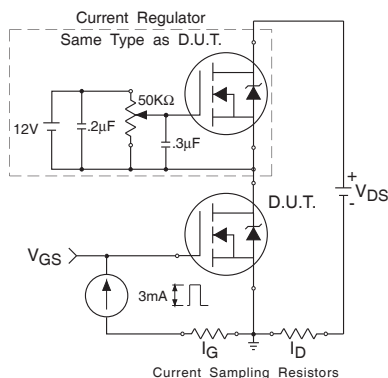


Fig 31a. Gate Charge Test Circuit

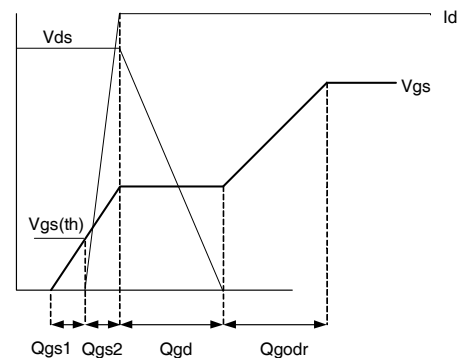
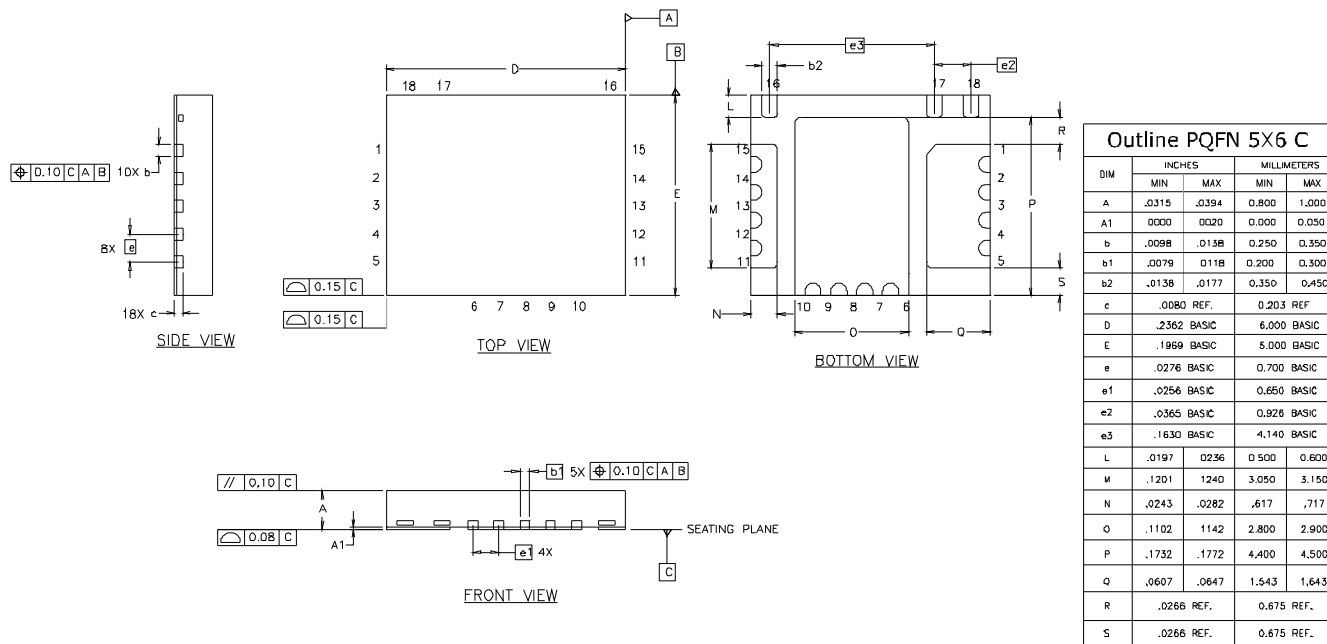


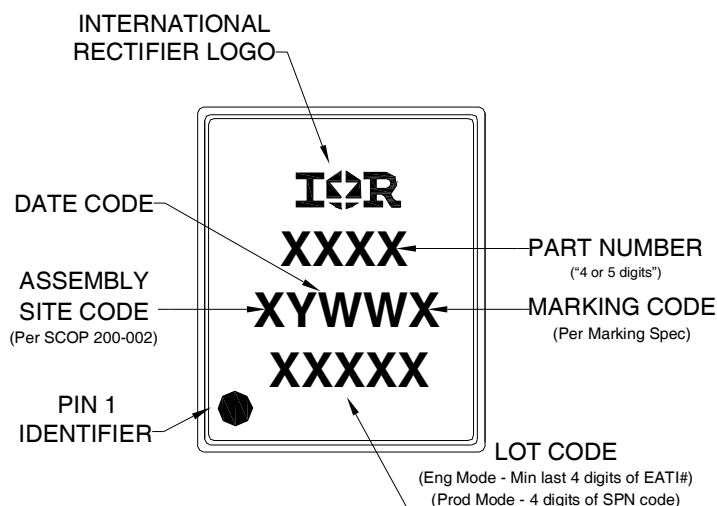
Fig 31b. Gate Charge Waveform

PQFN 5x6 Outline "C" Package Details



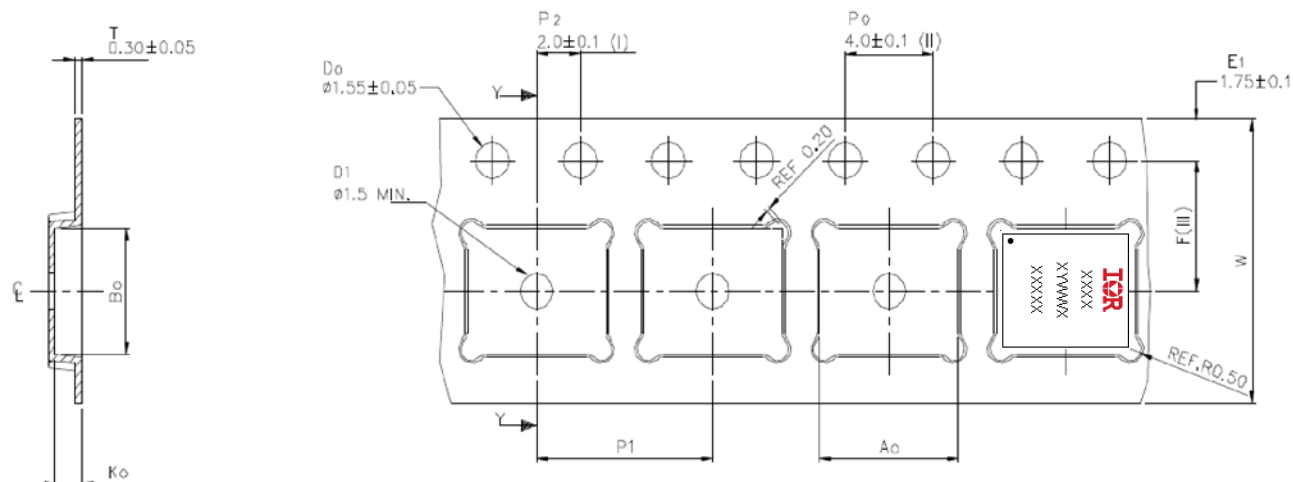
For footprint and stencil design recommendations, please refer to application note AN-1136 at <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

PQFN 5x6 Outline "C" Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

PQFN 5x6 Outline "C" Tape and Reel



SECTION Y-Y

A0	6.30 +/− 0.1
B0	5.30 +/− 0.1
K0	1.20 +/− 0.1
F	5.50 +/− 0.1
P1	8.00 +/− 0.1
W	12.00 +/− 0.3

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.
- (V) Typical SR of form tape Max 10^9 OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Consumer ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL2 ^{††††} (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

^{††} Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

^{†††} Applicable version of JEDEC standard at the time of product release.

^{††††} Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^{\circ}\text{C}$,
Q1: $L = 0.23\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 10\text{A}$;
Q2: $L = 0.15\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 21\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board.
- ⑤ R_{θ} is measured at T_J approximately 90°C .

Revision History

Date	Comment
1/8/2010	• Pin number on front page drawing has been corrected
7/15/2010	• MSL2 Consumer Qualification on page1 has been corrected
10/25/2011	• Link from AN-1152 to AN-1136 on page 9 has been corrected
5/9/2014	• Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259) • Updated data sheet based on corporate template.

International
 Rectifier

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