# LC²MOS Quad 14-Bit DAC

# AD7836

**FEATURES**
**Four 14-Bit DACs in One Package**
**Voltage Outputs**
**Separate Offset Adjust for Each Output**
**Reference Range of ±5 V**
**Maximum Output Voltage Range of ±10 V**
**Clear Function to User-Defined Code**
**44-Pin MQFP Package**

**APPLICATIONS**
**Process Control**
**Automatic Test Equipment**
**General Purpose Instrumentation**

**GENERAL DESCRIPTION**

The AD7836 contains four 14-bit DACs on one monolithic chip. It has output voltages with a full-scale range of ±10 V from reference voltages of ±5 V.

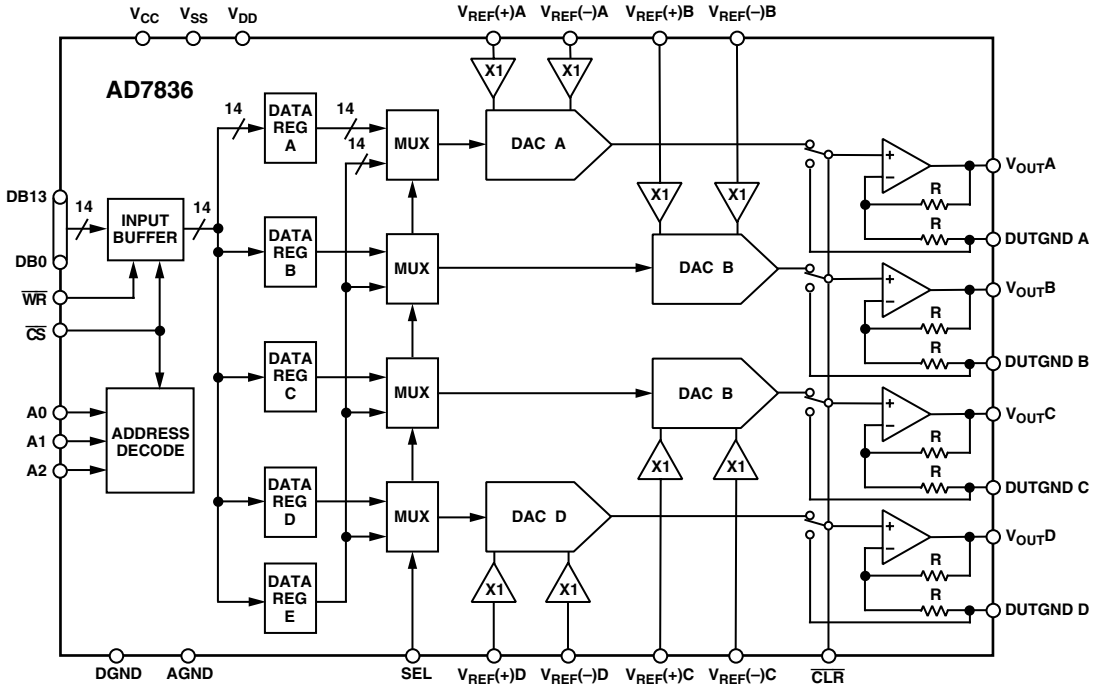
The AD7836 accepts 14-bit parallel loaded data from the external bus into one of the input latches under the control of the WR, CS and DAC channel address pins, A0–A2.

The DAC outputs are updated individually, on reception of new data. In addition, the SEL input can be used to apply the user programmed value in DAC Register E to all DACs, thus setting all DAC output voltages to the same level. The contents of the DAC data registers are not affected by the SEL input.

Each DAC output is buffered with a gain of two amplifier into which an external DAC offset voltage can be inserted via the DUTGNDx pins.

The AD7836 is available in a 44-lead MQFP package.

**FUNCTIONAL BLOCK DIAGRAM**




REV. A

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**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781/329-4700 World Wide Web Site: http://www.analog.com**
**Fax: 781/326-8703**
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# AD7836–SPECIFICATIONS

**($V_{CC}$ = +5 V ± 5%; $V_{DD}$ = +15 V ± 5%; $V_{SS}$ = –15 V ± 5%; AGND = DGND = DUTGND = 0 V; $R_L$ = 5 kΩ and $C_L$ = 50 pF to GND, $T_A$[1] = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted)**

| Parameter | A | Units | Test Conditions/Comments |
|---|---|---|---|
| ACCURACY | | | |
| Resolution | 14 | Bits | |
| Relative Accuracy | ±2 | LSB max | |
| Differential Nonlinearity | ±0.9 | LSB max | Guaranteed Monotonic Over Temperature |
| Full-Scale Error | ±8 | LSB max | $V_{REF}(+)$ = +5 V, $V_{REF}(–)$ = –5 V. Typically within ±1 LSB |
| Zero-Scale Error | ±8 | LSB max | $V_{REF}(+)$ = +5 V, $V_{REF}(–)$ = –5 V. Typically within ±1 LSB |
| Gain Error | ±2 | mV typ | $V_{REF}(+)$ = +5 V, $V_{REF}(–)$ = –5 V |
| Gain Temperature Coefficient[2] | 20 | ppm FSR/°C typ | |
| | 40 | ppm FSR/°C max | |
| DC Crosstalk[2] | 50 | µV max | See Terminology. $R_L$ = 5 kΩ |
| REFERENCE INPUTS | | | |
| DC Input Resistance | 100 | MΩ typ | |
| Input Current | ±1 | µA max | Per Input. Typically ±20 nA |
| $V_{REF}(+)$ Range | 0/+5 | V min/max | |
| $V_{REF}(–)$ Range | –5/0 | V min/max | |
| $[V_{REF}(+) – V_{REF}(–)]$ | 2/10 | V min/max | For Specified Performance. Can Go as Low as 0 V, but Performance Not Guaranteed |
| OUTPUT CHARACTERISTICS | | | |
| Output Voltage Swing | ±10 | V min | $2 \times (V_{REF}(–)+[V_{REF}(+)-V_{REF}(–)]\bullet D) – V_{DUTDGN}$ |
| Short Circuit Current | 25 | mA max | |
| Resistive Load | 5 | kΩ min | To 0 V |
| Capacitive Load | 50 | pF max | To 0 V |
| DIGITAL INPUTS | | | |
| $V_{INH}$, Input High Voltage | 2.4 | V min | |
| $V_{INL}$, Input Low Voltage | 0.8 | V max | |
| $I_{INH}$, Input Current | ±10 | µA max | Total for All Pins |
| $C_{IN}$, Input Capacitance | 10 | pF max | |
| POWER REQUIREMENTS | | | |
| $V_{CC}$ | 5.0 | V nom | ±5% for Specified Performance |
| $V_{DD}$ | 15.0 | V nom | ±5% for Specified Performance |
| $V_{SS}$ | –15.0 | V nom | ±5% for Specified Performance |
| Power Supply Sensitivity | | | |
| $\Delta$Full Scale/$\Delta V_{DD}$ | 110 | dB typ | |
| $\Delta$Full Scale/$\Delta V_{SS}$ | 100 | dB typ | |
| $I_{CC}$ | 0.5 | mA max | $V_{INH}$ = $V_{CC}$, $V_{INL}$ = DGND. Dynamic Current |
| | 8 | mA max | $V_{INH}$ = 2.4 V min, $V_{INL}$ = 0.8 V max |
| $I_{DD}$ | 14 | mA max | Outputs Unloaded. Typically 7 mA |
| $I_{SS}$ | 14 | mA max | Outputs Unloaded. Typically 7 mA |

# AC PERFORMANCE CHARACTERISTICS

**(These characteristics are included for Design Guidance and are not subject to production testing.)**

| Parameter | A | Units | Test Conditions/Comments |
|---|---|---|---|
| DYNAMIC PERFORMANCE | | | |
| Output Voltage Settling Time | 16 | µs typ | Full-Scale Change to ±1/2 LSB. DAC Latch Contents Alternately Loaded with All 0s and All 1s |
| Digital-to-Analog Glitch Impulse | 150 | nV-s typ | Measured with $V_{REF}(+)$ = +5 V, $V_{REF}(–)$ = –5 V. DAC Latch Alternately Loaded with 1FFF Hex and 2000 Hex. Not Dependent on Load Conditions |
| DC Output Impedance | 0.3 | Ω max | See Terminology |
| Channel-to-Channel Isolation | 115 | dB typ | See Terminology |
| DAC-to-DAC Crosstalk | 10 | nV-s typ | See Terminology |
| Digital Crosstalk | 10 | nV-s typ | Feedthrough to DAC Output Under Test Due to Change in Digital Input Code to Another Converter |
| Digital Feedthrough | 0.2 | nV-s typ | Effect of Input Bus Activity on DAC Output Under Test |
| Output Noise Spectral Density | | | |
| @ 1 kHz | 40 | nV/√Hz typ | All 1s Loaded to DAC. $V_{REF}(+)$ = $V_{REF}(–)$ = 0 V |

NOTES
[1]Temperature range for A Version: –40°C to +85°C
[2]Guaranteed by design.

Specifications subject to change without notice.

## TIMING SPECIFICATIONS[1] ($V_{CC}$ = +5 V ± 5%; $V_{DD}$ = +15 V ± 5%; $V_{SS}$ = –15 V ± 5%; AGND = DGND = 0 V)

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Units | Description |
|---|---|---|---|
| $t_1$ | 15 | ns min | A0, A1, A2 to WR Setup Time |
| $t_2$ | 0 | ns min | A0, A1, A2 to WR Hold Time |
| $t_3$ | 0 | ns min | CS to WR Setup Time |
| $t_4$ | 0 | ns min | WR to CS Hold Time |
| $t_5$ | 44 | ns min | WR Pulsewidth |
| $t_6$ | 15 | ns min | Data Setup Time |
| $t_7$ | 4.5 | ns min | Data Hold Time |
| $t_8$ | 44 | ns min | WR Pulse Interval |
| $t_9$ | 16 | µs typ | Settling Time |
| $t_{10}$ | 300 | ns max | CLR Pulse Activation Time |

NOTES
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Rise and fall times should be no longer than 50 ns.

Specifications subject to change without notice.

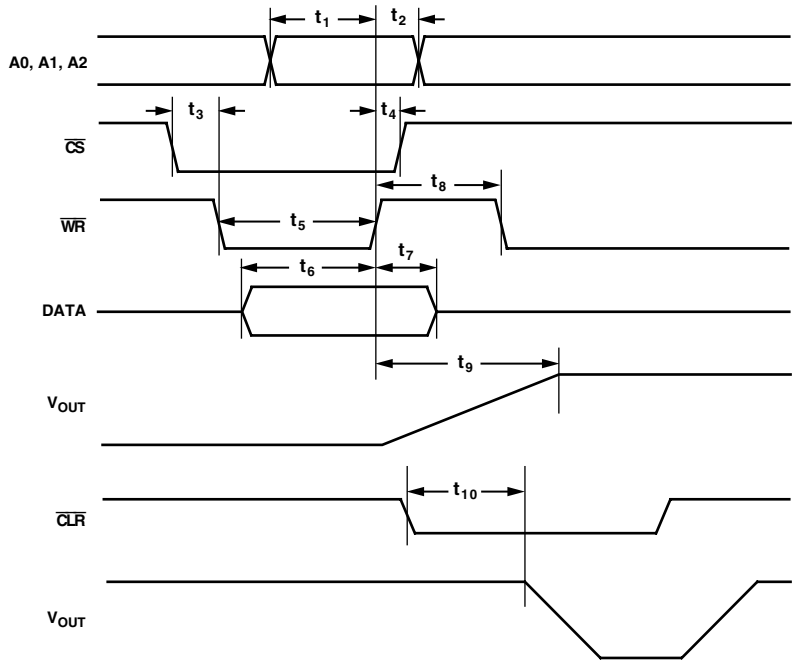



*Figure 1. Timing Diagram*

**ABSOLUTE MAXIMUM RATINGS**[1]

($T_A$ = +25°C unless otherwise noted)

$V_{CC}$ to DGND . . . . . –0.3 V, +7 V or $V_{DD}$ + 0.3 V (Whichever Is Lower)
$V_{DD}$ to AGND . . . . . –0.3 V, +17 V
$V_{SS}$ to AGND . . . . . +0.3 V, –17 V
AGND to DGND . . . . . –0.3 V, +0.3 V
Digital Inputs to DGND . . . . . –0.3 V, $V_{CC}$ + 0.3 V
$V_{REF}$(+) to $V_{REF}$(–) . . . . . –0.3 V, +18 V
$V_{REF}$(+) to AGND . . . . . $V_{SS}$ – 0.3 V, $V_{DD}$ + 0.3 V
$V_{REF}$(–) to AGND . . . . . $V_{SS}$ – 0.3 V, $V_{DD}$ + 0.3 V
DUTGND to AGND . . . . . $V_{SS}$ – 0.3 V, $V_{DD}$ + 0.3 V
$V_{OUT}$ (A–D) to AGND . . . . . $V_{SS}$ – 0.3 V, $V_{DD}$ + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
MQFP Package, Power Dissipation . . . . . 480 mW
$\theta_{JA}$ Thermal Impedance . . . . . 95°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

**ORDERING GUIDE**

| Model | Temperature Range | Linearity Error (LSBs) | DNL (LSBs) | Package Option* |
|---|---|---|---|---|
| AD7836AS | –40°C to +85°C | ±2 | ±0.9 | S-44 |

*S = Plastic Quad Flatpack (MQFP).

**CAUTION**

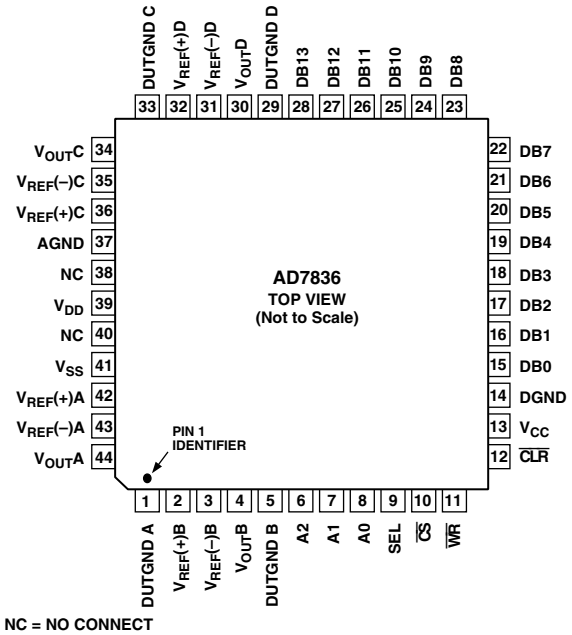
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7836 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



**PIN DESCRIPTION**

| Pin Mnemonic | Description |
|---|---|
| $V_{CC}$ | Logic Power Supply; +5 V ± 5%. |
| $V_{SS}$ | Negative Analog Power Supply; –15 V ± 5%. |
| $V_{DD}$ | Positive Analog Power Supply; +15 V ± 5%. |
| DGND | Digital Ground. |
| AGND | Analog Ground. |
| $V_{REF}(+)A$, $V_{REF}(-)A$ | Reference Inputs for DAC A. These reference voltages are referred to AGND. |
| $V_{REF}(+)B$, $V_{REF}(-)B$ | Reference Inputs for DAC B. These reference voltages are referred to AGND. |
| $V_{REF}(+)C$, $V_{REF}(-)C$ | Reference Inputs for DAC C. These reference voltages are referred to AGND. |
| $V_{REF}(+)D$, $V_{REF}(-)D$ | Reference Inputs for DAC D. These reference voltages are referred to AGND. |
| $V_{OUT}A \ldots V_{OUT}D$ | DAC Outputs. |
| CS | Level-Triggered Chip Select Input (active low). The device is selected when this input is low. |
| DB0 . . . DB13 | Parallel Data Inputs. The AD7836 can accept a straight 14-bit parallel word on DB0 to DB13 where DB13 is the MSB and DB0 is the LSB. |
| A0, A1, A2 | Address inputs. A0, A1 and A2 are decoded to select one of the five input latches for a data transfer. |
| CLR | Asynchronous Clear Input (level sensitive, active low). When this input is low, all analog outputs are switched to the externally set potential on the DUTGND pin. The contents of data registers A to E are not affected when the CLR pin is taken low. When CLR is brought back high, the DAC outputs revert back to their original outputs as determined by the data in their data registers. |
| WR | Level-Triggered Write Input (active low), when active and used in conjunction with CS to write data to the AD7836 input buffer. Data is latched into the selected data register on the rising edge of WR. |
| DUTGND A | Device Sense Ground for DAC A. Vout A is referenced to the voltage applied to this pin. |
| DUTGND B | Device Sense Ground for DAC B. Vout B is referenced to the voltage applied to this pin. |
| DUTGND C | Device Sense Ground for DAC C. Vout C is referenced to the voltage applied to this pin. |
| DUTGND D | Device Sense Ground for DAC D. Vout D is referenced to the voltage applied to this pin. |
| SEL | Select pin, active high level triggered input. When the SEL input is high, the user programmed value in DATAREG E will be loaded into all DAC registers and the DAC outputs updated accordingly. The contents of the other DATA REGs (A–D) will not be affected by the SEL pin. |

**PIN CONFIGURATION**



## TERMINOLOGY

**Relative Accuracy**
Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage of full-scale reading.

**Differential Nonlinearity**
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

**DC Crosstalk**
Although the common input reference voltage signals are internally buffered, small IR drops in the individual DAC reference inputs across the die can mean that an update to one channel can produce a dc output change in one or other of the channel outputs.

The four DAC outputs are buffered by op amps that share common $V_{DD}$ and $V_{SS}$ power supplies. If the dc load current changes in one channel (due to an update), this can result in a further dc change in one or other channel outputs. This effect is most obvious at high load currents and reduces as the load currents are reduced. With high impedance loads the effect is virtually unmeasurable.

**Output Voltage Settling Time**
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

**Digital-to-Analog Glitch Impulse**
This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV-secs. It is measured with $V_{REF}(+)$ = +5 V and $V_{REF}(-)$ = –5 V and the digital inputs toggled between 1FFFHEX and 8000H.

**Channel-to-Channel Isolation**
Channel-to-channel isolation refers to the proportion of input signal from one DACs reference input that appears at the output of the other DAC. It is expressed in dBs.

**DAC-to-DAC Crosstalk**
DAC-to-DAC crosstalk is defined as the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog O/P change at another converter. It is specified in nV-s.

**Digital Crosstalk**
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the digital crosstalk and is specified in nV-s.

**Digital Feedthrough**
When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the $V_{OUT}$ pins. This noise is digital feedthrough.

**DC Output Impedance**
This is the effective output source resistance. It is dominated by package lead resistance.

**Full-Scale Error**
This is the error in DAC output voltage when all 1s are loaded into the DAC latch. Ideally the output voltage, with all 1s loaded into the DAC latch, should be 2 $V_{REF}(+)$ – 1 LSB. Full-scale error does not include zero-scale error.

**Zero-Scale Error**
Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC latch. Ideally the output voltage, with all 0s in the DAC latch should be equal to 2 $V_{REF}(-)$. Zero-scale error is mainly due to offsets in the output amplifier.

**Gain Error**
Gain Error is defined as (Full-Scale Error) – (Zero-Scale Error).

## GENERAL DESCRIPTION

**DAC Architecture—General**
Each channel consists of a segmented 14-bit R-2R voltage-mode DAC. The full-scale output voltage range is equal to twice the reference span of $V_{REF}(+) - V_{REF}(-)$. The DAC coding is straight binary; all 0s produces an output of 2 $V_{REF}(-)$; all 1s produces an output of 2 $V_{REF}(+)$ – 1 LSB.

The analog output voltage of each DAC channel reflects the contents of its own DAC latch. Data is transferred from the external bus to the input register of each DAC latch on a per channel basis. The AD7836 has a feature whereby using the A2 pin, data can be transferred from the input data bus to all four input registers simultaneously.

Bringing the CLR line low switches all the signal outputs, $V_{OUT}A$ to $V_{OUT}D$, to the voltage level on the DUTGND pin. When CLR signal is brought back high the output voltages from the DACs will reflect the data stored in the relevant DAC registers.

**Data Loading to the AD7836**
Data is loaded into the AD7836 in straight parallel 14-bit wide words.

The DAC output voltages, $V_{OUT}A$–$V_{OUT}D$ are updated to reflect new data in the DAC input registers.

The actual DAC input register that is being written to is determined by the logic levels present on the devices address lines, as shown in Table I.

**Table I. Address Line Truth Table**

| A2 | A1 | A0 | DAC Selected |
|---|---|---|---|
| 0 | 0 | 0 | DATA REG A (DAC A) |
| 0 | 0 | 1 | DATA REG B (DAC B) |
| 0 | 1 | 0 | DATA REG C (DAC C) |
| 0 | 1 | 1 | DATA REG D (DAC D) |
| 1 | 0 | 0 | DATA REG E |
| 1 | 1 | 1 | DATA REG A–D |

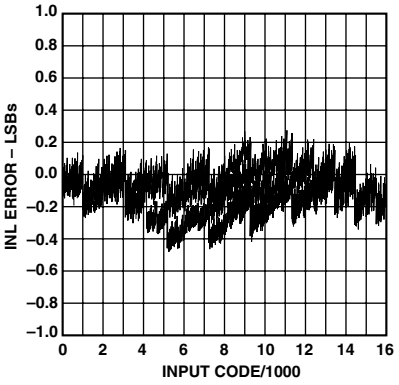



Figure 2. Typical INL Plot

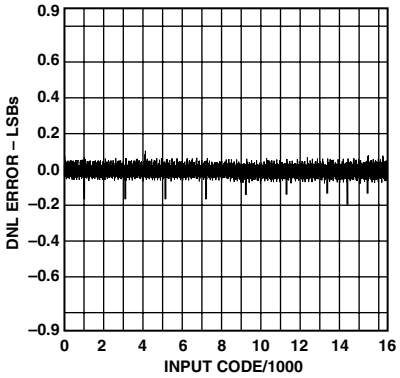



Figure 3. Typical DNL Plot

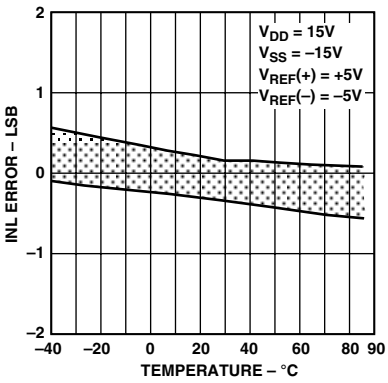



Figure 4. Typical INL Error vs. Temperature

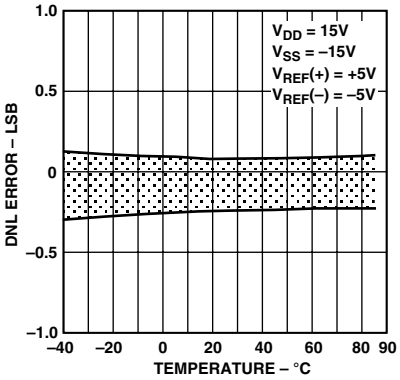



Figure 5. Typical DNL Error vs. Temperature

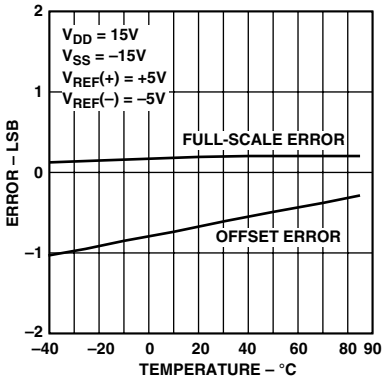



Figure 6. Offset and Full-Scale Error vs. Temperature

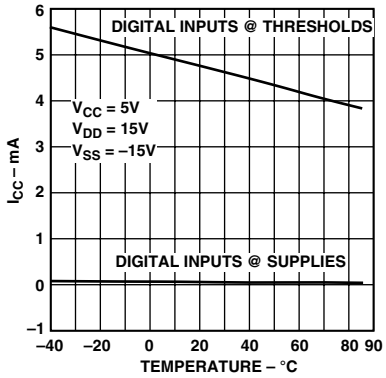



Figure 7. $I_{CC}$ vs. Temperature

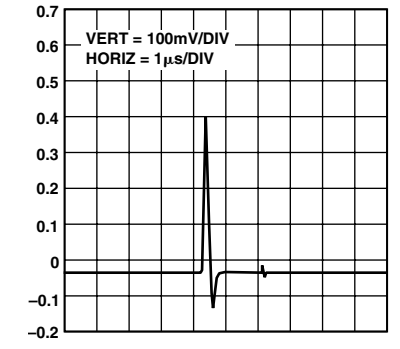



Figure 8. Typical Digital/Analog Glitch Impulse

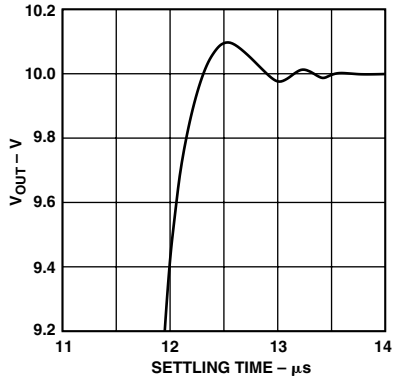



Figure 9. Settling Time (+)

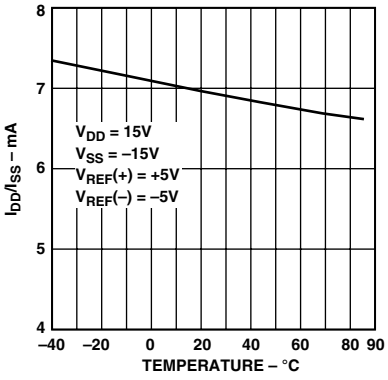



Figure 10. $I_{DD}/I_{SS}$ vs. Temperature

**Unipolar Configuration**

Figure 11 shows the AD7836 in the unipolar binary circuit configuration. The $V_{REF}(+)$ input of the DAC is driven by the AD586, a +5 V reference. $V_{REF}(-)$ is tied to ground. Table II gives the code table for unipolar operation of the AD7836. Other suitable references include the REF02, a precision 5 V reference, and the REF195, a low dropout, micropower precision +5 V reference.

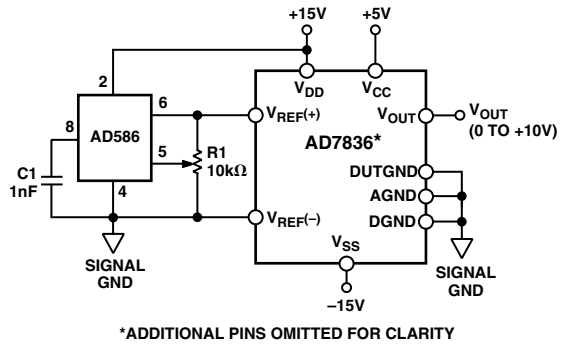



*Figure 11. Unipolar +5 V Operation*

Offset and gain may be adjusted in Figure 2 as follows: To adjust offset, disconnect the $V_{REF}(-)$ input from 0 V, load the DAC with all 0s and adjust the $V_{REF}(-)$ voltage until $V_{OUT}$ = 0 V. For gain adjustment, the AD7836 should be loaded with all 1s and R1 adjusted until $V_{OUT}$ = 10 V(16383/16384) = 9.999389.

Many circuits will not require these offset and gain adjustments. In these circuits R1 can be omitted. Pin 5 of the AD586 may be left open circuit and Pin 2 ($V_{REF}(-)$) of the AD7836 tied to 0 V.

**Table II. Code Table for Unipolar Operation**

| Binary Number in DAC Latch MSB | | | LSB | Analog Output ($V_{OUT}$) |
|---|---|---|---|---|
| 11 | 1111 | 1111 | 1111 | 2 $V_{REF}$ (16383/16384) V |
| 10 | 0000 | 0000 | 0000 | 2 $V_{REF}$ (8192/16384) V |
| 01 | 1111 | 1111 | 1111 | 2 $V_{REF}$ (8191/16384) V |
| 00 | 0000 | 0000 | 0001 | 2 $V_{REF}$ (1/16384) V |
| 00 | 0000 | 0000 | 0000 | 0 V |

NOTE
$V_{REF} = V_{REF}(+); V_{REF}(-) = 0$ V for unipolar operation.
For $V_{REF}(+)$ = +5 V, 1 LSB = +10 V/$2^{14}$ = +10 V/16384 = 610 μV.

**Bipolar Configuration**

Figure 12 shows the AD7836 set up for ±10 V operation. The AD588 provides precision ±5 V tracking outputs that are fed to the $V_{REF}(+)$ and $V_{REF}(-)$ inputs of the AD7836. The code table for bipolar operation of the AD7836 is shown in Table III.

In Figure 12, full-scale and bipolar zero adjustments are provided by varying the gain and balance on the AD588. R2 varies the gain on the AD588 while R3 adjusts the offset of both the +5 V and –5 V outputs together with respect to ground.

For bipolar-zero adjustment, the DAC is loaded with 1000 . . . 0000 and R3 is adjusted until $V_{OUT}$ = 0 V. Full scale is adjusted by loading the DAC with all 1s and adjusting R2 until $V_{OUT}$ = 10(8191/8192) V = 9.998779 V.

When bipolar-zero and full-scale adjustment are not needed, R2 and R3 can be omitted. Pin 12 on the AD588 should be connected to Pin 11 and Pin 5 should be left floating.

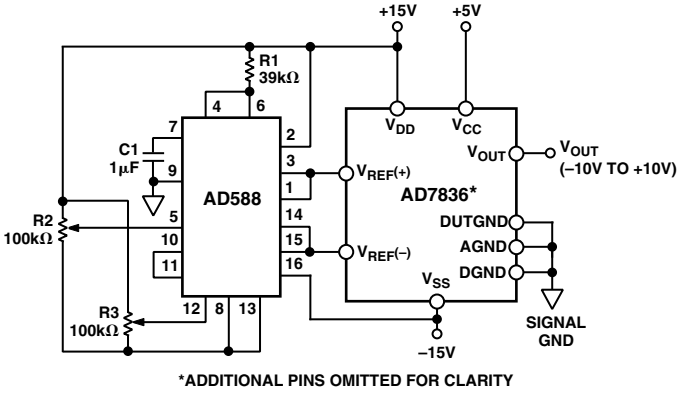



*Figure 12. Bipolar ±5 V Operation*

**Table III. Code Table for Bipolar Operation**

| Binary Number in DAC Latch MSB | | | LSB | Analog Output ($V_{OUT}$) |
|---|---|---|---|---|
| 11 | 1111 | 1111 | 1111 | 2[$V_{REF}(-)$ + $V_{REF}$ (16383/16384)] V |
| 10 | 0000 | 0000 | 0001 | 2[$V_{REF}(-)$ + $V_{REF}$ (8193/16384)] V |
| 10 | 0000 | 0000 | 0000 | 2[$V_{REF}(-)$ + $V_{REF}$ (8192/16384)] V |
| 01 | 1111 | 1111 | 1111 | 2[$V_{REF}(-)$ + $V_{REF}$ (8191/16384)] V |
| 00 | 0000 | 0000 | 0001 | 2[$V_{REF}(-)$ + $V_{REF}$ (1/16384)] V |
| 00 | 0000 | 0000 | 0000 | 2[$V_{REF}(-)$] V |

NOTE
$V_{REF} = (V_{REF}(+) - V_{REF}(-))$.
For $V_{REF}(+)$ = +5 V, and $V_{REF}(-)$ = –5 V, $V_{REF}$ =10 V, 1 LSB = 2 VREF V/$2^{14}$ = 20 V/16384 = 1220 μV.

**CONTROLLED POWER-ON OF THE OUTPUT STAGE**

A block diagram of the output stage of the AD7836 is shown in Figure 13. It is capable of driving a load of 5 kΩ in parallel with 50 pF. $G_1$ to $G_6$ are transmission gates that are used to control the power on voltage present at $V_{OUT}$. On power up $G_1$ and $G_2$ are also used in conjunction with the CLR input to set $V_{OUT}$ to the user defined voltage present at the DUTGND pin. When CLR is taken back high the DAC outputs reflect the data in the DAC registers.

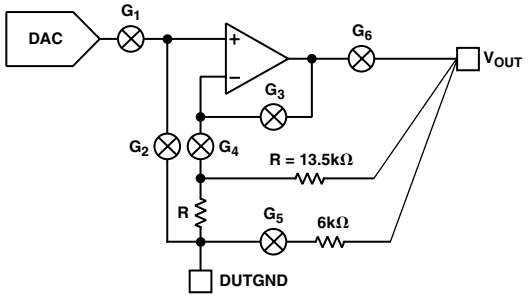



*Figure 13. Block Diagram of AD7836 Output Stage*

**Power-On with CLR Low**

The output stage of the AD7836 has been designed to allow output stability during power-on. If CLR is kept low during power-on, then just after power is applied to the AD7836, the situation is as depicted in Figure 14. $G_1$, $G_4$ and $G_6$ are open while $G_2$, $G_3$ and $G_5$ are closed.

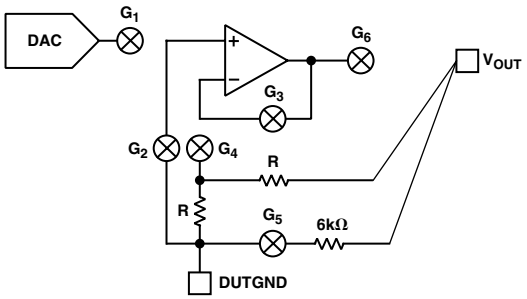



*Figure 14. Output Stage with $V_{DD}$ < 10 V*

$V_{OUT}$ is kept within a few hundred millivolts of DUTGND via $G_5$ and a 6kΩ resistor. This thin-film resistor is connected in parallel with the gain resistors of the output amplifier. The output amplifier is connected as a unity gain buffer via $G_3$, and the DUTGND voltage is applied to the buffer input via $G_2$. The amplifier's output is thus at the same voltage as the DUTGND pin. The output stage remains configured as in Figure 14 until the voltage at $V_{DD}$ and $V_{SS}$ reaches approximately ±10 V. By now the output amplifier has enough headroom to handle signals at its input and has also had time to settle. The internal power-on circuitry opens $G_3$ and $G_5$ and closes $G_4$ and $G_6$. This situation is shown in Figure 15. Now the output amplifier is configured in its noise gain configuration via $G_4$ and $G_6$. The DUTGND voltage is still connected to the noninverting input via G2 and this voltage appears at $V_{OUT}$.

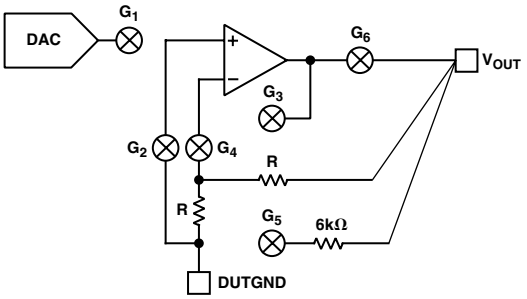



*Figure 15. Output Stage with $V_{DD}$ > 10 V and $\overline{CLR}$ Low*

$V_{OUT}$ has been disconnected from the DUTGND pin by the opening of $G_5$ but will track the voltage present at DUTGND via the configuration shown in Figure 15.

When CLR is taken back high, the output stage is configured as shown in Figure 16. The internal control logic closes $G_1$ and opens $G_2$. The output amplifier is connected in a noninverting gain of two configuration. The voltage that appears on the Vout pins is determined by the data present in the DAC registers. To set all output voltages to the same known state, a write to DATA REG E with the SEL pin high allows all DAC registers to be updated with the same data.

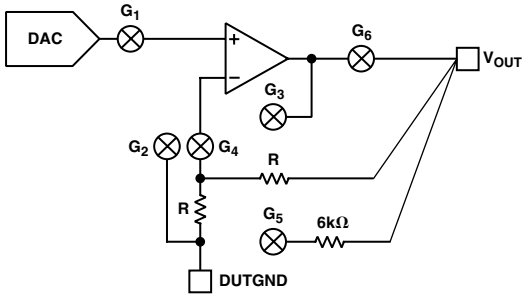



*Figure 16. Output Stage After $\overline{CLR}$ Is Taken High*

**Power-On with CLR High**

If CLR is high on the application of power to the device, the output stages of the AD7836 are configured as in Figure 17 while $V_{DD}/V_{SS}$ are less than ±10 V. $G_1$ is closed and $G_2$ is open thereby connecting the output of the DAC to the input of its output amplifier. $G_3$ and $G_5$ are closed while $G_4$ and $G_6$ are open thus connecting the output amplifier as a unity gain buffer. $V_{OUT}$ is connected to DUTGND via $G_5$ through a 6 kΩ resistor until $V_{DD}$ and $V_{SS}$ reach approximately ±10 V.

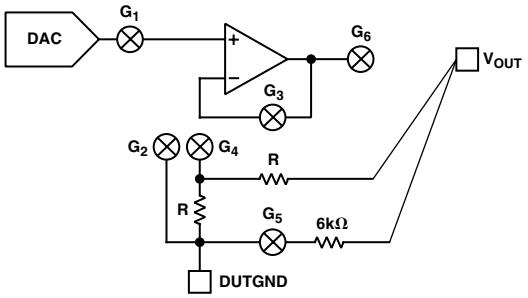



*Figure 17. Output Stage Powering Up with $\overline{CLR}$ High While $V_{DD}/V_{SS}$ < ±10 V*

When the supplies reach ±10 V, the internal power on circuitry opens $G_3$ and $G_5$ and closes $G_4$ and $G_6$ configuring the output stage as shown in Figure 18.

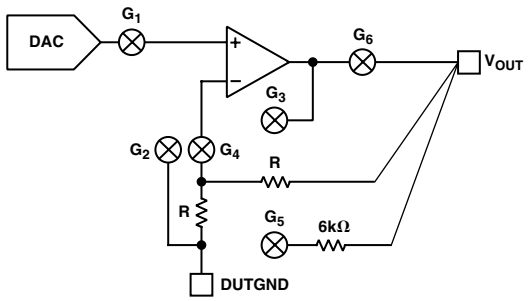



*Figure 18. Output Stage Powering Up with $\overline{CLR}$ High When $V_{DD}/V_{SS}$ > ±10 V*

**DUTGND Voltage Range**

During power-on, the $V_{OUT}$ pins of the AD7836 are connected to the relevant DUTGND pins via $G_6$ and the 6 kΩ thin-film resistor. The DUTGND potential must obey the max ratings at all times. Thus, the voltage at DUTGND must always be within the range $V_{SS}$ – 0.3 V, $V_{DD}$ + 0.3 V. However, in order that the voltages at the $V_{OUT}$ pins of the AD7836 stay within ±2 V of the relevant DUTGND potential during power-on, the voltage applied to DUTGND should also be kept within the range AGND – 2 V, AGND + 2 V.

Once the AD7836 has powered on and the on-chip amplifiers have settled, any voltage that is now applied to the DUTGND pin is subtracted from the DAC output which has been gained up by a factor of two. Thus, for specified operation, the maximum voltage that can be applied to the DUTGND pin increases to the maximum allowable $2 \times V_{REF}(+)$ voltage, and the minimum voltage that can be applied to DUTGND is the minimum $2 \times V_{REF}(-)$ voltage. After the AD7836 has fully powered on, the outputs can track any DUTGND voltage within this minimum/maximum range.

## MICROPROCESSOR INTERFACING

**Interfacing the AD7836—16-Bit Interface**

The AD7836 can be interfaced to a variety of 16-bit microcontrollers or DSP processors. Figure 19 shows the AD7836 interfaced to a generic 16-bit microcontroller/DSP processor. The lower address lines from the processor are connected to A0, A1 and A2 on the AD7836 as shown. The upper address lines are decoded to provide a chip select signal for the AD7836. They are also decoded (in conjunction with the lower address lines if need be) to provide a SEL signal. The fast interface timing of the AD7836 allows direct interface to a wide variety of microcontrollers and DSPs as shown in Figure 19.

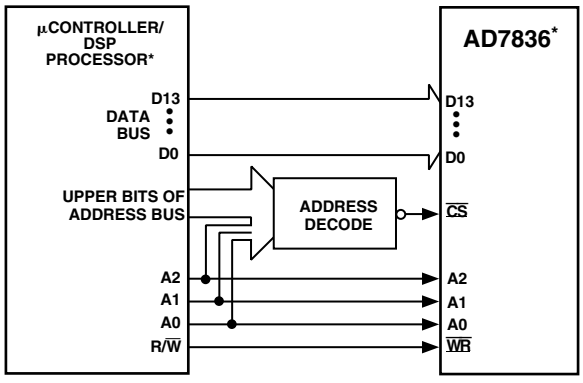



*Figure 19. AD7836 Parallel Interface*

## APPLICATIONS

**Power Supply Bypassing and Grounding**

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD7836 is mounted should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined at one place. If the AD7836 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD7836. If the AD7836 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7836.

Digital lines running under the device should be avoided as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7836 to avoid noise coupling. The power supply lines of the AD7836 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the analog inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but not always possible with a double sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

The AD7836 should have ample supply bypassing located as close to the package as possible, ideally right up against the device. Figure 20 shows the recommended capacitor values of 10 µF in parallel with 0.1 µF on each of the supplies. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

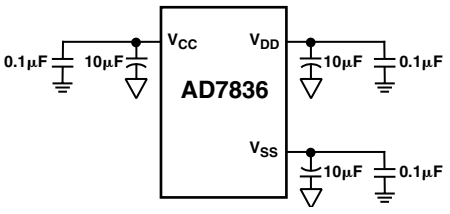



*Figure 20. Recommended Decoupling Scheme for AD7836*

**Automated Test Equipment**

The AD7836 is particularly suited for use in an automated test environment. Figure 21 shows the AD7836 providing the necessary voltages for the pin driver and the window comparator in a typical ATE pin electronics configuration. AD588s are used to provide reference voltages for the AD7836. In the configuration shown, the AD588s are configured so that the voltage at Pin 1 is 5 V greater than the voltage at Pin 9 and the voltage at Pin 15 is 5 V less than the voltage at Pin 9.

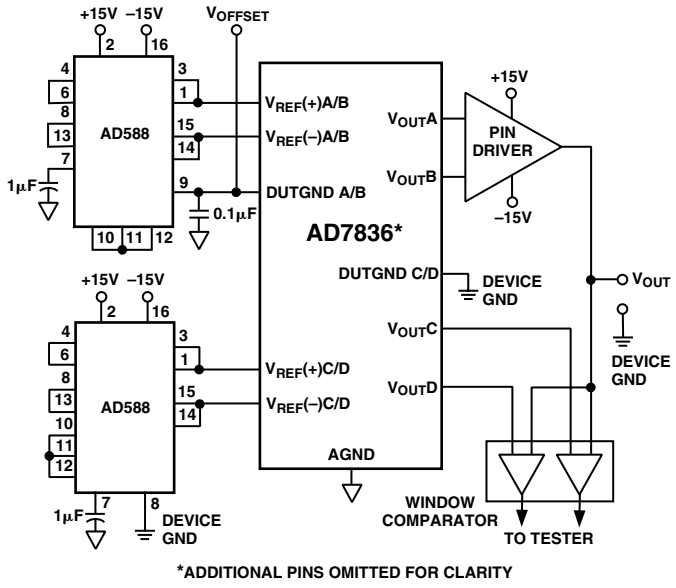



*Figure 21. ATE Application*

One of the AD588s is used as a reference for DACs 1 and 2. These DACs are used to provide high and low levels for the pin driver. The pin driver may have an associated offset. This can be nulled by applying an offset voltage to Pin 9 of the AD588. First, the code 1000 . . . 0000 is loaded into the DACA latch and the pin driver output is set to the DACA output. The $V_{OFFSET}$ voltage is adjusted until 0 V appears between the pin driver output and DUT GND. This causes both $V_{REF}(+)$ and $V_{REF}(–)$ to be offset with respect to AGND by an amount equal to $V_{OFFSET}$. However, the output of the pin driver will vary from –10 V to +10 V with respect to DUT GND as the DAC input code varies from 000 . . . 000 to 111 . . . 111. The $V_{OFFSET}$ voltage is also applied to the DUTGND pins. When a clear is performed on the AD7836, the output of the pin driver will be 0 V with respect to Device GND.

The other AD588 is used to provide a reference voltage for DACs C and D. These provide the reference voltages for the window comparator shown in the diagram. Note that Pin 9 of this AD588 is connected to Device GND. This causes $V_{REF}(+)$C & D and $V_{REF}(–)$C & D to be referenced to Device GND. As DAC 3 and DAC 4 input codes vary from 000 . . . 000 to 111 . . . 111, $V_{OUT}3$ and $V_{OUT}4$ vary from –10 V to +10 V with respect to Device GND. Device GND is also connected to DUTGND. When the AD7836 is cleared, $V_{OUT}$C and $V_{OUT}$D are cleared to 0 V with respect to DEVICE GND.

TrimDAC is a registered trademark of Analog Devices, Inc.

**Programmable Reference Generation for the AD7836 in an ATE Application**

The AD7836 is particularly suited for use in an automated test environment. The reference input for the AD7836 quad 14-bit DAC requires two references for each DAC. Programmable references may be a requirement in some ATE applications as the offset and gain errors at the output of each DAC can be adjusted by varying the voltages on the reference pins of the DAC. To trim offset errors, the DAC is loaded with the digital code 000 . . . 000 and the voltage on the $V_{REF}(–)$ pin is adjusted until the desired negative output voltage is obtained. To trim out gain errors, first the offset error is trimmed. Then the DAC is loaded with the code 111 . . . 111 and the voltage on the $V_{REF}(+)$ pin is adjusted until the desired full scale voltage minus one LSB is obtained.

It is not uncommon in ATE design, to have other circuitry at the output of the AD7836 that can have offset and gain errors of up to say ±300 mV. These offset and gain errors can be easily removed by adjusting the reference voltages of the AD7836. The AD7836 uses nominal reference values of ±5 V to achieve an output span of ±10 V. Since the AD7836 has a gain of two from the reference inputs to the DAC output, adjusting the reference voltages by ±150 mV will adjust the DAC offset and gain by ±300 mV.

There are a number of suitable 8- and 10-bit DACs available that would be suitable to drive the reference inputs of the AD7836, such as the AD7804 which is a quad 10-bit digital-to-analog converter with serial load capabilities. The voltage output from this DAC is in the form of $V_{BIAS} \pm V_{SWING}$ and rail to rail operation is achievable. The voltage reference for this DAC can be internally generated or provided externally. This DAC also contains an 8-bit SUB DAC which can be used to shift the complete transfer function of each DAC around the $V_{BIAS}$ point. This can be used as a fine trim on the output voltage. In this Application two AD7804s are required to provide programmable reference capability for all four DACs. One AD7804 is used to drive the $V_{REF}(+)$ pins and the second package used to drive the $V_{REF}(–)$ pins.

Another suitable DAC for providing programmable reference capability is the AD8803. This is an octal 8-bit trimDAC® and provides independent control of both the top and bottom ends of the trimDAC. This is helpful in maximizing the resolution of devices with a limited allowable voltage control range.

The AD8803 has an output voltage range of GND to $V_{DD}$ (0 V to +5 V). To trim the $V_{REF}(+)$ input, the appropriate trim range on the AD8803 DAC can be set using the $V_{REFL}$ and $V_{REFH}$ pins allowing 8 bits of resolution between the two points. This will allow the $V_{REF}(+)$ pin to be adjusted to remove gain errors.

To trim the $V_{REF}(–)$ voltage, some method of providing a trim voltage in the required negative voltage range is required. Neither the AD7804 or the AD8803 can provide this range in normal operation as their output range is 0 V to +5 V. There are two methods of producing this negative voltage. One method is to provide a positive output voltage and then to level shift that analog voltage to the required negative range. Alternatively

these DACs can be operated with supplies of 0 V and a –5 V, with the $V_{DD}$ pin connected to 0 V and the GND pin connected to –5 V. Now these can be used to provide the negative reference voltages for the $V_{REF}(–)$ inputs on the AD7836. However, the digital signals driving the DACs need to be level shifted from the 0 V to +5 V range to the –5 V to 0 V range. Figure 22 shows a typical application circuit to provide programmable reference capabilities for the AD7836.

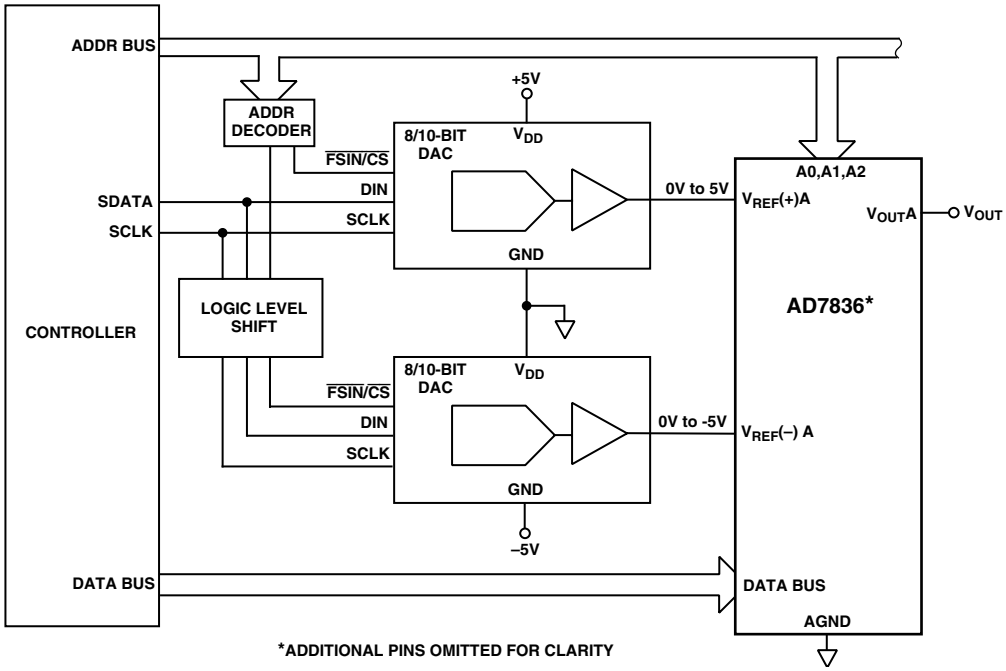
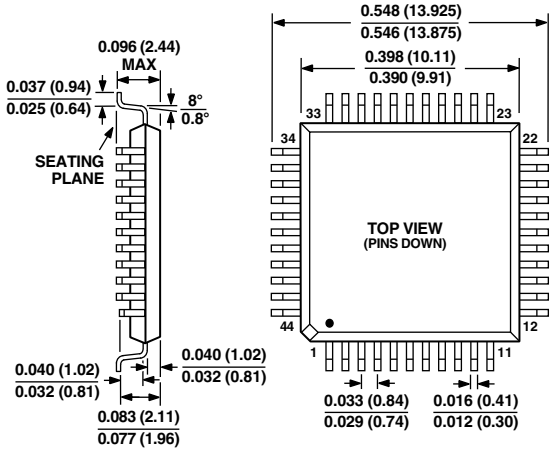



*Figure 22. Programmable Reference Generation for the AD7836*

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 44-Lead MQFP (S-44)

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