

# FDMA8051L

## Single N-Channel PowerTrench® MOSFET

40 V, 10 A, 14 mΩ

### Features

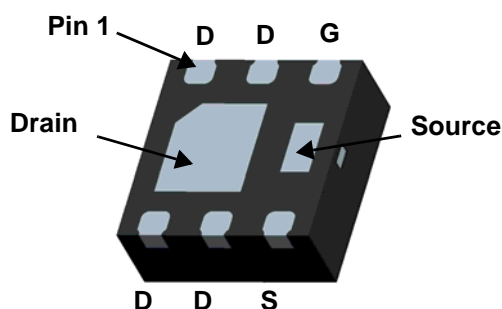
- Max  $r_{DS(on)}$  = 14 mΩ at  $V_{GS} = 10$  V,  $I_D = 10$  A
- Max  $r_{DS(on)}$  = 18 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 8.5$  A
- Low Profile - 0.8 mm maximum in the new package MicroFET 2x2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

### General Description

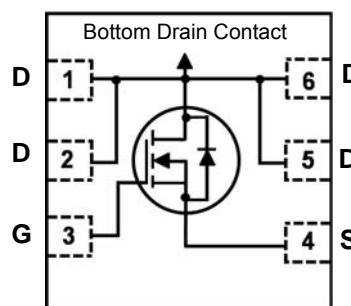
This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low  $r_{DS(on)}$  and gate charge provide excellent switching performance.

### Application

- DC – DC Buck Converters



MicroFET 2X2 (Bottom View)



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	10	A
	-Pulsed (Note 3)	80	
$P_D$	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.4	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
051	FDMA8051L	MicroFET 2X2	7"	8 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		22		mV/ $^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		-5		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$		11	14	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 8.5\text{ A}$		14	18	
		$V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$		15	19	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}$ , $I_D = 10\text{ A}$		35		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		901	1260	pF
$C_{oss}$	Output Capacitance			251	350	pF
$C_{rss}$	Reverse Transfer Capacitance			16	25	pF
$R_g$	Gate Resistance		0.1	0.6	1.8	$\Omega$

**Switching Characteristics**

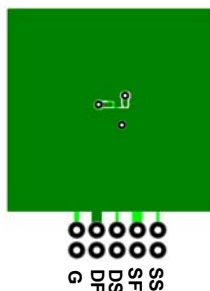
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{ V}$ , $I_D = 10\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		6.4	13	ns
$t_r$	Rise Time			1.8	10	ns
$t_{d(off)}$	Turn-Off Delay Time			17	31	ns
$t_f$	Fall Time			1.8	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$	$V_{DD} = 20\text{ V}$ , $I_D = 10\text{ A}$	14	20	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$		6.4	9.0	nC
$Q_{gs}$	Gate to Source Charge			2.4	3.7	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.8	2.5	nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 10\text{ A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		23	37	ns
$Q_{rr}$	Reverse Recovery Charge			6.7	14	nC

## NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a. 52  $^{\circ}\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 145  $^{\circ}\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Pulsed  $I_d$  limited by junction temperature,  $t_d \leq 100\text{ }\mu\text{s}$ , please refer to SOA curve for more details.

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

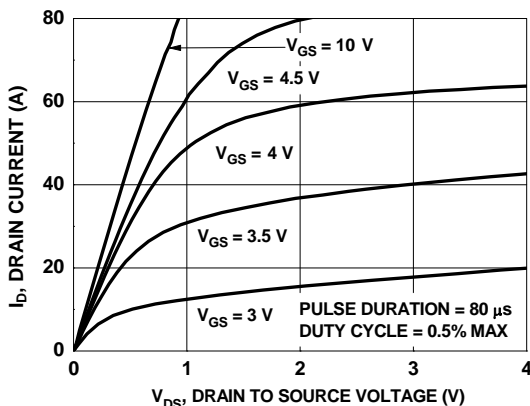


Figure 1. On-Region Characteristics

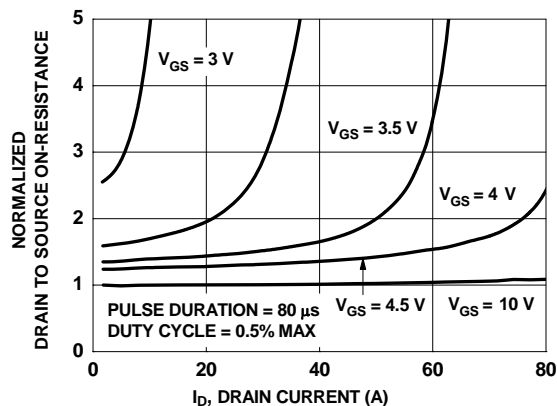


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

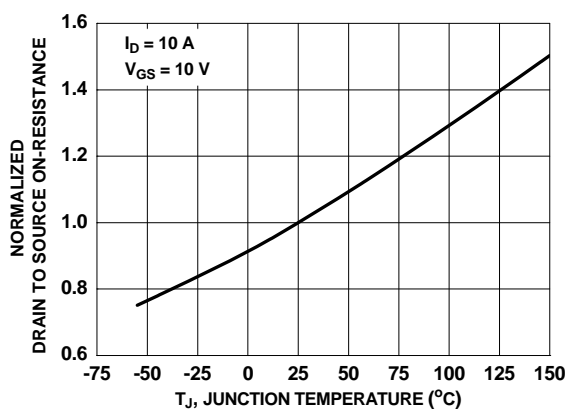


Figure 3. Normalized On-Resistance vs Junction Temperature

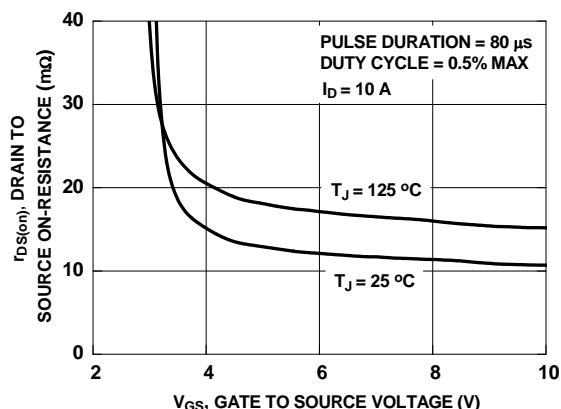


Figure 4. On-Resistance vs Gate to Source Voltage

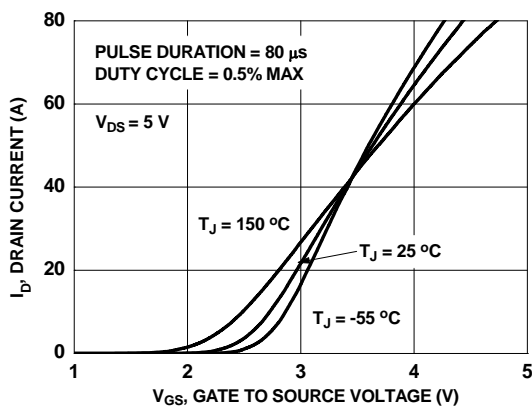


Figure 5. Transfer Characteristics

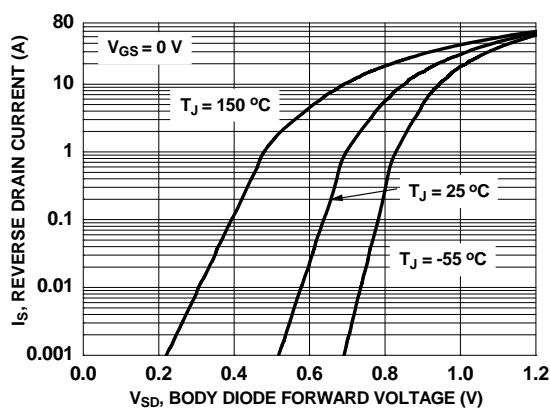


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

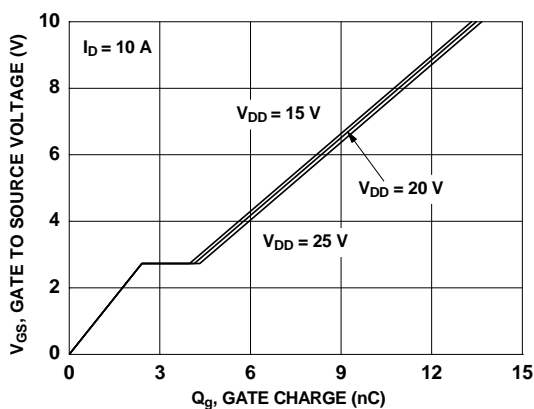


Figure 7. Gate Charge Characteristics

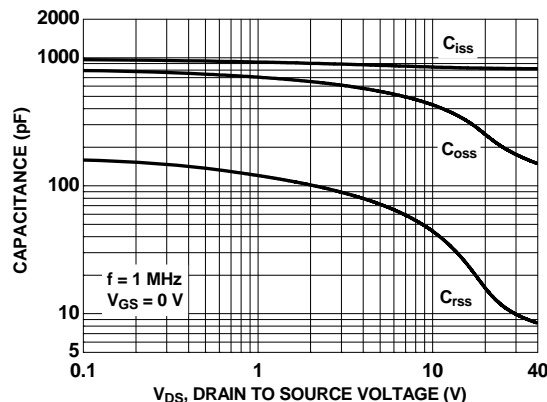


Figure 8. Capacitance vs Drain to Source Voltage

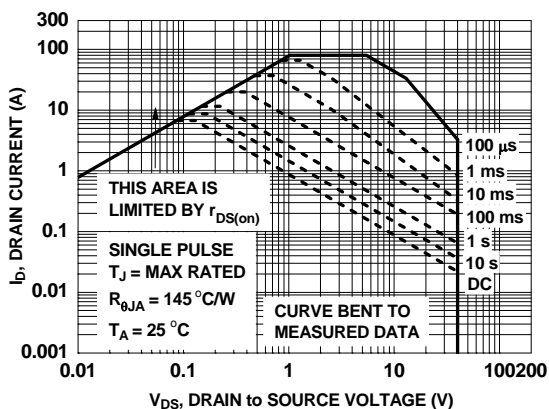


Figure 9. Forward Bias Safe Operating Area

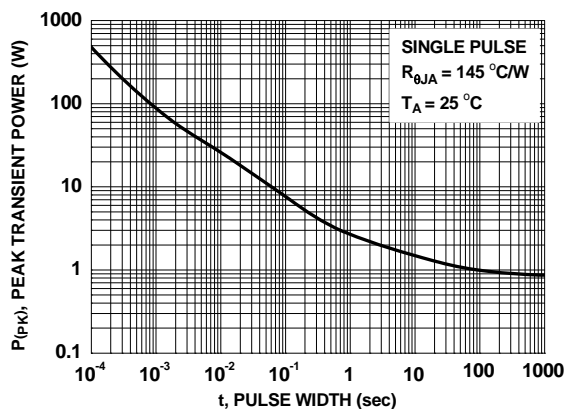


Figure 10. Single Pulse Maximum Power Dissipation

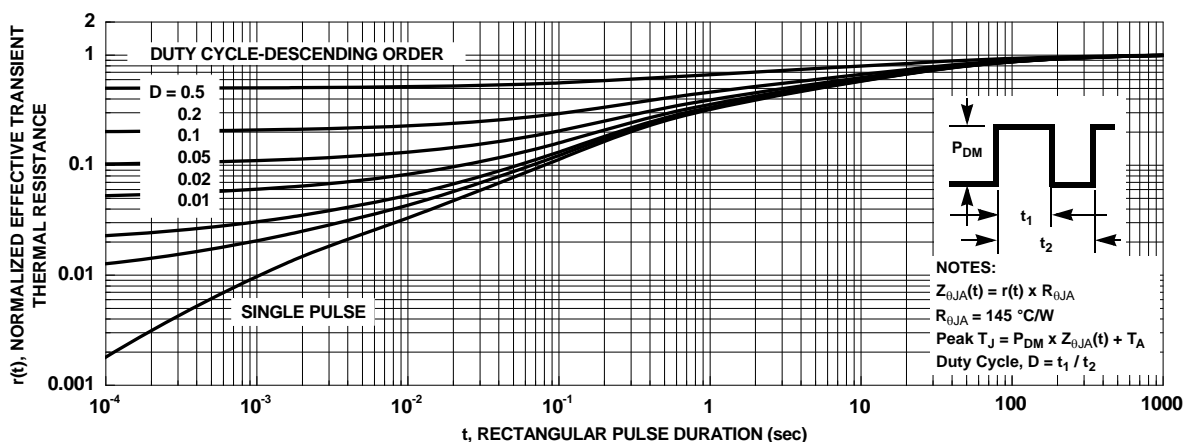
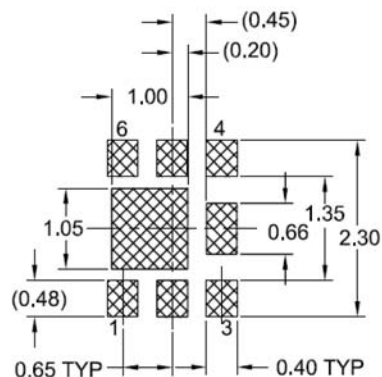
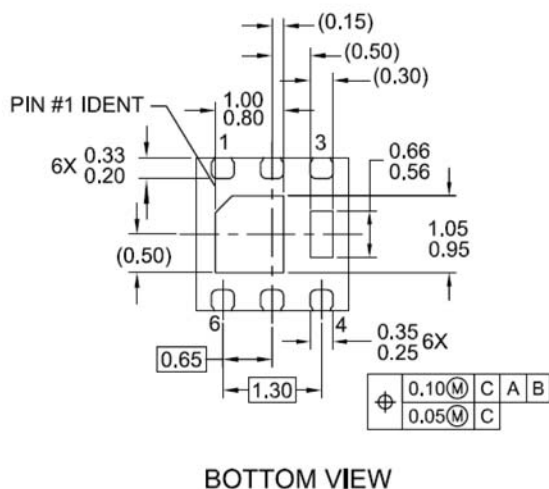
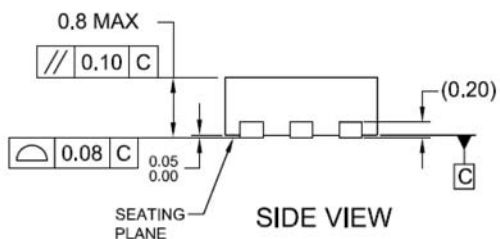
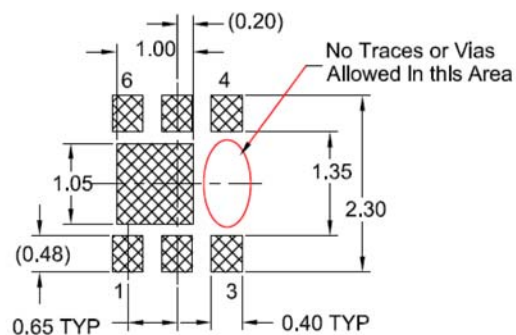
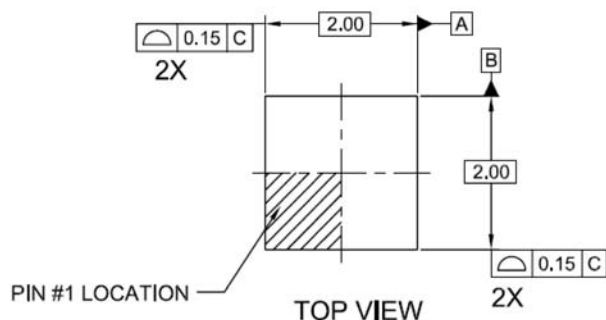


Figure 11. Single Pulse Junction-to-Ambient Transient Thermal Response Curve

# Dimensional Outline and Pad Layout



## NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DRAWING FILENAME:



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