7-CHANNEL INTEGRATED ESD SOLUTION FOR VGA PORT WITH INTEGRATED LEVEL SHIFTER AND MATCHING IMPEDANCE

Check for Samples: TPD7S019

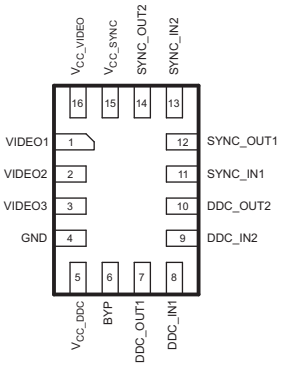
FEATURES

- **7-Channel ESD Protection Includes ESD Protection, Level-Shifting, Buffering and Sync Impedance Matching**
- **Exceeds IEC61000-4-2 (Level 4) ESD Protection to Requirements on the External Pins**
  - **±15-kV Human-Body Model (HBM)**
  - **±8-kV IEC 61000-4-2 Contact Discharge**
- **Very Low Loading Capacitance from ESD Protection Diodes on VIDEO Lines (2.5 pF)**
- **5-V Drivers for HSYNC and VSYNC Lines**
- **Integrated Impedance Matching Resistors on Sync Lines:**
  - **TPD7S019-15: 15-Ω Termination**
- **Bi-Directional Level Shifting N-Channel FETs Provided for DDC_CLK and DDC_DATA Channels**
- **Flow-Through Single-In-Line Pin Mapping Ensures no Additional Board Layout Burden while Placing the ESD Protection Chip Near the Connector**

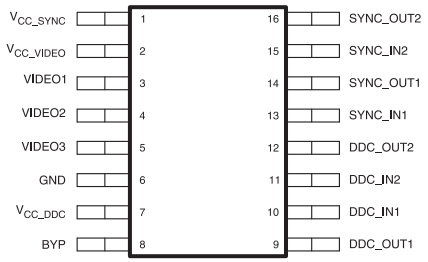
APPLICATIONS

- **VGA and DVI-I Ports in:**
  - **Desktop and Notebook PCs**
  - **Graphics Cards**
  - **Set Top Boxes**
  - **TV**

RSV PACKAGE
(TOP VIEW)



DBQ PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	µQFN – RSV	Tape and reel	TPD7S019-15RSVR	ZUS
	SSOP/QSOP – DBQ	Tape and reel	TPD7S019-15DBQR	PQ19-15

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TERMINATION AT SYNC	PITCH	LENGTH (TYP)	WIDTH (TYP)	HEIGHT (MAX)	ORDERABLE PART NO.
15-Ω	0.635 mm	4.9 mm	6.0 mm	1.75 mm	TPD7S019-15DBQR
15-Ω	0.4 mm	2.6 mm	1.8 mm	0.55 mm	TPD7S019-15RSVR

DESCRIPTION/ORDERING INFORMATION

The TPD7S019 is an integrated 7-channel ESD solution for the VGA or DVI-I port connector. This device integrates ESD protection for all signals, level shifting for the DDC signals and buffering for the SYNC signals.

Three individual supply lines control the power rails of the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage video controller ICs in mixed supply-voltage environments.

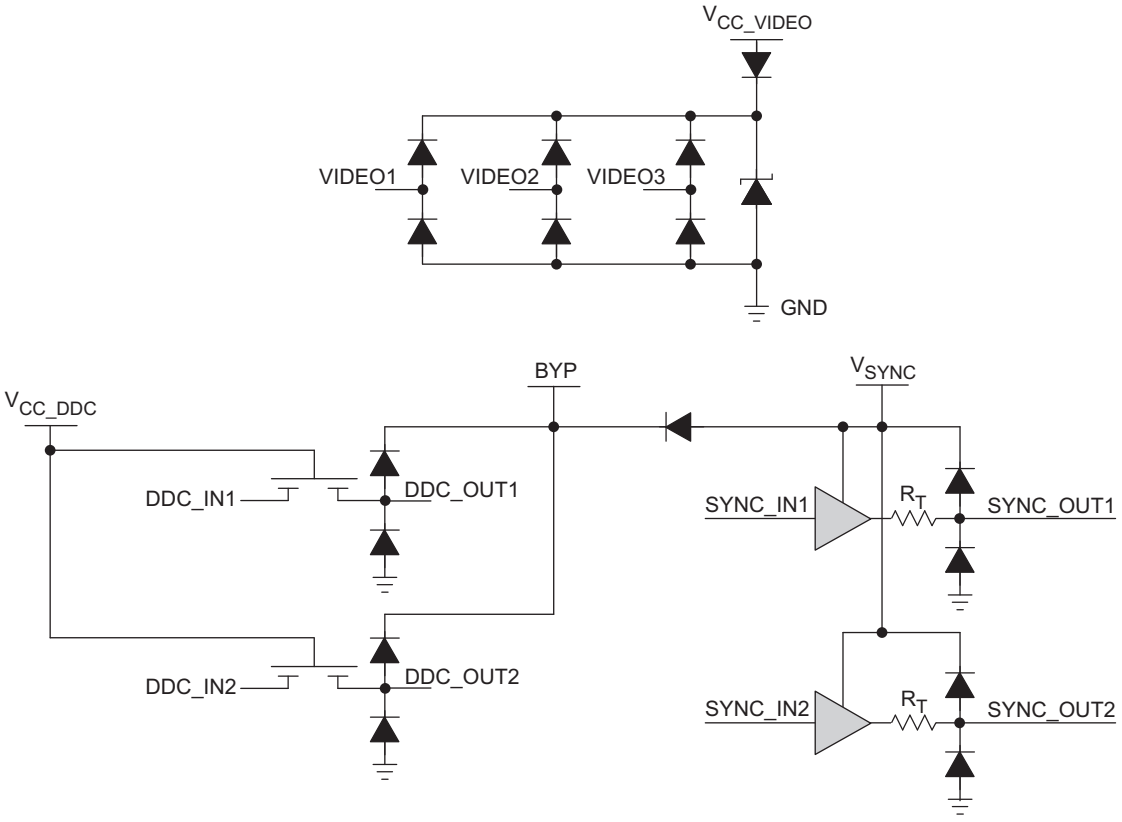
Two non-inverting drivers provide buffering for the HSYNC and VSYNC signals from the video controller IC (SYNC1, SYNC2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and VCC_SYNC, which is typically 5 V. Additionally, each driver has a series termination resistor (RT) connected to the SYNC_OUT pin, eliminating the external termination resistors typically required for the HSYNC and VSYNC lines of the video cable. At the SYNC output the TPD7S019 offers a 15-Ω series termination resistor to match transmission line impedances.

Two N-channel MOSFETs provide the level shifting function required when the DDC controller is operated at a lower supply voltage than the monitor. The gate terminals for the MOSFETs (VCC_DDC) should be connected to the supply rail (typically 3.3 V) that supplies power to the transceivers of the DDC controller.

The TPD7S019 confirms the IEC61000-4-2 (Level 4) system level ESD protection and ±15KV HBM ESD protection. This device is offered in space-saving 16-pin DBQ and 16-pin RSV packages.

The TPD7S019 is characterized for operation over ambient air temperature of –40°C to 85°C.

CIRCUIT DIAGRAM



TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	DBQ	RSV		
BYP	8	6	Power	Bypass pin. Using a 0.2 µF bypass capacitor will increase the ESD robustness of the system.

TERMINAL FUNCTIONS (continued)

TERMINAL			TYPE	DESCRIPTION
NAME	NO.			
	DBQ	RSV		
DDC_IN1 DDC_IN2	10 11	8 9	I	DDC signal input. Connects to the VGA controller side of one of the sync lines.
DDC_OUT1 DDC_OUT2	9 12	7 10	O	DDC signal output. Connects to the video connector side of one of the sync lines.
GND	6	4	–	Ground
SYNC_IN1 SYNC_IN2	13 15	11 13	I	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
SYNC_OUT1 SYNC_OUT2	14 16	12 14	O	Sync signal buffer output. Connects to the video connector side of one of the sync lines
VCC_DDC	7	5	Power	Isolated supply input for the DDC_1 and DDC_2 level-shifting N-FET gates
VCC_SYNC	1	15	Power	Isolated supply input for the SYNC_1 and SYNC_2 level shifters and their associated ESD protection circuits
VCC_VIDEO	2	16	Power	Supply pin specifically for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD protection circuits
VIDEO1 VIDEO2 VIDEO3	3 4 5	1 2 3	ESD	High-speed ESD clamp input

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC_VIDEO}, V_{CC_DDC}, V_{CC_SYNC}	Supply voltage		–0.5	6.0	V
$V_{IO(VIDEO)}$	IO voltage	VIDEOx pins	–0.5	V_{CC_VIDEO}	V
$V_{I(SYNC)}$	Input voltage	SYNC pins	–0.5	V_{CC_SYNC}	V
$V_{I(DDC)}$	Input voltage	DDC_INx pins	–0.5	6.0	V
$V_{O(DDC)}$	Output voltage	DDC_INx pins	–0.5	6.0	V
T_{stg}	Storage temperature		–55	125	°C
	IEC 61000-4-2 Contact Discharge	VIDEO, DDC_OUT, SYNC_OUT pins		±8	kV
	HBM ESD	VIDEO, DDC_OUT, SYNC_OUT pins		±15	kV
		VCC, DDC_IN, SYNC_IN, BYP Pins		±2	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC_VIDEO}, V_{CC_DDC}, V_{CC_SYNC}	Supply voltage		0	5.5	V
$V_{IO(VIDEO)}$	IO voltage	VIDEOx pins	0	VCC_VIDEO	V
$V_{I(SYNC)}$	Input voltage	SYNC pins	0	VCC_SYNC	V
$V_{I(DDC)}$	Input voltage	DDC_INx pins	0	5.5	V
$V_{O(DDC)}$	Output voltage	DDC_INx Pins	0	5.5	V
T_A	Operating temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITION		MIN	TYP	MAX	UNIT
I_{CC_VIDEO}	V_{CC_VIDEO} supply current		V_{CC_VIDEO} = 5 V, VIDEO inputs at V_{CC_VIDEO} or GND			1	10	µA
I_{CC_DDC}	V_{CC_DDC} supply current		V_{CC_DDC} = 5 V			1	10	µA
I_{CC_SYNC}	V_{CC_SYNC} supply current		V_{CC_SYNC} = 5 V,	SYNC inputs at GND or V_{CC_SYNC}, SYNC outputs unloaded		1	50	µA
				SYNC inputs at 3 V; SYNC outputs unloaded			2.0	mA
I_{IO_VIDEO}	VIDEO input/output pins		V_{IO_VIDEO} = 3 V			0.01	1.0	µA
I_{OFF}	DDC pin power down leakage current		V_{CC_DDC} ≤ 0.4 V, V_{DDC_OUT} = 5 V			0.01	1.0	µA
V_D	Diode forward voltage for lower clamp of VIDEO, DDC, SYNC output pins		I_D = 8 mA, lower clamp diode		–0.6	–0.8	–0.95	V
R_{DYN_VIDEO}	Dynamic resistance (VIDEO pins)		I = 1 A			1.0		Ω
V_{IH}	High-level SYNC logic input voltage		V_{CC_SYNC} = 5 V		2.0			V
V_{IL}	Low-level SYNC logic input voltage		V_{CC_SYNC} = 5 V				0.6	V
V_{OH}	High-level SYNC logic output voltage		I_{OH} = 0 mA, V_{CC_SYNC} = 5 V		4.85			V
V_{OH-15}	High-level SYNC logic output voltage	TPD7S019-15	I_{OH} = 24 mA, V_{CC_SYNC} = 5 V		2			V
V_{OL}	Low-level SYNC logic output voltage		I_{OH} = 0 mA, V_{CC_SYNC} = 5 V				0.15	V
V_{OL-15}	Low-level SYNC logic output voltage	TPD7S019-15	I_{OH} = 24 mA, V_{CC_SYNC} = 5 V				0.8	V
R_T	SYNC driver output resistance	TPD7S019-15	V_{CC_SYNC} = 5 V, SYNC inputs at GND or 3 V			15		Ω
C_{IO_VIDEO}	IO capacitance of VIDEO pins		V_{IO} = 2.5 V			2.5	4	pF
t_{PLH}	SYNC driver L => H propagation delay		C_L = 50 pF; V_{CC} = 5 V, input t_R and t_F ≤ 5ns				12	ns
t_{PHL}	SYNC driver H => L propagation delay		C_L = 50 pF; V_{CC} = 5 V, input t_R and t_F ≤ 5ns				12	ns
t_R, t_F	SYNC driver output rise & fall times		C_L = 50 pF; V_{CC} = 5 V, input t_R and t_F ≤ 5ns			4		ns
V_{BR}	VIDEO ESD diode break-down voltage		I_{IO} = 1 mA		9			V

Typical Characteristics

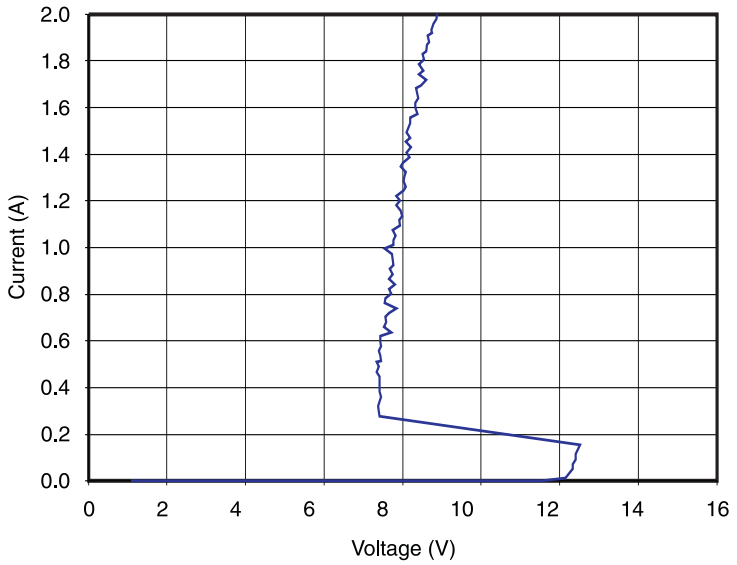


Figure 1. TPD7S019-xx TLP VID1 to GND, Barth, T_{rf} = 10 ns

Typical Characteristics (continued)

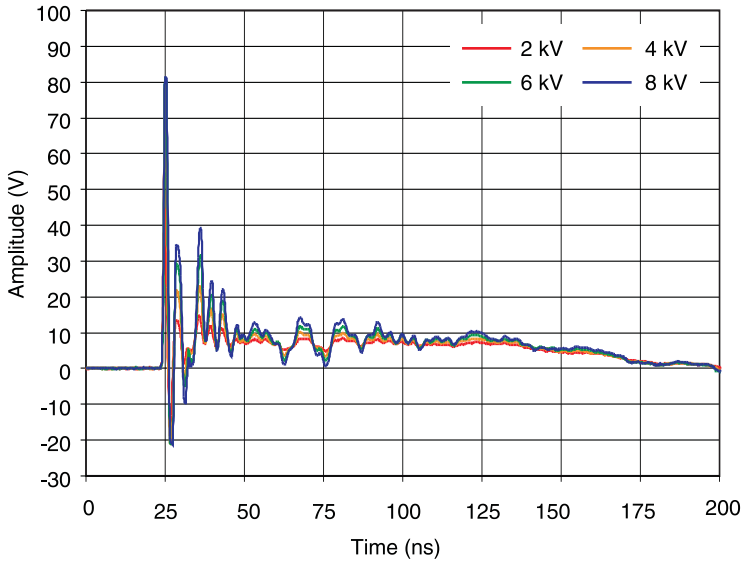


Figure 2. TPD7S019-xx IEC Clamping Waveforms Positive Contact

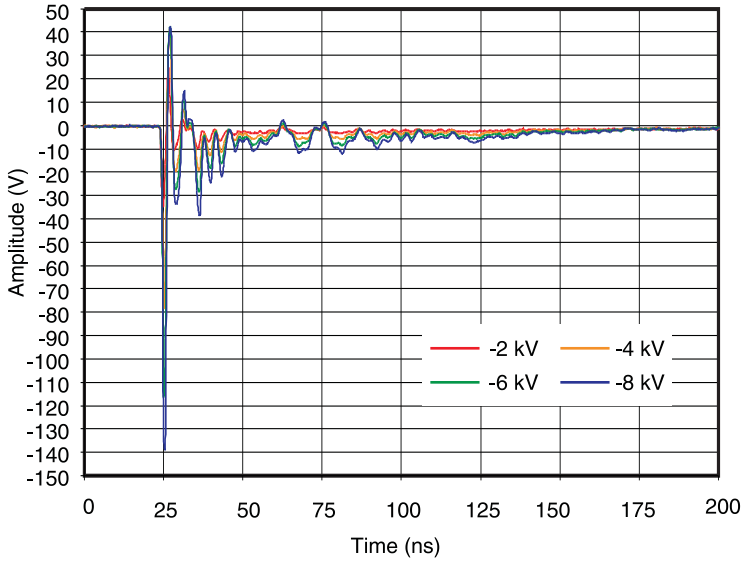


Figure 3. TPD7S019-xx IEC Clamping Waveforms Negative Contact

Typical Characteristics (continued)

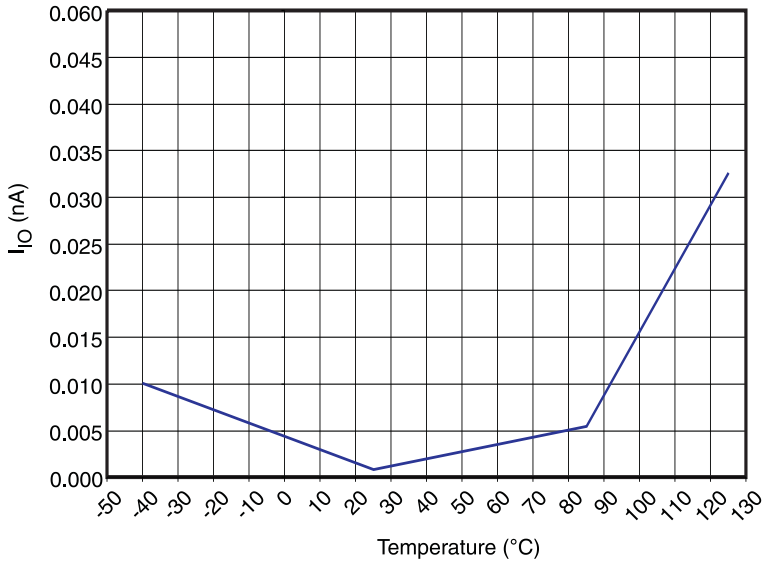


Figure 4. Leakage Current Trough VIDEO Pins
V_{CC_VIDEO} = 5 V

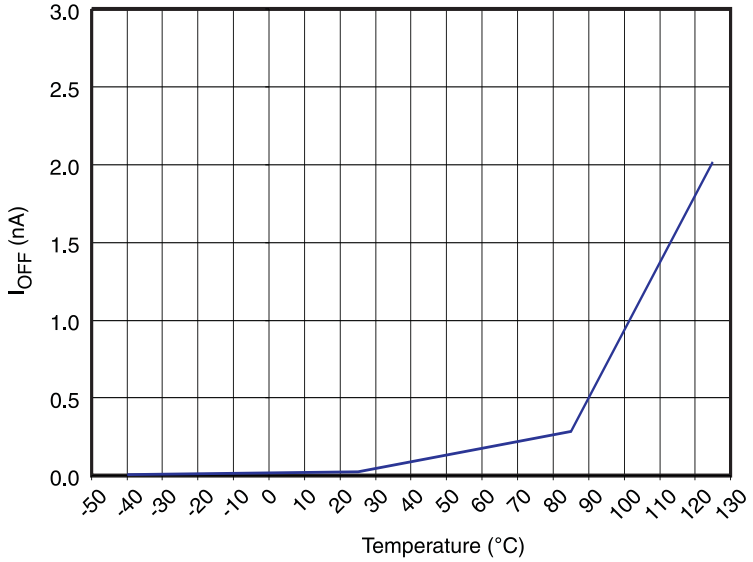


Figure 5. I_{OFF} (DDC_OUTx)
V_{CC_DDC} = 0 V

APPLICATION INFORMATION

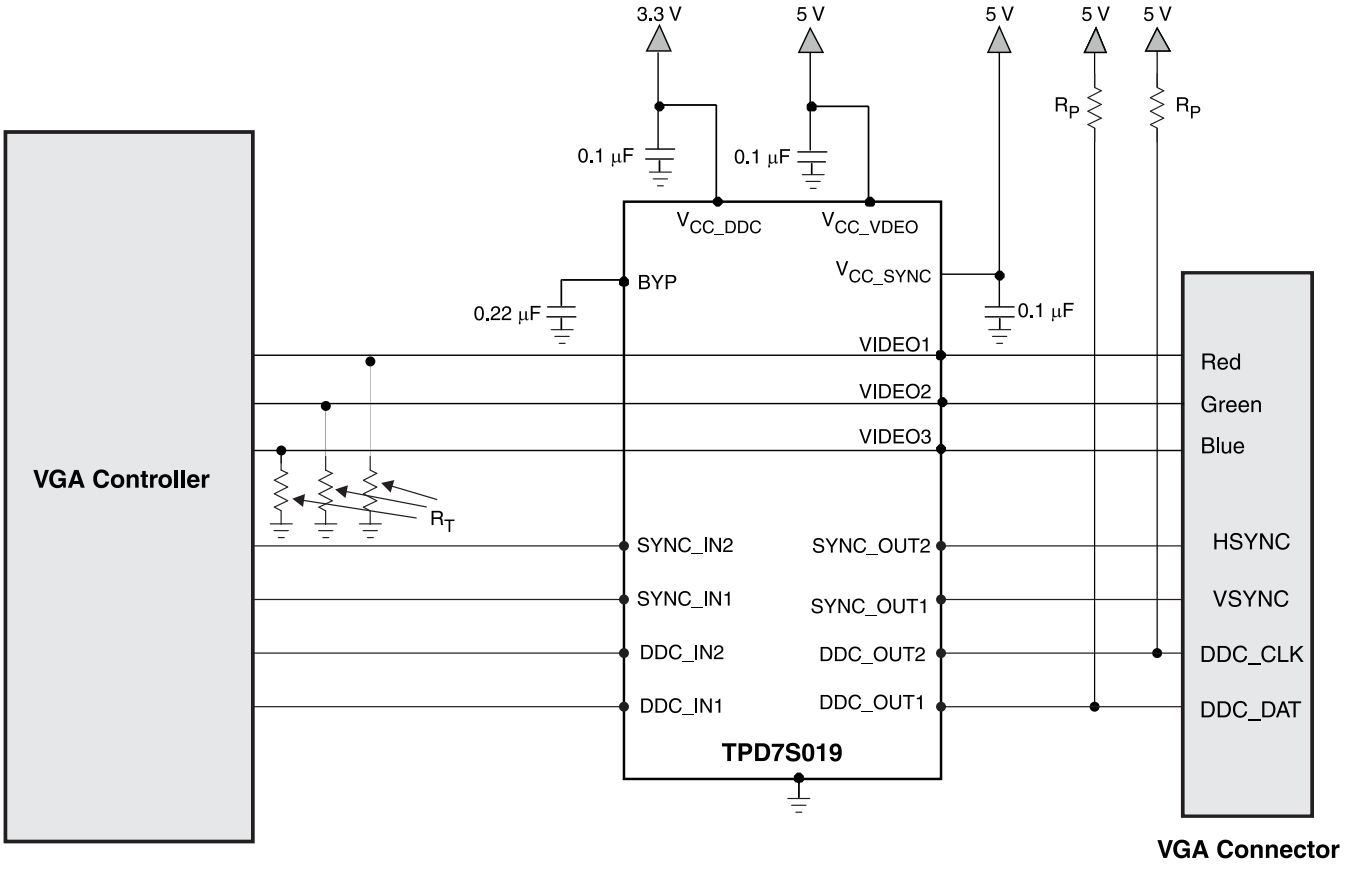


Figure 6. Typical Application Schematics with TPD7S019

R_P: Pullup resistor for the DDC data and clock lines. Typically system designer selects 47 kΩ pullup values

R_T: Line termination resistor for the RGB lines. RT is selected to match the transmission line. For a single-ended transmission line, RT can be anywhere from 50 Ω to 75 Ω depending on board trace impedance.

Some systems may require additional filters at the SYNC and RGB lines.

The TPD7S019 should be placed as close to the VGA port as possible.

The ESD protection channels VIDEO1, VIDEO2, VIDEO3 are identical circuits, they can be used interchangeably between the R, G, B signals.

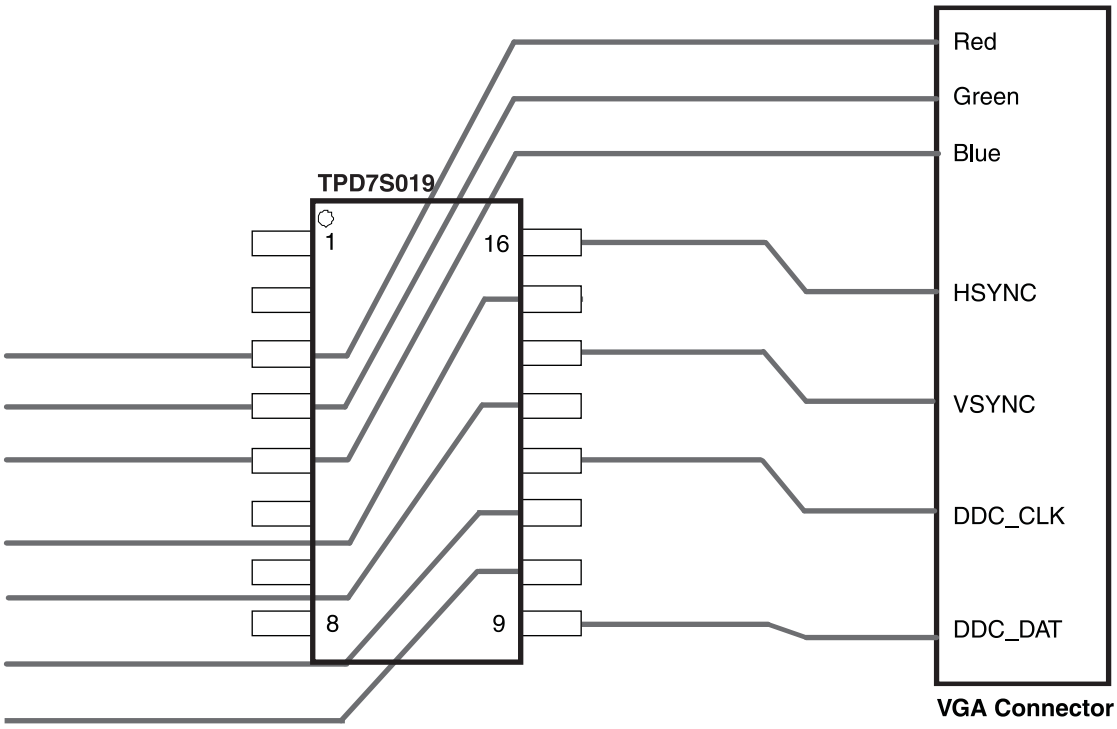


Figure 7. Simplified Layout with TPD7S019 (Only IO Lines are Shown)

REVISION HISTORY

Changes from Original (August 2010) to Revision A	Page
• Removed PREVIEW status from the RSV package.	1

Changes from Revision A (March 2012) to Revision B	Page
• Removed non released part descriptions from the datasheet.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD7S019-15DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PQ19-15	Samples
TPD7S019-15RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZUS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

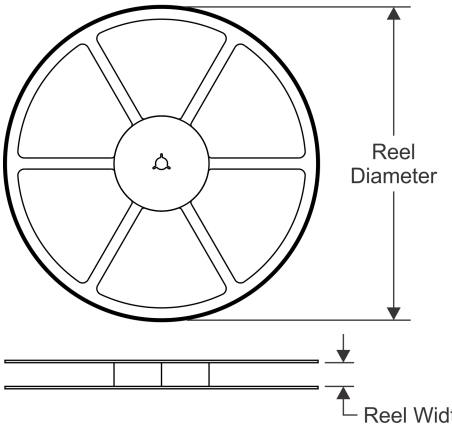
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

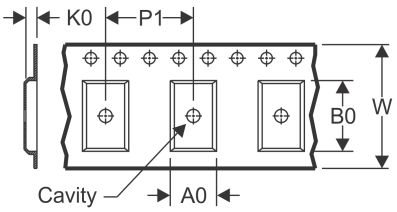
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

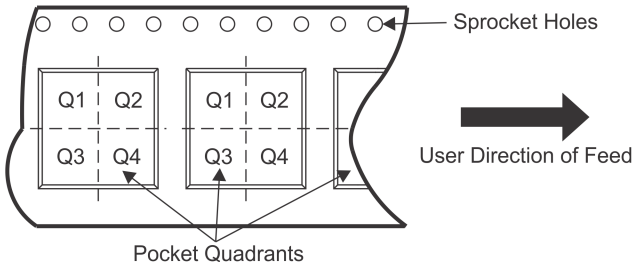


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

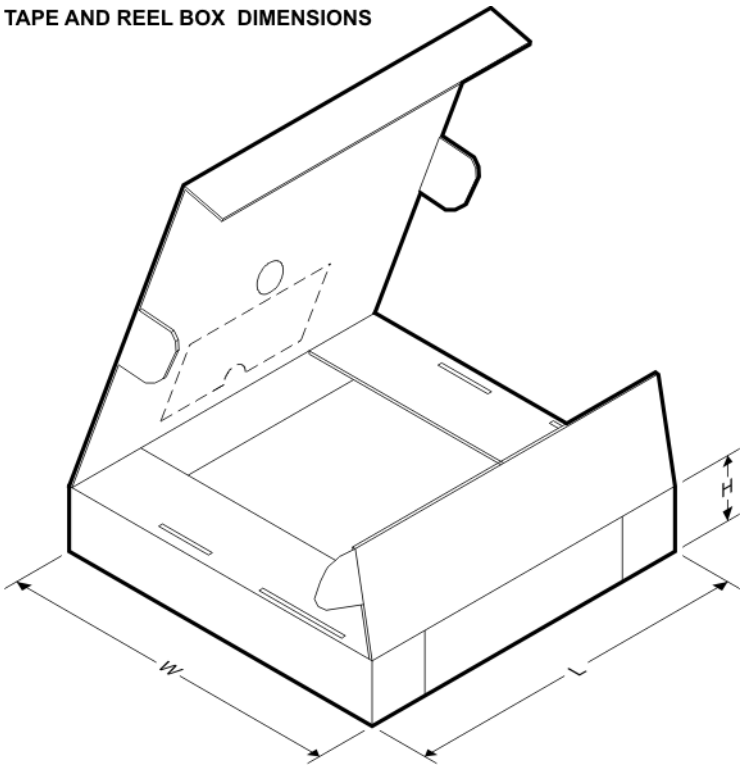
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD7S019-15DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPD7S019-15RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1

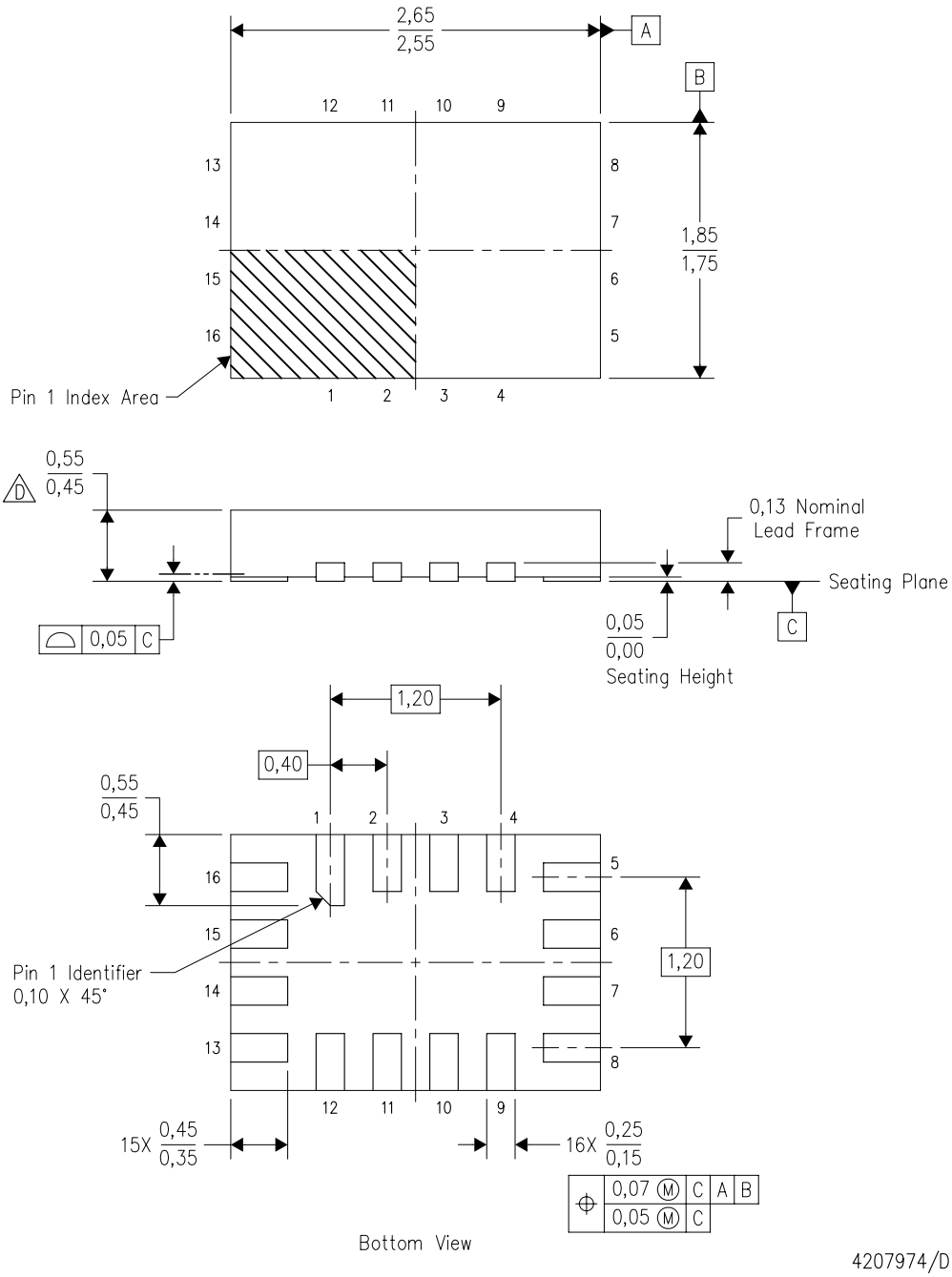
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

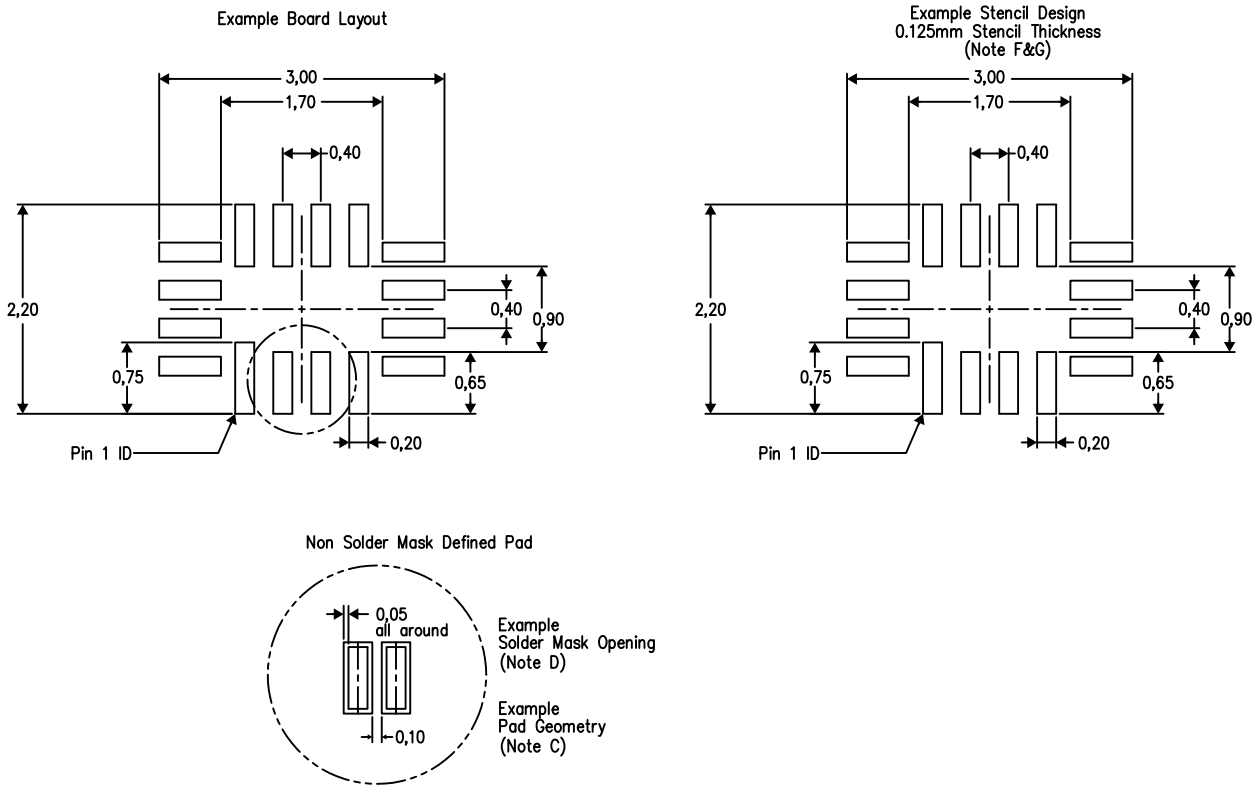
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD7S019-15DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
TPD7S019-15RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



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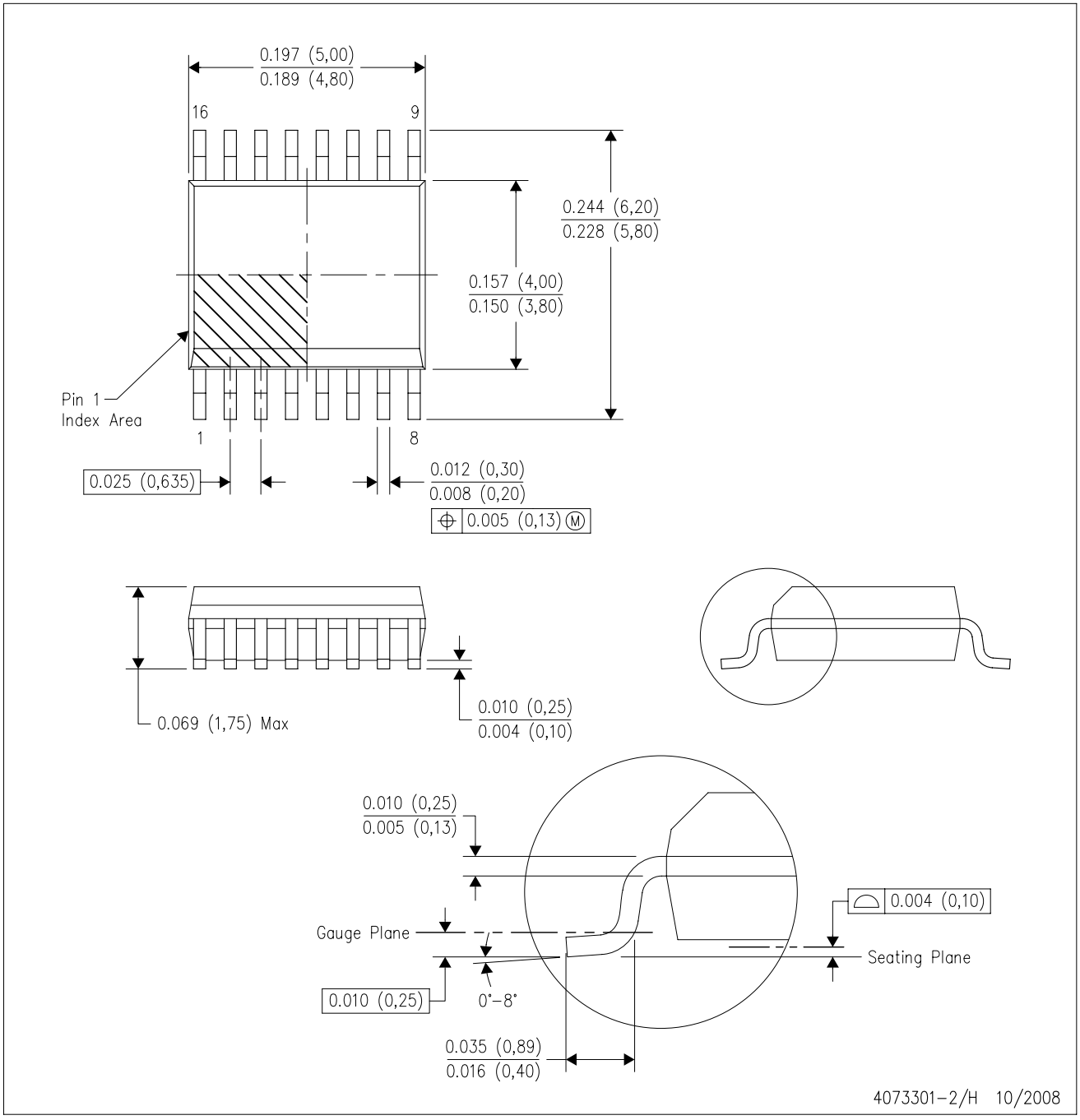
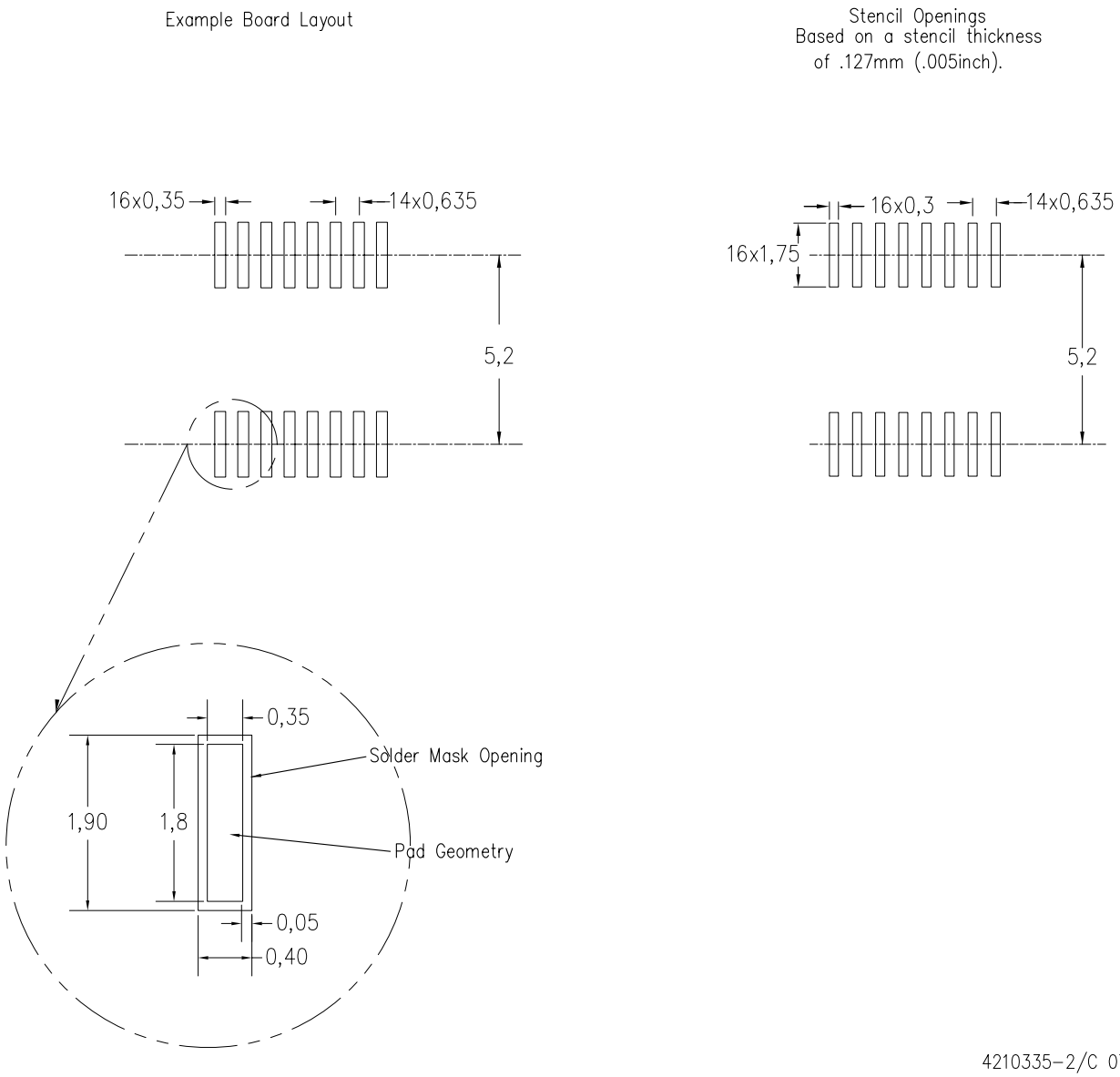
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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