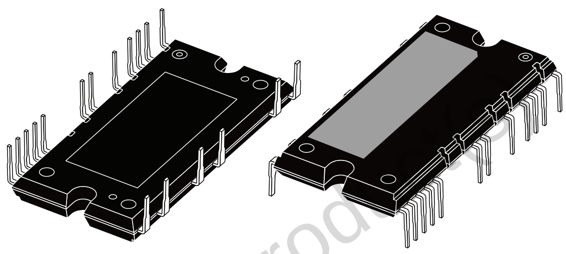
STGIPL35K120L1

SLLIMM™ (small low-loss intelligent molded module) IPM, single phase - 35 A, 1200 V short-circuit rugged IGBT

Datasheet — preliminary data

Features

- IPM 35 A, 1200 V single phase IGBT including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- $V_{CE(sat)}$ negative temperature coefficient
- Active Miller clamp feature
- Undervoltage lockout
- Desaturation detection
- Fault status output
- Input compatible with pulse transformer or optocoupler
- DBC substrate leading to low thermal resistance
- Isolation rating of 2500 V_{rms}/min
- 4.7 kΩ NTC for temperature control



SDIP-18L

Applications

- Power inverters

Description

This intelligent power module provides a compact, high performance AC motor drive for a simple and rugged design. It targets power inverters for air conditioners. It combines ST proprietary control ICs with the most advanced short-circuit rugged IGBT system technology. SLLIMM™ is a trademark of STMicroelectronics.

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPL35K120L1	GIPL35K120L1	SDIP-18L	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

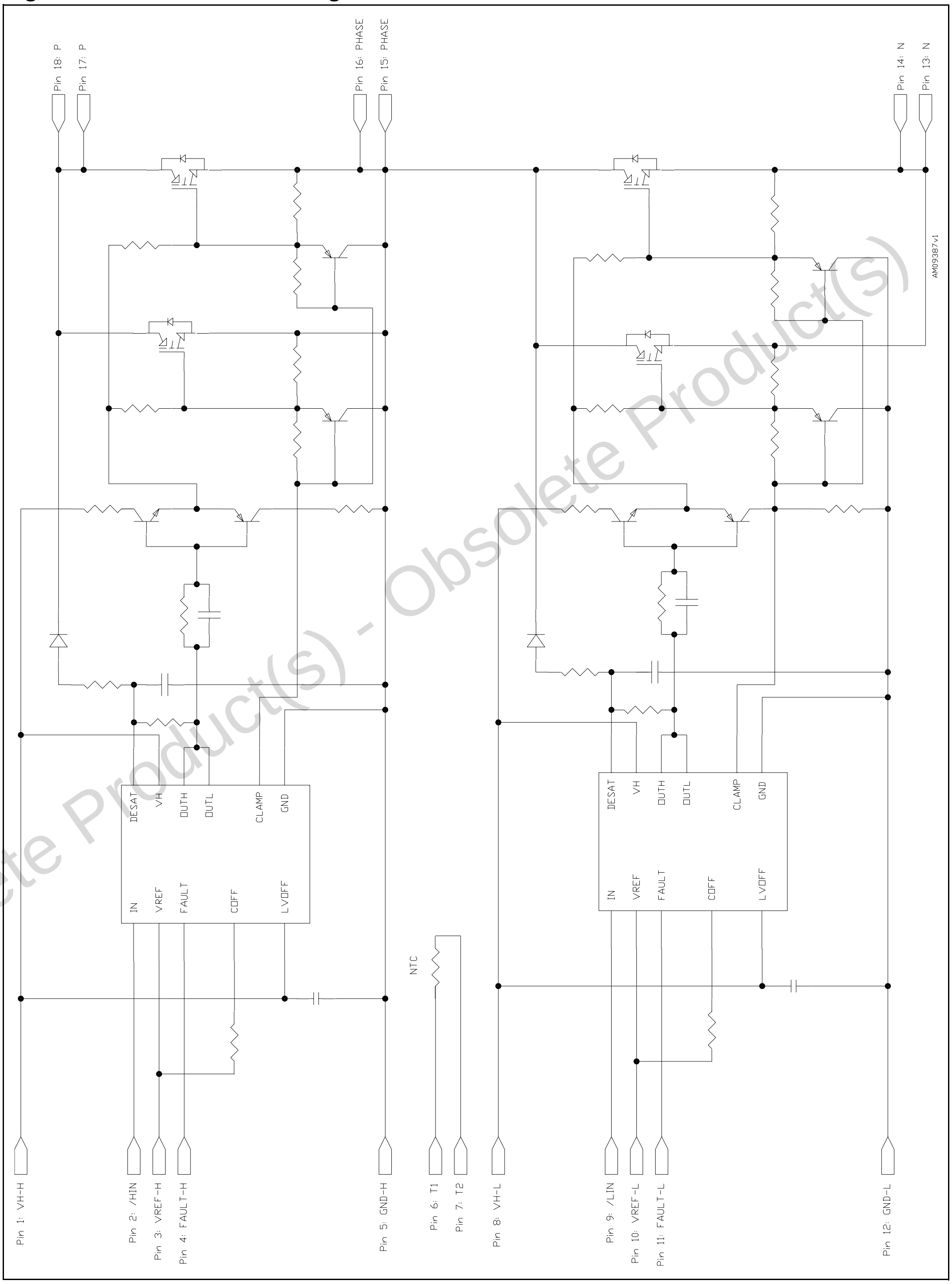
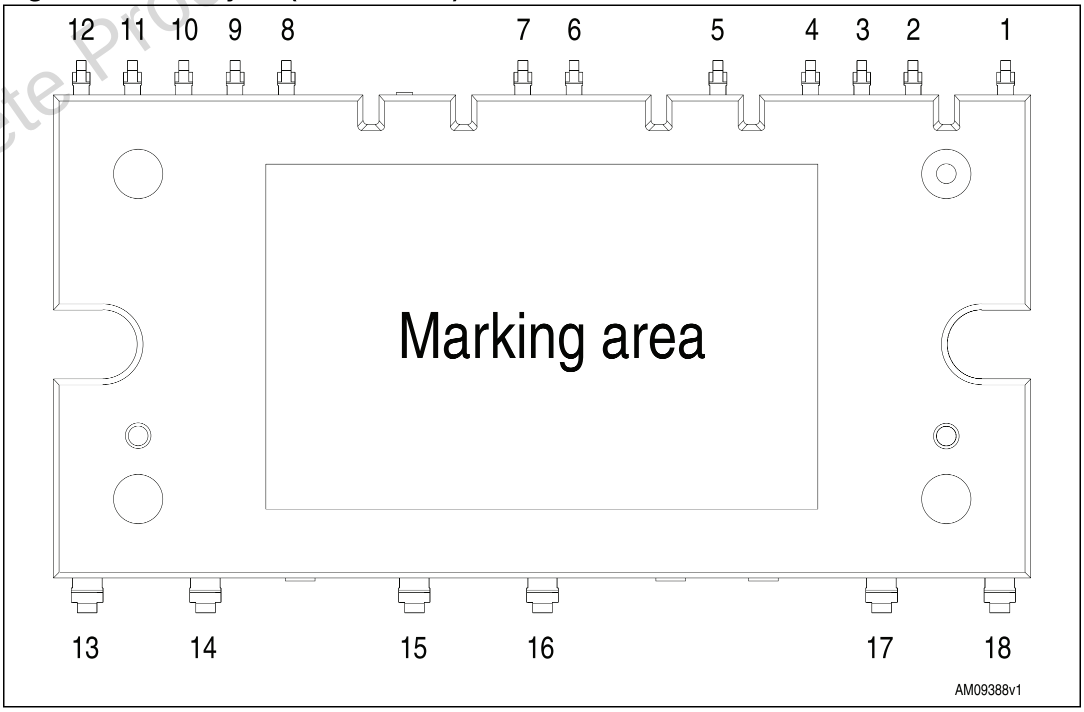


Table 2. Pin description

Pin	Symbol	Description
1	VH-H	High side gate driver power supply
2	$\overline{\text{HIN}}$	High side logic input (active low)
3	VREF-H	High side gate driver +5 V reference voltage
4	FAULT-H	High side gate driver fault output status
5	GND-H	High side gate driver ground
6	T1	NTC thermistor terminal 1
7	T2	NTC thermistor terminal 2
8	VH-L	Low side gate driver power supply
9	$\overline{\text{LIN}}$	Low side logic input (active low)
10	VREF-L	Low side gate driver +5 V reference voltage
11	FAULT-L	Low side gate driver fault output status
12	GND-L	Low side gate driver ground
13	N	Negative DC input
14	N	Negative DC input
15	PHASE	Phase output
16	PHASE	Phase output
17	P	Positive DC input
18	P	Positive DC input

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{CE}	Each IGBT collector emitter voltage	1200	V
$\pm I_C$ (1)	Each IGBT continuous collector current at $T_C = 25°C$	35	A
$\pm I_{CP}$ (2)	Each IGBT pulsed collector current	70	A
P_{TOT}	Each IGBT total dissipation at $T_C = 25°C$	100	W
t_{scw}	Short circuit withstand time, $V_{CE} = 0.5\ V_{(BR)CES}$ $T_J = 125\ °C$, $V_{H\text{-}H} = 15\ V$, $V_I = 1$ "logic state"	5	µs

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

2. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Value	Unit
VH	Maximum VH-H, VH-L voltages vs. GND	28	V
V_{fault}	Voltage on FAULT pin	-0.3 to VH+0.3	V
V_{other}	Voltage on other pins (IN, VREF)	-0.3 to 7	V

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 sec.)	2500	V
T_J (1)	Operating junction temperature for IGBT and diode	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

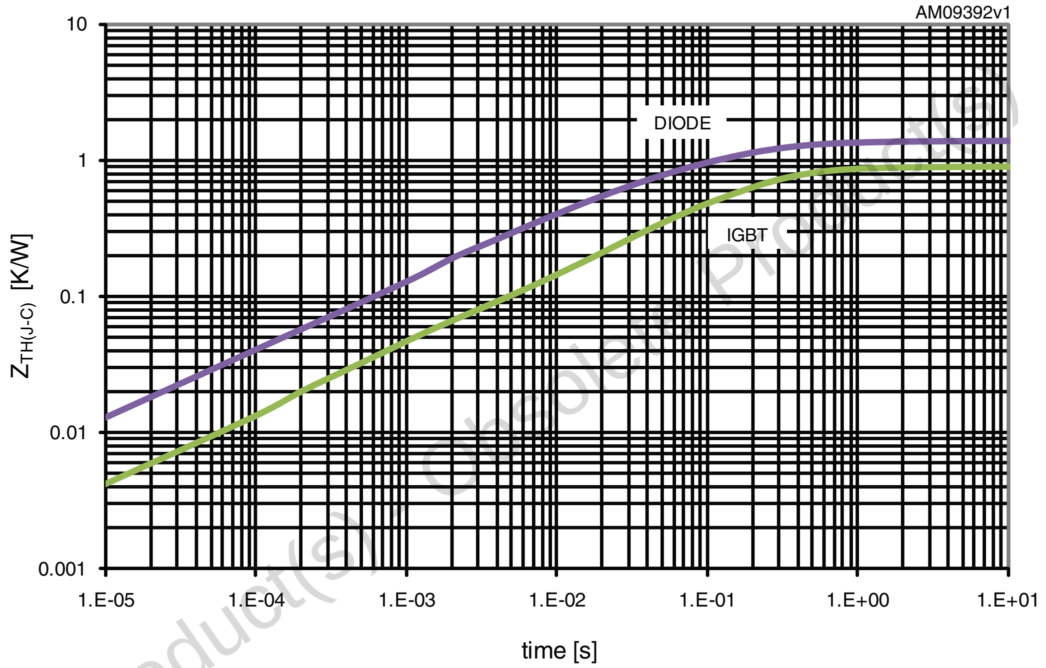
1. The maximum junction temperature rating of the power chips integrated within the SDIP module is 150 °C (@$T_C \leq 100$ °C). To ensure safe operation of the NDIP module, the average junction temperature should be limited to $T_{J(avg)} \leq 125$ °C (@$T_C \leq 100$ °C).

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case single IGBT	0.9	°C/W
	Thermal resistance junction-case single diode	1.4	°C/W

Figure 3. Transient thermal impedance IGBT/diode - inverter



3 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{H-H} (V_{H-L}) = 15 V, V_{IN} (1) = 1 "logic state", I_C = 30 A	-	2.8	3.6	V
		V_{H-H} (V_{H-L}) = 15 V, V_{IN} (1) = 1 "logic state", I_C = 30 A, T_J = 125°C	-	2.4		
I_{CES}	Collector-cut off current (V_{IN} (1)= 0 “logic state”)	V_{CE} = 1200 V, V_{H-H} (V_{H-L}) = 15 V	-		10	mA
V_F	Diode forward voltage	V_{IN} (1) = 0 "logic state", I_F = 30 A	-		2.3	V
Switching on/off (inductive load) (2)						
t_{on}	Turn-on time	V_{DD} = 600 V, V_{H-H} (V_{H-L}) = 15 V, V_{IN} = 1 "logic state" (see *Table 9*) I_C = 30 A (see *Figure 4* and *5*)	-	720	-	ns
$t_{c(on)}$	Crossover time (on)		-	300	-	
t_{off}	Turn-off time		-	880	-	
$t_{c(off)}$	Crossover time (off)		-	275	-	
t_{rr}	Reverse recovery time		-	520	-	
E_{on}	Turn-on switching losses		-	3.7	-	mJ
E_{off}	Turn-off switching losses		-	1.9	-	
t_{on}	Turn-on time	V_{DD} = 600 V, V_{H-H} (V_{H-L}) = 15 V, V_{IN} = 1 "logic state" (see *Table 9*) I_C = 30 A, T_J = 125 °C (see *Figure 4* and *5*)	-	820	-	ns
$t_{c(on)}$	Crossover time (on)		-	350	-	
t_{off}	Turn-off time		-	1400	-	
$t_{c(off)}$	Crossover time (off)		-	700	-	
t_{rr}	Reverse recovery time		-	620	-	
E_{on}	Turn-on switching losses		-	5.6	-	mJ
E_{off}	Turn-off switching losses		-	5.8	-	

1. See *Table 9: Truth table*.
2. t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition. Parameter values take into account a 20 nH stray inductance.

Figure 4. Switching time test circuit

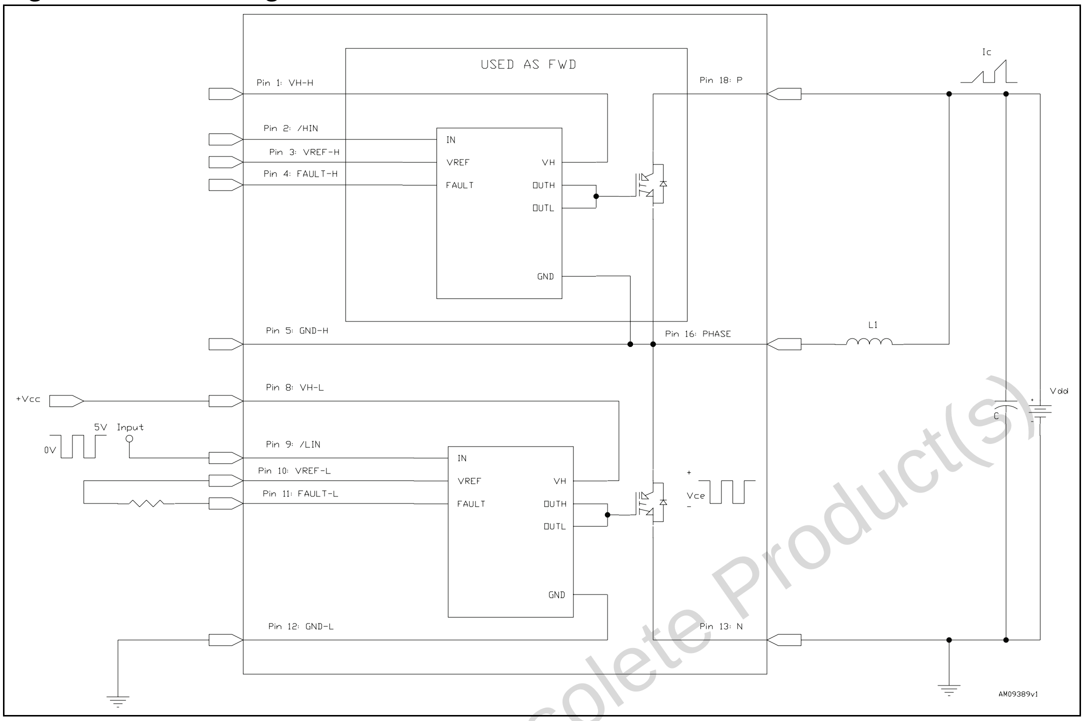
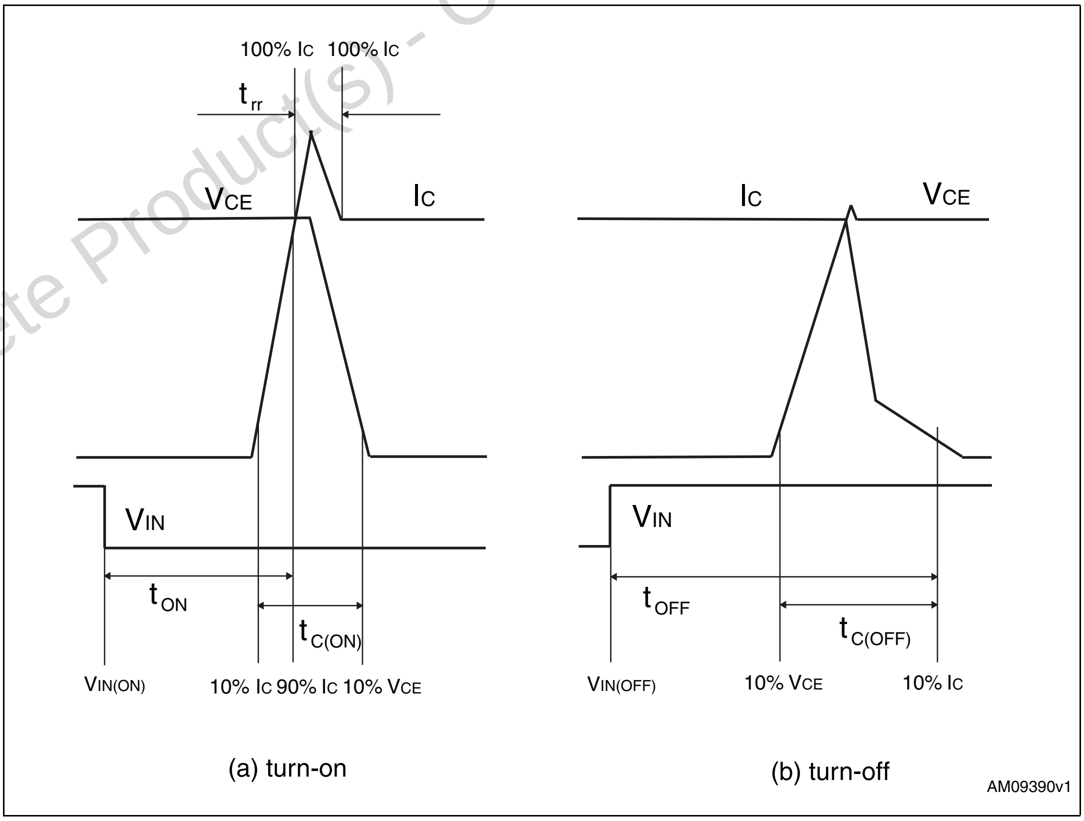


Figure 5. Switching time definition



3.1 Control part

T_A = - 20 to 125 °C, V_H = 16 V (unless otherwise specified).

Table 8. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Input						
V_{ton}	IN turn-on threshold voltage		0.8	1.0		V
V_{toff}	IN turn-off threshold voltage			4.0	4.2	V
t_{onmin}	Minimum pulse width		100	135	220	ns
I_{inp}	IN input current				1	µA
Voltage reference (1)						
V_{ref}	Voltage reference	$T_{min} < T < T_{max}$	4.77		5.22	V
I_{ref}	Maximum output current		10			mA
Fault output						
t_{fault}	Delay for fault detection				500	ns
V_{FL}	FAULT low voltage	I_{FLsink} = 10 mA			1	V
Under voltage lockout (UVLO)						
UVLOH	UVLO top threshold		10	11	12	V
UVLOL	UVLO bottom threshold		9	10	11	V
V_{hyst}	UVLO hysteresis	UVLOH-UVLOL	0.5	1		V
Supply current						
I_{in}	Quiescent current	Output = 0 V, no load			5	mA

1. Recommended capacitor range on VREF pin is 10 nF to 100 nF.

Table 9. Truth table

Condition	Logic input (V_I)		Output	
	$\overline{LIN}$	$\overline{HIN}$	Low side gate driver output	High side gate driver output
0 "logic state" half-bridge tri-state	H	H	L	L
1 "logic state" low side direct driving	L	H	H	L
1 "logic state" high side direct driving	H	L	L	H

Note: X: don't care

3.1.1 NTC thermistor

Table 10. NTC thermistor

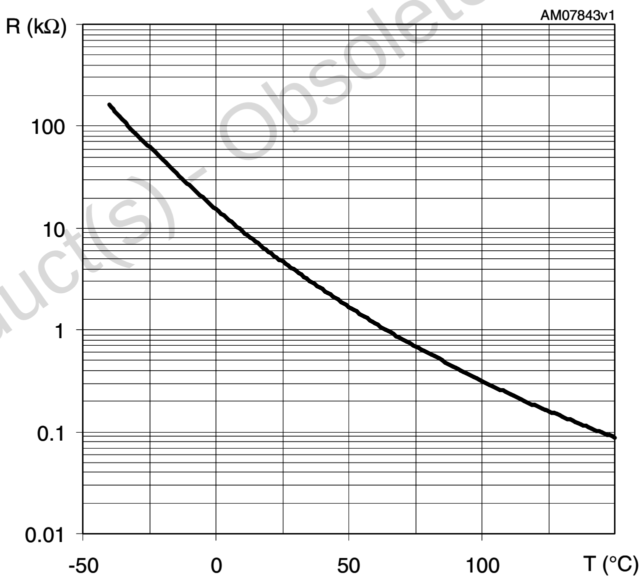
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
R_{25}	Resistance	T_C = 25°C		4.7		kΩ
R_{125}	Resistance	T_C = 125°C		160		Ω
B	B-constant	T_C = 25°C		3950		K
T	Operating temperature		-40		150	°C

Equation 1: resistance variation vs. temperature

$$R(T) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

Where T are temperatures in Kelvins

Figure 6. NTC resistance vs. temperature



3.2 Recommendations

- As the IPM may be used in a very noisy environment, care should be taken to decouple the supplies. Small ceramic capacitors, connected inside the IPM as close as possible to the gate driver pins, are used to improve noise-withstand capability.
- The IPM is compatible with both pulse transformers or optocouplers. When using an optocoupler, the IN input must be limited to approximately 5 V. The pull-up resistor to V_H must be between 5 kΩ and 20 kΩ, depending on optocoupler characteristics. An optional filtering capacitor can be added in the event of a highly noisy environment, although the IPM already includes a filtering on input signals and rejects signals smaller than 100 ns (t_{ONMIN} specification).
- When using a pulse transformer, a 2.5 V reference point can be built from the 5 V V_{REF} pin with a resistor divider. The capacitor between the V_{REF} pin and the resistor divider middle point provides decoupling of the 2.5 V reference, and also ensures a high level on the IN input pin at power-up to start the IPM in OFF state. The waveform from the pulse transformer must comply with the t_{ONMIN} and V_{tON} / V_{tOFF} specifications. To turn ON the IPM outputs, the input signal must be lower than 0.8 V for at least 220 ns. Conversely, the input signal must be higher than 4.2 V for at least 200 ns to turn OFF the outputs. A pulse width of about 500 ns at these threshold levels is recommended. In all cases, the input signal at the IN pin must be between 0 and 5 V.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- When setting the maximum voltage to be applied between P-N, the internal stray inductance and the maximum di/dt should be considered. Due to both internal and layout stray inductances, the di/dt results in a voltage surges between the DC-link capacitor and the switches during commutations.
- FAULT pin is externally available to provide a feedback signal about IPM status. Please refer to undervoltage protection and desaturation fault timing diagrams for more information. Fault output signals the undervoltage state and is reset only when undervoltage state disappears. When a desaturation event occurs, the fault output is pulled down and IPM outputs are low (IGBT off) until the IN input signal is released (high level), then activated again (low level).

4 Functional description

4.1 Input

The input is compatible with optocouplers or pulse transformers. The input is triggered by the signal edge and allows the use of low-sized, low-cost pulse transformer. Input is active low (output is high when input is low) to ease the use of optocoupler. When driven by a pulse transformer, the input pulse (positive and negative) width must be larger than the minimum pulse width t_{onmin}.

4.2 Voltage reference

A voltage reference is used to create accurate timing for the two-level turn-off with external resistor and capacitor.

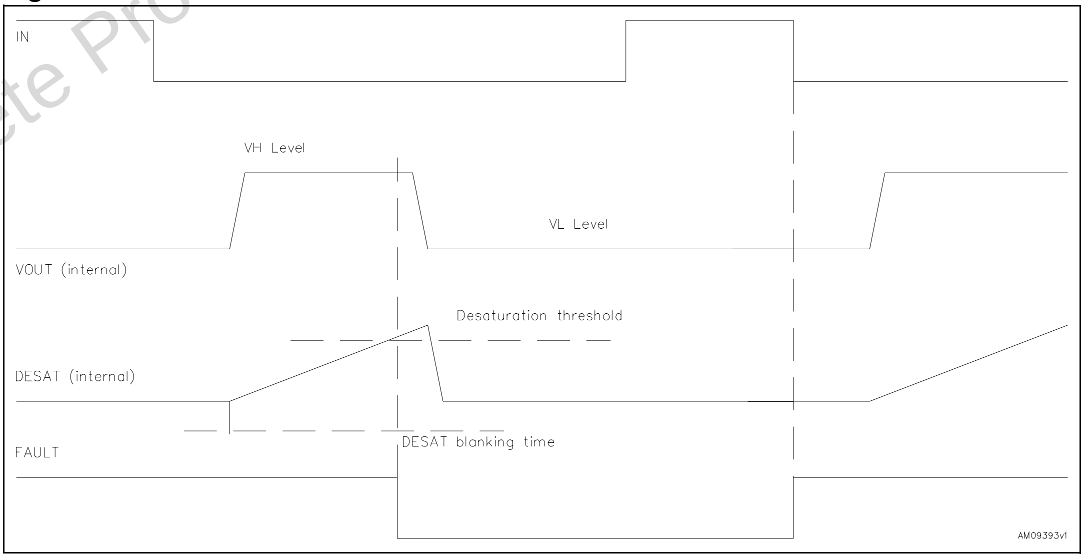
4.3 Desaturation protection

The desaturation function provides a protection against over-current events. Voltage across the IGBT is monitored, and the IGBT is turned off if the voltage threshold is reached. A blanking time is made of an internal current source and a capacitor.

During operation, the DESAT capacitor is discharged when IPM output is low (IGBT off). When the IGBT is turned on, the DESAT capacitor starts charging and desaturation protection is effective after the blanking time (fixed by design showing a typical value of 2 µs).

When a desaturation event occurs, the fault output is pulled down and IPM outputs are low (IGBT off) until the IN input signal is released (high level), then activated again (low level).

Figure 7. Desaturation 1200 V



4.4 Active Miller clamp

A Miller clamp allows the control of the Miller current during a high d_V/d_t situation and can avoid the use of a negative supply voltage.

During turn-off, the gate voltage is monitored and the clamp output is activated when gate voltage goes below 2 V (relative to GND). The clamp is disabled when the IN input is triggered again.

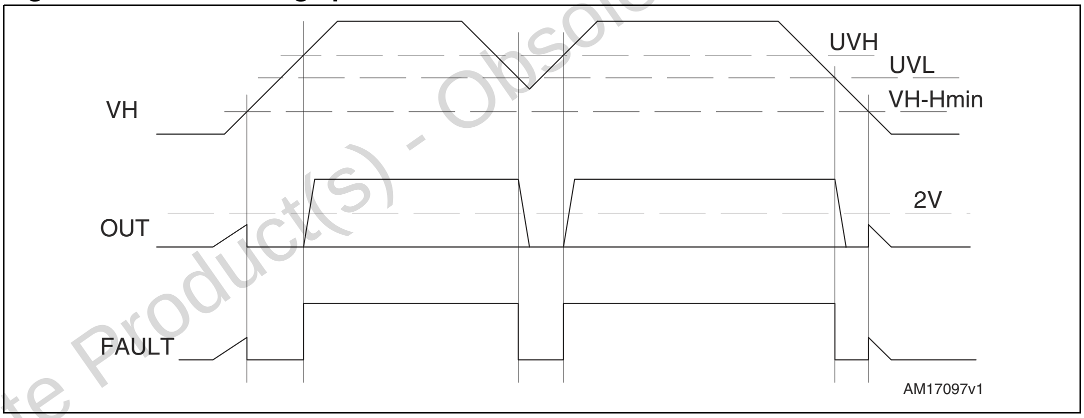
4.5 Fault status output

Fault output is used to signal a fault event (desaturation, UVLO) to a controller. The fault pin is designed to drive an optocoupler.

4.6 Undervoltage protection

Undervoltage detection protects the application in the event of a low VH supply voltage (during start-up or a fault situation). Fault output signals the undervoltage state and is reset only when undervoltage state disappears.

Figure 8. Undervoltage protection



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

Table 11. SDIP-18L package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	49.10	49.60	50.10
A1	1.10	1.30	1.50
A2	1.40	1.60	1.80
A3	44.10	44.60	45.10
B	24.00	24.50	25.00
B1	11.25	11.85	12.45
B2	27.10	27.60	28.10
C	5.00	5.40	6.00
C1	6.50	7.00	7.50
C2	10.35	10.85	11.35
e	2.40	2.60	2.80
e1	11.80	12.00	12.20
e2	7.10	7.30	7.50
e3	4.50	4.70	4.90
e4	5.80	6.00	6.20
e5	6.30	6.50	6.70
e6	10.40	10.60	10.80
e7	17.00	17.20	17.40
D		38.00	
D1		5.70	
E		11.80	
E1		2.15	
F	0.85	1.00	1.15
F1	0.35	0.50	0.65
R	1.55	1.75	1.95
T	0.45	0.55	0.65
V	0°		6°

Figure 9. SDIP-18L package drawing (dimensions are in mm.)

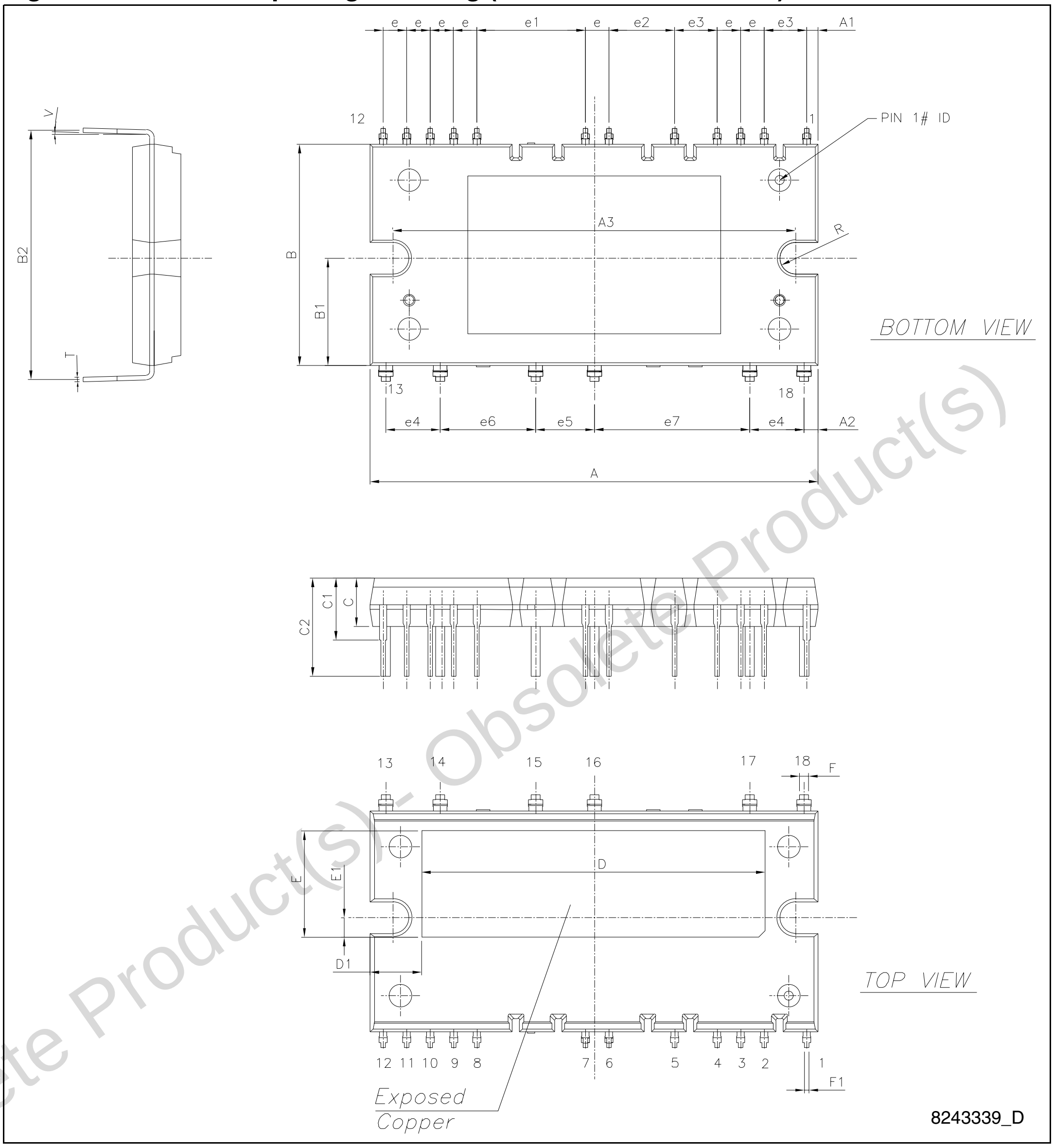


Figure 10. SDIP-18L shipping tube type A (dimensions are in mm.)

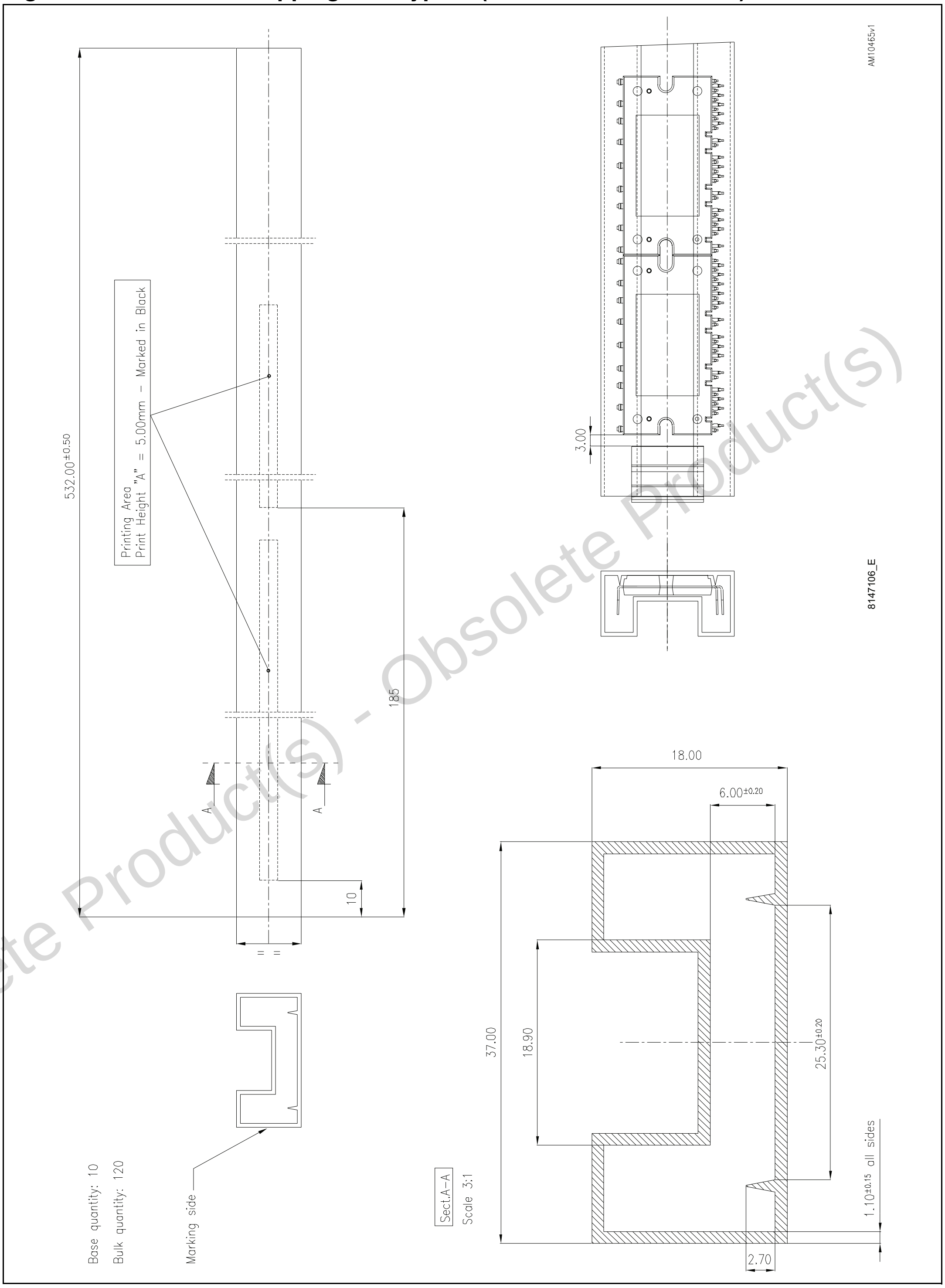
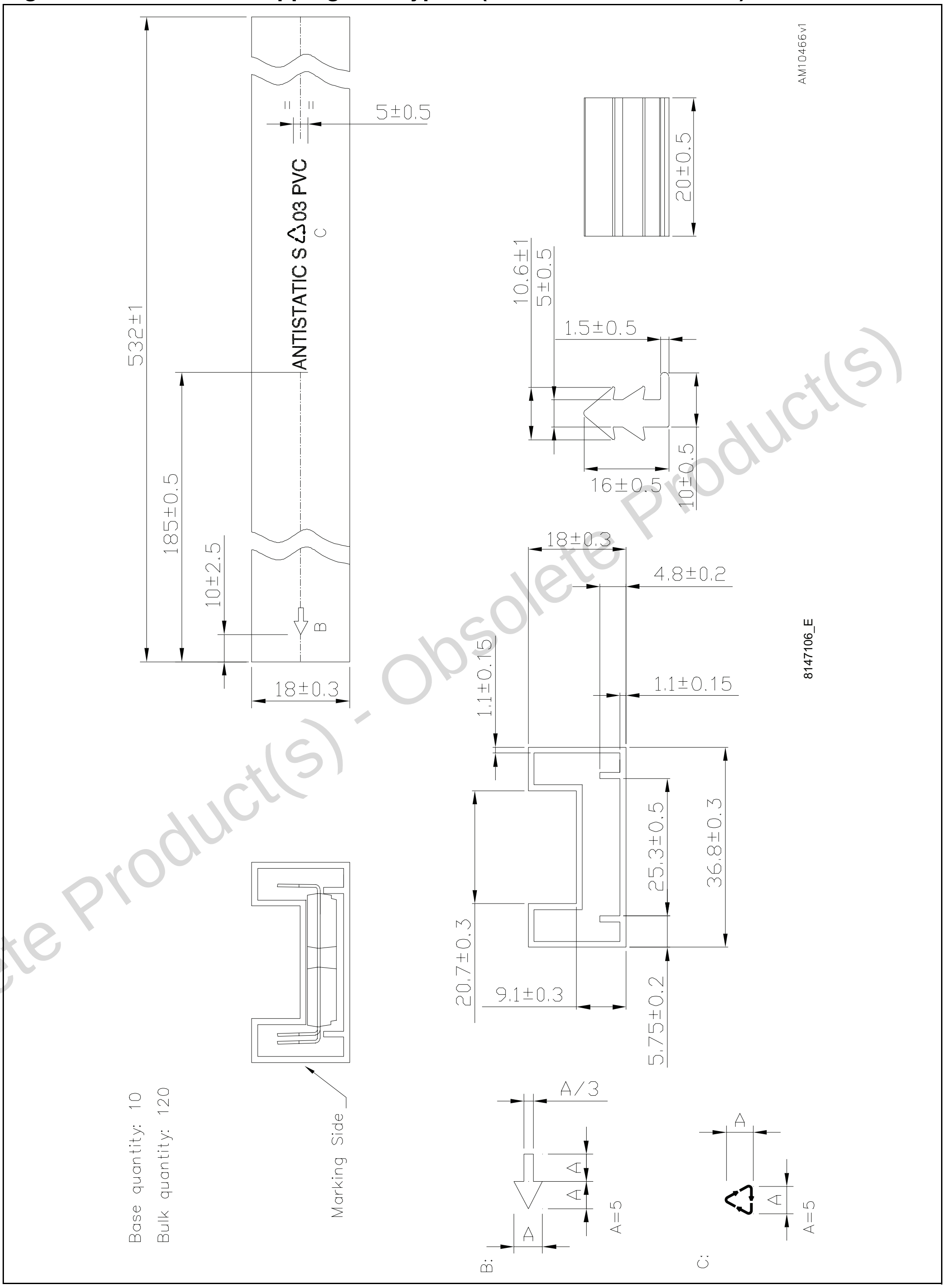


Figure 11. SDIP-18L shipping tube type B (dimensions are in mm.)



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
30-Jan-2012	1	Initial release.
28-Feb-2012	2	Added: $V_{CE(sat)}$ max. value *Table 7 on page 7*.
15-Oct-2012	3	Modified: V_F max. value 2.3 V *Table 7 on page 7*.
07-Feb-2013	4	Modified: t_{scw} parameter *Table 3 on page 5*. Updated: *Figure 8 on page 13*.

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