

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

Self-Supplied Monolithic Switcher for Low Standby- Power Offline SMPS

The NCP101X series integrates a fixed-frequency current-mode controller and a 700 V MOSFET. Housed in a PDIP-7 or SOT-223 package, the NCP101X offers everything needed to build a rugged and low-cost power supply, including soft-start, frequency jittering, short-circuit protection, skip-cycle, a maximum peak current setpoint and a Dynamic Self-Supply (no need for an auxiliary winding).

Unlike other monolithic solutions, the NCP101X is quiet by nature: during nominal load operation, the part switches at one of the available frequencies (65 – 100 – 130 kHz). When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so-called skip-cycle mode and provides excellent efficiency at light loads. Because this occurs at typically 1/4 of the maximum peak value, no acoustic noise takes place. As a result, standby power is reduced to the minimum without acoustic noise generation.

Short-circuit detection takes place when the feedback signal fades away, e.g. in true short-circuit conditions or in broken Optocoupler cases. External disabling is easily done either simply by pulling the feedback pin down or latching it to ground through an inexpensive SCR for complete latched-off. Finally soft-start and frequency jittering further ease the designer task to quickly develop low-cost and robust offline power supplies.

For improved standby performance, the connection of an auxiliary winding stops the DSS operation and helps to consume less than 100 mW at high line. In this mode, a built-in latched overvoltage protection prevents from lethal voltage runaways in case the Optocoupler would brake. These devices are available in economical 8-pin dual-in-line and 4-pin SOT-223 packages.

Features

- Built-in 700 V MOSFET with Typical $R_{DS(on)}$ of 11 Ω and 22 Ω
- Large Creepage Distance Between High-Voltage Pins
- Current-Mode Fixed Frequency Operation:
65 kHz – 100 kHz – 130 kHz
- Skip-Cycle Operation at Low Peak Currents Only:
No Acoustic Noise!
- Dynamic Self-Supply, No Need for an Auxiliary Winding
- Internal 1.0 ms Soft-Start
- Latched Overvoltage Protection with Auxiliary Winding Operation
- Frequency Jittering for Better EMI Signature

- Auto-Recovery Internal Output Short-Circuit Protection
- Below 100 mW Standby Power if Auxiliary Winding is Used
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient Analysis
- These are Pb-Free and Halide-Free Devices

Typical Applications

- Low Power AC/DC Adapters for Chargers
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)



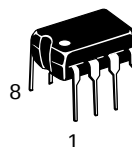
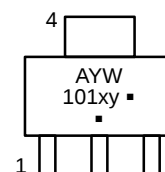
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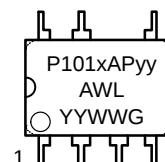
MARKING DIAGRAMS



**SOT-223
CASE 318E
ST SUFFIX**



**PDIP-7
CASE 626A
AP SUFFIX**



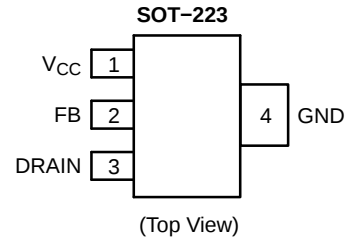
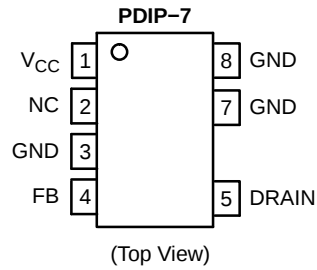
x = Current Limit (0, 1, 2, 3, 4)
y = Oscillator Frequency
A (65 kHz), B (100 kHz), C (130 kHz)
yy = 06 (65 kHz), 10 (100 kHz), 13 (130 kHz)
A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW, W = Work Week
▪ or G = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

PIN CONNECTIONS



Indicative Maximum Output Power from NCP1014

$R_{DSon} - I_p$	230 Vac	100 – 250 Vac
11 Ω – 450 mA DSS	14 W	6.0 W
11 Ω – 450 mA Auxiliary Winding	19 W	8.0 W

1. Informative values only, with: $T_{amb} = 50^\circ\text{C}$, $F_{switching} = 65\text{ kHz}$, circuit mounted on minimum copper area as recommended.

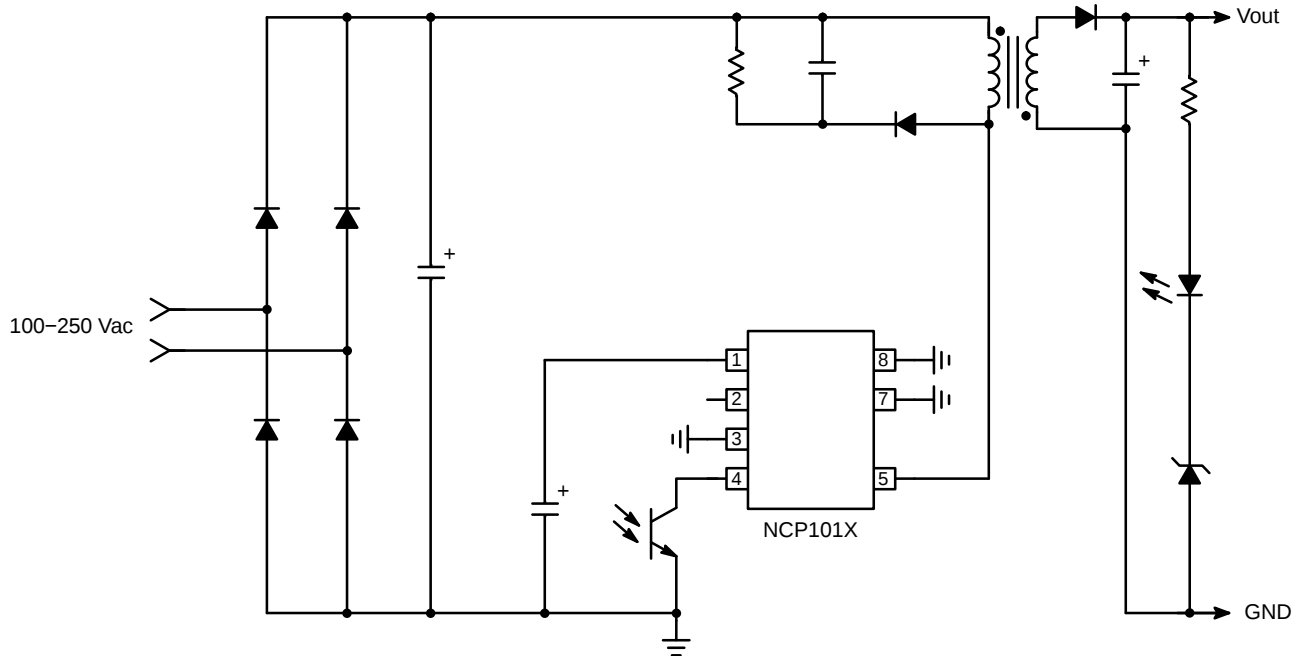


Figure 1. Typical Application Example

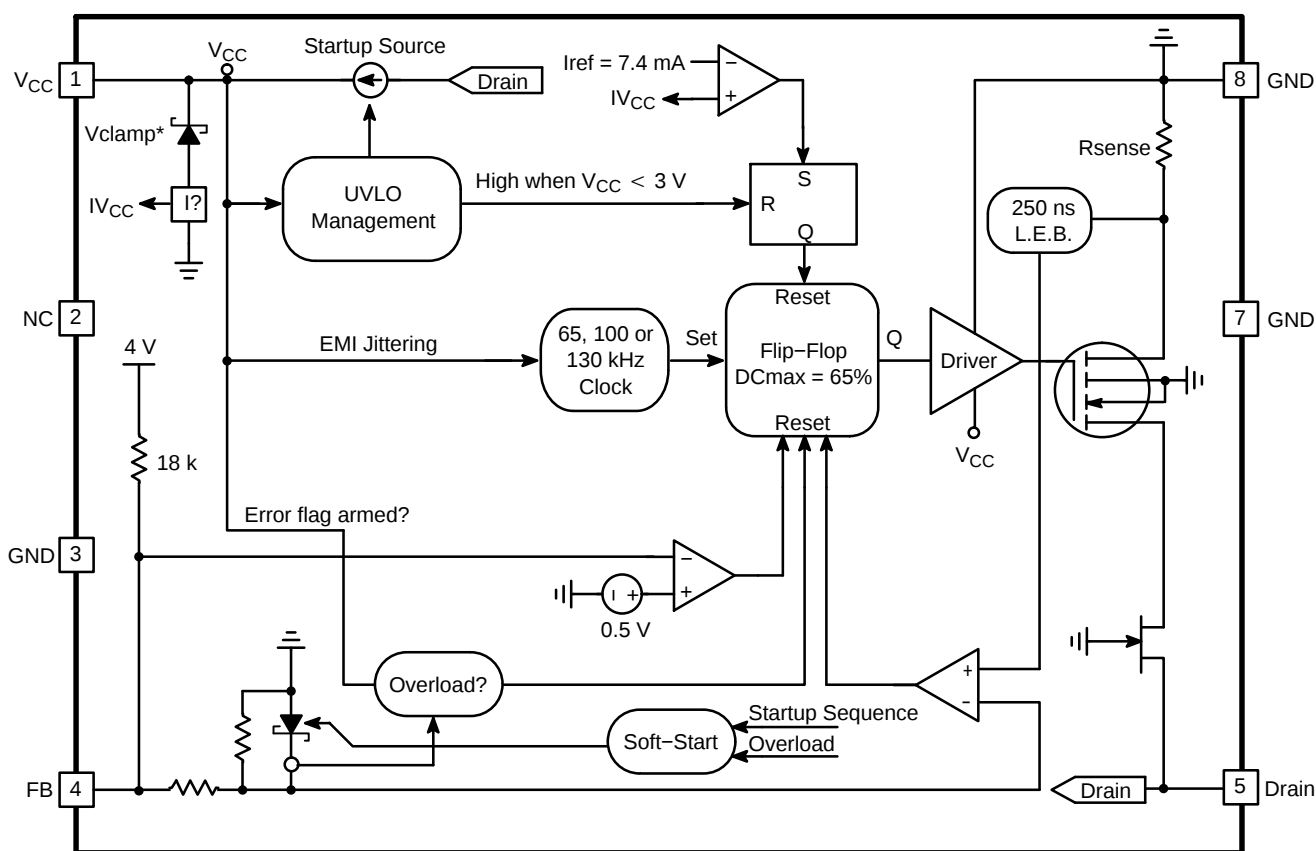
Quick Selection Table

	NCP1010			NCP1011			NCP1012			NCP1013			NCP1014	
R _{DSon} [Ω]	22						11							
I _{peak} [mA]	100			250			250			350			450	
Freq [kHz]	65	100	130	65	100	130	65	100	130	65	100	130	65	100

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

PIN FUNCTION DESCRIPTION

Pin No. (SOT-223)	Pin No. (PDIP-7)	Pin Name	Function	Description
1	1	V _{CC}	Powers the Internal Circuitry	This pin is connected to an external capacitor of typically 10 μ F. The natural ripple superimposed on the V _{CC} participates to the frequency jittering. For improved standby performance, an auxiliary V _{CC} can be connected to Pin 1. The V _{CC} also includes an active shunt which serves as an opto fail-safe protection.
–	2	NC	–	–
–	3	GND	The IC Ground	–
2	4	FB	Feedback Signal Input	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand.
3	5	Drain	Drain Connection	The internal drain MOSFET connection.
–	–	–	–	–
–	7	GND	The IC Ground	–
4	8	GND	The IC Ground	–



*Vclamp = VCC_{OFF} + 200 mV (8.7 V Typical)

Figure 2. Simplified Internal Circuit Architecture

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage on all pins, except Pin 5 (Drain)	V_{CC}	-0.3 to 10	V
Drain Voltage	–	-0.3 to 700	V
Drain Current Peak during Transformer Saturation NCP1010/11 NCP1012/13/14	$I_{DS(pk)}$	550 1.0	mA A
Maximum Current into Pin 1 when Activating the 8.7 V Active Clamp	$I_{V_{CC}}$	15	mA
Thermal Characteristics P Suffix, Case 626A Junction-to-Lead Junction-to-Air, 2.0 oz (70 μ m) Printed Circuit Copper Clad 0.36 Sq. Inch (2.32 Sq. Cm) 1.0 Sq. Inch (6.45 Sq. Cm) ST Suffix, Plastic Package Case 318E Junction-to-Lead Junction-to-Air, 2.0 oz (70 μ m) Printed Circuit Copper Clad 0.36 Sq. Inch (2.32 Sq. Cm) 1.0 Sq. Inch (6.45 Sq. Cm)	$R_{\theta JL}$ $R_{\theta JA}$ $R_{\theta JL}$ $R_{\theta JA}$	9.0 77 60 14 74 55	$^{\circ}$ C/W
Maximum Junction Temperature	T_{Jmax}	150	$^{\circ}$ C
Storage Temperature Range	–	-60 to +150	$^{\circ}$ C
ESD Capability, Human Body Model (All pins except HV)	–	2.0	kV
ESD Capability, Machine Model	–	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

ELECTRICAL CHARACTERISTICS (For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 8.0\text{ V}$ unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
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SUPPLY SECTION AND V_{CC} MANAGEMENT

V_{CC} Increasing Level at which the Current Source Turns-off	1	$V_{CC\text{OFF}}$	7.9	8.5	9.1	V
V_{CC} Decreasing Level at which the Current Source Turns-on	1	$V_{CC\text{ON}}$	6.9	7.5	8.1	V
Hysteresis between $V_{CC\text{OFF}}$ and $V_{CC\text{ON}}$	1	–	–	1.0	–	V
V_{CC} Decreasing Level at which the Latch-off Phase Ends	1	$V_{CC\text{latch}}$	4.4	4.7	5.1	V
V_{CC} Decreasing Level at which the Internal Latch is Released	1	$V_{CC\text{reset}}$	–	3.0	–	V
Internal IC Consumption, MOSFET Switching at 65 kHz (Note 2)	1	ICC1	–	0.92	1.1	mA
Internal IC Consumption, MOSFET Switching at 100 kHz (Note 2)	1	ICC1	–	0.95	1.15	mA
Internal IC Consumption, MOSFET Switching at 130 kHz (Note 2)	1	ICC1	–	0.98	1.2	mA
Internal IC Consumption, Latch-off Phase, $V_{CC} = 6.0\text{ V}$	1	ICC2	–	290	–	μA
Active Zener Voltage Positive Offset to $V_{CC\text{OFF}}$	1	V_{clamp}	140	200	300	mV
Latch-off Current	1	I_{Latch}				mA
NCP1012/13/14 $0^\circ\text{C} < T_J < 125^\circ\text{C}$			6.3	7.4	9.2	
$-40^\circ\text{C} < T_J < 125^\circ\text{C}$			5.8	7.4	9.2	
NCP1010/11 $0^\circ\text{C} < T_J < 125^\circ\text{C}$			5.8	7.3	9.0	
$-40^\circ\text{C} < T_J < 125^\circ\text{C}$			5.3	7.3	9.0	

POWER SWITCH CIRCUIT

Power Switch Circuit On-state Resistance NCP1012/13/14 ($I_d = 50\text{ mA}$) $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ NCP1010/11 ($I_d = 50\text{ mA}$) $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	5	R_{DSon}	–			Ω
				11 19	16 24	
				22 38	35 50	
Power Switch Circuit and Startup Breakdown Voltage ($I_{D(\text{off})} = 120\text{ }\mu\text{A}$, $T_J = 25^\circ\text{C}$)	5	BV_{dss}	700	–	–	V
Power Switch and Startup Breakdown Voltage Off-state Leakage Current $T_J = -40^\circ\text{C}$ ($V_{\text{ds}} = 650\text{ V}$) $T_J = 25^\circ\text{C}$ ($V_{\text{ds}} = 700\text{ V}$) $T_J = 125^\circ\text{C}$ ($V_{\text{ds}} = 700\text{ V}$)	5 5 5	$I_{\text{DS(OFF)}}$	– – –	70 50 30	120 – –	μA
Switching Characteristics ($R_L = 50\text{ }\Omega$, V_{ds} Set for $I_{\text{drain}} = 0.7 \times I_{\text{lim}}$) Turn-on Time (90%–10%) Turn-off Time (10%–90%)	5 5	t_{on} t_{off}	– –	20 10	– –	ns

INTERNAL STARTUP CURRENT SOURCE

High-voltage Current Source, $V_{CC} = 8.0\text{ V}$ NCP1012/13/14 $0^\circ\text{C} < T_J < 125^\circ\text{C}$ $-40^\circ\text{C} < T_J < 125^\circ\text{C}$ NCP1010/11 $0^\circ\text{C} < T_J < 125^\circ\text{C}$ $-40^\circ\text{C} < T_J < 125^\circ\text{C}$	1	IC1	5.0 5.0 5.0 5.0	8.0 8.0 8.0 8.0	10 11 10.3 11.5	mA
High-voltage Current Source, $V_{CC} = 0$	1	IC2	–	10	–	mA

CURRENT COMPARATOR $T_J = 25^\circ\text{C}$ (Note 2)

Maximum Internal Current Setpoint, NCP1010 (Note 3)	5	$I_{\text{peak}} (22)$	90	100	110	mA
Maximum Internal Current Setpoint, NCP1011 (Note 3)	5	$I_{\text{peak}} (22)$	225	250	275	mA
Maximum Internal Current Setpoint, NCP1012 (Note 3)	5	$I_{\text{peak}} (11)$	225	250	275	mA
Maximum Internal Current Setpoint, NCP1013 (Note 3)	5	$I_{\text{peak}} (11)$	315	350	385	mA
Maximum Internal Current Setpoint, NCP1014 (Note 3)	5	$I_{\text{peak}} (11)$	405	450	495	mA
Default Internal Current Setpoint for Skip-Cycle Operation, Percentage of Max I_p	–	I_{Lskip}	–	25	–	%
Propagation Delay from Current Detection to Drain OFF State	–	T_{DEL}	–	125	–	ns
Leading Edge Blanking Duration	–	T_{LEB}	–	250	–	ns

- See characterization curves for temperature evolution.
- Adjust di/dt to reach I_{peak} in $3.2\text{ }\mu\text{sec}$.

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

ELECTRICAL CHARACTERISTICS (continued) (For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 8.0\text{ V}$ unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
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INTERNAL OSCILLATOR

Oscillation Frequency, 65 kHz Version, $T_J = 25^\circ\text{C}$ (Note 4)	–	f_{OSC}	59	65	71	kHz
Oscillation Frequency, 100 kHz Version, $T_J = 25^\circ\text{C}$ (Note 4)	–	f_{OSC}	90	100	110	kHz
Oscillation Frequency, 130 kHz Version, $T_J = 25^\circ\text{C}$ (Note 4)	–	f_{OSC}	117	130	143	kHz
Frequency Dithering Compared to Switching Frequency (with active DSS)	–	f_{dither}	–	± 3.3	–	%
Maximum Duty-cycle	–	Dmax	62	67	72	%

FEEDBACK SECTION

Internal Pull-up Resistor	4	Rup	–	18	–	k Ω
Internal Soft-Start (Guaranteed by Design)	–	Tss	–	1.0	–	ms

SKIP-CYCLE GENERATION

Default Skip Mode Level on FB Pin	4	Vskip	–	0.5	–	V
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TEMPERATURE MANAGEMENT

Temperature Shutdown	–	TSD	140	150	160	$^\circ\text{C}$
Hysteresis in Shutdown	–	–	–	50	–	$^\circ\text{C}$

4. See characterization curves for temperature evolution.

TYPICAL CHARACTERISTICS

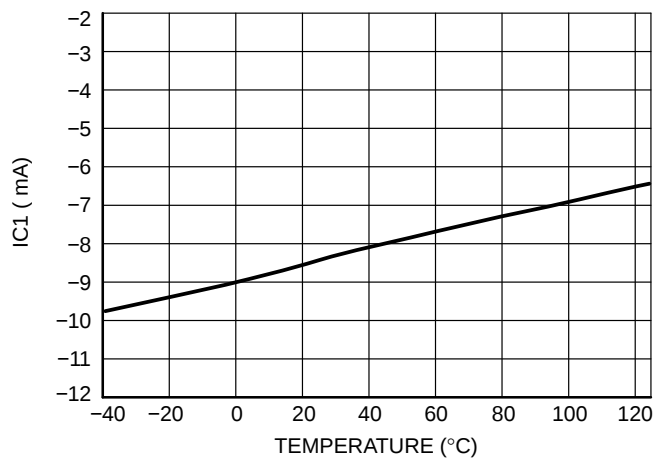


Figure 3. IC1 @ $V_{CC} = 8.0\text{ V}$, FB = 1.5 V vs. Temperature

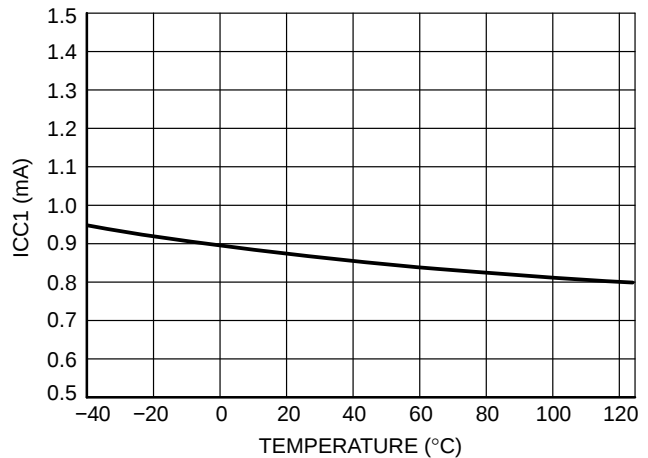


Figure 4. ICC1 @ $V_{CC} = 8.0\text{ V}$, FB = 1.5 V vs. Temperature

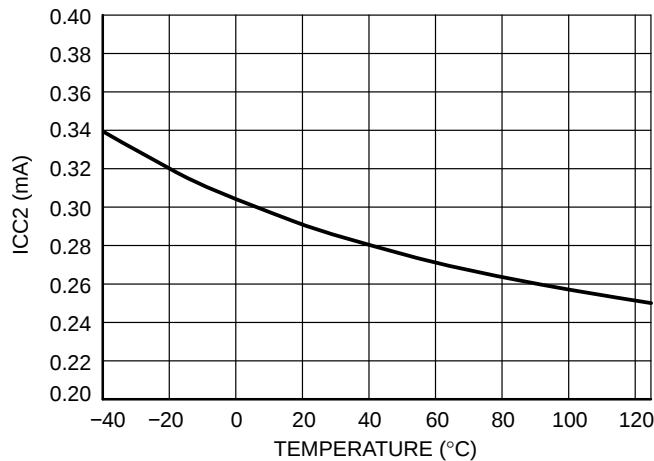


Figure 5. ICC2 @ $V_{CC} = 6.0\text{ V}$, FB = Open vs. Temperature

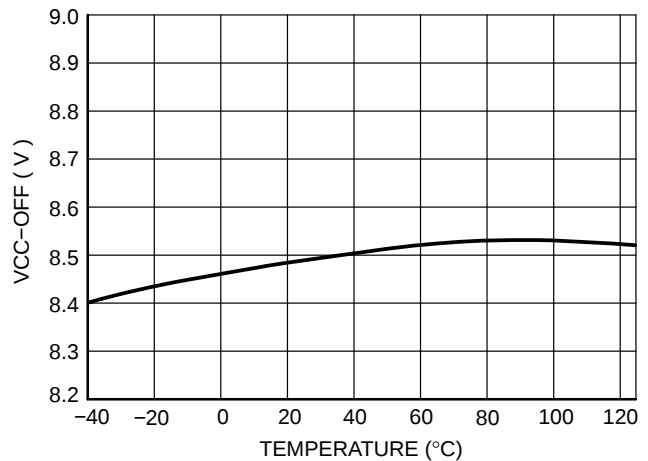


Figure 6. V_{CC} OFF, FB = 1.5 V vs. Temperature

TYPICAL CHARACTERISTICS

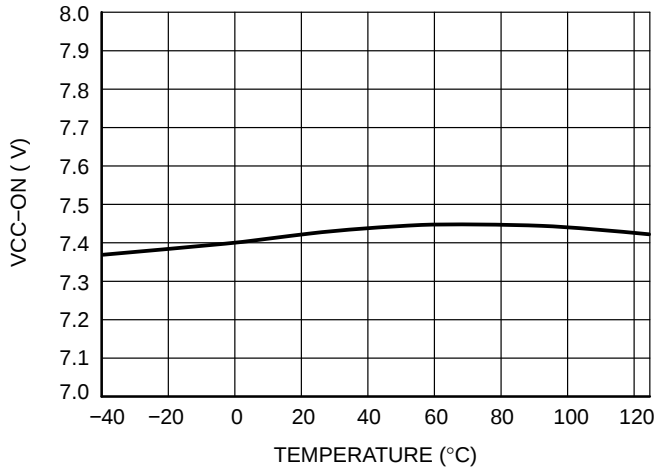


Figure 7. V_{CC} ON, FB = 3.5 V vs. Temperature

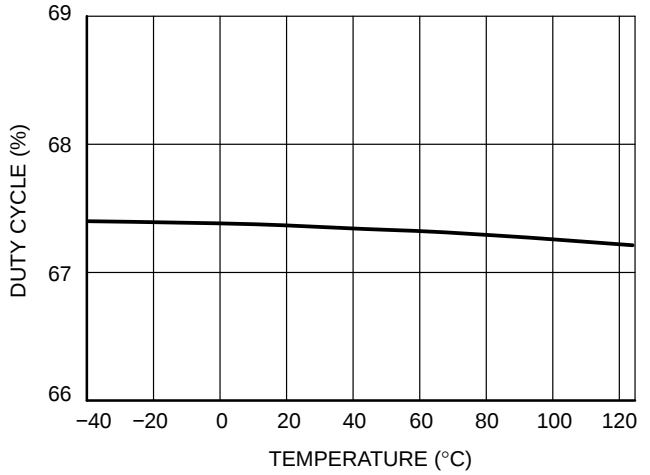


Figure 8. Duty Cycle vs. Temperature

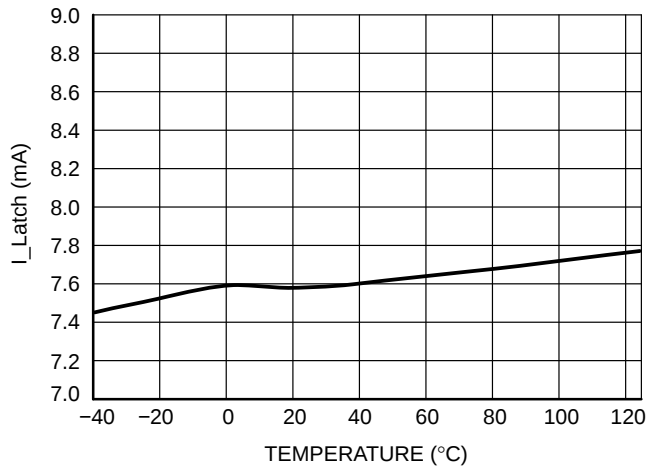


Figure 9. I_{Latch} , FB = 1.5 V vs. Temperature

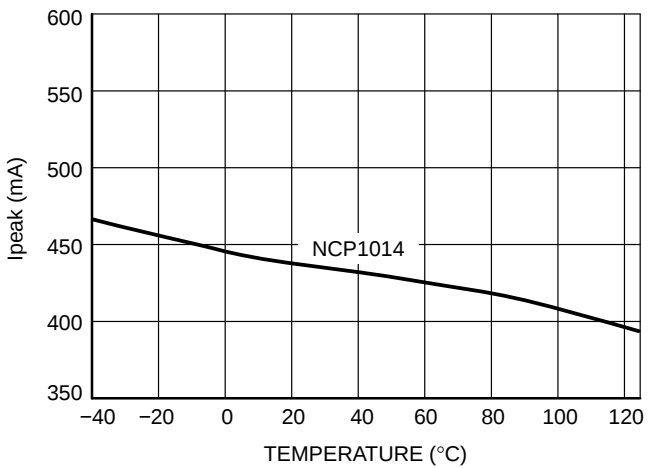


Figure 10. $I_{peak-RR}$, $V_{CC} = 8.0$ V, FB = 3.5 V vs. Temperature

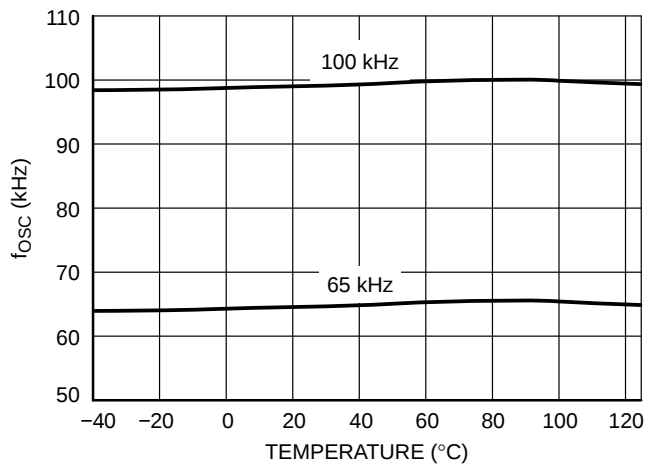


Figure 11. Frequency vs. Temperature

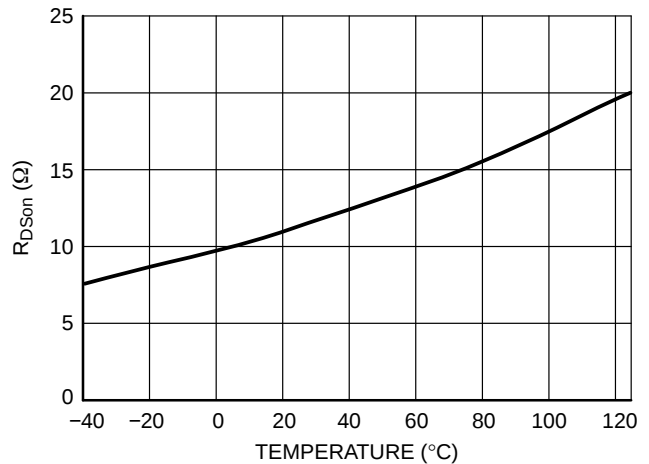


Figure 12. ON Resistance vs. Temperature, NCP1012/1013

APPLICATION INFORMATION

Introduction

The NCP101X offers a complete current-mode control solution (actually an enhanced NCP1200 controller section) together with a high-voltage power MOSFET in a monolithic structure. The component integrates everything needed to build a rugged and low-cost Switch-Mode Power Supply (SMPS) featuring low standby power. The Quick Selection Table on Page 2, details the differences between references, mainly peak current setpoints and operating frequency.

No need for an auxiliary winding: ON Semiconductor Very High Voltage Integrated Circuit technology lets you supply the IC directly from the high-voltage DC rail. We call it Dynamic Self-Supply (DSS). This solution simplifies the transformer design and ensures a better control of the SMPS in difficult output conditions, e.g. constant current operations. However, for improved standby performance, an auxiliary winding can be connected to the V_{CC} pin to disable the DSS operation.

Short-circuit protection: By permanently monitoring the feedback line activity, the IC is able to detect the presence of a short-circuit, immediately reducing the output power for a total system protection. Once the short has disappeared, the controller resumes and goes back to normal operation.

Fail-safe optocoupler and OVP: When an auxiliary winding is connected to the V_{CC} pin, the device stops its internal Dynamic Self-Supply and takes its operating power from the auxiliary winding. A 8.7 V active clamp is connected between V_{CC} and ground. In case the current injected in this clamp exceeds a level of 7.4 mA (typical), the controller immediately latches off and stays in this position until V_{CC} cycles down to 3.0 V (e.g. unplugging the converter from the wall). By adjusting a limiting resistor in series with the V_{CC} terminal, it becomes possible to implement an overvoltage protection function, latching off the circuit in case of broken optocoupler or feedback loop problems.

Low standby-power: If SMPS naturally exhibits a good efficiency at nominal load, it begins to be less efficient when the output power demand diminishes. By skipping unneeded switching cycles, the NCP101X drastically reduces the power wasted during light load conditions. An auxiliary winding can further help decreasing the standby power to extremely low levels by invalidating the DSS operation. Typical measurements show results below 80 mW @ 230 Vac for a typical 7.0 W universal power supply.

No acoustic noise while operating: Instead of skipping cycles at high peak currents, the NCP101X waits until the peak current demand falls below a fixed 1/4 of the maximum limit. As a result, cycle skipping can take place without having a singing transformer ... You can thus select cheap magnetic components free of noise problems.

SPICE model: A dedicated model to run transient cycle-by-cycle simulations is available but also an averaged version to help close the loop. Ready-to-use templates can be downloaded in OrCAD's PSpice, and INTUSOFT's IsSpice4 from ON Semiconductor web site, NCP101X related section.

Dynamic Self-Supply

When the power supply is first powered from the mains outlet, the internal current source (typically 8.0 mA) is biased and charges up the V_{CC} capacitor from the drain pin. Once the voltage on this V_{CC} capacitor reaches the V_{CCOFF} level (typically 8.5 V), the current source turns off and pulses are delivered by the output stage: the circuit is awake and activates the power MOSFET. Figure 13 details the internal circuitry.

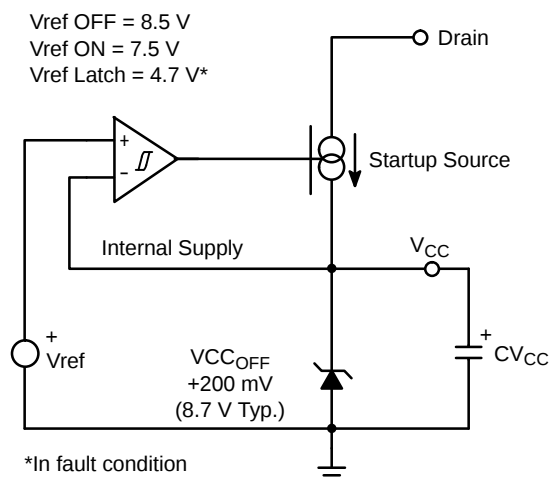


Figure 13. The Current Source Regulates V_{CC} by Introducing a Ripple

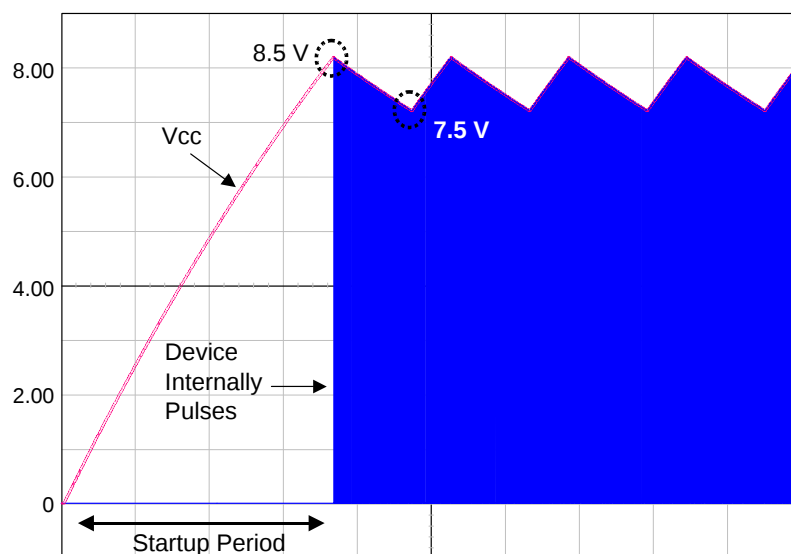


Figure 14. The Charge/Discharge Cycle Over a 10 µF V_{CC} Capacitor

The protection burst duty-cycle can easily be computed through the various timing events as portrayed by Figure 16.

Being loaded by the circuit consumption, the voltage on the V_{CC} capacitor goes down. When the DSS controller detects that V_{CC} has reached 7.5 V (V_{CCON}), it activates the internal current source to bring V_{CC} toward 8.5 V and stops again: a cycle takes place whose low frequency depends on the V_{CC} capacitor and the IC consumption. A 1.0 V ripple takes place on the V_{CC} pin whose average value equals (V_{CCOFF} + V_{CCON})/2. Figure 14 portrays a typical operation of the DSS.

As one can see, the V_{CC} capacitor shall be dimensioned to offer an adequate startup time, i.e. ensure regulation is reached before V_{CC} crosses 7.5 V (otherwise the part enters the fault condition mode). If we know that $\Delta V = 1.0$ V and ICC1 (max) is 1.1 mA (for instance we selected an 11 Ω device switching at 65 kHz), then the V_{CC} capacitor can be calculated using: $C \geq \frac{ICC1 \cdot t_{startup}}{\Delta V}$ (eq. 1). Let's suppose that the SMPS needs 10 ms to startup, then we will calculate C to offer a 15 ms period. As a result, C should be greater than 20 µF thus the selection of a 33 µF/16 V capacitor is appropriate.

Short Circuit Protection

The internal protection circuitry involves a patented arrangement that permanently monitors the assertion of an internal error flag. This error flag is, in fact, a signal that instructs the controller that the internal maximum peak current limit is reached. This naturally occurs during the startup period (V_{out} is not stabilized to the target value) or when the optocoupler LED is no longer biased, e.g. in a short-circuit condition or when the feedback network is broken. When the DSS normally operates, the logic checks

for the presence of the error flag every time V_{CC} crosses V_{CCON}. If the error flag is low (peak limit not active) then the IC works normally. If the error signal is active, then the NCP101X immediately stops the output pulses, reduces its internal current consumption and does not allow the startup source to activate: V_{CC} drops toward ground until it reaches the so-called latch-off level, where the current source activates again to attempt a new restart. When the error is gone, the IC automatically resumes its operation. If the default is still there, the IC pulses during 8.5 V down to 7.5 V and enters a new latch-off phase. The resulting burst operation guarantees a low average power dissipation and lets the SMPS sustain a permanent short-circuit. Figure 15 shows the corresponding diagram.

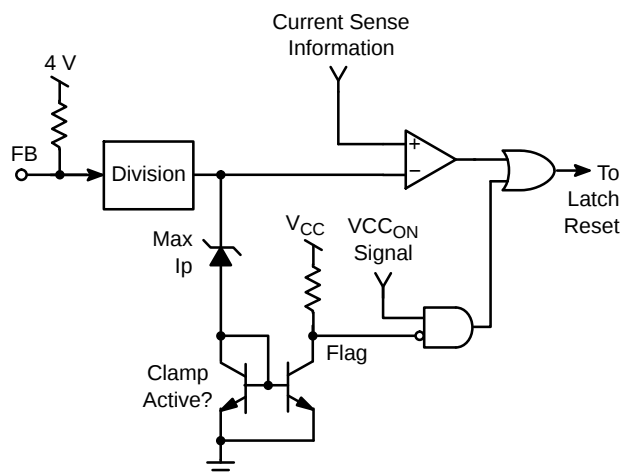


Figure 15. Simplified NCP101X Short-Circuit Detection Circuitry

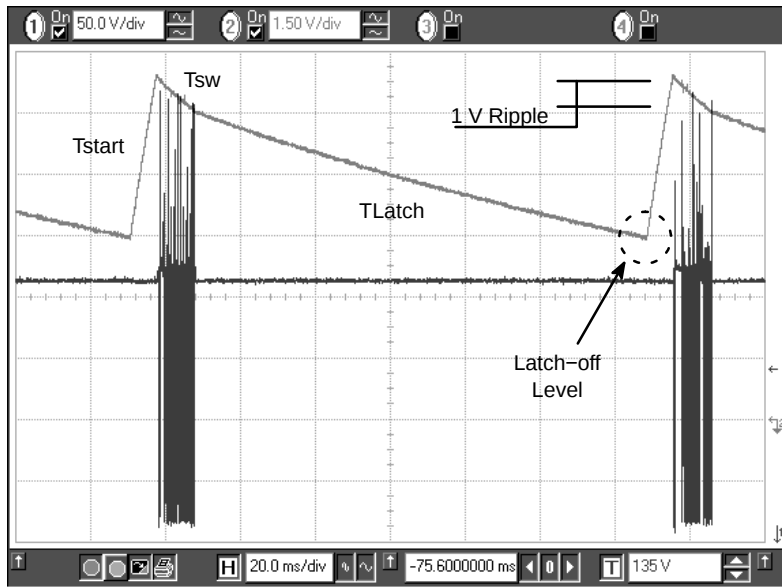


Figure 16. NCP101X Facing a Fault Condition (Vin = 150 Vdc)

The rising slope from the latch-off level up to 8.5 V is expressed by: $T_{start} = \frac{\Delta V1 \cdot C}{ICC1}$. The time during which the IC actually pulses is given by $t_{sw} = \frac{\Delta V2 \cdot C}{ICC1}$. Finally, the latch-off time can be derived using the same formula topology: $T_{Latch} = \frac{\Delta V3 \cdot C}{ICC2}$. From these three definitions, the burst duty-cycle can be computed: $dc = \frac{T_{sw}}{T_{start} + T_{sw} + T_{Latch}}$ (eq. 2). $dc = \frac{\Delta V2}{ICC1 \cdot \left(\frac{\Delta V2}{ICC1} + \frac{\Delta V1}{ICC1} + \frac{\Delta V3}{ICC2} \right)}$ (eq. 3). Feeding the equation with values extracted from the parameter section gives a typical duty-cycle of 13%, precluding any lethal thermal runaway while in a fault condition.

DSS Internal Dissipation

The Dynamic Self-Supplied pulls energy out from the drain pin. In Flyback-based converters, this drain level can easily go above 600 V peak and thus increase the stress on the DSS startup source. However, the drain voltage evolves with time and its period is small compared to that of the DSS. As a result, the averaged dissipation, excluding capacitive losses, can be derived by: $P_{DSS} = ICC1 \cdot \langle V_{ds}(t) \rangle$. (eq. 4). Figure 17 portrays a typical drain-ground waveshape where leakage effects have been removed.

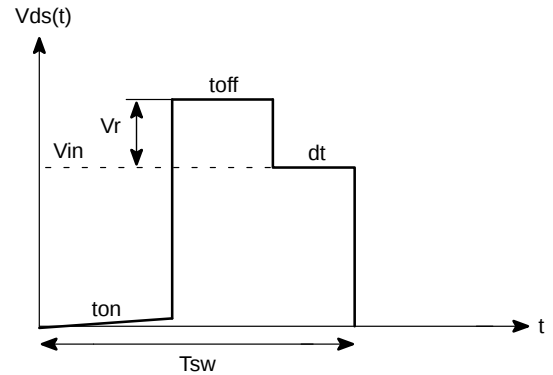


Figure 17. A typical drain-ground waveshape where leakage effects are not accounted for.

By looking at Figure 17, the average result can easily be derived by additive square area calculation:

$$\langle V_{ds}(t) \rangle = V_{in} \cdot (1 - d) + V_r \cdot \frac{t_{off}}{T_{sw}} \quad (\text{eq. 5})$$

By developing Equation 5, we obtain:

$$\langle V_{ds}(t) \rangle = V_{in} - V_{in} \cdot \frac{t_{on}}{T_{sw}} + V_r \cdot \frac{t_{off}}{T_{sw}} \quad (\text{eq. 6})$$

t_{off} can be expressed by: $t_{off} = I_p \cdot \frac{L_p}{V_r}$ (eq. 7) where t_{on}

can be evaluated by: $t_{on} = I_p \cdot \frac{L_p}{V_{in}}$ (eq. 8).

Plugging Equations 7 and 8 into Equation 6 leads to $V_{DS}(t) > V_{in}$ and thus, $P_{DSS} = V_{in} \times ICC1$ (eq. 9).

The worse case occurs at high line, when V_{in} equals 370 Vdc. With $ICC1 = 1.1$ mA (65 kHz version), we can expect a DSS dissipation around 407 mW. If you select a higher switching frequency version, the $ICC1$ increases and it is likely that the DSS consumption exceeds that number. In that case, we recommend to add an auxiliary winding in order to offer more dissipation room to the power MOSFET.

Please read application note AND8125/D, "Evaluating the Power Capability of the NCP101X Members" to help in selecting the right part/configuration for your application.

Lowering the Standby Power with an Auxiliary Winding

The DSS operation can bother the designer when its dissipation is too high and extremely low standby power is a must. In both cases, one can connect an auxiliary winding to disable the self-supply. The current source then ensures the startup sequence only and stays in the off state as long as V_{CC} does not drop below V_{CCON} or 7.5 V. Figure 18 shows that the insertion of a resistor (R_{limit}) between the auxiliary DC level and the V_{CC} pin is mandatory to not damage the internal 8.7 V active Zener diode during an overshoot for instance (absolute maximum current is 15 mA) and to implement the fail-safe optocoupler protection as offered by the active clamp. Please note that there cannot be bad interaction between the clamping voltage of the internal Zener and V_{CCOFF} since this clamping voltage is actually built on top of V_{CCOFF} with a fixed amount of offset (200 mV typical).

Self-supplying controllers in extremely low standby applications often puzzles the designer. Actually, if a SMPS operated at nominal load can deliver an auxiliary voltage of an arbitrary 16 V (V_{nom}), this voltage can drop to below 10 V (V_{stby}) when entering standby. This is because the recurrence of the switching pulses expands so much that the low frequency refueling rate of the V_{CC} capacitor is not enough to keep a constant auxiliary voltage. Figure 19 portrays a typical scope shot of a SMPS entering deep standby (output unloaded). So care must be taken when calculating R_{limit} 1) to not trigger the V_{CC} over current latch [by injecting 6.3 mA (min. value) into the active clamp] in normal operation but 2) not to drop too much voltage over R_{limit} when entering standby. Otherwise the DSS could reactivate and the standby performance would degrade. We are thus able to bound R_{limit} between two equations:

$$\frac{V_{nom} - V_{clamp}}{I_{trip}} \leq R_{limit} \leq \frac{V_{stby} - V_{CCON}}{ICC1} \quad (\text{eq. 10})$$

Where:

V_{nom} is the auxiliary voltage at nominal load.

V_{stby} is the auxiliary voltage when standby is entered.

I_{trip} is the current corresponding to the nominal operation. It must be selected to avoid false tripping in overshoot conditions.

$ICC1$ is the controller consumption. This number slightly decreases compared to $ICC1$ from the spec since the part in standby almost does not switch.

V_{CCON} is the level above which V_{aux} must be maintained to keep the DSS in the OFF mode. It is good to shoot around 8.0 V in order to offer an adequate design margin, e.g. to not reactivate the startup source (which is not a problem in itself if low standby power does not matter).

Since R_{limit} shall not bother the controller in standby, e.g. keep V_{aux} to around 8.0 V (as selected above), we purposely select a V_{nom} well above this value. As explained before, experience shows that a 40% decrease can be seen on auxiliary windings from nominal operation down to standby mode. Let's select a nominal auxiliary winding of 20 V to offer sufficient margin regarding 8.0 V when in standby (R_{limit} also drops voltage in standby...). Plugging the values in Equation 10 gives the limits within which R_{limit} shall be selected:

$$\frac{20 - 8.7}{6.3 \text{ m}} \leq R_{limit} \leq \frac{12 - 8}{1.1 \text{ m}}, \text{ that is to say:} \quad (\text{eq. 11})$$

$$1.8 \text{ k} < R_{limit} < 3.6 \text{ k}$$

If we design a power supply delivering 12 V, then the ratio between auxiliary and power must be: $12/20 = 0.6$. The OVP latch will activate when the clamp current exceeds 6.3 mA. This will occur when V_{aux} increases to: $8.7 \text{ V} + 1.8 \text{ k} \times (6.4 \text{ m} + 1.1 \text{ m}) = 22.2 \text{ V}$ for the first boundary or $8.7 \text{ V} + 3.6 \text{ k} \times (6.4 \text{ m} + 1.1 \text{ m}) = 35.7 \text{ V}$ for second boundary. On the power output, it will respectively give $22.2 \times 0.6 = 13.3 \text{ V}$ and $35.7 \times 0.6 = 21.4 \text{ V}$. As one can see, tweaking the R_{limit} value will allow the selection of a given overvoltage output level. Theoretically predicting the auxiliary drop from nominal to standby is an almost impossible exercise since many parameters are involved, including the converter time constants. Fine tuning of R_{limit} thus requires a few iterations and experiments on a breadboard to check V_{aux} variations but also output voltage excursion in fault. Once properly adjusted, the fail-safe protection will preclude any lethal voltage runaways in case a problem would occur in the feedback loop.

When an OVP occurs, all switching pulses are permanently disabled, the output voltage thus drops to zero. The V_{CC} cycles up and down between 8.5–4.7 V and stays in this state until the user unplugs the power supply and forces V_{CC} to drop below 3.0 V ($V_{CCreset}$). Below this value, the internal OVP latch is reset and when the high voltage is reapplied, a new startup sequence can take place in an attempt to restart the converter.

The schematic diagram illustrates a latch circuit with a startup source and a permanent latch. The circuit is powered by $V_{CC_ON} = 8.5\text{ V}$ and $V_{CC_OFF} = 7.5\text{ V}$. The startup source is connected to the V_{CC} node through a resistor R_{limit} . The V_{CC} node is also connected to a diode $D1$ and a capacitor C_{Vcc} . The diode $D1$ is connected to a capacitor C_{aux} and an inductor L_{aux} . The inductor L_{aux} is connected to ground. The permanent latch is formed by two cross-coupled inverters. The first inverter has its input connected to the V_{CC} node and its output connected to the input of the second inverter. The second inverter has its input connected to the output of the first inverter and its output connected to the input of the first inverter. The output of the second inverter is labeled "Permanent Latch". The circuit also includes a resistor R_{limit} and a capacitor C_{Vcc} connected to the V_{CC} node, and a capacitor C_{aux} and an inductor L_{aux} connected to the output of the second inverter. The inductor L_{aux} is connected to ground. The circuit also includes a resistor R_{limit} and a capacitor C_{Vcc} connected to the V_{CC} node, and a capacitor C_{aux} and an inductor L_{aux} connected to the output of the second inverter. The inductor L_{aux} is connected to ground.

12

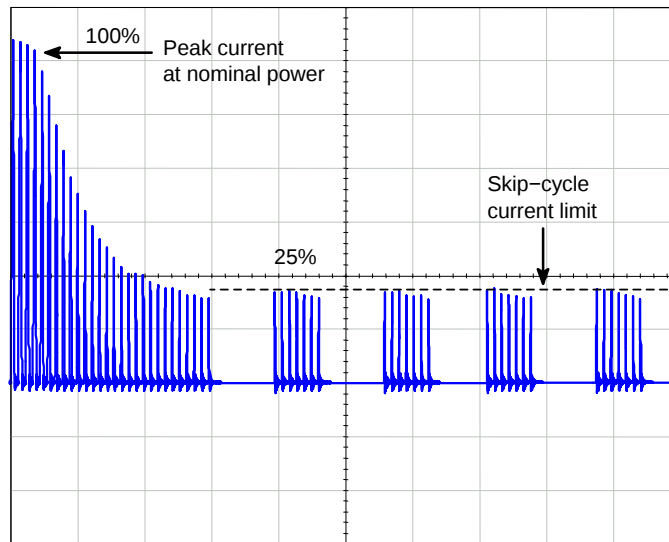


Figure 20. Low Peak Current Skip-Cycle Guarantees Noise-Free Operation

Full power operation involves the nominal switching frequency and thus avoids any noise when running.

Experiments carried on a 5.0 W universal mains board unveiled a standby power of 300 mW @ 230 Vac with the DSS activated and dropped to less than 100 mW when an auxiliary winding is connected.

Frequency Jittering for Improved EMI Signature

By sweeping the switching frequency around its nominal value, it spreads the energy content on adjacent frequencies rather than keeping it centered in one single ray. This offers

the benefit to artificially reduce the measurement noise on a standard EMI receiver and pass the tests more easily. The EMI sweep is implemented by routing the V_{CC} ripple (induced by the DSS activity) to the internal oscillator. As a result, the switching frequency moves up and down to the DSS rhythm. Typical deviation is $\pm 3.3\%$ of the nominal frequency. With a 1.0 V peak-to-peak ripple, the frequency will equal 65 kHz in the middle of the ripple and will increase as V_{CC} rises or decrease as V_{CC} ramps down. Figure 21 portrays the behavior we have adopted.

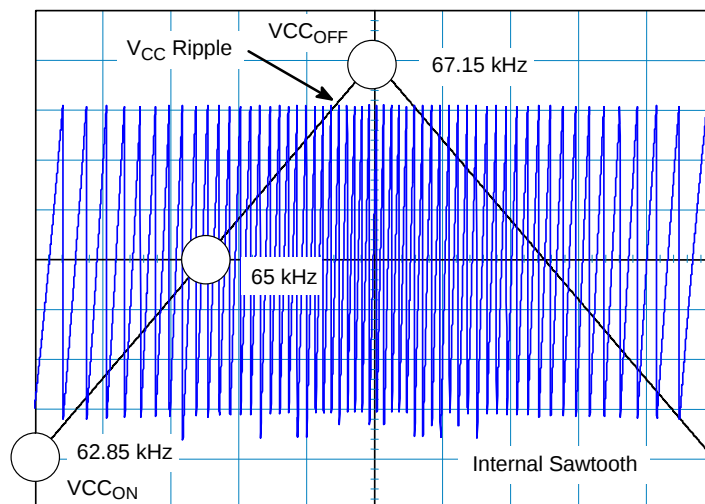


Figure 21. The V_{CC} ripple is used to introduce a frequency jittering on the internal oscillator sawtooth. Here, a 65 kHz version was selected.

Soft-Start

The NCP101X features an internal 1.0 ms soft-start activated during the power on sequence (PON). As soon as V_{CC} reaches V_{CCOFF} , the peak current is gradually increased from nearly zero up to the maximum internal clamping level (e.g. 350 mA). This situation lasts 1.0 ms and further to that time period, the peak current limit is blocked to the maximum until the supply enters regulation. The soft-start is also activated during the over current burst

(OCP) sequence. Every restart attempt is followed by a soft-start activation. Generally speaking, the soft-start will be activated when V_{CC} ramps up either from zero (fresh power-on sequence) or 4.7 V, the latch-off voltage occurring during OCP. Figure 22 portrays the soft-start behavior. The time scales are purposely shifted to offer a better zoom portion.

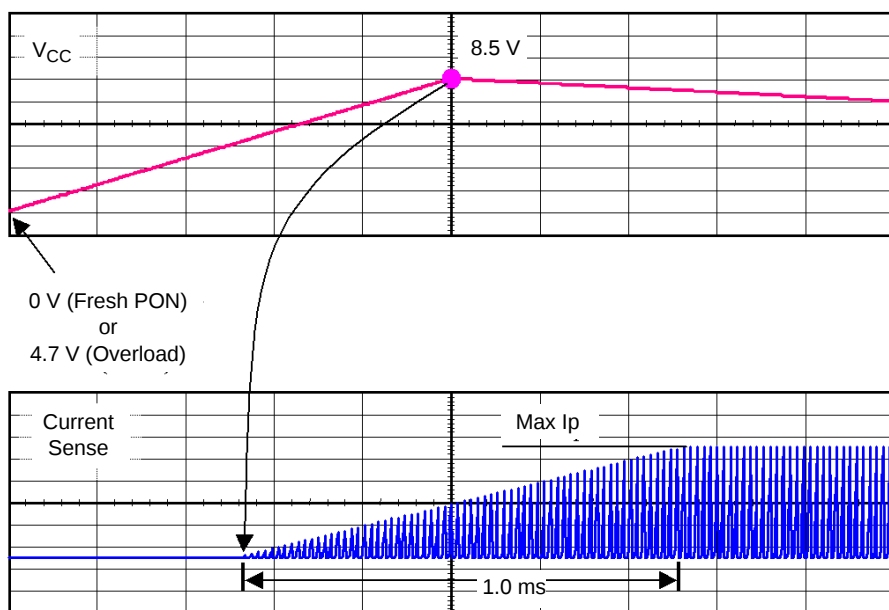


Figure 22. Soft-Start is activated during a startup sequence or an OCP condition.

Non-Latching Shutdown

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB

and ground. By pulling FB below the internal skip level (V_{skip}), the output pulses are disabled. As soon as FB is relaxed, the IC resumes its operation. Figure 23 depicts the application example.

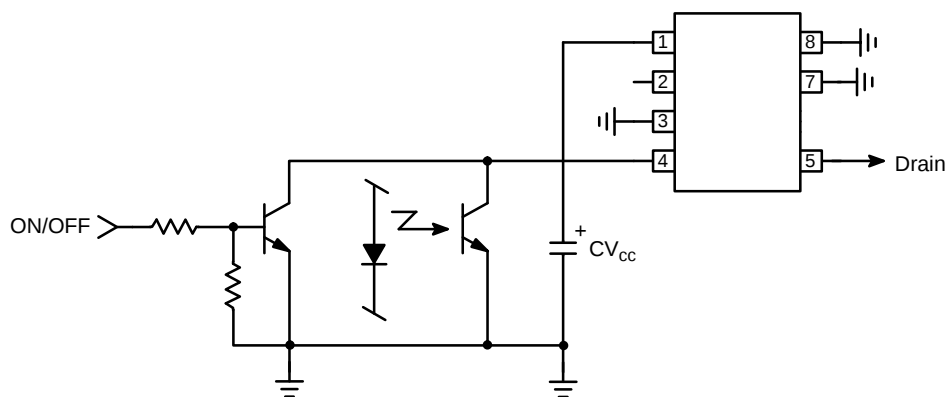


Figure 23. A non-latching shutdown where pulses are stopped as long as the NPN is biased.

Full Latching Shutdown

Other applications require a full latching shutdown, e.g. when an abnormal situation is detected (overtemperature or overvoltage). This feature can easily be implemented through two external transistors wired as a discrete SCR. When the OVP level exceeds the Zener breakdown

voltage, the NPN biases the PNP and fires the equivalent SCR, permanently bringing down the FB pin. The switching pulses are disabled until the user unplugs the power supply.

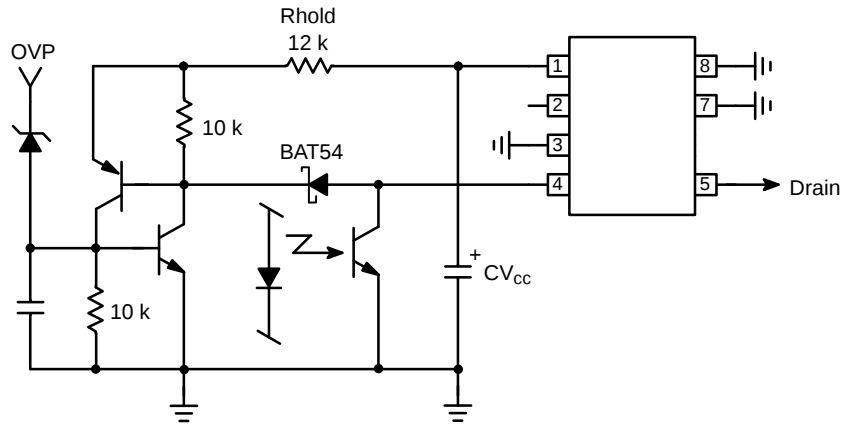


Figure 24. Two Bipolars Ensure a Total Latch-Off of the SMPS in Presence of an OVP

Rhold ensures that the SCR stays on when fired. The bias current flowing through Rhold should be small enough to let the VCC ramp up (8.5 V) and down (7.5 V) when the SCR is fired. The NPN base can also receive a signal from a temperature sensor. Typical bipolars can be MMBT2222 and MMBT2907 for the discrete latch. The MMBT3946 features two bipolars NPN+PNP in the same package and could also be used.

Power Dissipation and Heatsinking

The NCP101X welcomes two dissipating terms, the DSS current-source (when active) and the MOSFET. Thus, $P_{tot} = P_{DSS} + P_{MOSFET}$. When the PDIP-7 package is surrounded by copper, it becomes possible to drop its thermal resistance junction-to-ambient, $R_{\theta JA}$ down to 75°C/W and thus dissipate more power. The

maximum power the device can thus evacuate is:

$$P_{max} = \frac{T_{Jmax} - T_{ambmax}}{R_{\theta JA}} \quad (\text{eq. 12})$$

which gives around 1.0 W for an ambient of 50°C. The losses inherent to the MOSFET R_{DSon} can be evaluated using the following

$$\text{formula: } P_{mos} = \frac{1}{3} \cdot I_p^2 \cdot d \cdot R_{DSon} \quad (\text{eq. 13})$$

, where I_p is the worse case peak current (at the lowest line input), d is the converter operating duty-cycle and R_{DSon} , the MOSFET resistance for $T_j = 100^\circ\text{C}$. This formula is only valid for Discontinuous Conduction Mode (DCM) operation where the turn-on losses are null (the primary current is zero when you restart the MOSFET). Figure 25 gives a possible layout to help drop the thermal resistance. When measured on a 35 μm (1 oz) copper thickness PCB, we obtained a thermal resistance of 75°C/W.

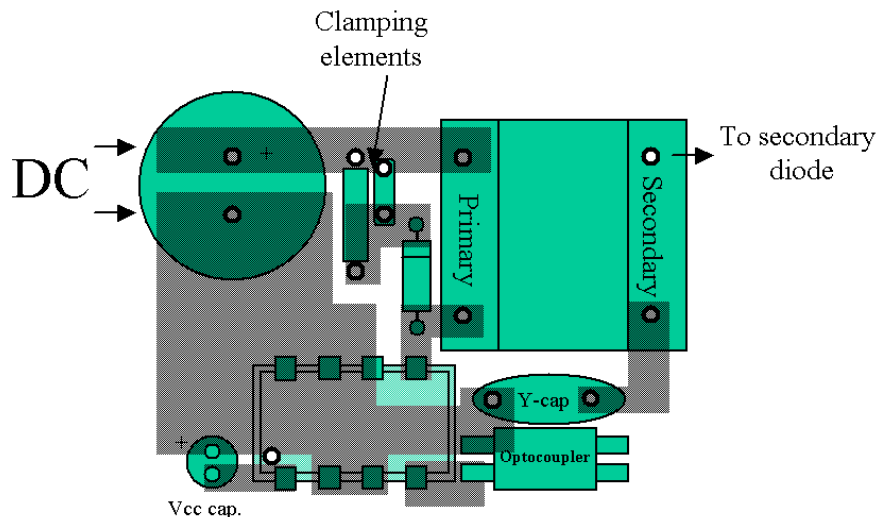


Figure 25. A Possible PCB Arrangement to Reduce the Thermal Resistance Junction-to-Ambient

Design Procedure

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller

and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices:

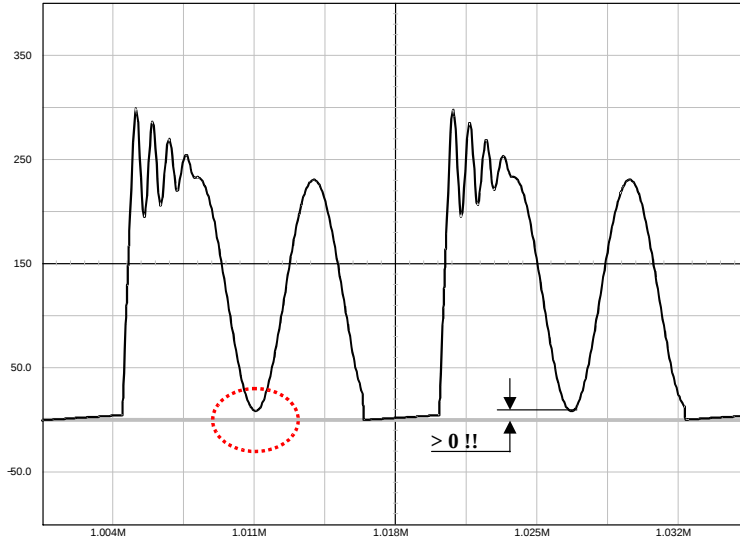


Figure 26. The Drain–Source Wave Shall Always be Positive . . .

1. In any case, the lateral MOSFET body–diode shall never be forward biased, either during startup (because of a large leakage inductance) or in normal operation as shown by Figure 26.

As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation: $N \cdot (V_{out} + V_f) < V_{in_min}$ (eq. 14). For instance, if operating from a 120 V DC rail, with a delivery of 12 V, we can select a reflected voltage of 100 Vdc maximum: $120 - 100 > 0$. Therefore, the turn ratio $N_p:N_s$ must be smaller than $100/(12 + 1) = 7.7$ or $N_p:N_s < 7.7$. We will see later on how it affects the calculation.

2. A current–mode architecture is, by definition, sensitive to subharmonic oscillations. Subharmonic oscillations only occur when the SMPS is operating in Continuous Conduction Mode (CCM) together with a duty–cycle greater than 50%. As a result, we recommend to operate the device in DCM only, whatever duty–cycle it implies (max = 65%). However, CCM operation with duty–cycles below 40% is possible.
3. Lateral MOSFETs have a poorly doped body–diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since

$$V_{drain_max} = V_{in} + N \cdot (V_{out} + V_f) + I_p \cdot \sqrt{\frac{L_f}{C_{tot}}} \quad (\text{eq. 15}), \text{ where } L_f \text{ is the leakage inductance,}$$

C_{tot} is the total capacitance at the drain node (which is increased by the capacitor wired between drain and source), N the $N_p:N_s$ turn ratio, V_{out} the output voltage, V_f the secondary diode forward drop and finally, I_p the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the V_{out} target is almost reached and I_p is still pushed to the maximum.

Taking into account all previous remarks, it becomes possible to calculate the maximum power that can be transferred at low line.

When the switch closes, V_{in} is applied across the primary inductance L_p until the current reaches the level imposed by the feedback loop. The duration of this event is called the ON time and can be defined by:

$$t_{on} = \frac{L_p \cdot I_p}{V_{in}} \quad (\text{eq. 16})$$

At the switch opening, the primary energy is transferred to the secondary and the flyback voltage appears across L_p , resetting the transformer core with a slope of $\frac{N \cdot (V_{out} + V_f)}{L_p}$. toff, the OFF time is thus:

$$t_{off} = \frac{L_p \cdot I_p}{N \cdot (V_{out} + V_f)} \quad (\text{eq. 17})$$

If one wants to keep DCM only, but still need to pass the maximum power, we will not allow a dead–time after the core is reset, but rather immediately restart. The switching time can be expressed by:

$$T_{sw} = t_{off} + t_{on} = L_p \cdot I_p \cdot \left(\frac{1}{V_{in}} + \frac{1}{N \cdot (V_{out} + V_f)} \right) \quad (\text{eq. 18})$$

The Flyback transfer formula dictates that:

$\frac{P_{out}}{\eta} = \frac{1}{2} \cdot L_p \cdot I_{p2}^2 \cdot F_{sw}$ (eq. 19) which, by extracting I_p and plugging into Equation 19, leads to:

$$T_{sw} = L_p \sqrt{\frac{2 \cdot P_{out}}{\eta \cdot F_{sw} \cdot L_p}} \cdot \left(\frac{1}{V_{in}} + \frac{1}{N \cdot (V_{out} + V_f)} \right) \quad (\text{eq. 20})$$

Extracting L_p from Equation 20 gives:

$$L_{p\text{critical}} = \frac{(V_{in} \cdot V_r)^2 \cdot \eta}{2 \cdot F_{sw} \cdot [P_{out} \cdot (V_r^2 + 2 \cdot V_r \cdot V_{in} + V_{in}^2)]}$$

(eq. 21) , with $V_r = N \cdot (V_{out} + V_f)$ and η the efficiency.

If L_p critical gives the inductance value above which DCM operation is lost, there is another expression we can write to connect L_p , the primary peak current bounded by the NCP101X and the maximum duty-cycle that needs to stay below 50%:

$$L_{p\text{max}} = \frac{DC_{\text{max}} \cdot V_{in\text{min}} \cdot T_{sw}}{I_{p\text{max}}} \quad (\text{eq. 22}) \quad \text{where } V_{in\text{min}}$$

corresponds to the lowest rectified bulk voltage, hence the longest ton duration or largest duty-cycle. $I_{p\text{max}}$ is the available peak current from the considered part, e.g. 350 mA typical for the NCP1013 (however, the minimum value of this parameter shall be considered for reliable evaluation). Combining Equations 21 and 22 gives the maximum theoretical power you can pass respecting the peak current capability of the NCP101X, the maximum duty-cycle and the discontinuous mode operation:

$$P_{\text{max}} := \frac{T_{sw}^2 \cdot V_{in\text{min}}^2 \cdot V_r^2 \cdot \eta \cdot F_{sw}}{(2 \cdot L_{p\text{max}} \cdot V_r^2 + 4 \cdot L_{p\text{max}} \cdot V_r \cdot V_{in\text{min}} + 2 \cdot L_{p\text{max}} \cdot V_{in\text{min}}^2)} \quad (\text{eq. 23})$$

From Equation 22 we obtain the operating duty-cycle

$d = \frac{I_p \cdot L_p}{V_{in} \cdot T_{sw}}$ (eq. 24) which lets us calculate the RMS current circulating in the MOSFET:

$I_{d\text{RMS}} = I_p \cdot \sqrt{\frac{d}{3}}$ (eq. 25) . From this equation, we obtain the average dissipation in the MOSFET: $P_{\text{avg}} = \frac{1}{3} \cdot I_p^2 \cdot d \cdot R_{DSon}$ (eq. 26) to which switching losses shall be added.

If we stick to Equation 23, compute L_p and follow the above calculations, we will discover that a power supply built with the NCP101X and operating from a 100 Vac line minimum will not be able to deliver more than 7.0 W continuous, regardless of the selected switching frequency (however the transformer core size will go down as $F_{\text{switching}}$ is increased). This number increases significantly when operated from a single European mains (18 W). Application note AND8125/D, "Evaluating the Power Capability of the NCP101X Members" details how to assess the available power budget from all the NCP101X series.

Example 1. A 12 V 7.0 W SMPS operating on a large mains with NCP101X:

$V_{in} = 100 \text{ Vac}$ to 250 Vac or 140 Vdc to 350 Vdc once rectified, assuming a low bulk ripple

Efficiency = 80%

$V_{out} = 12 \text{ V}$, $I_{out} = 580 \text{ mA}$

$F_{\text{switching}} = 65 \text{ kHz}$

$I_{p\text{max}} = 350 \text{ mA} - 10\% = 315 \text{ mA}$

Applying the above equations leads to:

Selected maximum reflected voltage = 120 V

with $V_{out} = 12 \text{ V}$, secondary drop = 0.5 V $\rightarrow N_p:N_s = 1:0.1$

L_p critical = 3.2 mH

$I_p = 292 \text{ mA}$

Duty-cycle worse case = 50%

$I_{\text{drain RMS}} = 119 \text{ mA}$

$P_{\text{MOSFET}} = 354 \text{ mW}$ at $R_{DSon} = 24 \Omega$ ($T_J > 100^\circ\text{C}$)

$P_{\text{DSS}} = 1.1 \text{ mA} \times 350 \text{ V} = 385 \text{ mW}$, if DSS is used

Secondary diode voltage stress = $(350 \times 0.1) + 12 = 47 \text{ V}$ (e.g. a MBRS360T3, 3.0 A/60 V would fit)

Example 2. A 12 V 16 W SMPS operating on narrow European mains with NCP101X:

$V_{in} = 230 \text{ Vac} \pm 15\%$, 276 Vdc for $V_{in\text{min}}$ to 370 Vdc once rectified

Efficiency = 80%

$V_{out} = 12 \text{ V}$, $I_{out} = 1.25 \text{ A}$

$F_{\text{switching}} = 65 \text{ kHz}$

$I_{p\text{max}} = 350 \text{ mA} - 10\% = 315 \text{ mA}$

Applying the equations leads to:

Selected maximum reflected voltage = 250 V

with $V_{out} = 12 \text{ V}$, secondary drop = 0.5 V $\rightarrow N_p:N_s = 1:0.05$

$L_p = 6.6 \text{ mH}$

$I_p = 0.305 \text{ mA}$

Duty-cycle worse case = 0.47

$I_{\text{drain RMS}} = 121 \text{ mA}$

$P_{\text{MOSFET}} = 368 \text{ mW}$ at $R_{DSon} = 24 \Omega$ ($T_J > 100^\circ\text{C}$)

$P_{\text{DSS}} = 1.1 \text{ mA} \times 370 \text{ V} = 407 \text{ mW}$, if DSS is used below an ambient of 50°C .

Secondary diode voltage stress = $(370 \times 0.05) + 12 = 30.5 \text{ V}$ (e.g. a MBRS340T3, 3.0 A/40 V)

Please note that these calculations assume a flat DC rail whereas a 10 ms ripple naturally affects the final voltage available on the transformer end. Once the Bulk capacitor has been selected, one should check that the resulting ripple (min V_{bulk} ?) is still compatible with the above calculations. As an example, to benefit from the largest operating range, a 7.0 W board was built with a 47 μF bulk capacitor which ensured discontinuous operation even in the ripple minimum waves.

MOSFET Protection

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET

BV_{DSS} which is 700 V. Figure 27 presents possible implementations:

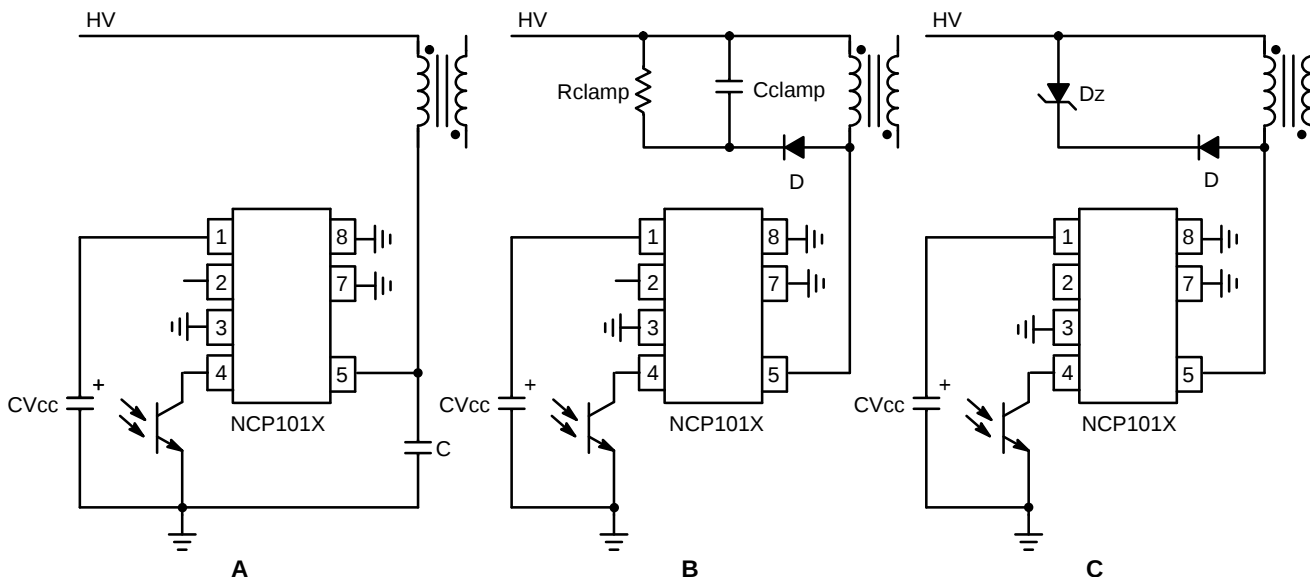


Figure 27. Different Options to Clamp the Leakage Spike

Figure 27A: The simple capacitor limits the voltage according to Equation 15. This option is only valid for low power applications, e.g. below 5.0 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute C with Equation 15. Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses.

Figure 27B: This diagram illustrates the most standard circuitry called the RCD network. Rclamp and Cclamp are calculated using the following formulas:

$$R_{\text{clamp}} = \frac{2 \cdot V_{\text{clamp}} \cdot (V_{\text{clamp}} - (V_{\text{out}} + V_f) \cdot N)}{I_{\text{leak}} \cdot I_p^2 \cdot F_{\text{sw}}} \quad (\text{eq. 27})$$

$$C_{\text{clamp}} = \frac{V_{\text{clamp}}}{V_{\text{ripple}} \cdot F_{\text{sw}} \cdot R_{\text{clamp}}} \quad (\text{eq. 28})$$

V_{clamp} is usually selected 50–80 V above the reflected value $N \times (V_{\text{out}} + V_f)$. The diode needs to be a fast one and a MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worst case occurs when I_p and V_{in} are maximum and V_{out} is close to reach the steady-state value.

Figure 27C: This option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a Zener diode or a TVS. There are little technology differences behind a standard Zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of Zener. A 5.0 W Zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal Zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5.0 W of continuous power but is able to accept surges up to 600 W @ 1.0 ms. Select the Zener or TVS clamping level between 40 to 80 V above the reflected output voltage when the supply is heavily loaded.

Typical Application Examples

A 6.5 W NCP1012-Based Flyback Converter

Figure 28 shows a converter built with a NCP1012 delivering 6.5 W from a universal input. The board uses the Dynamic Self-Supply and a simplified Zener-type

feedback. This configuration was selected for cost reasons and a more precise circuitry can be used, e.g. based on a TL431:

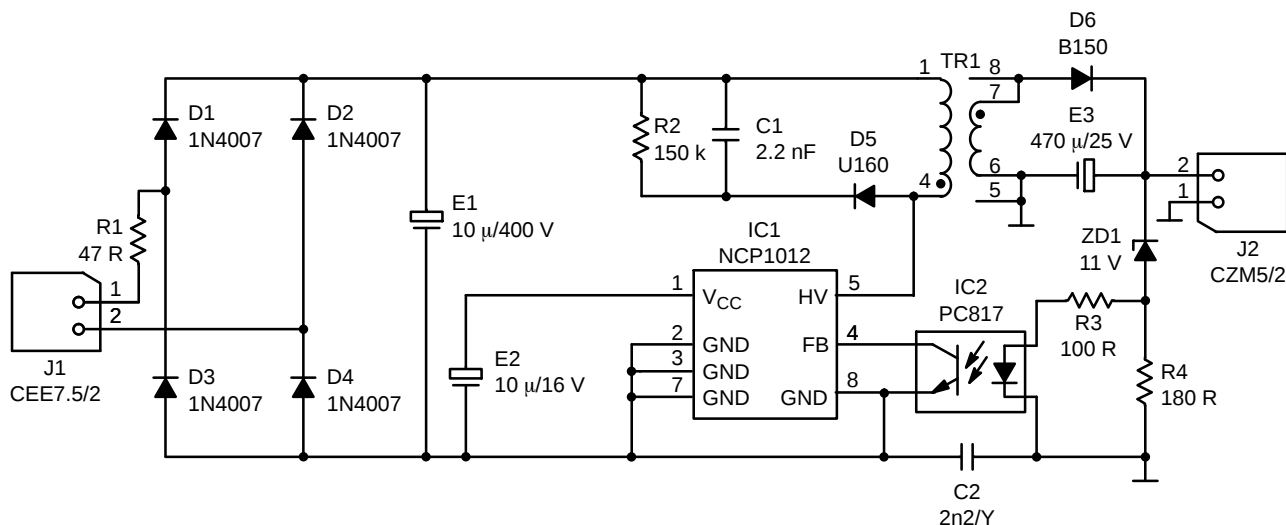


Figure 28. An NCP1012-Based Flyback Converter Delivering 6.5 W

The converter built according to Figure 29 layouts, gave the following results:

- Efficiency at $V_{in} = 100 \text{ Vac}$ and $P_{out} = 6.5 \text{ W} = 75.7\%$
- Efficiency at $V_{in} = 230 \text{ Vac}$ and $P_{out} = 6.5 \text{ W} = 76.5\%$

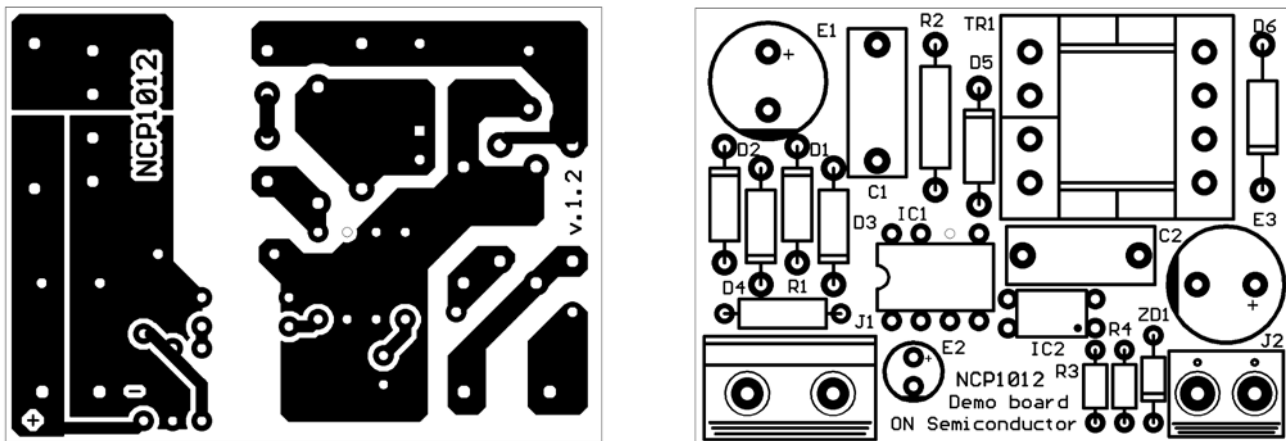


Figure 29. The NCP1012-Based PCB Layout . . . and its Associated Component Placement

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

A 7.0 W NCP1013-based Flyback Converter Featuring Low Standby Power

Figure 30 depicts another typical application showing a NCP1013-65 kHz operating in a 7.0 W converter up to 70°C of ambient temperature. We can increase the output

power since an auxiliary winding is used, the DSS is disabled, and thus offering more room for the MOSFET. In this application, the feedback is made via a TLV431 whose low bias current (100 μ A min) helps to lower the no-load standby power.

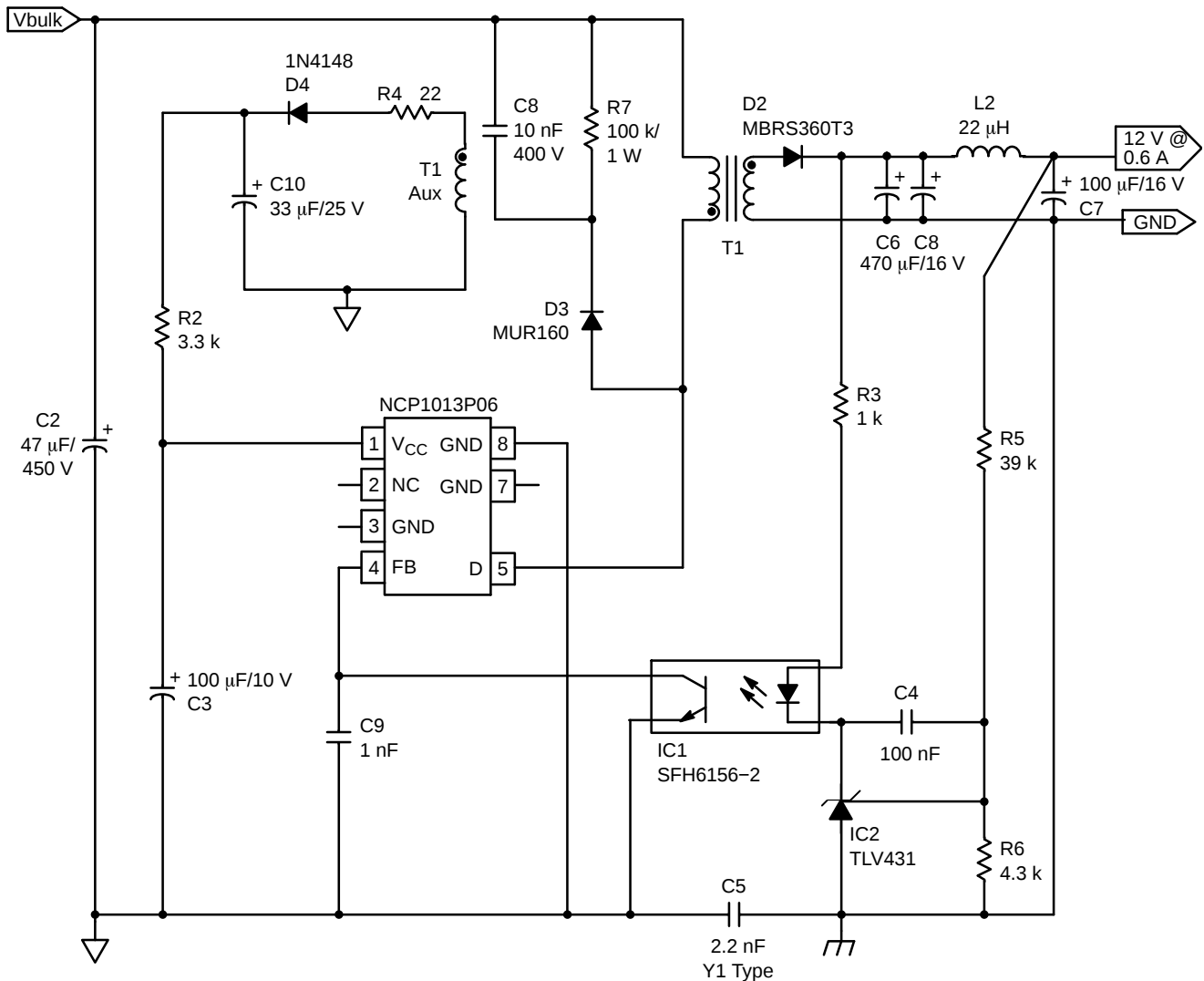


Figure 30. A Typical Converter Delivering 7.0 W from a Universal Mains

Measurements have been taken from a demonstration board implementing the diagram in Figure 30 and the following results were achieved, with either the auxiliary winding in place or through the Dynamic Self-Supply:

Vin = 230 Vac, auxiliary winding, Pout = 0, Pin = 60 mW

Vin = 100 Vac, auxiliary winding, Pout = 0, Pin = 42 mW

Vin = 230 Vac, Dynamic Self-Supply, Pout = 0, Pin = 300 mW

Vin = 100 Vac, Dynamic Self-Supply, Pout = 0, Pin = 130 mW

Pout = 7.0 W, η = 81% @ 230 Vac, with auxiliary winding

Pout = 7.0 W, η = 81.3 @ 100 Vac, with auxiliary winding

For a quick evaluation of Figure 30 application example, the following transformers are available from Coilcraft:

A9619-C, Lp = 3.0 mH, Np:Ns = 1:0.1, 7.0 W application on universal mains, including auxiliary winding, NCP1013-65kHz.

A0032-A, Lp = 6.0 mH, Np:Ns = 1:0.055, 10 W application on European mains, DSS operation only, NCP1013-65 kHz.

Coilcraft
1102 Silver Lake Road
CARY IL 60013
Email: info@coilcraft.com
Tel.: 847-639-6400
Fax.: 847-639-1469

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

ORDERING INFORMATION

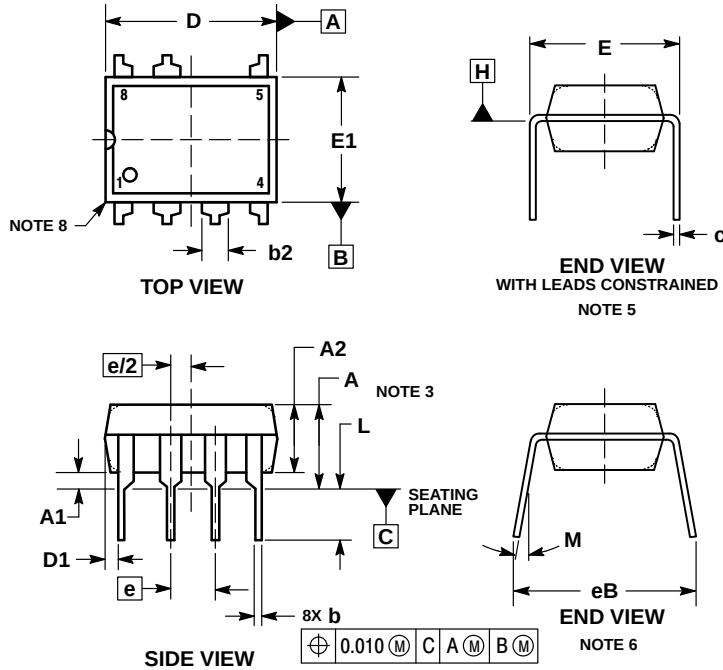
Device Order Number	Frequency (kHz)	Package Type	Shipping [†]	R _{DSon} (Ω)	I _{pk} (mA)
NCP1010AP065G	65	PDIP-7 (Pb-Free)	50 Units / Rail	23	100
NCP1010AP100G	100			23	100
NCP1010AP130G	130			23	100
NCP1010ST65T3G	65	SOT-223 (Pb-Free)	4000 / Tape & Reel	23	100
NCP1010ST100T3G	100			23	100
NCP1010ST130T3G	130			23	100
NCP1011AP065G	65	PDIP-7 (Pb-Free)	50 Units / Rail	23	250
NCP1011AP100G	100		50 Units / Rail	23	250
NCP1011AP130G	130			23	250
NCP1011ST65T3G	65	SOT-223 (Pb-Free)	4000 / Tape & Reel	23	250
NCP1011ST100T3G	100			23	250
NCP1011ST130T3G	130			23	250
NCP1012AP065G	65	PDIP-7 (Pb-Free)	50 Units / Rail	11	250
NCP1012AP100G	100		50 Units / Rail	11	250
NCP1012AP133G	130		50 Units / Rail	11	250
NCP1012ST65T3G	65	SOT-223 (Pb-Free)	4000 / Tape & Reel	11	250
NCP1012ST100T3G	100			11	250
NCP1012ST130T3G	130		4000 / Tape & Reel	11	250
NCP1013AP065G	65	PDIP-7 (Pb-Free)	50 Units / Rail	11	350
NCP1013AP100G	100			11	350
NCP1013AP133G	130			11	350
NCP1013ST65T3G	65	SOT-223 (Pb-Free)	4000 / Tape & Reel	11	350
NCP1013ST100T3G	100			11	350
NCP1013ST130T3G	130			11	350
NCP1014AP065G	65	PDIP-7 (Pb-Free)	50 Units / Rail	11	450
NCP1014AP100G	100		50 Units / Rail	11	450
NCP1014ST65T3G	65	SOT-223 (Pb-Free)	4000 / Tape & Reel	11	450
NCP1014ST100T3G	100			11	450

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

PACKAGE DIMENSIONS

PDIP-7
AP SUFFIX
CASE 626A
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION E3 IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

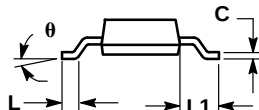
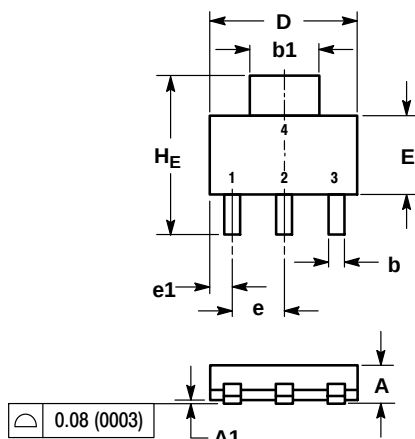
NCP1010, NCP1011, NCP1012, NCP1013, NCP1014

PACKAGE DIMENSIONS

SOT-223 (TO-261)

CASE 318E-04

ISSUE N

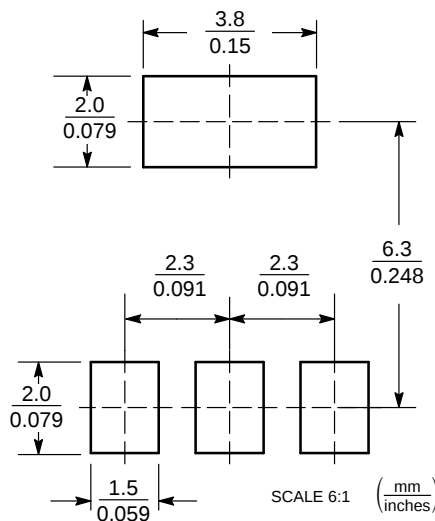


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
theta	0°	---	10°	0°	---	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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