

SA572

Programmable Analog Compandor

The SA572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The SA572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

Features

- Independent Control of Attack and Recovery Time
- Improved Low Frequency Gain Control Ripple
- Complementary Gain Compression and Expansion with External Op Amp
- Wide Dynamic Range – Greater than 110 dB
- Temperature-Compensated Gain Control
- Low Distortion Gain Cell
- Low Noise – 6.0 μV Typical
- Wide Supply Voltage Range – 6.0 V-22 V
- System Level Adjustable with External Components
- Pb-Free Packages are Available*

Applications

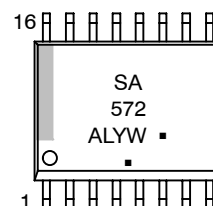
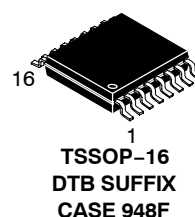
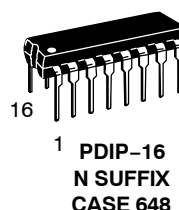
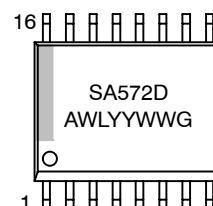
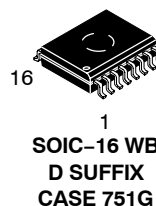
- Dynamic Noise Reduction System
- Voltage Control Amplifier
- Stereo Expander
- Automatic Level Control
- High-Level Limiter
- Low-Level Noise Gate
- State Variable Filter



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS

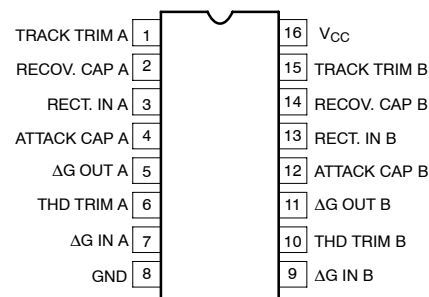


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

D, N, DTB Packages*



*D package released in large SO (SOL) package only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

SA572

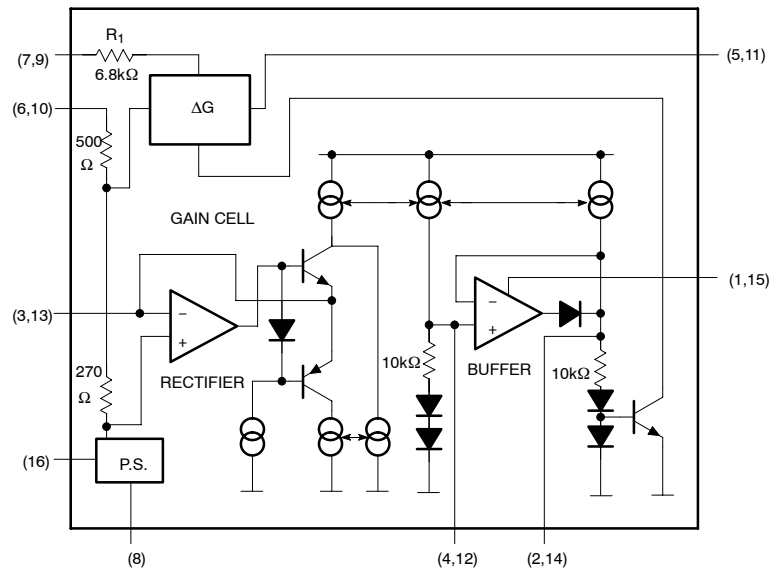


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	TRACK TRIM A	Tracking Trim A
2	RECOV. CAP A	Recovery Capacitor A
3	RECT. IN A	Rectifier A Input
4	ATTACK CAP A	Attack Capacitor A
5	ΔG OUT A	Variable Gain Cell A Output
6	THD TRIM A	Total Harmonic Distortion Trim A
7	ΔG IN A	Variable Gain Cell A Input
8	GND	Ground
9	ΔG IN B	Variable Gain Cell B Input
10	THD TRIM B	Total Harmonic Distortion Trim B
11	ΔG OUT B	Variable Gain Cell B Output
12	ATTACK CAP B	Attack Capacitor B
13	RECT. IN B	Rectifier B Input
14	RECOV. CAP B	Recovery Capacitor B
15	TRACK TRIM B	Tracking Trim B
16	V_{CC}	Positive Power Supply

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	22	V_{DC}
Operating Temperature Range	T_A	-40 to +85	$^{\circ}C$
Operating Junction Temperature	T_J	150	$^{\circ}C$
Power Dissipation	P_D	500	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	N Package D Package DTB Package	$^{\circ}C/W$
		75 105 133	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

DC ELECTRICAL CHARACTERISTICS Standard test conditions, $V_{CC} = 15\text{ V}$, $T_A = 25^{\circ}C$; Expander mode (see Test Circuit). Input signals at unity gain level (0 dB) = 100 mV_{RMS} at 1.0 kHz; $V_1 = V_2$; $R_2 = 3.3\text{ k}\Omega$; $R_3 = 17.3\text{ k}\Omega$, unless otherwise noted.

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	–	6.0	–	22	V_{DC}
Supply Current	I_{CC}	No Signal	–	–	6.3	mA
Internal Voltage Reference	V_R	–	2.3	2.5	2.7	V_{DC}
Total Harmonic Distortion (Untrimmed)	THD	1.0 kHz, $C_A = 1.0\text{ }\mu\text{F}$	–	0.2	1.0	%
Total Harmonic Distortion (Trimmed)	THD	1.0 kHz, $C_R = 10\text{ }\mu\text{F}$	–	0.05	–	%
Total Harmonic Distortion (Trimmed)	THD	100 Hz	–	0.25	–	%
No Signal Output Noise		Input to V_1 and V_2 grounded (20–20 kHz)	–	6.0	25	μV
DC Level Shift (Untrimmed)		Input change from no signal to 100 mV _{RMS}	–	± 20	± 50	mV
Unity Gain Level		–	-1.5	0	+1.5	dB
Large-Signal Distortion		$V_1 = V_2 = 400\text{ mV}$	–	0.7	3.0	%
Tracking Error (Measured relative to value at unity gain) = [$V_O - V_O$ (unity gain)] dB– V_2 dB		Rectifier Input $V_2 = +6.0\text{ dB}$, $V_1 = 0\text{ dB}$ $V_2 = -30\text{ dB}$, $V_1 = 0\text{ dB}$	–	± 0.2 ± 0.5	-2.5, +1.6	dB dB
Channel Crosstalk		200 mV _{RMS} into channel A, measured output on channel B	60	–	–	dB
Power Supply Rejection Ratio	PSRR	120 Hz	–	70	–	dB

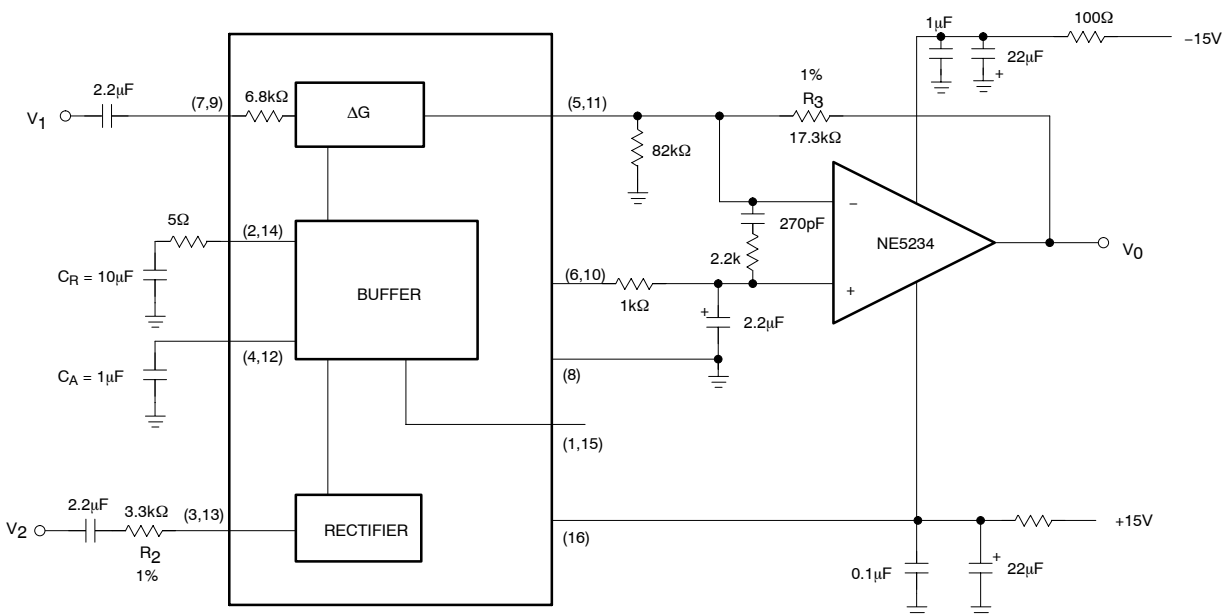


Figure 2. Test Circuit

Audio Signal Processing IC Combines VCA and Fast Attack/Slow Recovery Level Sensor

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the SA572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The SA572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal $10\text{ k}\Omega$ resistor R_A defines the attack time τ_A . The recovery time τ_R of a tone burst is defined by a recovery capacitor C_R and an internal $10\text{ k}\Omega$ resistor R_R . Typical attack time of 4.0 ms for the high-frequency spectrum and 40 ms for the low frequency band can be obtained with $0.1\text{ }\mu\text{F}$ and $1.0\text{ }\mu\text{F}$ attack capacitors, respectively. Recovery time of 200 ms can be obtained with a $4.7\text{ }\mu\text{F}$ recovery capacitor for a 100 Hz signal, the third harmonic distortion is improved by more than 10 dB over the simple RC ripple filter with a single $1.0\text{ }\mu\text{F}$ attack and recovery capacitor, while the attack time remains the same.

The SA572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6.0 V to 22 V . Supply current is less than 6.0 mA . The SA572 is designed for applications from -40°C to $+85^\circ\text{C}$.

BASIC APPLICATIONS

Description

The SA572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5 V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 3 shows the circuit configuration of the gain cell. Bases of the differential pairs Q_1 - Q_2 and Q_3 - Q_4 are both tied to the output and inputs of OPA A_1 . The negative feedback through Q_1 holds the V_{BE} of Q_1 - Q_2 and the V_{BE} of Q_3 - Q_4 equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q3Q4}} = \Delta V_{BE_{Q1Q2}}$$

$$(V_{BE} = V_T \ln IC/IS)$$

$$V_{T \ln} \left(\frac{\frac{1}{2} I_G + \frac{1}{2} I_O}{I_S} \right) - V_{T \ln} \left(\frac{\frac{1}{2} I_G - \frac{1}{2} I_O}{I_S} \right) \quad (\text{eq. 1})$$

$$= V_{T \ln} \left(\frac{I_1 + I_{IN}}{I_S} \right) - V_{T \ln} \left(\frac{I_2 - I_1 - I_{IN}}{I_S} \right)$$

$$\text{where } I_{IN} = \frac{V_{IN}}{R_1}$$

$$R_1 = 6.8\text{ k}\Omega$$

$$I_1 = 140\text{ }\mu\text{A}$$

$$I_2 = 280\text{ }\mu\text{A}$$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation 1 can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2} (I_2 - 2I_1) \cdot I_G \quad (\text{eq. 2})$$

The first term of equation 2 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\text{ }\mu\text{A}$ into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100 mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals

is only 6.0 μV in the audio spectrum (10 Hz-20 kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

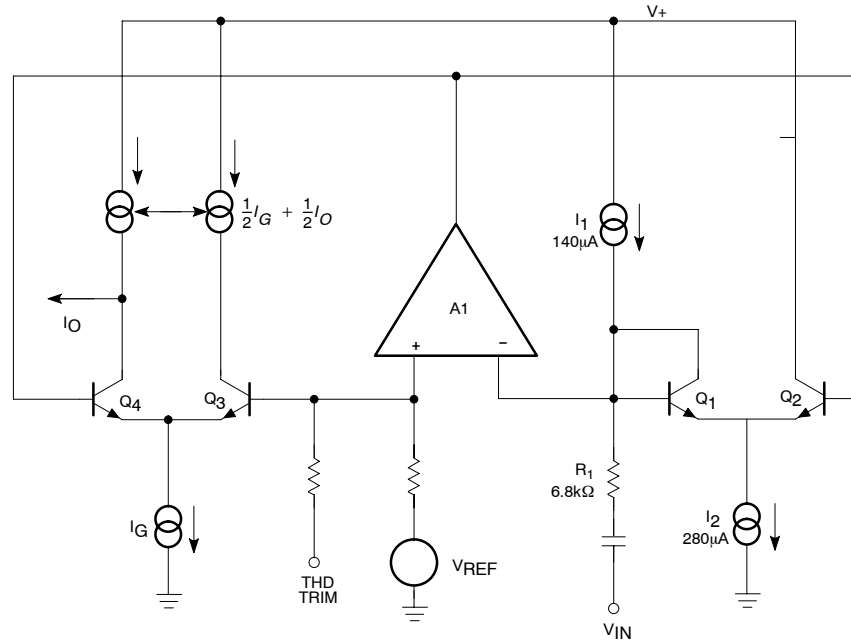


Figure 3. Basic Gain Cell Schematic

Rectifier

The rectifier is a full-wave design as shown in Figure 4. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2 . If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2 . The input bias current is typically about 70 nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R . The rectifier transfer function is:

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (\text{eq. 3})$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN}(\text{AVG})}{R_2}$$

The internal bias scheme limits the maximum output current I_R to be around 300 μA . Within a ± 1.0 dB error band the input range of the rectifier is about 52 dB.

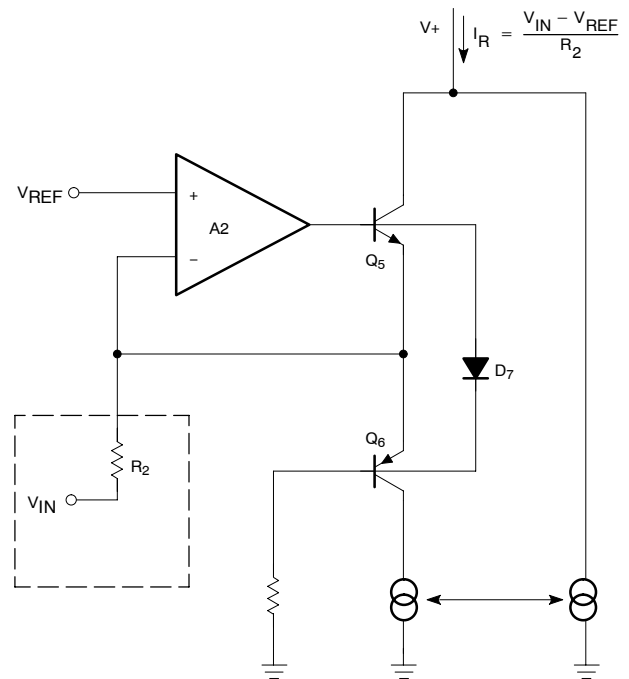


Figure 4. Simplified Rectifier Schematic

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 5, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A₃ through Q₈, Q₉ and Q₁₀. Diodes D₁₁ and D₁₂ improve tracking accuracy and provide common-mode bias for A₃. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A₃ makes the contribution of capacitor C_R to attack time insignificant. Neglecting diode impedance, the gain G_A(t) for ΔG can be expressed as follows:

$$G_A(t) = (G_{AINT} - G_{AFNL}) e^{-\frac{t}{\tau_A}} + G_{AFNL}$$

G_{AINT} = Initial Gain

G_{AFNL} = Final Gain

$$\tau_A = R_A \cdot C_A = 10 \text{ k}\Omega \cdot C_A$$

where τ_A is the attack time constant and R_A is a 10 kΩ internal resistor. Diode D₁₅ opens the feedback loop of A₃ for a negative-going signal if the value of capacitor C_R is larger than capacitor C_A. The recovery time depends only on C_R • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R(t) for ΔG is expressed as follows:

$$G_R(t) = (G_{RINT} - G_{RFNL}) e^{-\frac{t}{\tau_R}} + G_{RFNL}$$

$$G_R(t) = (G_{RINT} - G_{RFNL}) e^{-\frac{t}{\tau_R}} + G_{RFNL}$$

$$\tau_R = R_R \cdot C_R = 10 \text{ k}\Omega \cdot C_R$$

where τ_R is the recovery time constant and R_R is a 10 kΩ internal resistor. The gain control current is mirrored to the gain cell through Q₁₄. The low level gain errors due to input bias current of A₂ and A₃ can be trimmed through the tracking trim pin into A₃ with a current source of ± 3.0 μA.

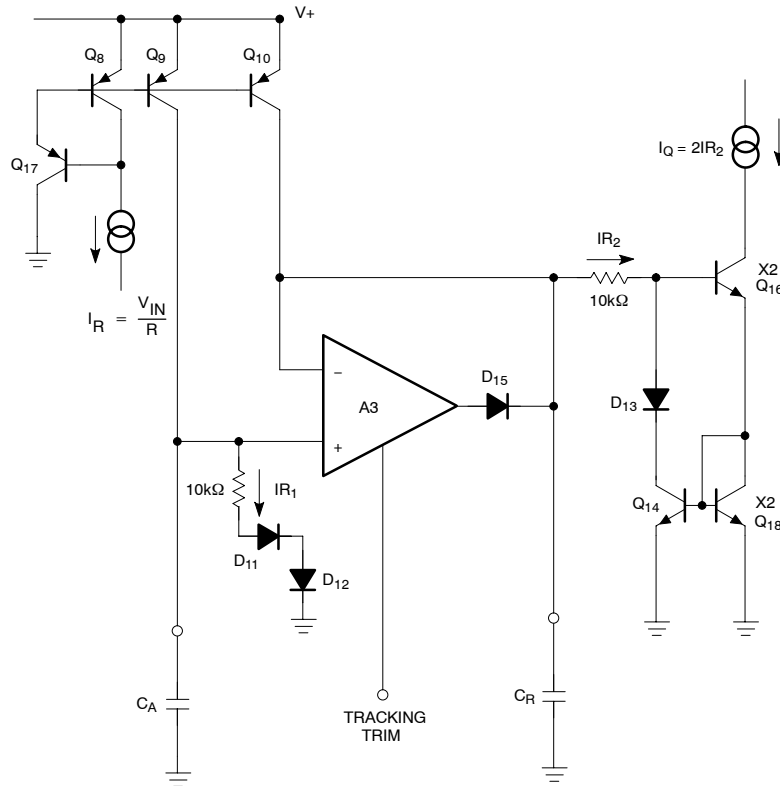


Figure 5. Buffer Amplifier Schematic

Basic Expander

Figure 6 shows an application of the circuit as a simple expander. The gain expression of the system is given by:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \right)^2 \quad (\text{eq. 4})$$

($I_1 = 140 \mu\text{A}$)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a $6.8 \text{ k}\Omega$ internal resistor. The maximum input current into the gain cell can be as large as $140 \mu\text{A}$. This corresponds to a voltage level of $140 \mu\text{A} \cdot 6.8 \text{ k}\Omega = 952 \text{ mV}$ peak. The input peak current into the rectifier is limited to $300 \mu\text{A}$ by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance

buffer A_1 may be necessary if the input is voltage driven with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2 . R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by:

$$V_{OUT \text{ DC}} = V_{REF} \left(1 + \frac{R_3}{R_4} \right) - V_B \frac{R_3}{R_4} \quad (\text{eq. 5})$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. C_A sets the attack time constant and C_R sets the recovery time constant.

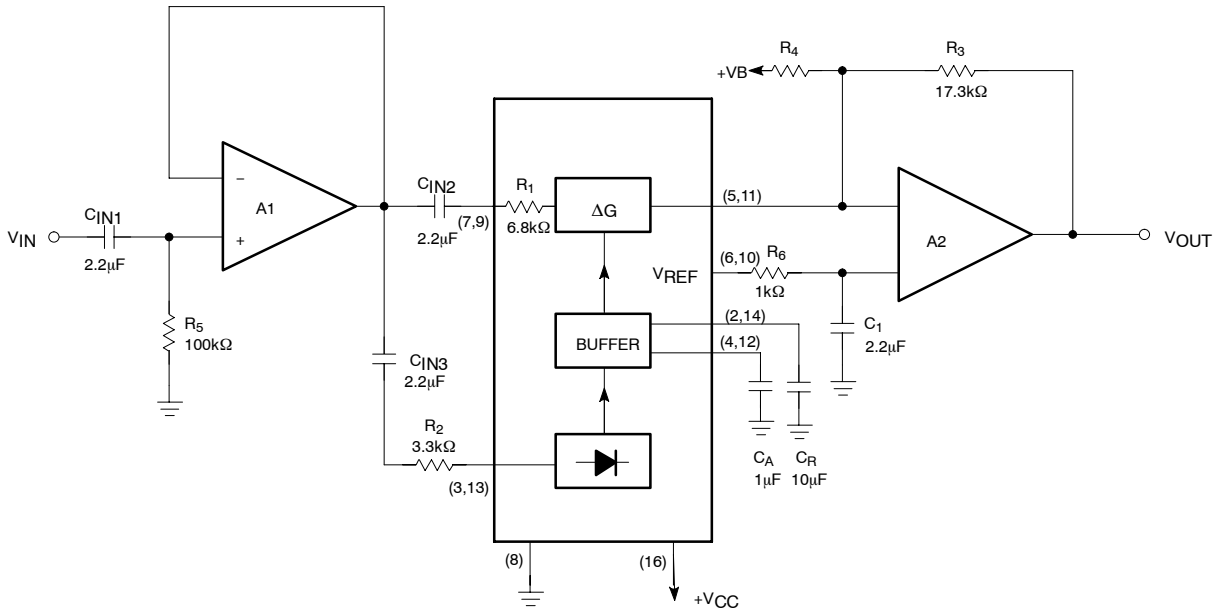


Figure 6. Basic Expander Schematic

Basic Compressor

Figure 7 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1 . The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}} \right)^{\frac{1}{2}} \quad (\text{eq. 6})$$

($I_1 = 140 \mu\text{A}$)

R_{DC1} , R_{DC2} , and CDC form a DC feedback for A_1 . The output DC level of A_1 is given by:

$$V_{OUT \text{ DC}} = V_{REF} \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4} \right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4} \right) \quad (\text{eq. 7})$$

The zener diodes D_1 and D_2 are used for channel overload protection.

SA572

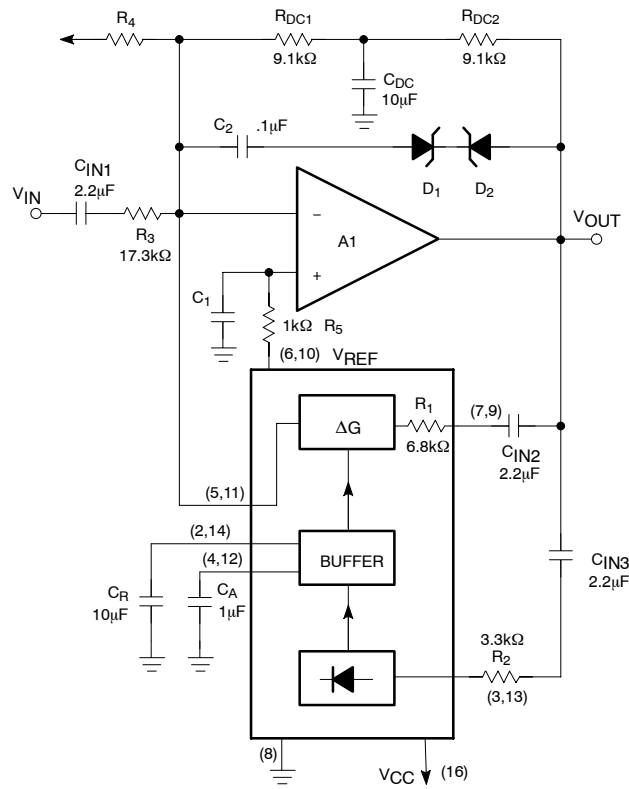


Figure 7. Basic Compressor Schematic

Basic Compressor System

The above basic compressor and expander can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting,

pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 8 shows the system level diagram for reference.

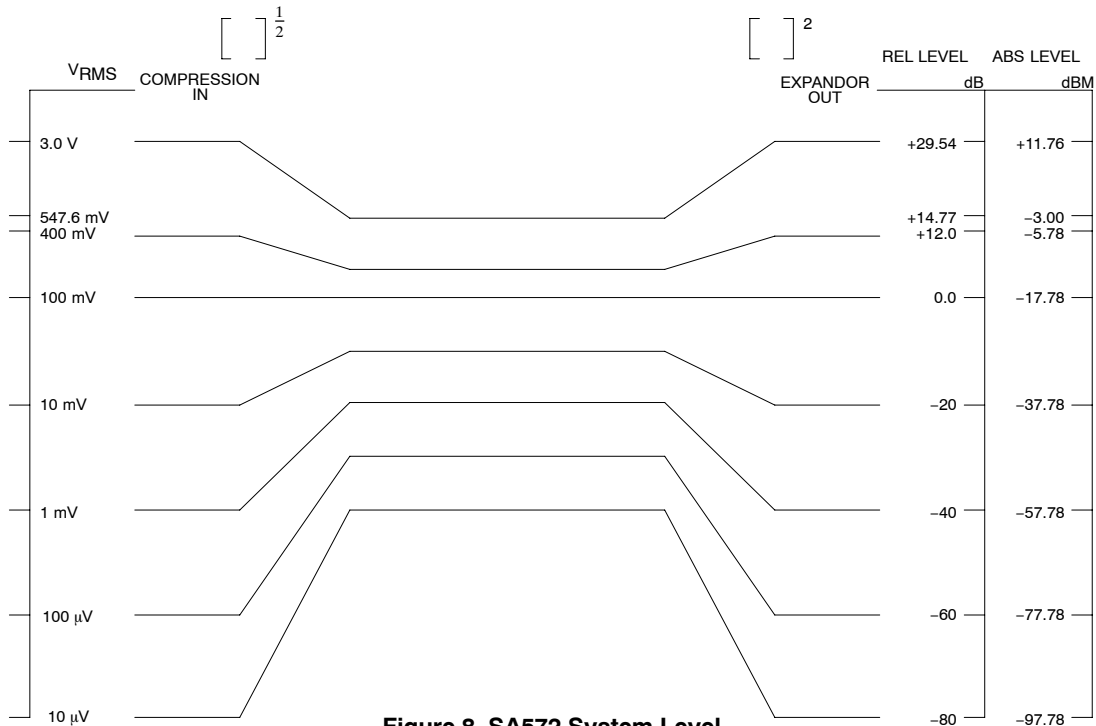


Figure 8. SA572 System Level

SA572

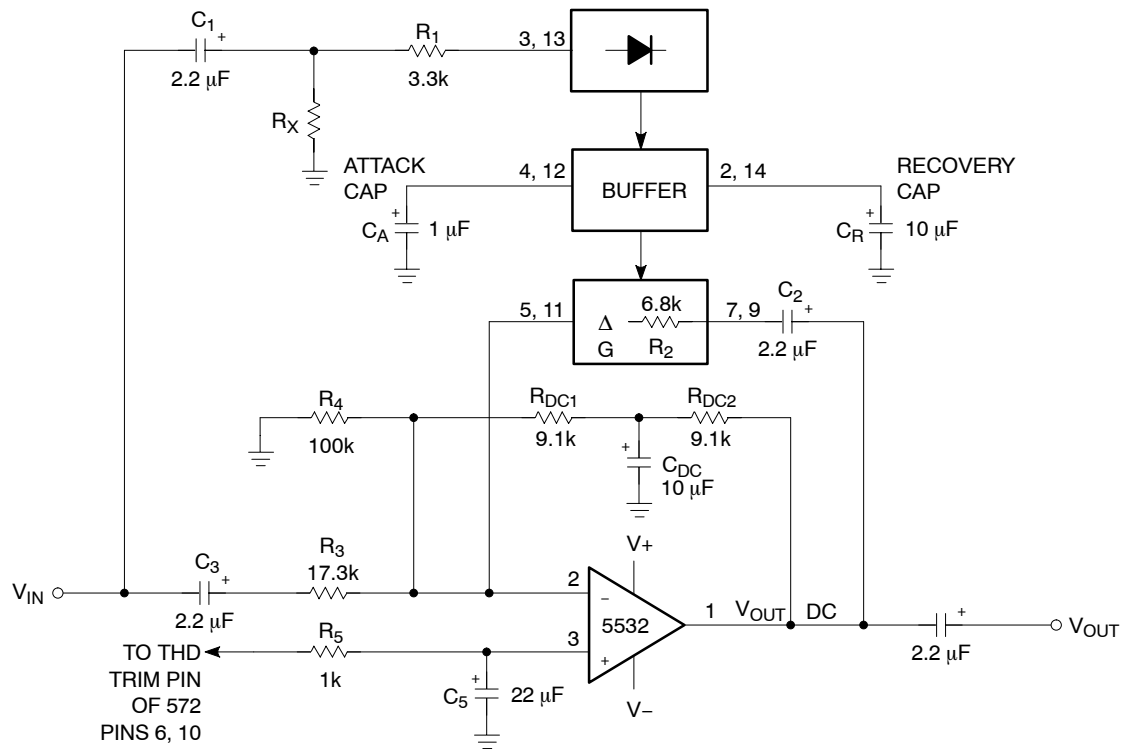


Figure 9. Automatic Level Control

Automatic Level Control (ALC)

In the ALC configuration, the variable gain cell is placed in the feedback loop of the operational amplifier and the rectifier is connected to the input. As the input amplitude increases above the crossover point, the overall system gain decreases proportionally, holding the output amplitude constant. As the input amplitude decreases below the crossover point, the overall system gain increases proportionally, holding the output amplitude at the same constant level.

$$\text{Gain} = \frac{R_1 R_2 I_1}{2 R_3 V_{IN}(\text{avg})}$$

where: $R_1 = 6.8 \text{ k}\Omega$ (Internal)
 $R_2 = 3.3 \text{ k}\Omega$
 $R_3 = 17.3 \text{ k}\Omega$
 $I_1 = 140 \text{ }\mu\text{A}$

The output DC level can be set using the following equation:

$$V_{OUT \text{ DC}} = \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) V_{REF}$$

where: $R_4 = 100 \text{ k}\Omega$
 $R_{DC1} = R_{DC2} = 9.1 \text{ k}\Omega$
 $V_{REF} = 2.5 \text{ V}$

The output level is calculated using the following equation:

$$V_{OUT_LEVEL} = \frac{R_1 R_2 I_1}{2 R_3} \left(\frac{V_{IN}}{V_{IN}(\text{avg})} \right)$$

where: $R_1 = 6.8 \text{ k}\Omega$ (Internal)
 $R_2 = 3.3 \text{ k}\Omega$
 $R_3 = 17.3 \text{ k}\Omega$
 $I_1 = 140 \text{ }\mu\text{A}$

$$\frac{V_{IN}}{V_{IN}(\text{avg})} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine waves)}$$

Note that for very low input levels, ALC may not be desired and to limit the maximum gain, resistor R_X has been added.

$$\text{Gain max.} = \frac{\left(\frac{R_1 + R_X}{V_{REF}}\right) \cdot R_2 \cdot I_B}{2 R_3}$$

$$R_X \approx ((\text{desired max gain}) \times 26 \text{ k}\Omega) - 10 \text{ k}\Omega$$

SA572

ORDERING INFORMATION

Device	Description	Package	Temperature Range	Shipping†
SA572D	16-Pin Plastic Small Outline Package	SO-16 WB	-40 to +85°C	47 Units / Rail
SA572DG	16-Pin Plastic Small Outline Package (Pb-Free)	SO-16 WB	-40 to +85°C	47 Units / Rail
SA572DR2	16-Pin Plastic Small Outline Package	SO-16 WB	-40 to +85°C	1000 / Tape & Reel
SA572DR2G	16-Pin Plastic Small Outline Package (Pb-Free)	SO-16 WB	-40 to +85°C	1000 / Tape & Reel
SA572DTB	16-Pin Thin Shrink Small Outline Package	TSSOP-16*	-40 to +85°C	96 Units / Rail
SA572DTBG	16-Pin Thin Shrink Small Outline Package	TSSOP-16*	-40 to +85°C	96 Units / Tube
SA572DTBR2	16-Pin Thin Shrink Small Outline Package	TSSOP-16*	-40 to +85°C	2500 / Tape & Reel
SA572DTBR2G	16-Pin Thin Shrink Small Outline Package	TSSOP-16*	-40 to +85°C	2500 / Tape & Reel
SA572NG	16-Pin Plastic Dual In-Line Package	PDIP-16	-40 to +85°C	25 Units / Rail
SA572NG	16-Pin Plastic Dual In-Line Package (Pb-Free)	PDIP-16	-40 to +85°C	25 Units / Rail

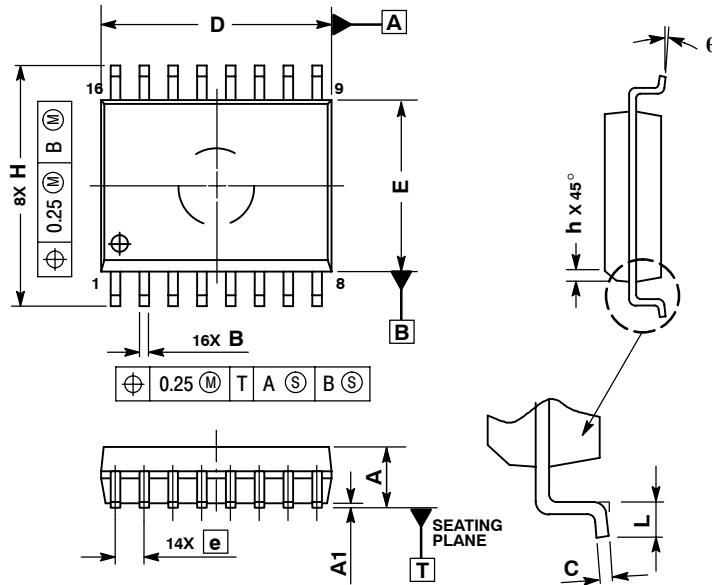
†For information on / Tape and reel specifications, including part orientation and / Tape sizes, please refer to our / Tape and Reel Packaging Specification Brochure, BRD8011/D.

*This package is inherently Pb-Free.

SA572

PACKAGE DIMENSIONS

SOIC-16 WB
D SUFFIX
CASE 751G-03
ISSUE C

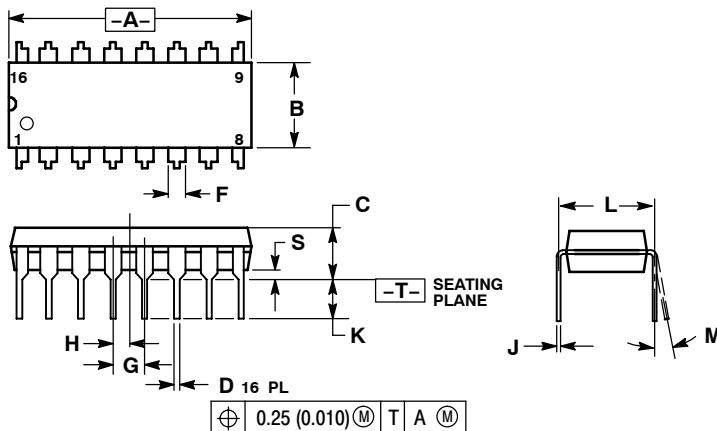


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

PDIP-16
CASE 648-08
ISSUE T



NOTES:

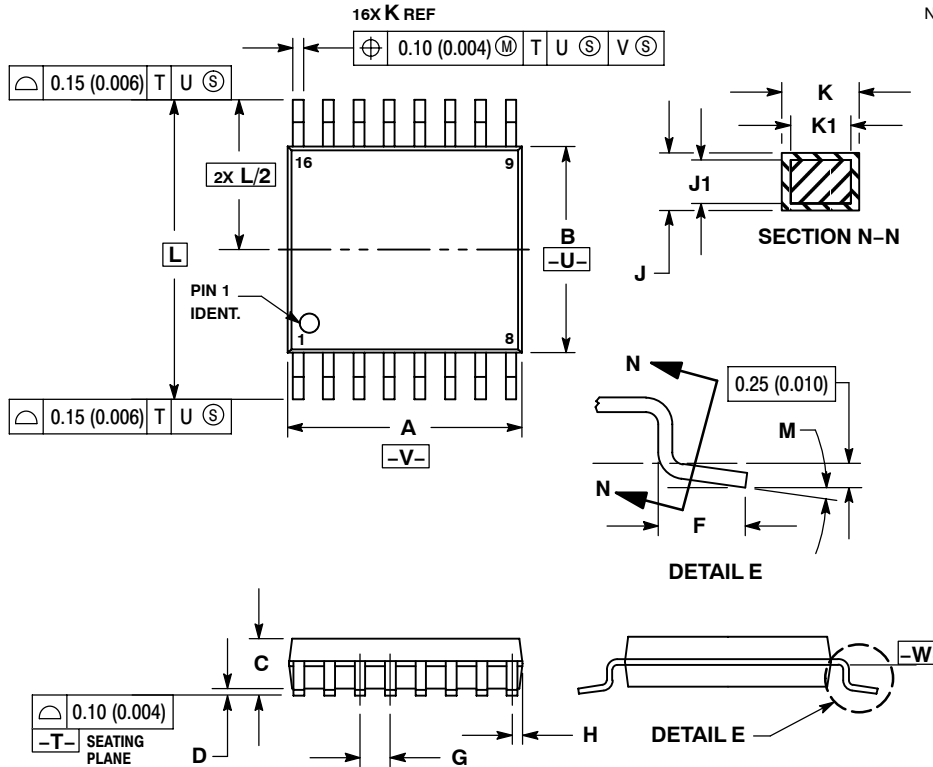
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
E	0.040	0.70	1.02	1.77
F	0.100 BSC		2.54 BSC	
G	0.050 BSC		1.27 BSC	
H	0.008	0.015	0.21	0.38
J	0.110	0.130	2.80	3.30
K	0.295	0.305	7.50	7.74
L	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SA572

PACKAGE DIMENSIONS

TSSOP-16 CASE 948F-01 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
M	0°	8°	0°	8°

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692
Email amall@ameya360.com
QQ 800077892
Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333
Email mkt@ameya360.com