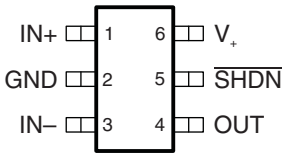
RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS

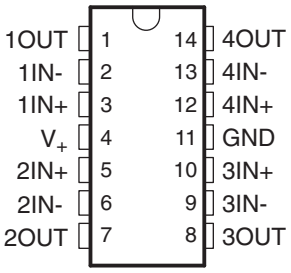
FEATURES

- **Qualified for Automotive Applications**
- **2.7-V and 5-V Performance**
- **Rail-to-Rail Output Swing**
- **Input Bias Current: 1 pA Typ**
- **Input Offset Voltage: 0.25 mV Typ**
- **Low Supply Current: 100 μA Typ**
- **Gain Bandwidth: 1 MHz Typ**
- **Slew Rate: 1 V/μs Typ**
- **Turn-On Time From Shutdown: 5 μs Typ**
- **Input Referred Voltage Noise (at 10 kHz): 20 nV/√Hz**

LMV341
DBV OR DCK PACKAGE
(TOP VIEW)



LMV344
PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The LMV341 and LMV344 devices are single and quad CMOS operational amplifiers, respectively, with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1 pA (typ) and an offset voltage of 0.25 mV (typ). The single supply amplifier is designed specifically for low-voltage (2.7 V to 5 V) operation, with a wide common-mode input voltage range that typically extends from –0.2 V to 0.8 V from the positive supply rail. Additional features are a 20-nV/√Hz voltage noise at 10 kHz, 1-MHz unity-gain bandwidth, 1-V/μs slew rate, and 100-μA current consumption per channel.

An extended industrial temperature range from –40°C to 125°C makes this device suitable for automotive applications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 125°C	SC-70 – DCK	Reel of 3000	LMV341QDCKRQ1	RR_
	SOT-23 – DBV	Reel of 3000	LMV341QDBVRQ1	RCH_
	TSSOP – PW	Reel of 2000	LMV344IPWRQ1	LMV344Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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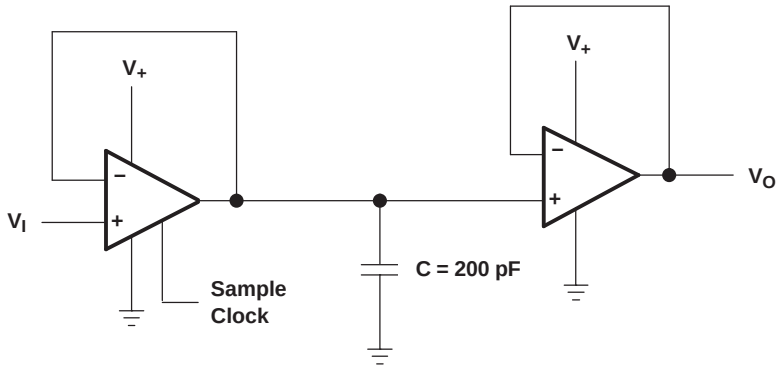
APPLICATION CIRCUIT: SAMPLE-AND-HOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_+	Supply voltage(2)		5.5 V
V_{ID}	Differential input voltage(3)		±5.5 V
V_I	Input voltage range (either input)		0 to 5.5 V
θ_{JA}	Package thermal impedance(4)(5)	DBV package	165°C/W
		DCK package	259°C/W
		PW package	113°C/W
T_J	Operating virtual junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_+ specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN−.
(4) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_+	Supply voltage (single-supply operation)	2.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

ESD PROTECTION

TEST CONDITIONS	TYP	UNIT
Human-Body Model (HBM)	2000	V
Machine Model (MM)	200	V

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ELECTRICAL CHARACTERISTICS

V_+ = 2.7 V, GND = 0 V, $V_{IC} = V_O = V_+/2$, R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV341			LMV344			UNIT
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IO}	Input offset voltage			25°C		0.25	4		0.25	4	mV
				Full range			4.5			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.7			1.7		µV/°C
I_{IB}	Input bias current			25°C		1	120		1	120	pA
				–40°C to 85°C			250			250	
				–40°C to 125°C			3			3	nA
I_{IO}	Input offset current			25°C		6.6			6.6		fA
CMRR	Common-mode rejection ratio	0 ≤ V_{ICR} ≤ 1.7 V		25°C	40	80		56	80		dB
		0 ≤ V_{ICR} ≤ 1.6 V		Full range	36			50			
k_{SVR}	Supply-voltage rejection ratio	2.7 V ≤ V_+ ≤ 5 V		25°C	45	82		65	82		dB
				Full range	60			60			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0	–0.2 to 1.9	1.7	0	–0.2 to 1.9	1.7	V
A_V	Large-signal voltage gain(2)	R_L = 10 kΩ to 1.35 V		25°C	73	113		78	113		dB
				Full range	66			70			
		R_L = 2 kΩ to 1.35 V		25°C	70	103		72	103		
				Full range	63			64			
V_O	Output swing (delta from supply rails)	R_L = 2 kΩ to 1.35 V	Low level	25°C		24	60		24	60	mV
				Full range			95			95	
			High level	25°C		26	60		26	60	
				Full range			95			95	
		R_L = 10 kΩ to 1.35 V	Low level	25°C		5	30		5	30	
				Full range			40			40	
			High level	25°C		5.3	30		5.3	30	
				Full range			40			40	
I_{CC}	Supply current (per channel)			25°C		100	170		100	170	µA
				Full range			230			230	
I_{OS}	Output short- circuit current	Sourcing		25°C	20	32		18	24		mA
		Sinking			15	24		15	24		
SR	Slew rate	R_L = 10 kΩ(3)		25°C		1			1		V/µs
GBM	Unity-gain bandwidth	R_L = 10 kΩ, C_L = 200 pF		25°C		1			1		MHz
Φ_m	Phase margin	R_L = 100 kΩ		25°C		72			72		deg
G_m	Gain margin	R_L = 100 kΩ		25°C		20			20		dB
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		40			40		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.001			0.001		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_I = 1 V_{PP}		25°C		0.017			0.017		%

(1) Typical values represent the most likely parametric norm.
(2) GND + 0.2 V ≤ V_O ≤ V_+ – 0.2 V
(3) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

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SHUTDOWN CHARACTERISTICS

V_+ = 2.7 V, GND = 0 V, V_{IC} = V_O = V_+/2, R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	V_{SD} = 0 V	25°C		0.045	1000	nA
			Full range			1.5	µA
$t_{(on)}$	Amplifier turn-on time		25°C		5		µs
V_{SD}	Shutdown pin voltage range	ON mode	25°C		1.7 to 2.7	2.4 to 2.7	V
		Shutdown mode			0 to 1	0 to 0.8	

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ELECTRICAL CHARACTERISTICS

V_+ = 5 V, GND = 0 V, $V_{IC} = V_O = V_+/2$, R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	LMV341			LMV344			UNIT
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IO}	Input offset voltage			25°C		0.25	4		0.25	4	mV
				Full range			4.5			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.9			1.9		µV/°C
I_{IB}	Input bias current			25°C		1	200		1	200	pA
				–40°C to 85°C			375			375	
				–40°C to 125°C			5			5	nA
I_{IO}	Input offset current			25°C		6.6			6.6		fA
CMRR	Common-mode rejection ratio	0 ≤ V_{ICR} ≤ 4 V		25°C	46	86		56	86		dB
		0 ≤ V_{ICR} ≤ 3.9 V		Full range	47			50			
k_{SVR}	Supply-voltage rejection ratio	2.7 V ≤ V_+ ≤ 5 V		25°C	45	82		65	82		dB
				Full range	44			60			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0	–0.2 to 4.2	4	0	–0.2 to 4.2	4	V
A_V	Large-signal voltage gain(2)	R_L = 10 kΩ to 2.5 V		25°C	78	116		78	116		dB
				Full range	70			70			
		R_L = 2 kΩ to 2.5 V		25°C	72	107		72	107		
				Full range	64			64			
V_O	Output swing (delta from supply rails)	R_L = 2 kΩ to 2.5 V	Low level	25°C		32	67		32	60	mV
				Full range			95			95	
			High level	25°C		34	60		34	60	
				Full range			95			95	
		R_L = 10 kΩ to 2.5 V	Low level	25°C		7	30		7	30	
				Full range			45			40	
			High level	25°C		7	30		7	30	
				Full range			40			40	
I_{CC}	Supply current (per channel)			25°C		107	200		107	200	µA
				Full range			260			260	
I_{OS}	Output short-circuit current	Sourcing		25°C	85	113		70	90		mA
		Sinking			50	75		50	75		
SR	Slew rate	R_L = 10 kΩ(3)		25°C		1			1		V/µs
GBM	Unity-gain bandwidth	R_L = 10 kΩ, C_L = 200 pF		25°C		1			1		MHz
Φ_m	Phase margin	R_L = 100 kΩ		25°C		70			70		deg
G_m	Gain margin	R_L = 100 kΩ		25°C		20			20		dB
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		39			39		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.001			0.001		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_I = 1 V_{PP}		25°C		0.012			0.012		%

(1) Typical values represent the most likely parametric norm.
(2) GND + 0.2 V ≤ V_O ≤ V_+ – 0.2 V
(3) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

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SHUTDOWN CHARACTERISTICS

V_+ = 5 V, GND = 0 V, V_{IC} = V_O = V_+/2, R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	V_{SD} = 0 V	25°C		0.033	1	µA
			Full range			1.5	
$t_{(on)}$	Amplifier turn-on time		25°C		5		µs
V_{SD}	Shutdown pin voltage range	ON mode	25°C		3.1 to 5	4.5 to 5	V
		Shutdown mode			0 to 1	0 to 0.8	

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TYPICAL CHARACTERISTICS

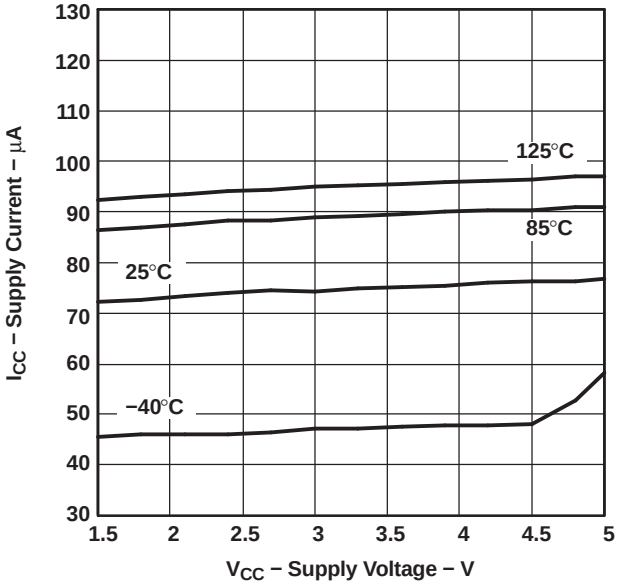
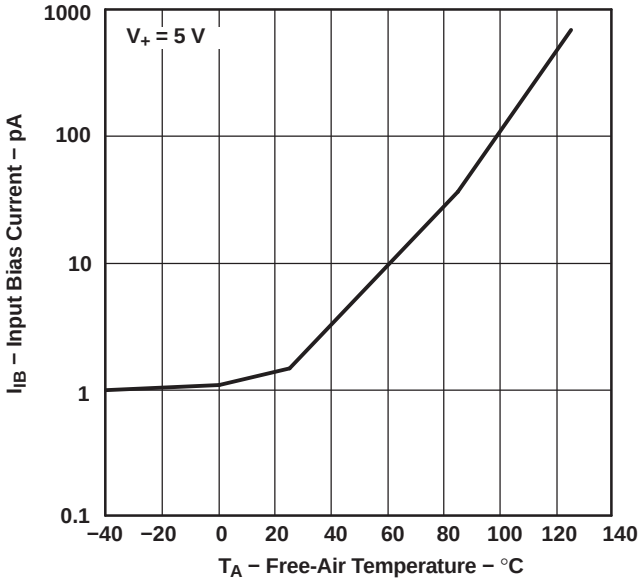


Figure 1.



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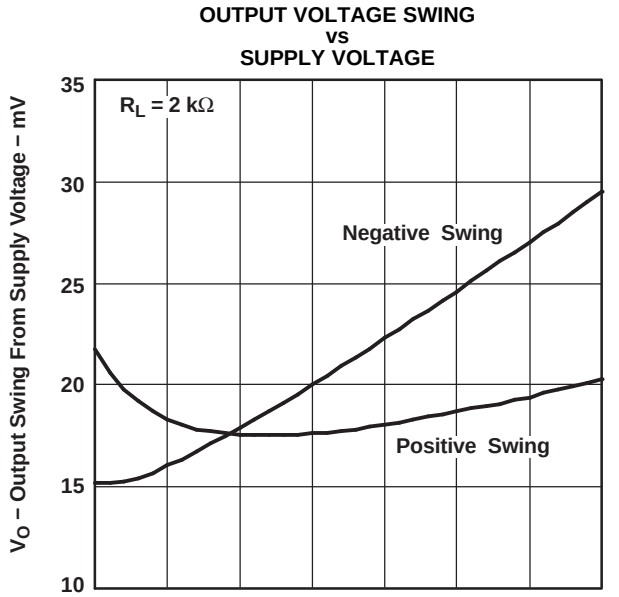

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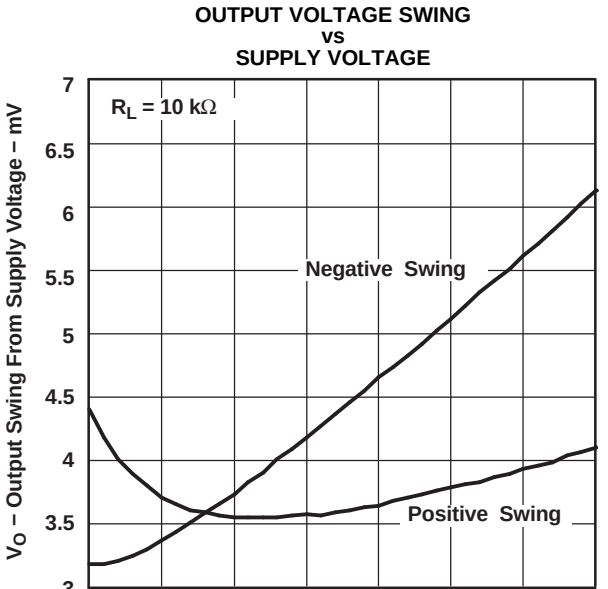

Figure 4.

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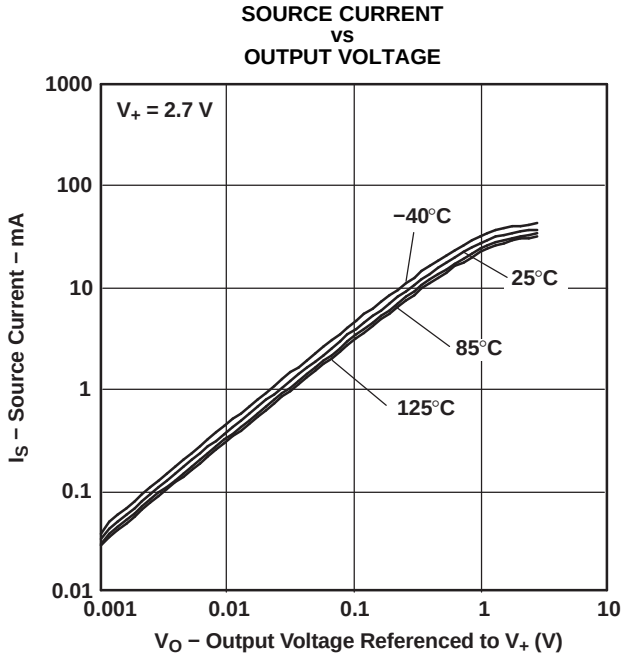
TYPICAL CHARACTERISTICS (continued)



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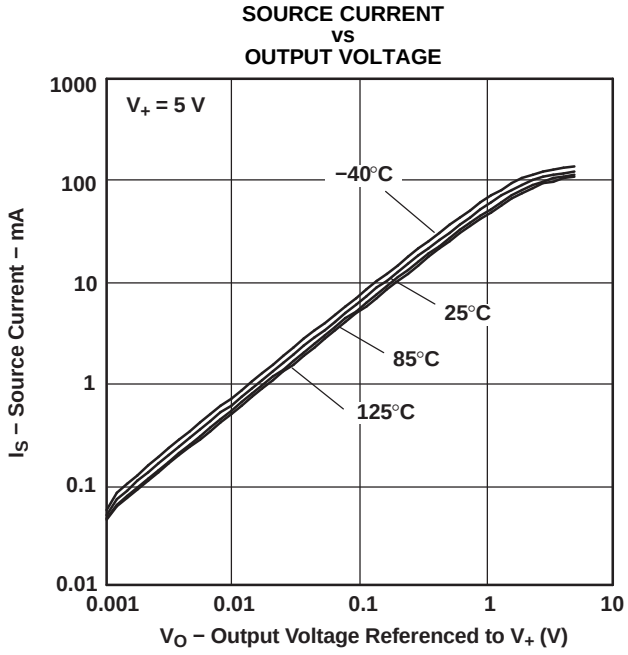

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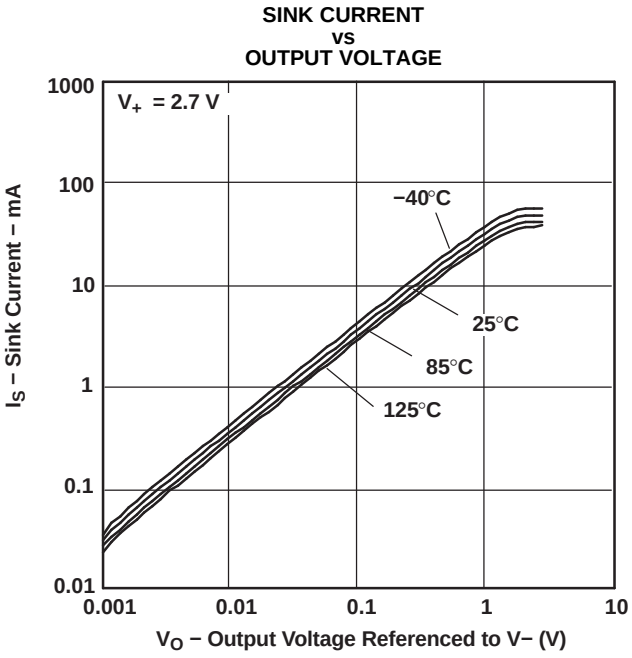

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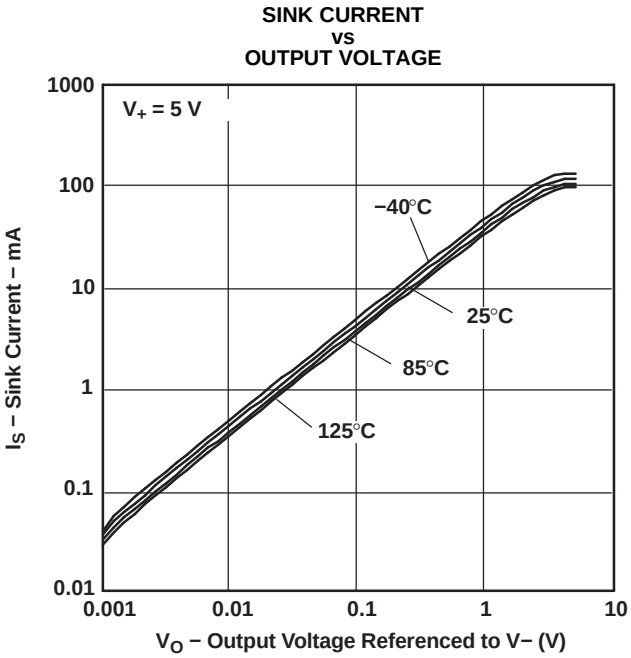

Figure 8.

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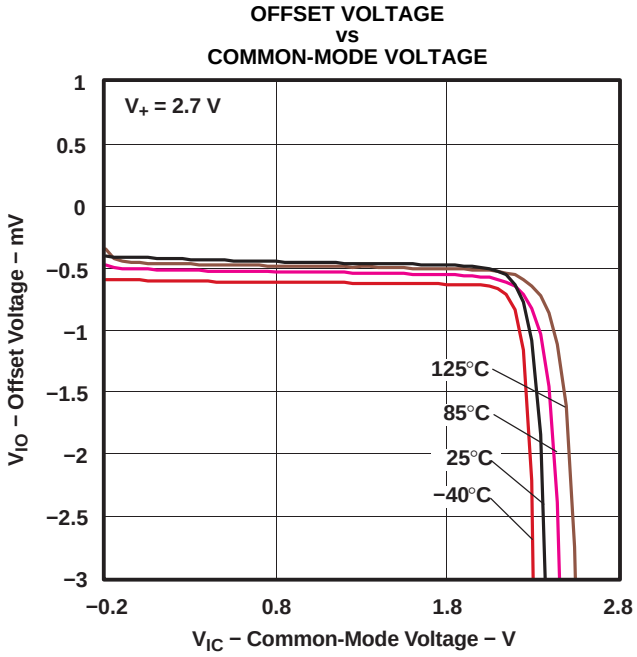
TYPICAL CHARACTERISTICS (continued)



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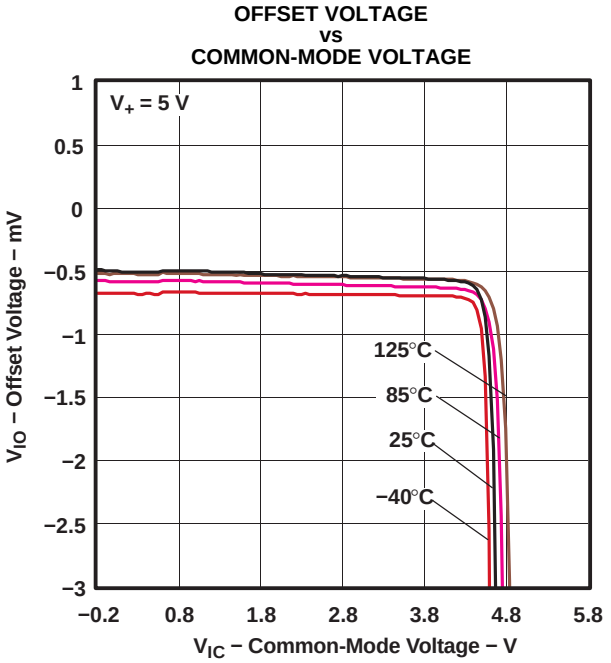

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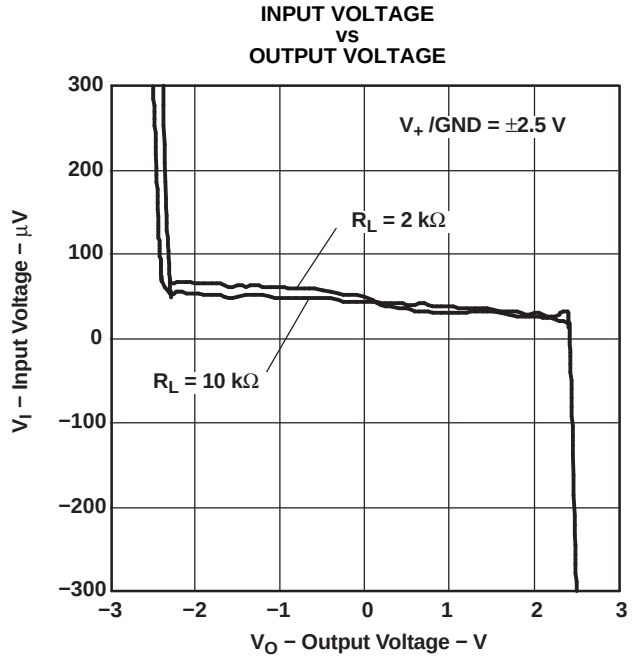

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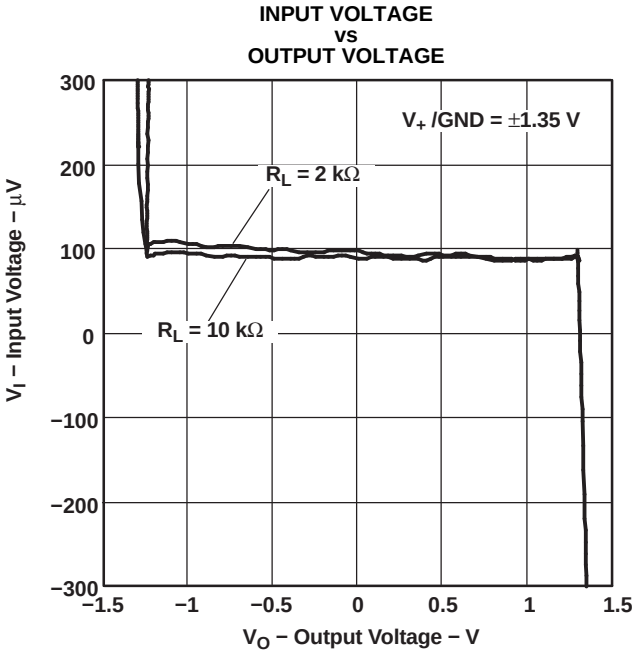

Figure 12.

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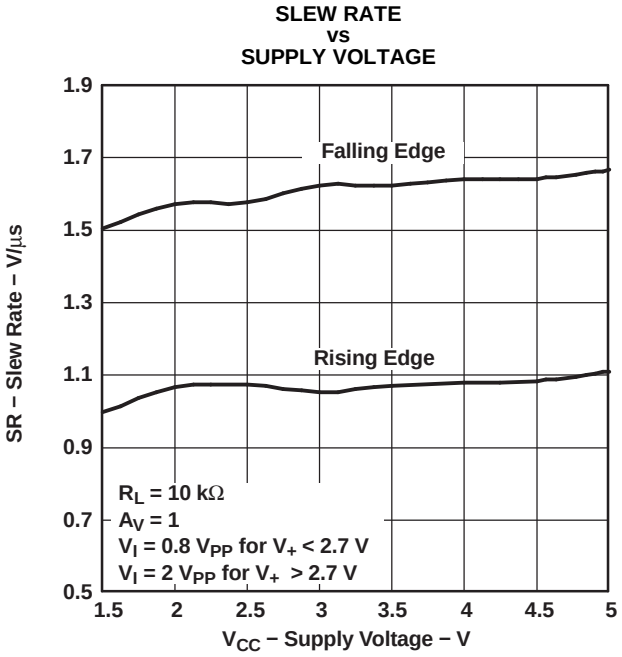
TYPICAL CHARACTERISTICS (continued)



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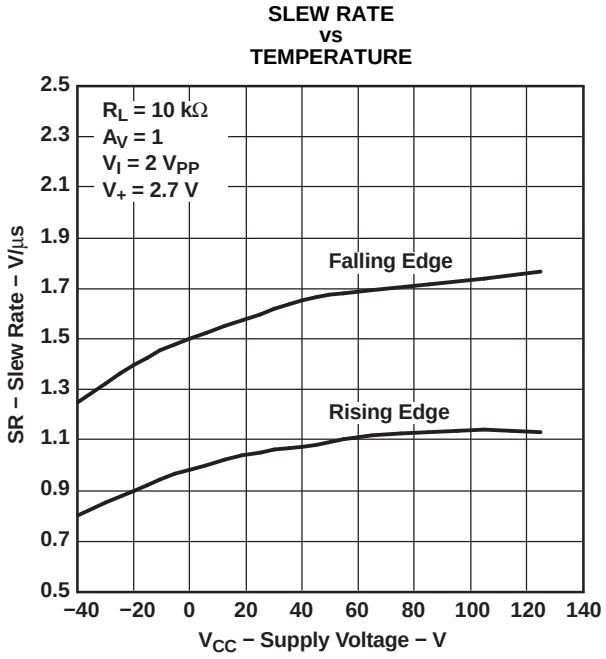

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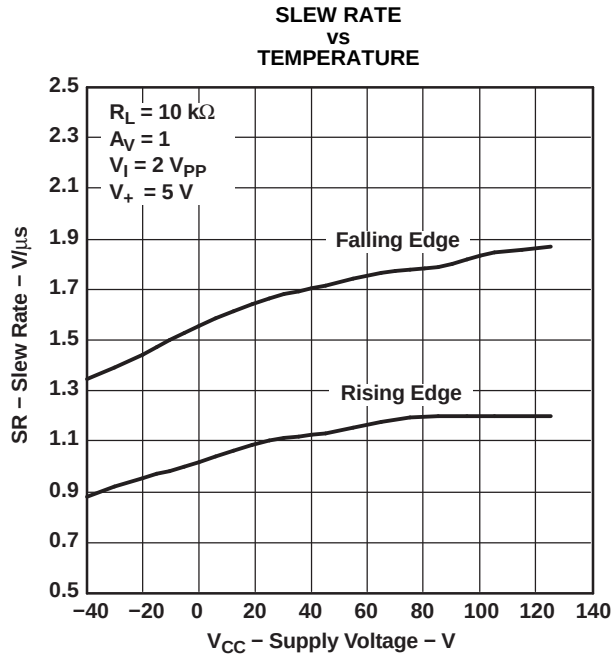

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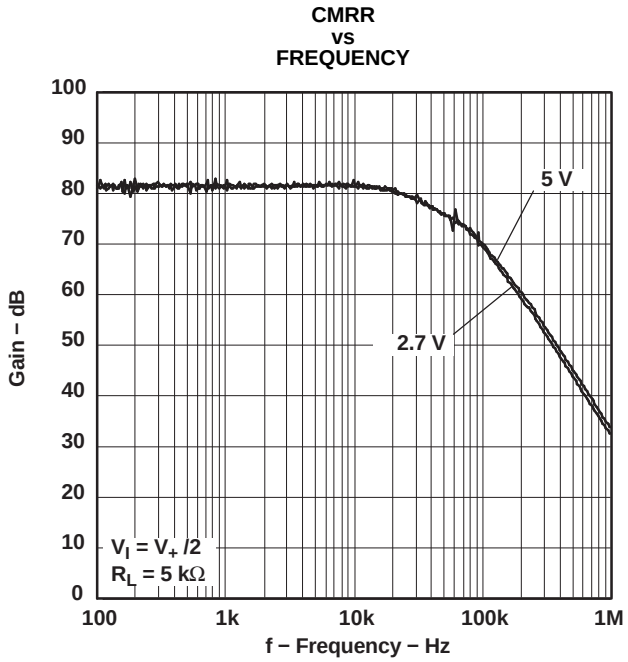

Figure 16.

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TYPICAL CHARACTERISTICS (continued)

PSRR
vs
FREQUENCY

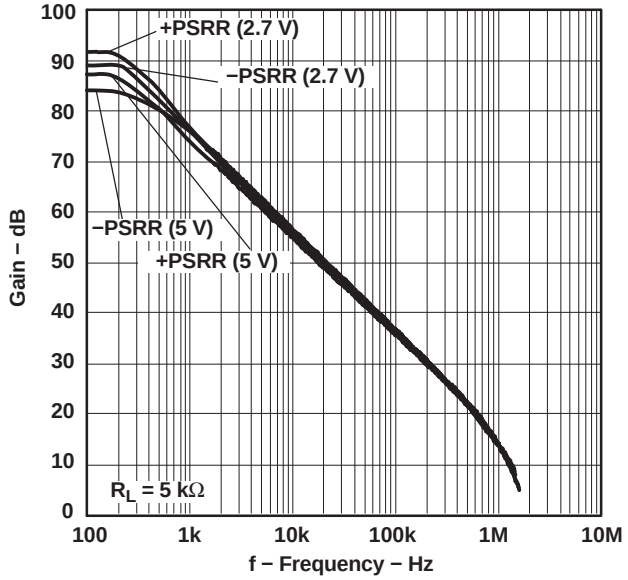

Figure 17.

INPUT VOLTAGE NOISE
vs
FREQUENCY

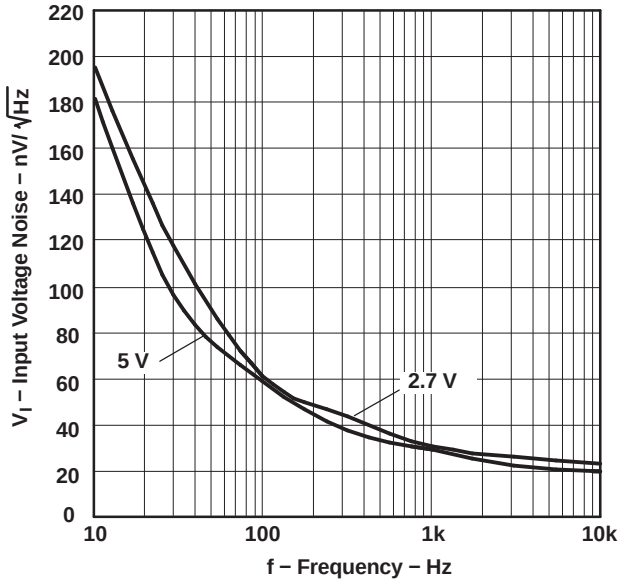

Figure 18.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

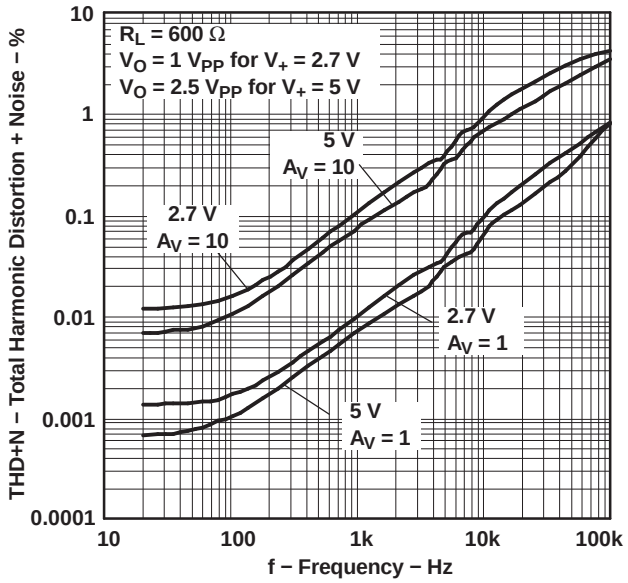

Figure 19.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT VOLTAGE

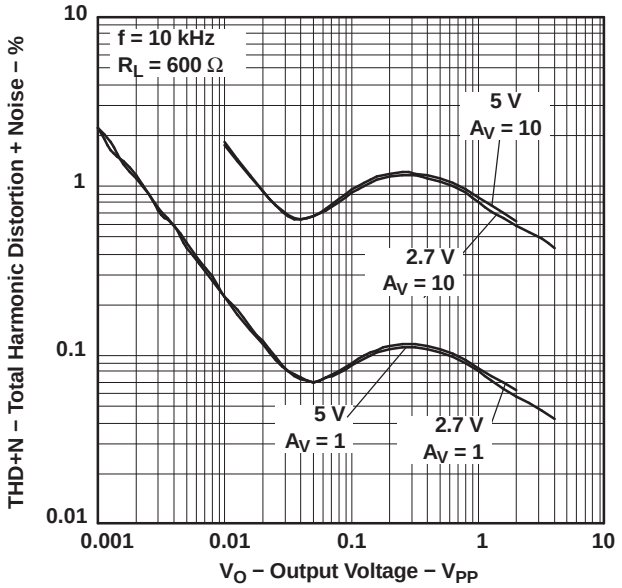

Figure 20.

TYPICAL CHARACTERISTICS (continued)

GAIN AND PHASE MARGIN vs FREQUENCY (T_A = –40°C, 25°C, 125°C)

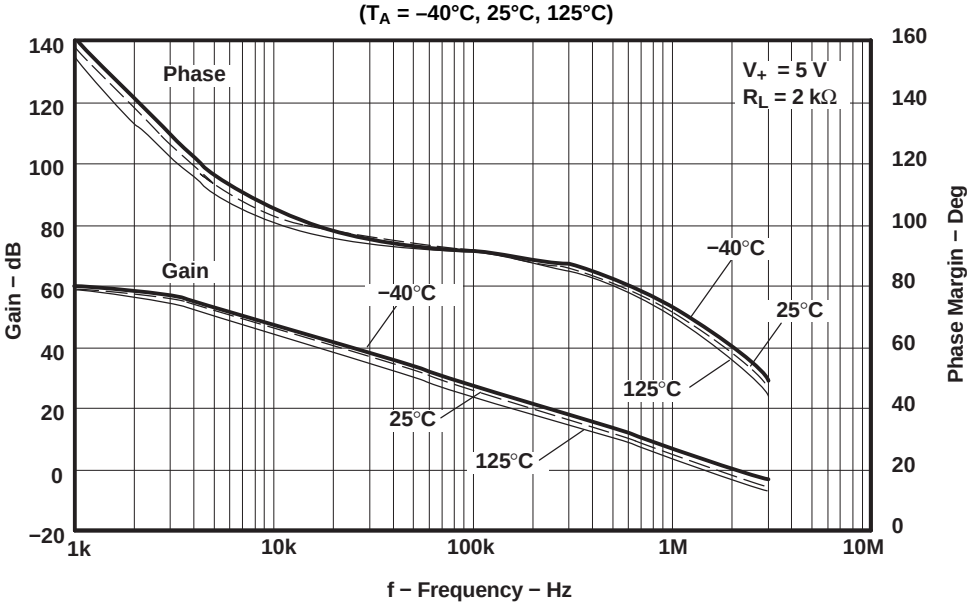

Figure 21.

GAIN AND PHASE MARGIN vs FREQUENCY (R_L = 600 Ω, 2 kΩ, 100 kΩ)

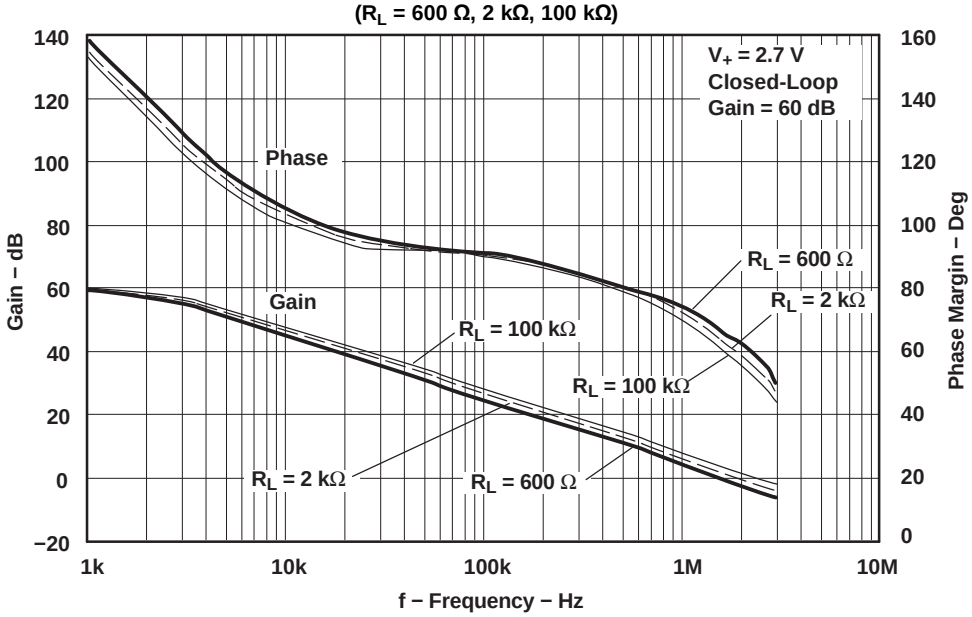

Figure 22.

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TYPICAL CHARACTERISTICS (continued)

GAIN AND PHASE MARGIN vs FREQUENCY (R_L = 600 Ω, 2 kΩ, 100 kΩ)

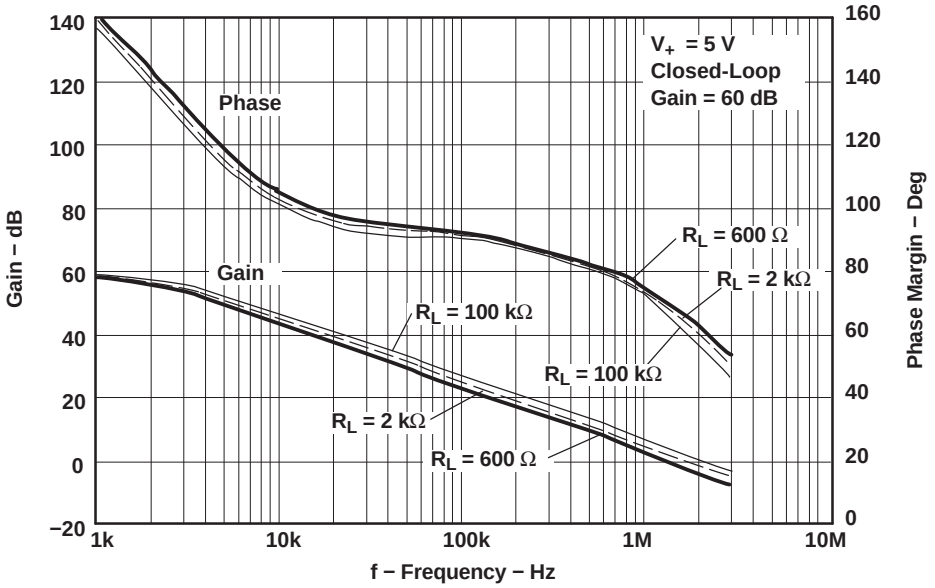

Figure 23.

GAIN AND PHASE MARGIN vs FREQUENCY (C_L = 0 pF, 100 pF, 500 pF, 1000 pF)

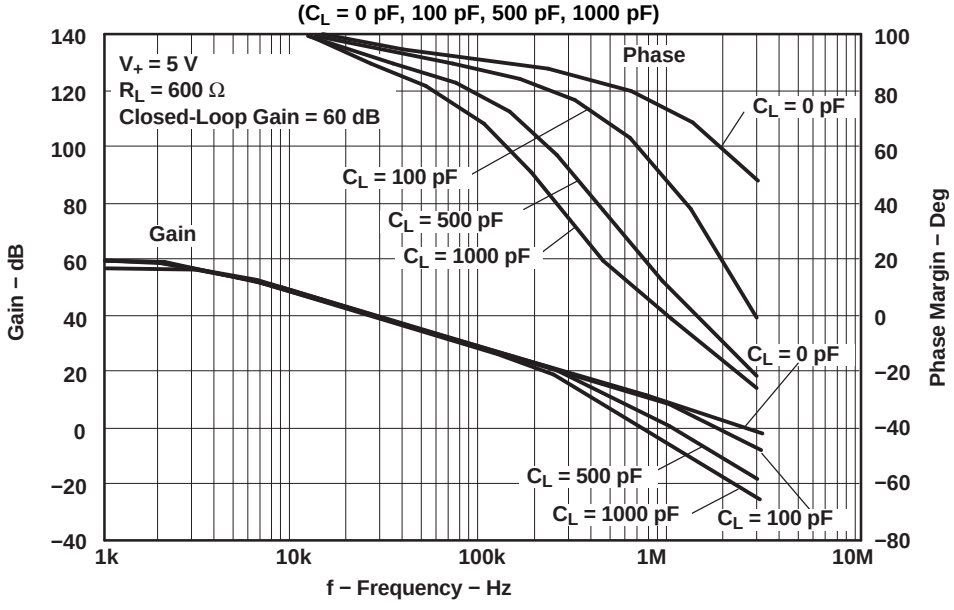

Figure 24.

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TYPICAL CHARACTERISTICS (continued)

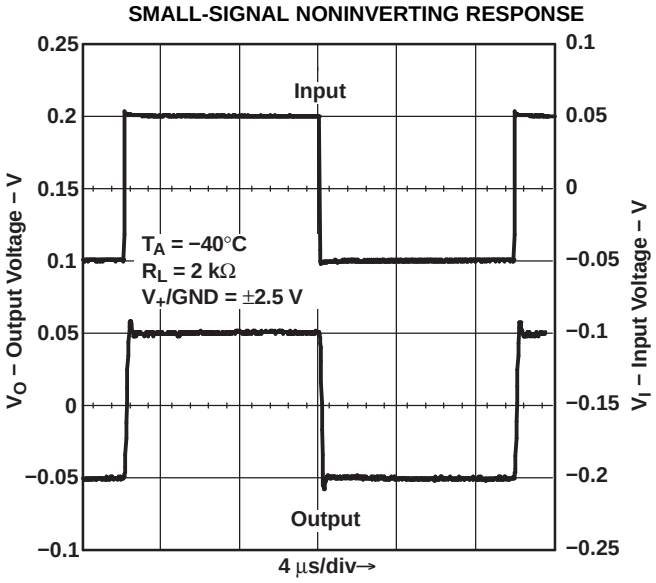

Figure 25.

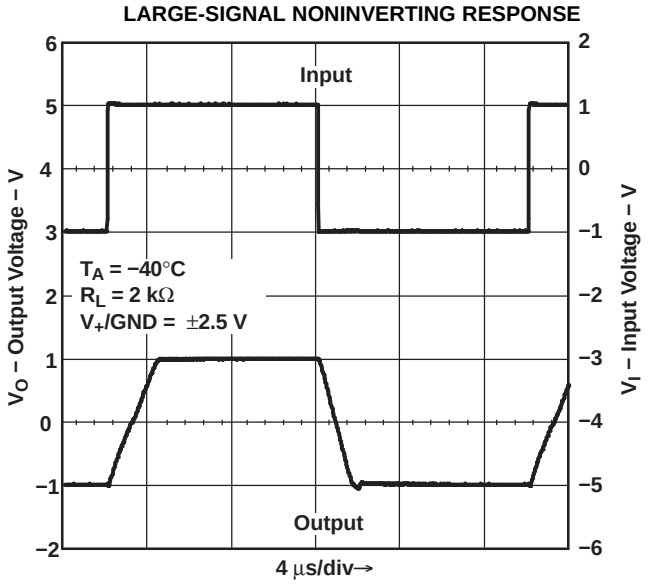

Figure 26.

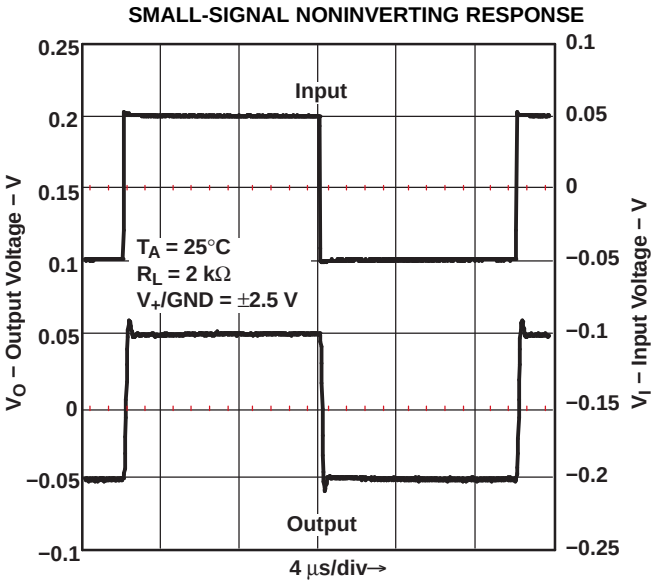

Figure 27.

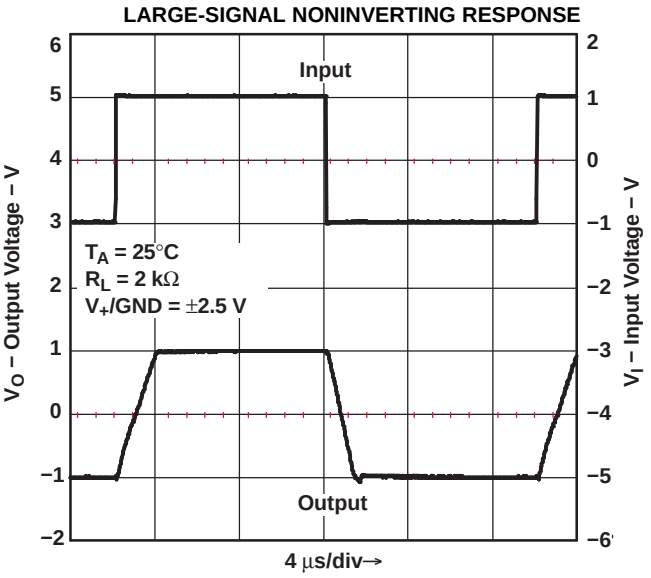

Figure 28.

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TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL NONINVERTING RESPONSE

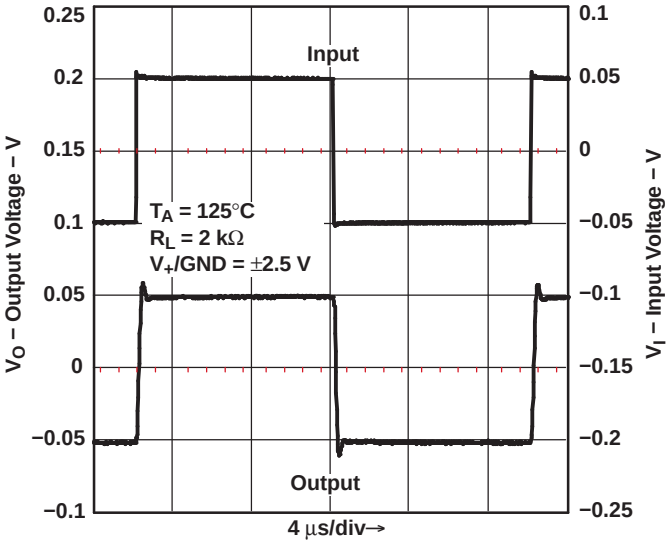

Figure 29.

LARGE-SIGNAL NONINVERTING RESPONSE

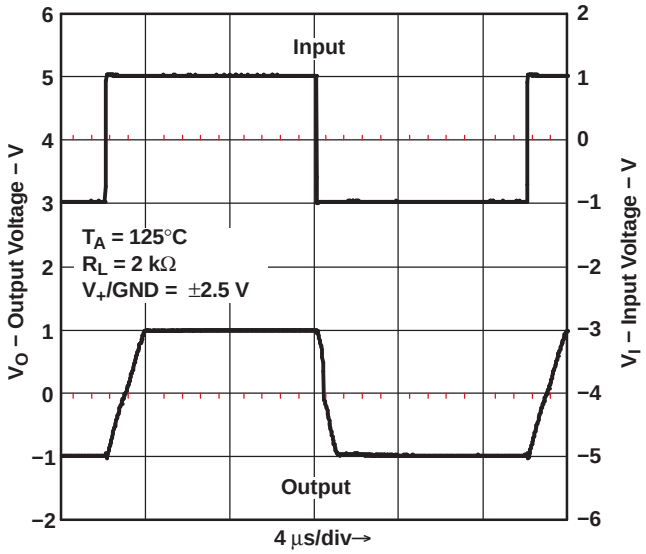

Figure 30.

SMALL-SIGNAL INVERTING RESPONSE

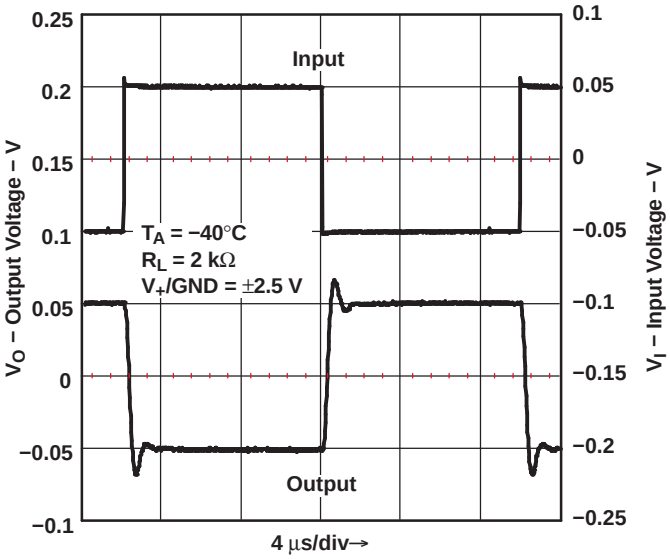

Figure 31.

LARGE-SIGNAL INVERTING RESPONSE

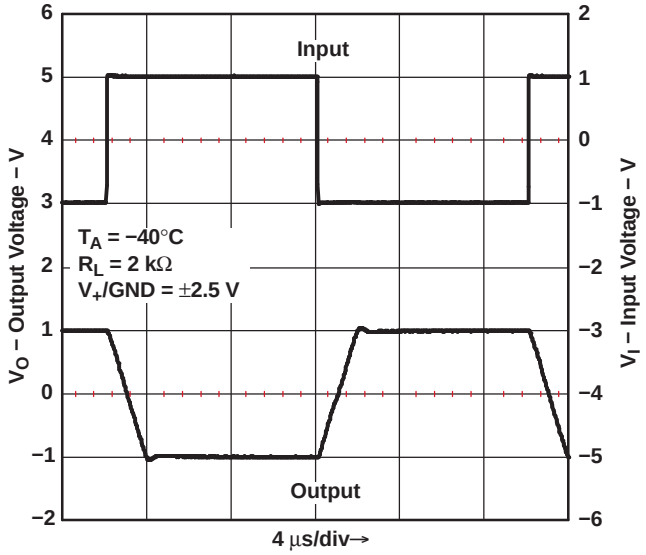

Figure 32.

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TYPICAL CHARACTERISTICS (continued)

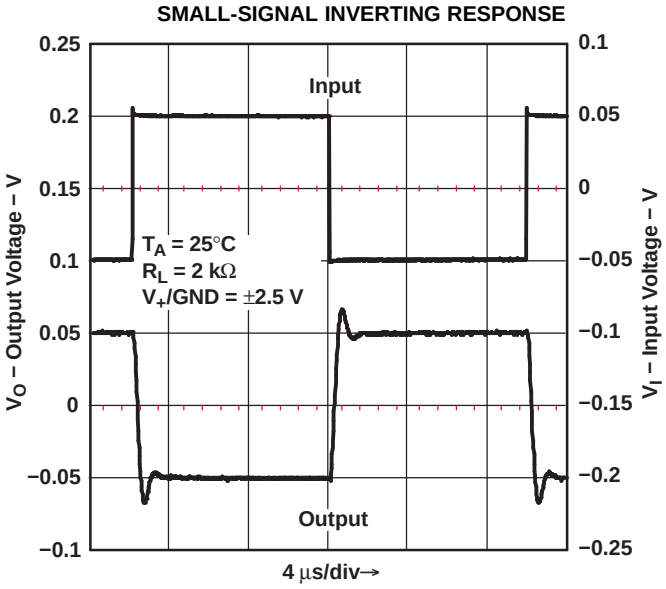

Figure 33.

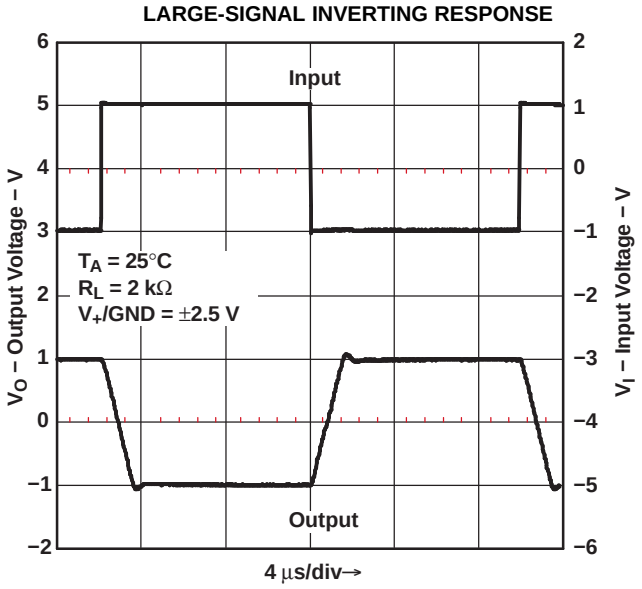

Figure 34.

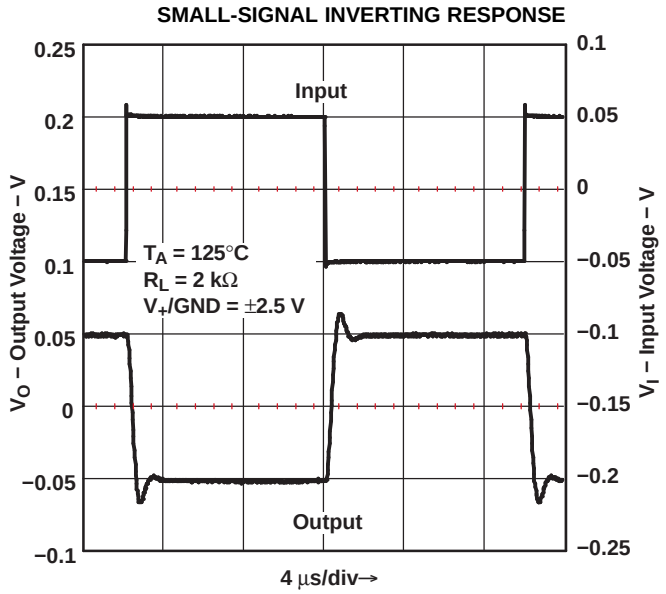

Figure 35.

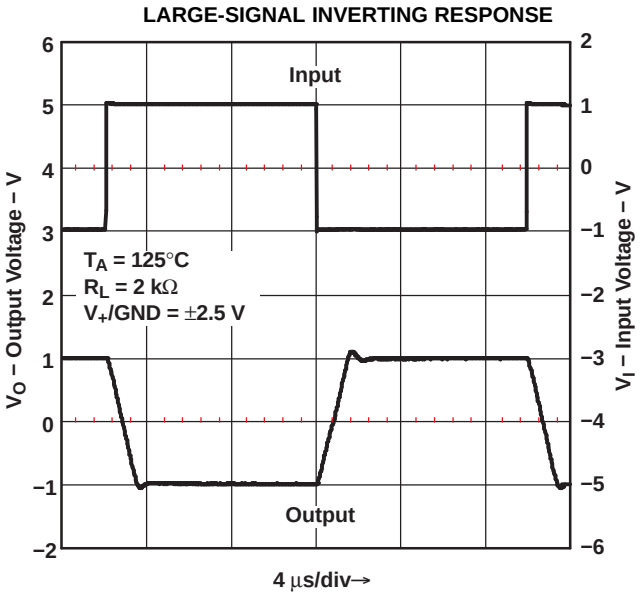

Figure 36.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV341QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RCHE	Samples
LMV341QDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RRE	Samples
LMV344IPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LMV344Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF LMV341-Q1, LMV344-Q1 :

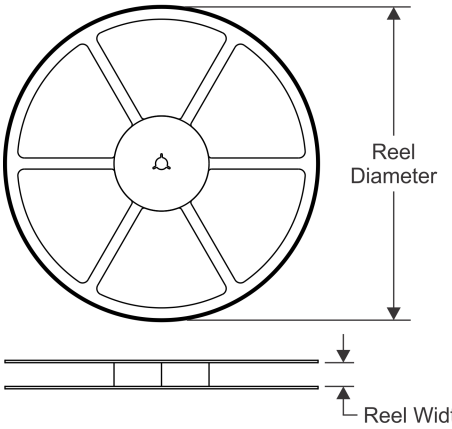
- Catalog: LMV341, LMV344

NOTE: Qualified Version Definitions:

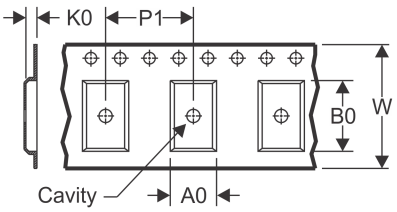
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

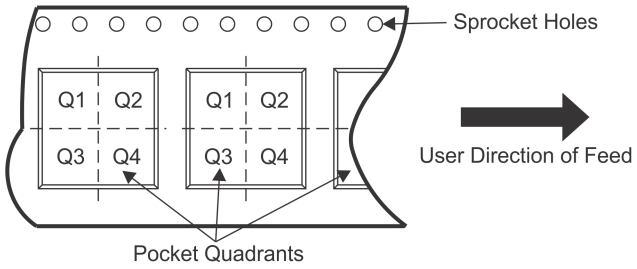


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

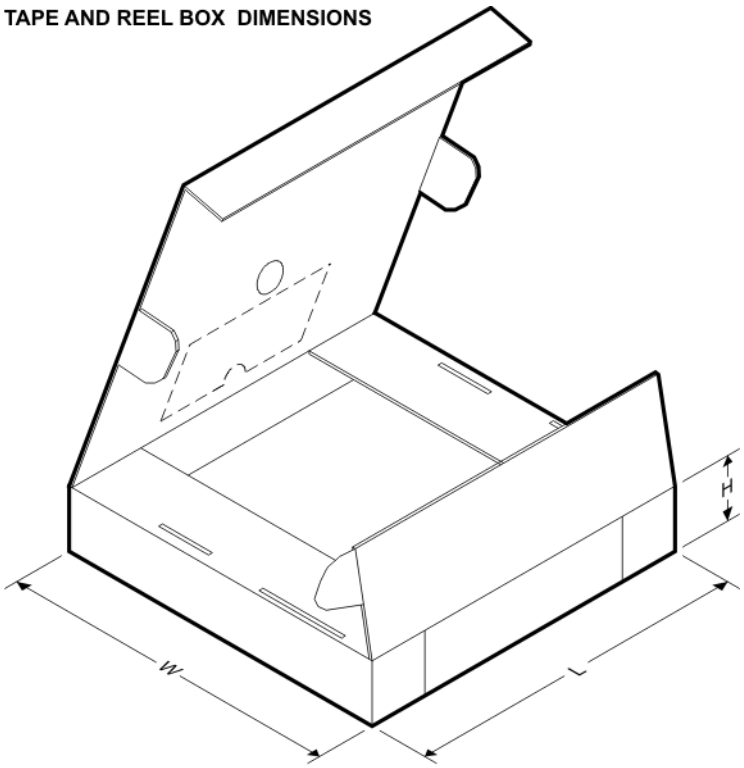
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV341QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV341QDCKRQ1	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV344IPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

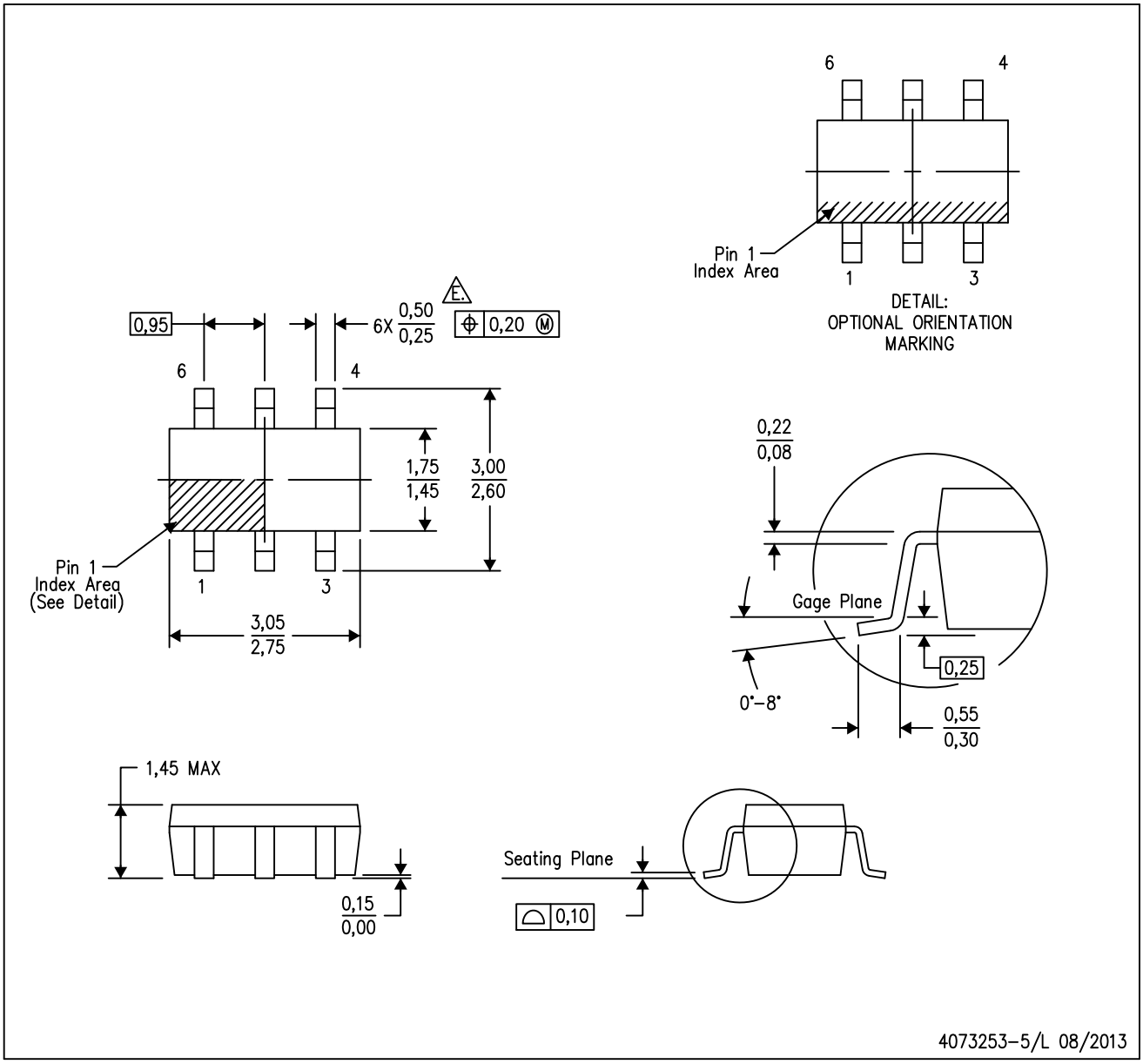
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

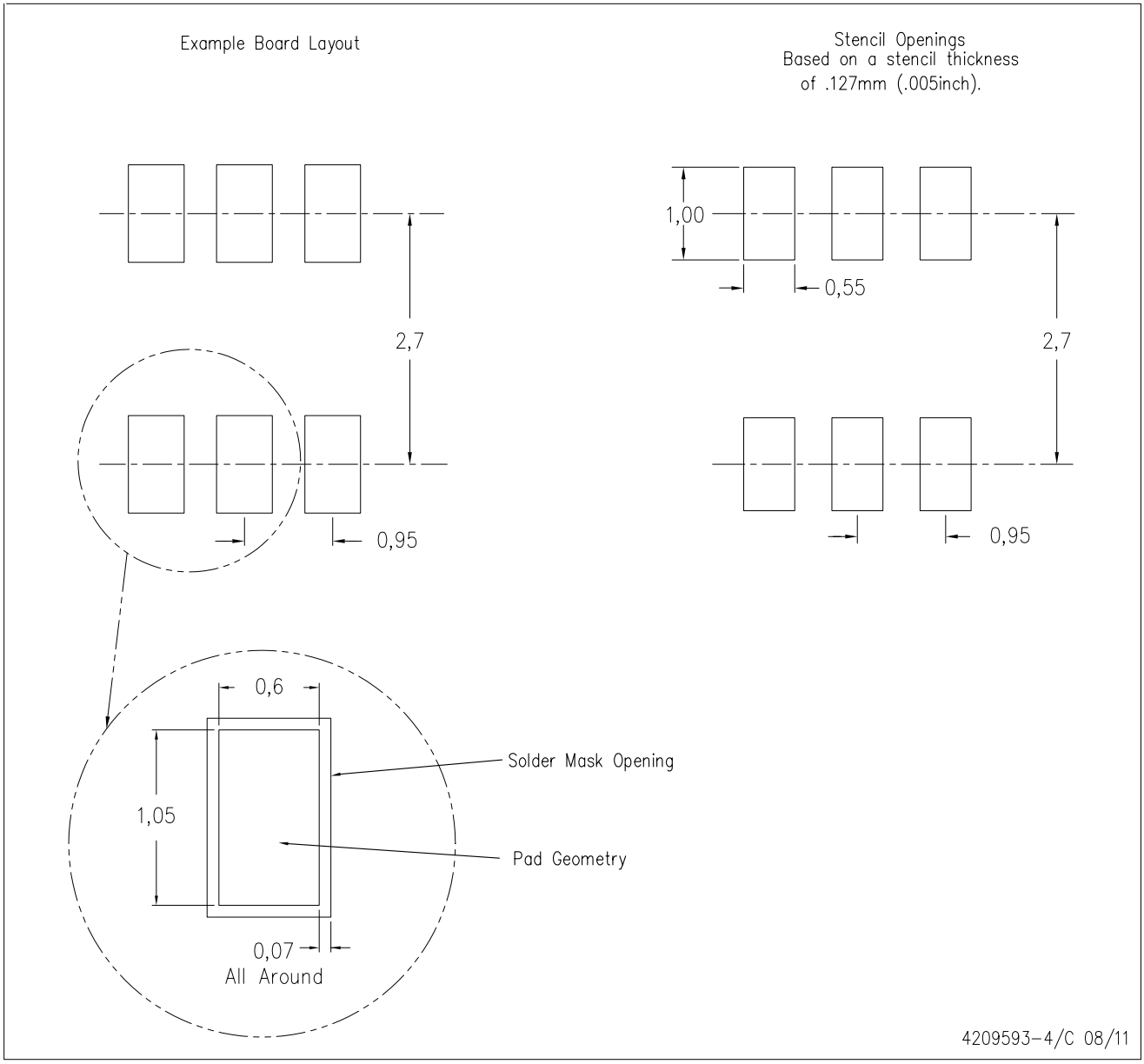
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV341QDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0
LMV341QDCKRQ1	SC70	DCK	6	3000	203.0	203.0	35.0
LMV344IPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



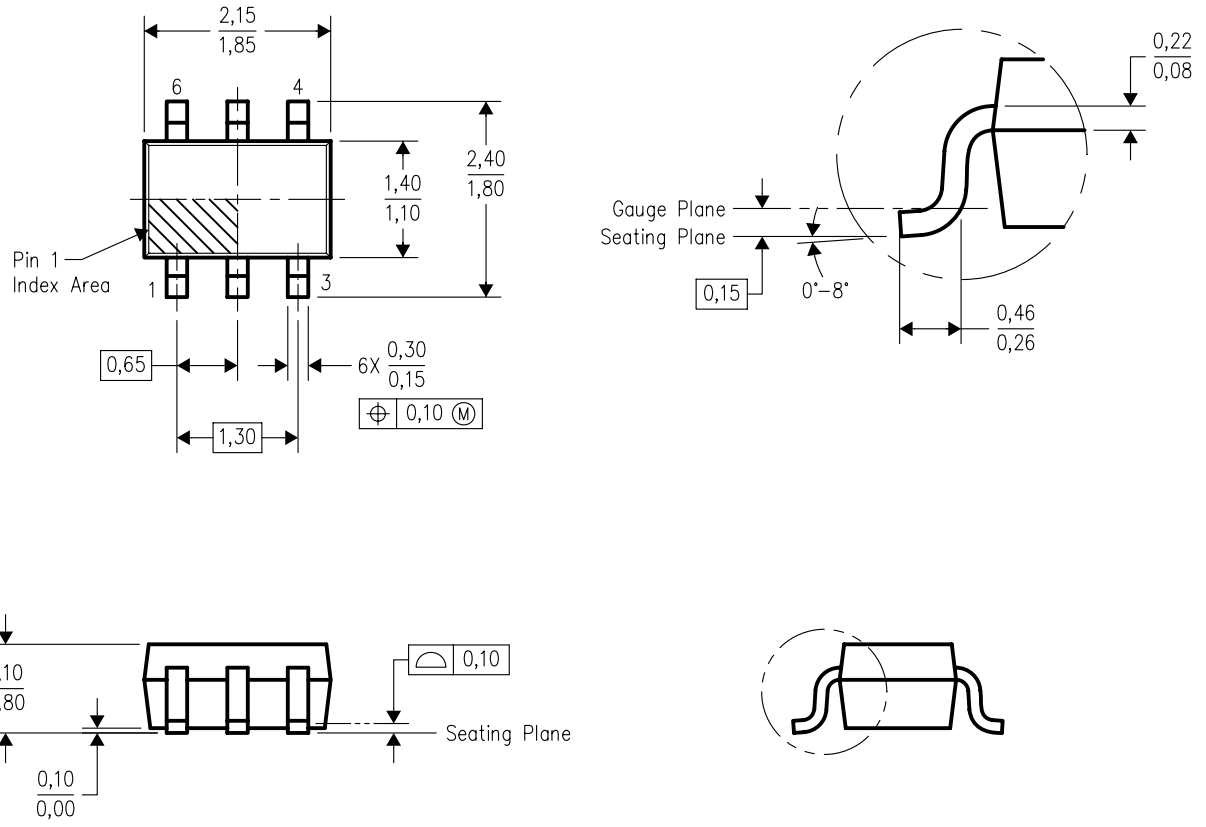
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

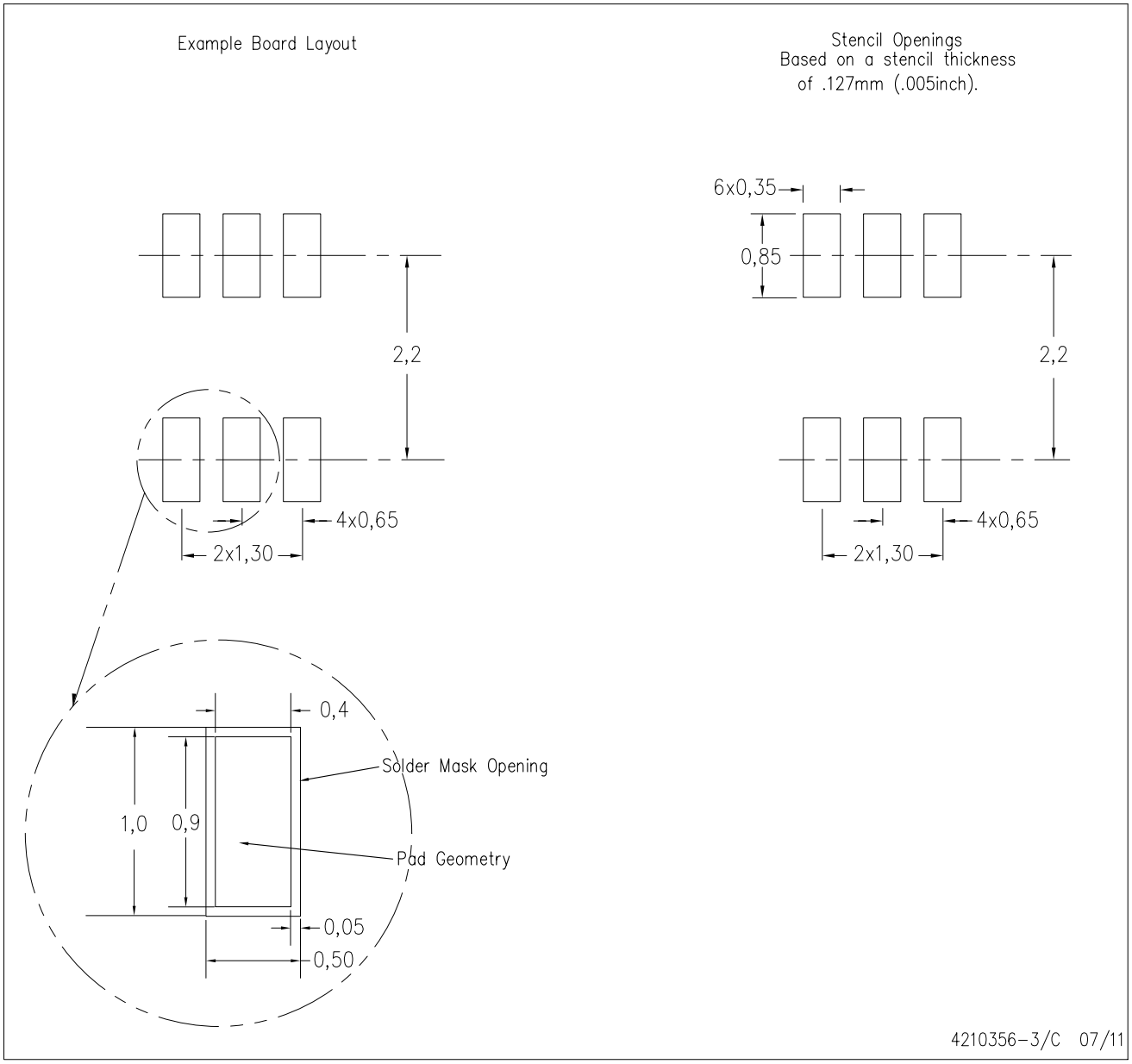
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

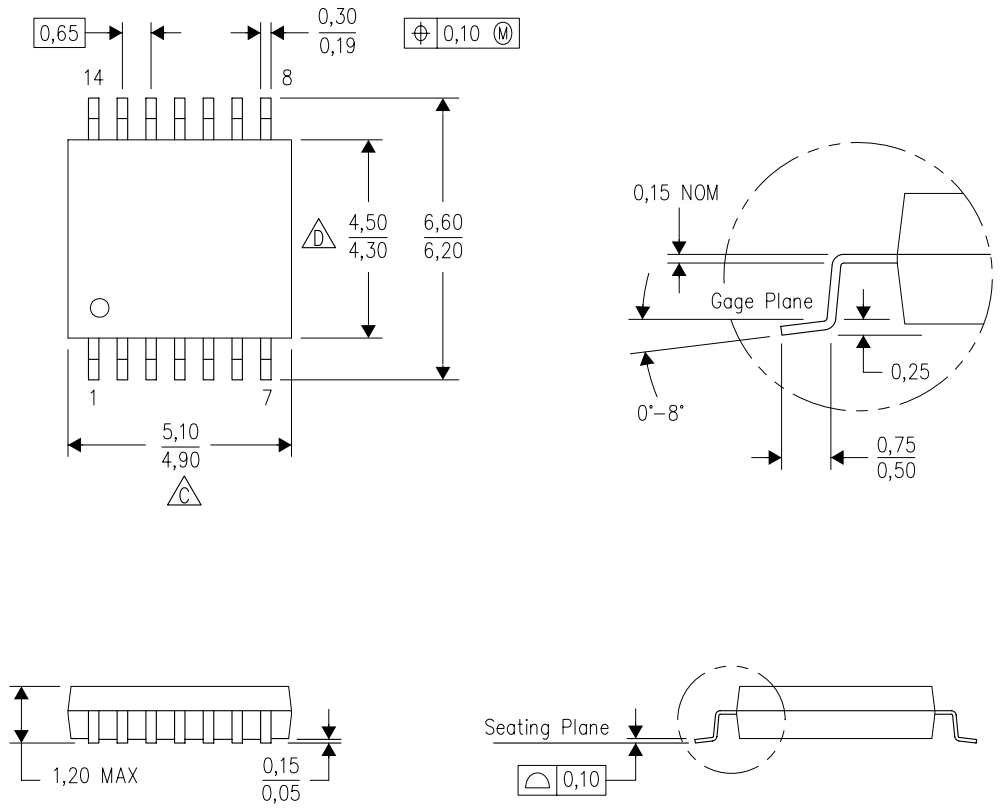
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

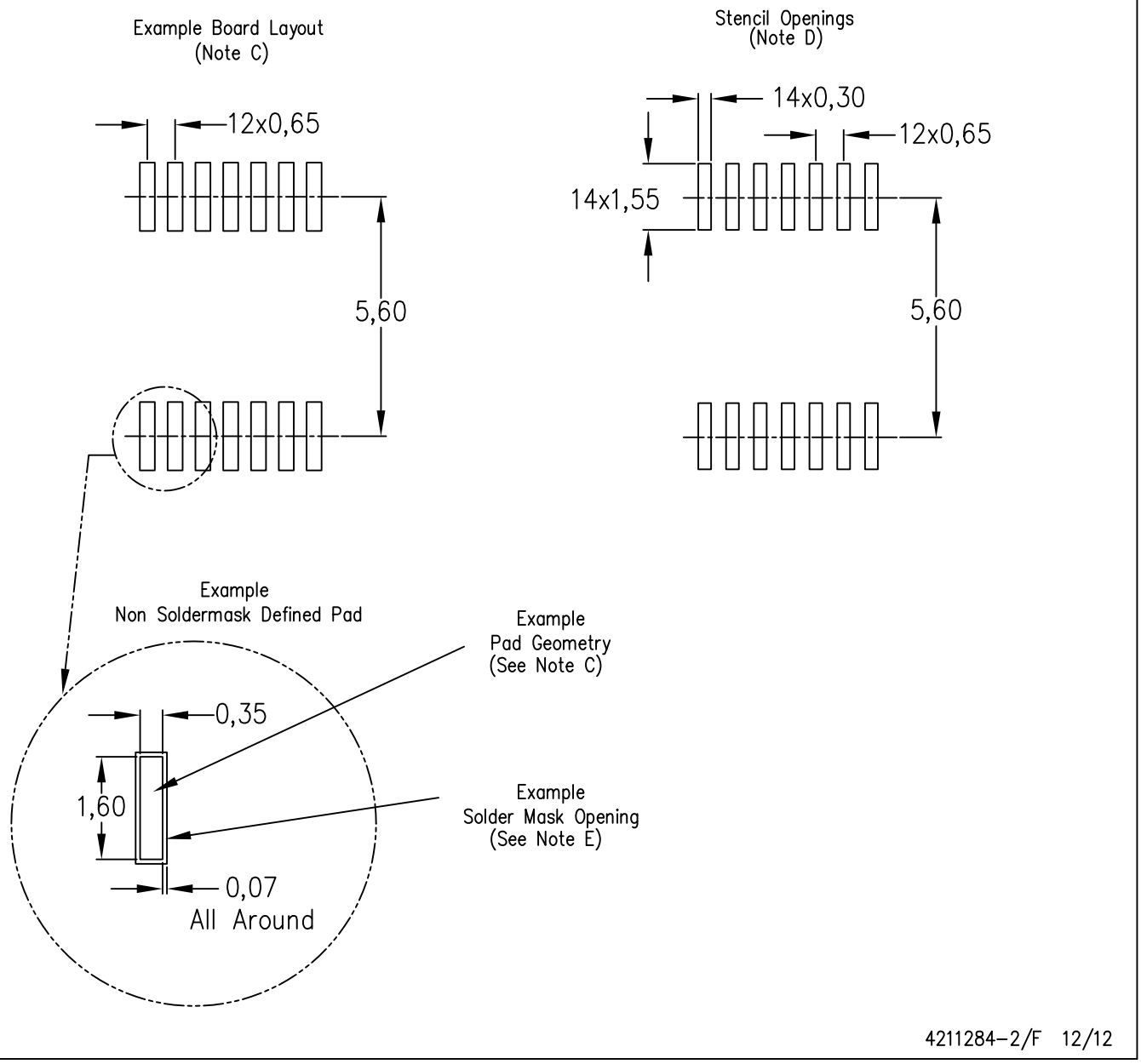
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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