

DATA SHEET

74AVCM162834

18-bit registered driver
with inverted register enable and
15 Ω termination resistors (3-State)

Product specification

2001 Apr 20

File under Integrated Circuits ICL03

18-bit registered driver with inverted register enable and 15 Ω termination resistors (3-State)

74AVCM162834

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A/5/7.
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Integrated 15 Ω termination resistors to minimize output overshoot and undershoot
- Full PC133 solution provided when used with PCK2510S and CBT16292

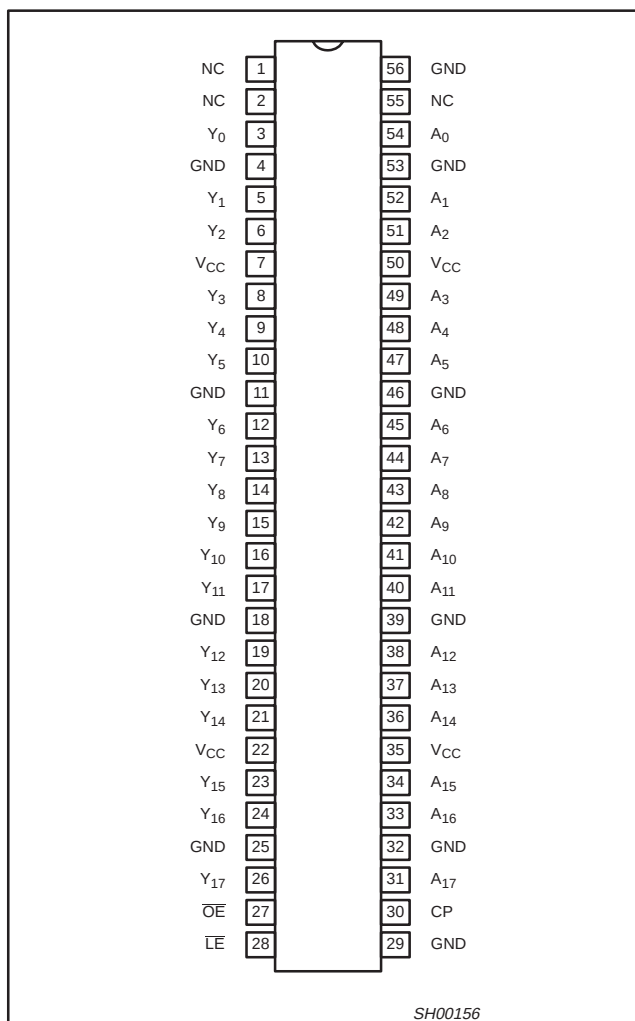
DESCRIPTION

The 74AVCM162834 is an 18-bit universal bus driver. Data flow is controlled by output enable ($\overline{OE}$), latch enable ($\overline{LE}$) and clock inputs (CP).

This product is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor (Live Insertion).

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.0\text{ ns}$; $C_L = 30\text{ pF}$.

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay An to Yn	V _{CC} = 1.8 V V _{CC} = 2.5 V V _{CC} = 3.3 V		2.6 2.0 1.7	ns
t _{PHL} /t _{PLH}	Propagation delay LE to Yn; CP to Yn	V _{CC} = 1.8 V V _{CC} = 2.5 V V _{CC} = 3.3 V		2.9 2.3 1.9	ns
C _I	Input capacitance			5.0	pF
C _{PD}	Power dissipation capacitance per buffer	V _I = GND to V _{CC} ¹	Outputs enabled Output disabled	25 6	pF

NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	-40 to $+85^\circ\text{C}$	74AVCM162834DGG	SOT364-1

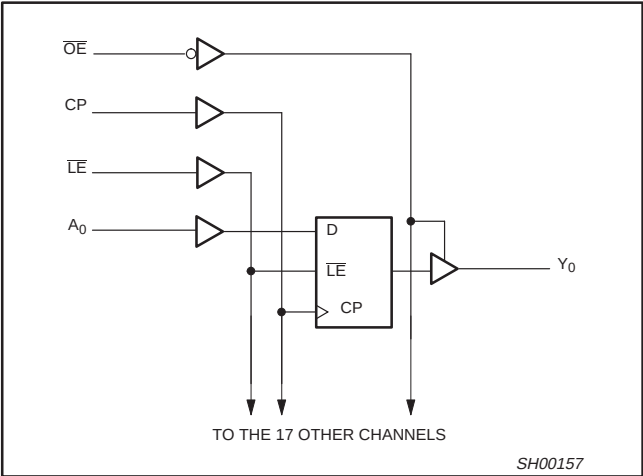
18-bit registered driver with inverted register enable
and 15 Ω termination resistors (3-State)

74AVCM162834

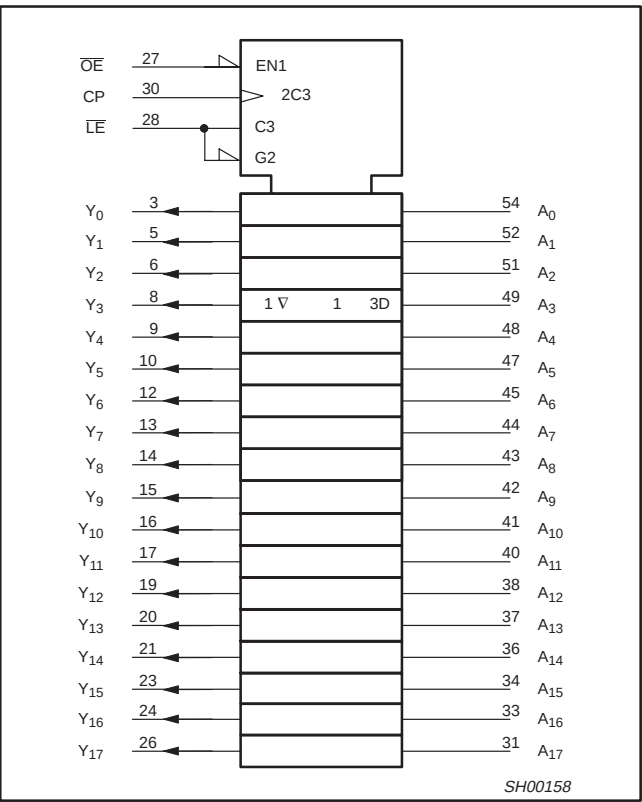
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 55	NC	No connection
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	Y ₀ to Y ₁₇	Data outputs
4, 11, 18, 25, 32, 39, 46, 53, 56	GND	Ground (0 V)
7, 22, 35, 50	V _{CC}	Positive supply voltage
27	$\overline{\text{OE}}$	Output enable input (active LOW)
28	$\overline{\text{LE}}$	Latch enable input (active LOW)
30	CP	Clock input
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	A ₀ to A ₁₇	Data inputs

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

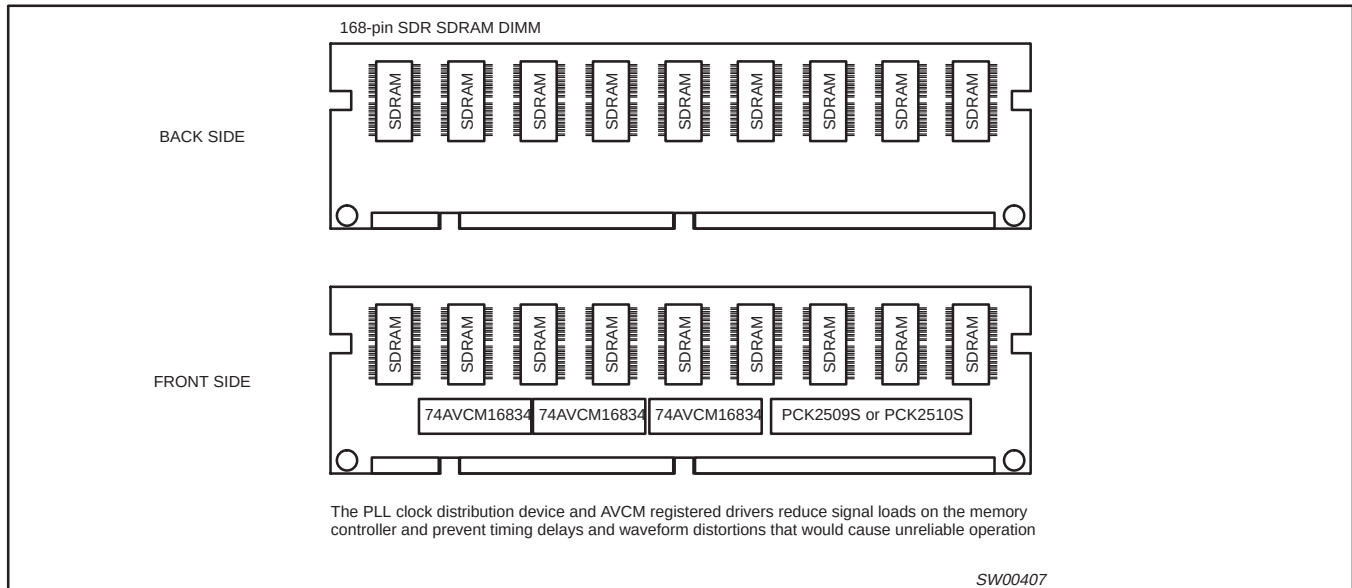
INPUTS				OUTPUTS
$\overline{\text{OE}}$	$\overline{\text{LE}}$	CP	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y ₀ ¹
L	H	L	X	Y ₀ ²

- H = HIGH voltage level
- L = LOW voltage level
- X = Don't care
- Z = High impedance "off" state
- ↑ = LOW-to-HIGH level transition

- NOTES:
1. Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.
2. Output level before the indicated steady-state input conditions were established.

18-bit registered driver with inverted register enable and 15 Ω termination resistors (3-State)

74AVCM162834



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage (according to JEDEC Low Voltage Standards)		1.65 2.3 3.0	1.95 2.7 3.6	V
	DC supply voltage (for low voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	3.6	V
V_O	DC output voltage range; output 3-State		0	3.6	V
	DC output voltage range; output HIGH or LOW state		0	V_{CC}	
T_{amb}	Operating free-air temperature range		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.65$ to 2.3 V $V_{CC} = 2.3$ to 3.0 V $V_{CC} = 3.0$ to 3.6 V	0 0 0	30 20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	For all inputs ¹	-0.5 to 4.6	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage; output 3-State	Note 1	-0.5 to 4.6	V
V_O	DC output voltage; output HIGH or LOW state	Note 1	-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

18-bit registered driver with inverted register enable and 15 Ω termination resistors (3-State)

74AVCM162834

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40 to +85 °C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2 V	V _{CC}	—	—	V
		V _{CC} = 1.65 to 1.95 V	0.65V _{CC}	0.9	—	
		V _{CC} = 2.3 to 2.7 V	1.7	1.2	—	
		V _{CC} = 3.0 to 3.6 V	2.0	1.5	—	
V _{IL}	LOW level Input voltage	V _{CC} = 1.2 V	—	—	GND	V
		V _{CC} = 1.65 to 1.95 V	—	0.9	0.35V _{CC}	
		V _{CC} = 2.3 to 2.7 V	—	1.2	0.7	
		V _{CC} = 3.0 to 3.6 V	—	1.5	0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 1.65 to 3.6 V; V _I = V _{IH} or V _{IL} ; I _O = -100 μA	V _{CC} - 0.20	V _{CC}	—	V
		V _{CC} = 1.65 V; V _I = V _{IH} or V _{IL} ; I _O = -4 mA	V _{CC} - 0.45	V _{CC} - 0.10	—	
		V _{CC} = 2.3 V; V _I = V _{IH} or V _{IL} ; I _O = -8 mA	V _{CC} - 0.55	V _{CC} - 0.28	—	
		V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; I _O = -12 mA	V _{CC} - 0.70	V _{CC} - 0.32	—	
V _{OL}	LOW level output voltage	V _{CC} = 1.65 to 3.6 V; V _I = V _{IH} or V _{IL} ; I _O = 100 μA	—	GND	0.20	V
		V _{CC} = 1.65 V; V _I = V _{IH} or V _{IL} ; I _O = 4 mA	—	0.10	0.45	
		V _{CC} = 2.3 V; V _I = V _{IH} or V _{IL} ; I _O = 8 mA	—	0.26	0.55	
		V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; I _O = 12 mA	—	0.36	0.70	
I _I	Input leakage current	V _{CC} = 1.65 to 3.6 V; V _I = V _{CC} or GND	—	0.1	2.5	μA
I _{OFF}	3-State output OFF-state current	V _{CC} = 0V; V _I or V _O = 3.6 V	—	0.1	± 10	μA
I _{IHZ} /I _{ILZ}	3-State output OFF-state current	V _{CC} = 1.65 to 3.6 V; V _I = V _{CC} or GND	—	0.1	12.5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 1.65 to 2.7 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	—	0.1	5	μA
		V _{CC} = 3.0 to 3.6 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	—	0.1	10	
I _{CC}	Quiescent supply current	V _{CC} = 1.65 to 2.7 V; V _I = V _{CC} or GND; I _O = 0	—	0.1	20	μA
		V _{CC} = 3.0 to 3.6 V; V _I = V _{CC} or GND; I _O = 0	—	0.2	40	

NOTES:

1. All typical values are at $T_{amb} = 25 \text{ }^\circ\text{C}$.

18-bit registered driver with inverted register enable and 15 Ω termination resistors (3-State)

74AVCM162834

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.0$ ns; $C_L = 30$ pF

SYMBOL	PARAMETER	WAVE-FORM	LIMITS											UNIT
			V _{CC} = 3.3 ± 0.3 V			V _{CC} = 2.5 ± 0.2 V			V _{CC} = 1.8 ± 0.15 V			V _{CC} = 1.2 V		
			MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	MIN	TYP ¹	MAX	MIN	TYP	
t _{PHL} /t _{PLH}	Propagation delay An to Yn	1, 7	0.7	1.7	2.5	0.8	2.0	3.1	1.0	2.6	4.5	–	5.2	ns
	Propagation delay $\overline{LE}$ to Yn	2, 7	0.7	1.9	2.7	0.8	2.3	3.3	1.0	2.9	5.0	–	5.6	
	Propagation delay CP to Yn	3, 7	0.7	1.7	2.5	0.8	2.0	3.0	1.0	2.6	4.5	–	5.2	
t _{PZH} /t _{PZL}	3-State output enable time $\overline{OE}$ to Yn	6, 7	1.0	2.3	4.5	1.0	2.5	4.5	1.5	3.0	6.5	–	5.5	ns
t _{PHZ} /t _{PLZ}	3-State output disable time $\overline{OE}$ to Yn	6, 7	1.0	2.3	3.5	1.0	2.2	4.0	1.5	3.5	6.5	–	6.9	ns
t _W	CP pulse width HIGH or LOW	3, 7	1.0	–	–	1.2	–	–	2.0	–	–	–	–	ns
	$\overline{LE}$ pulse width HIGH	2, 7	1.0	–	–	1.2	–	–	2.0	–	–	–	–	
t _{SU}	Set-up time An to CP	5, 7	0.7	–	–	0.7	–	–	0.7	–	–	1.0	–	ns
	Set-up time An to $\overline{LE}$ HIGH	4, 7	0.5	–	–	0.5	–	–	0.5	–	–	0.2	–	
	Set-up time An to $\overline{LE}$ LOW	4, 7	0.5	–	–	0.5	–	–	0.6	–	–	2.0	–	ns
t _h	Hold time An to CP	5, 7	0.9	–	–	0.9	–	–	1.0	–	–	1.5	–	ns
	Hold time An to $\overline{LE}$ HIGH	4, 7	1.6	–	–	1.7	–	–	2.0	–	–	3.2	–	
	Hold time An to $\overline{LE}$ LOW	4, 7	1.4	–	–	1.5	–	–	1.7	–	–	2.8	–	ns
F _{max}	Maximum clock pulse frequency	3, 7	500	–	–	400	–	–	250	–	–	–	–	MHz

NOTES:

1. All typical values are measured at $T_{amb} = 25$ °C and at $V_{CC} = 1.8$ V, 2.5 V, 3.3 V.

18-bit registered driver with inverted register enable and 15 Ω termination resistors (3-State)

74AVCM162834

AC WAVEFORMS FOR $V_{CC} = 3.0\text{ V TO } 3.6\text{ V RANGE}$

$$V_M = 0.5 V_{CC}$$

$$V_X = V_{OL} + 0.300\text{ V}$$

$$V_Y = V_{OH} - 0.300\text{ V}$$

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$$V_I = V_{CC}$$

AC WAVEFORMS FOR $V_{CC} = 2.3\text{ V TO } 2.7\text{ V AND } V_{CC} < 2.3\text{ V RANGE}$

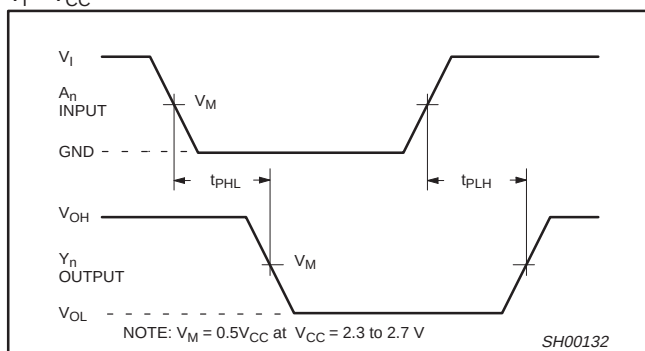
$$V_M = 0.5 V_{CC}$$

$$V_X = V_{OL} + 0.15\text{ V}$$

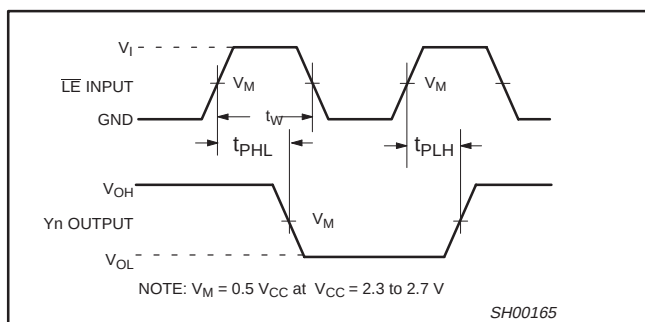
$$V_Y = V_{OH} - 0.15\text{ V}$$

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

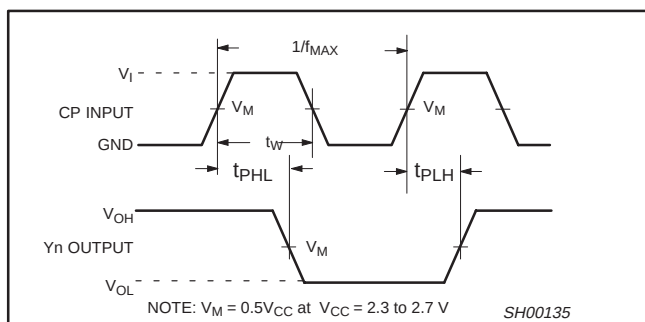
$$V_I = V_{CC}$$



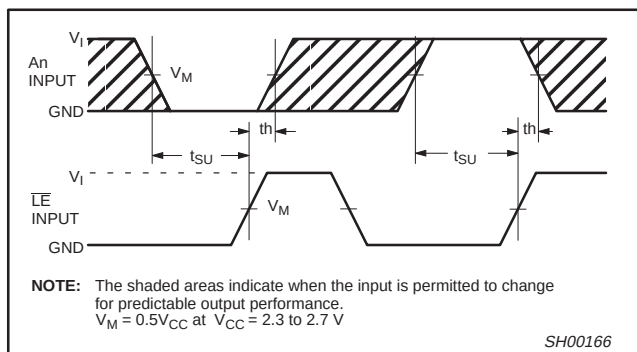
Waveform 1. Input (An) to output (Yn) propagation delay



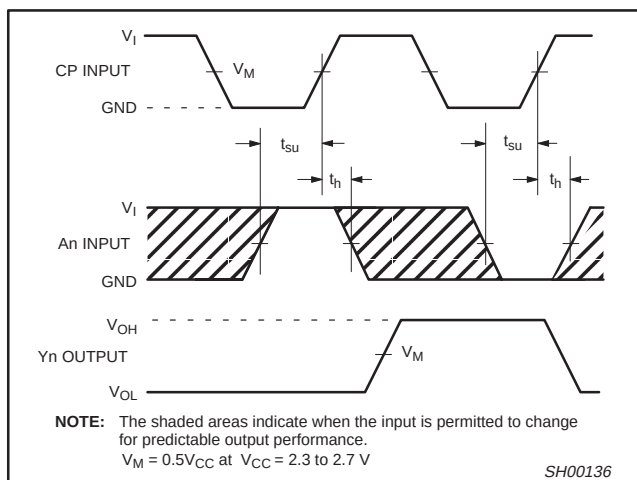
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Yn) propagation delays.



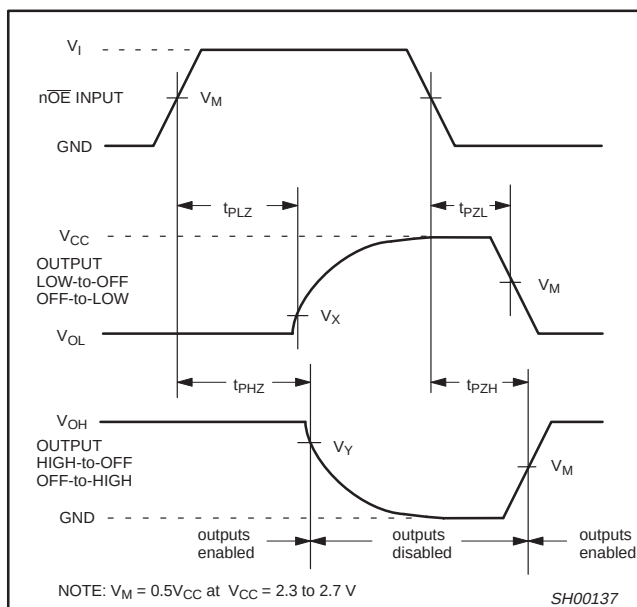
Waveform 3. The clock (CP) to Yn propagation delays, the clock pulse width and the maximum clock frequency.



Waveform 4. Data set-up and hold times for the An input to the LE input



Waveform 5. Data set-up and hold times for the An input to the clock CP input

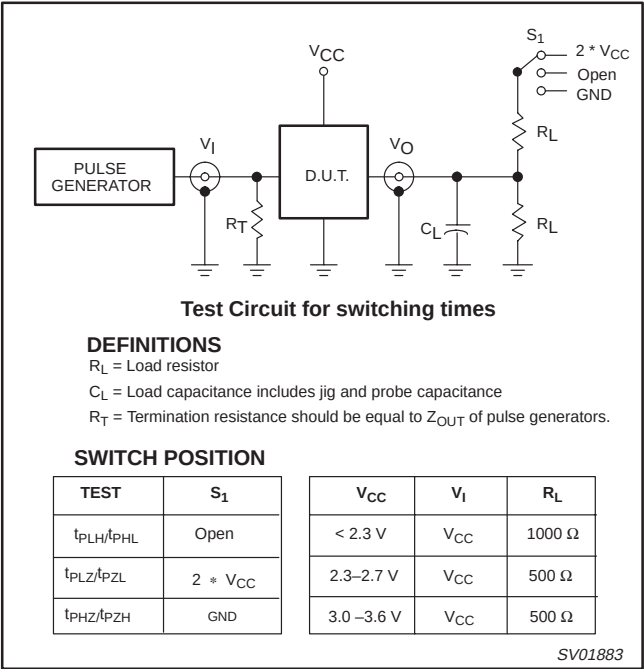


Waveform 6. 3-State enable and disable times

18-bit registered driver with inverted register enable
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74AVCM162834

TEST CIRCUIT



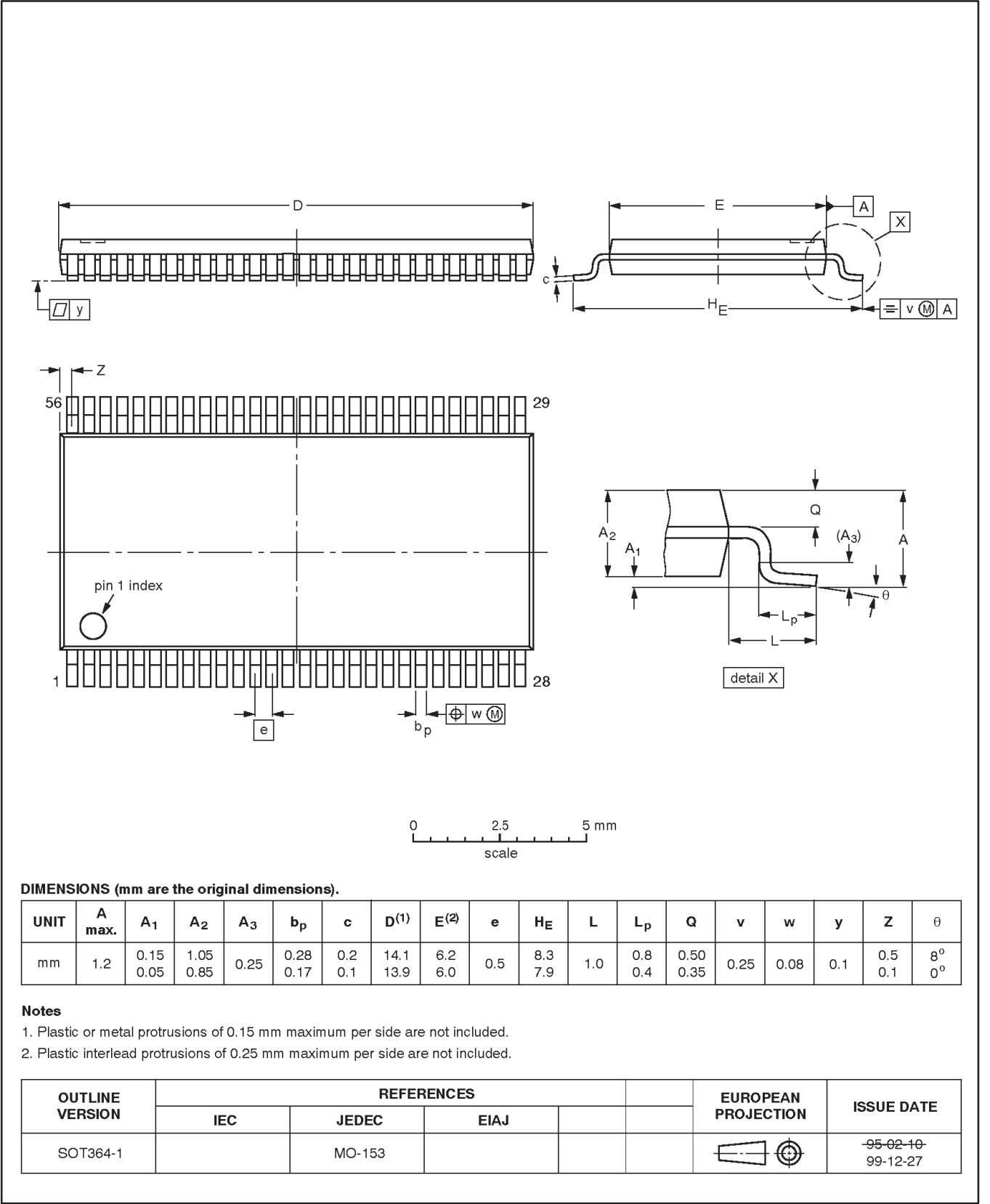
Waveform 7. Load circuitry for switching times

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74AVCM162834

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



18-bit registered driver with inverted register enable and 15 Ω termination resistors (3-State)

74AVCM162834

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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