

DUAL SCHOTTKY DIODE BRIDGE

FEATURES

- **Monolithic Eight-Diode Array**
- **Exceptional Efficiency**
- **Low Forward Voltage**
- **Fast Recovery Time**
- **High Peak Current**
- **Small Size**

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in both hermetic Cerdip and copper-leaded plastic packages. The UC1610 in ceramic is designed for -55°C to 125°C environments but with reduced peak current capability. The UC2610 in plastic and ceramic is designed for -25°C to 125°C environments also with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to 70°C temperature range.

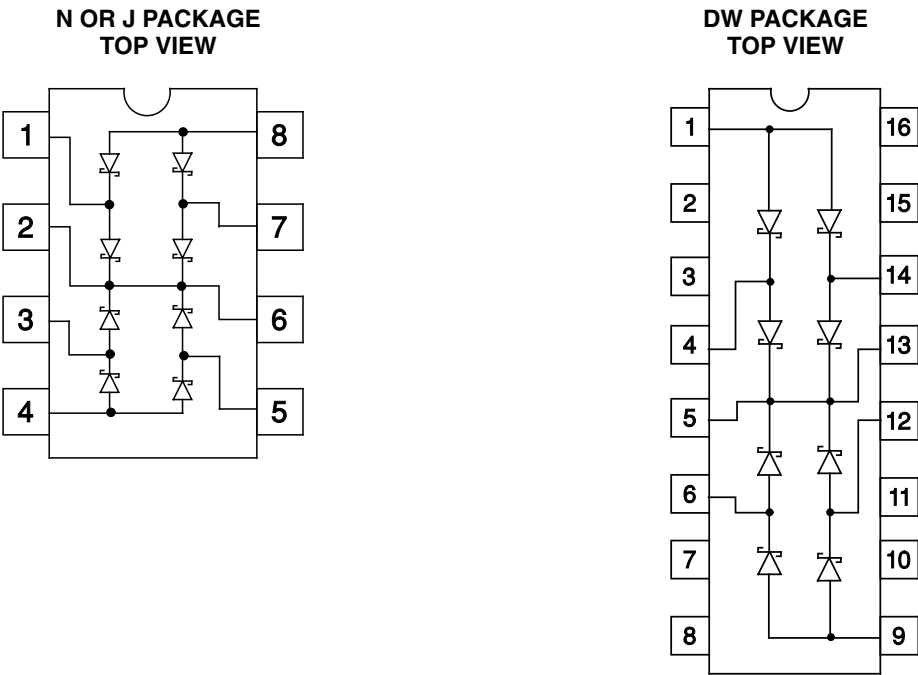
AVAILABLE OPTIONS

| $T_A = T_J$ | Packaged Devices | | |
|--|------------------|---------|---------|
| | SOIC Wide (DW) | DIL (J) | DIL (N) |
| -55°C to 125°C | UC1610DW | UC1610J | UC1610N |
| -25°C to 125°C | UC2610DW | UC2610J | UC2610N |
| 0°C to 70°C | UC3610DW | UC3610J | UC3610N |

THERMAL INFORMATION

| PACKAGE | θ_{JA} | θ_{JC} |
|------------------|-------------------------|-------------------|
| SOIC (DW) 16 pin | 50 – 100 ⁽¹⁾ | 27 |
| DIP (J) 8 pin | 125 – 160 | 20 ⁽²⁾ |
| DIP (N) 8 pin | 103 ⁽¹⁾ | 50 |

- NOTES: 1. Specified θ_{JA} (junction-to-ambient) is for devices mounted to 5-in² FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5-in² aluminum PC board. Test PWB was 0.062 in thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with a 100-mil x 100-mil probe land area at the end of each trace.
2. θ_{JC} data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that the baseline values shown are worst case (mean + 2s) for a 60-mil x 60-mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W.



absolute maximum ratings over operating free-air temperature (unless otherwise noted)^{†‡}

| | |
|---|----------------|
| Peak inverse voltage (per diode) | 50 V |
| Peak forward current | |
| UC1611 | 1 A |
| UC2610 | 1 A |
| UC3611 | 3 A |
| Power dissipation at T _A = 70°C | 1 W |
| Storage temperature range, T _{stg} | –65°C to 150°C |
| Lead temperature (soldering, 10 seconds) | 300°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Consult packaging section of databook for thermal limitations and considerations of package.

electrical characteristics, all specifications apply to each individual diode, T_J = 25°C, T_A = T_J, (except as noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------|---|------|------|-----|-------|
| Forward voltage drop | I _F = 100 mA | 0.35 | 0.5 | 0.7 | V |
| | I _F = 1 A | 0.8 | 1.0 | 1.3 | V |
| Leakage current | V _R = 40 V | | 0.01 | 0.1 | mA |
| | V _R = 40 V, T _J = 100°C | | 0.1 | 1.0 | mA |
| Reverse recovery | 0.5 A forward to 0.5 A reverse | | 15 | | ns |
| Forward recovery | 1 A forward to 1.1 V recovery | | 30 | | ns |
| Junction capacitance | V _R = 5 V | | 70 | | pF |

NOTE: At forward currents of greater than 1.0 A, a parasitic current of approximately 10 mA may be collected by adjacent diodes.

APPLICATION INFORMATION

REVERSE CURRENT
vs
VOLTAGE

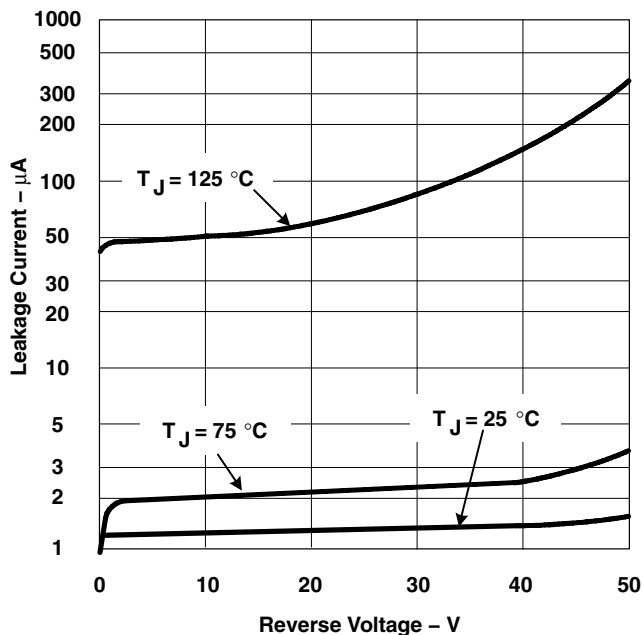


Figure 1

FORWARD CURRENT
vs
VOLTAGE

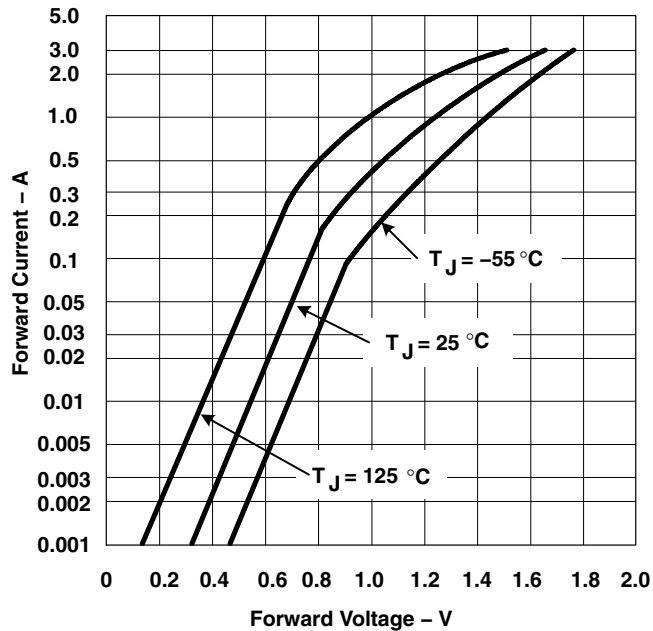


Figure 2

REVERSE RECOVERY CHARACTERISTICS

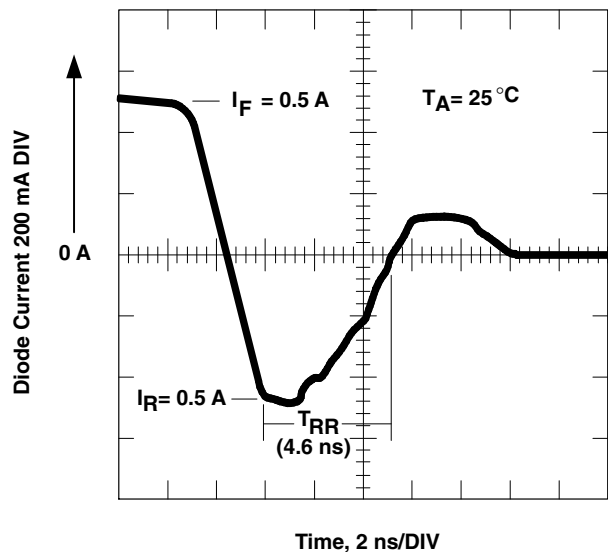


Figure 3

FORWARD RECOVERY CHARACTERISTICS

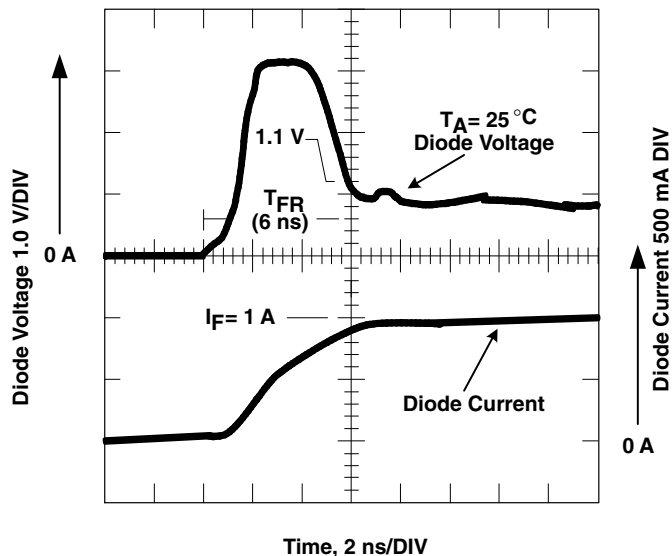


Figure 4

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| UC1610J | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |
| UC1610J883B | OBSOLETE | CDIP | JG | 8 | | TBD | Call TI | Call TI |
| UC2610N | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC2610NG4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3610DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3610DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3610DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3610DWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| UC3610N | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3610NG4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| UC3610Q | OBSOLETE | PLCC | FN | 20 | | TBD | Call TI | Call TI |
| UC3610QTR | OBSOLETE | PLCC | FN | 20 | | TBD | Call TI | Call TI |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

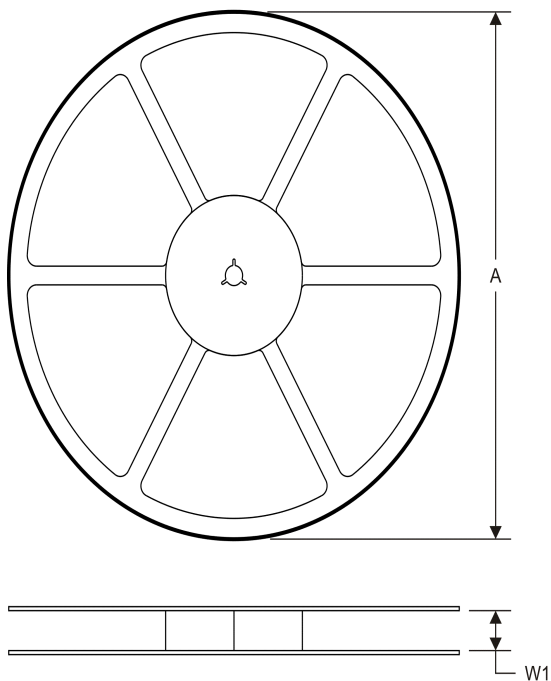
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UC3610DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UC3610DWTR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification.
 - Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

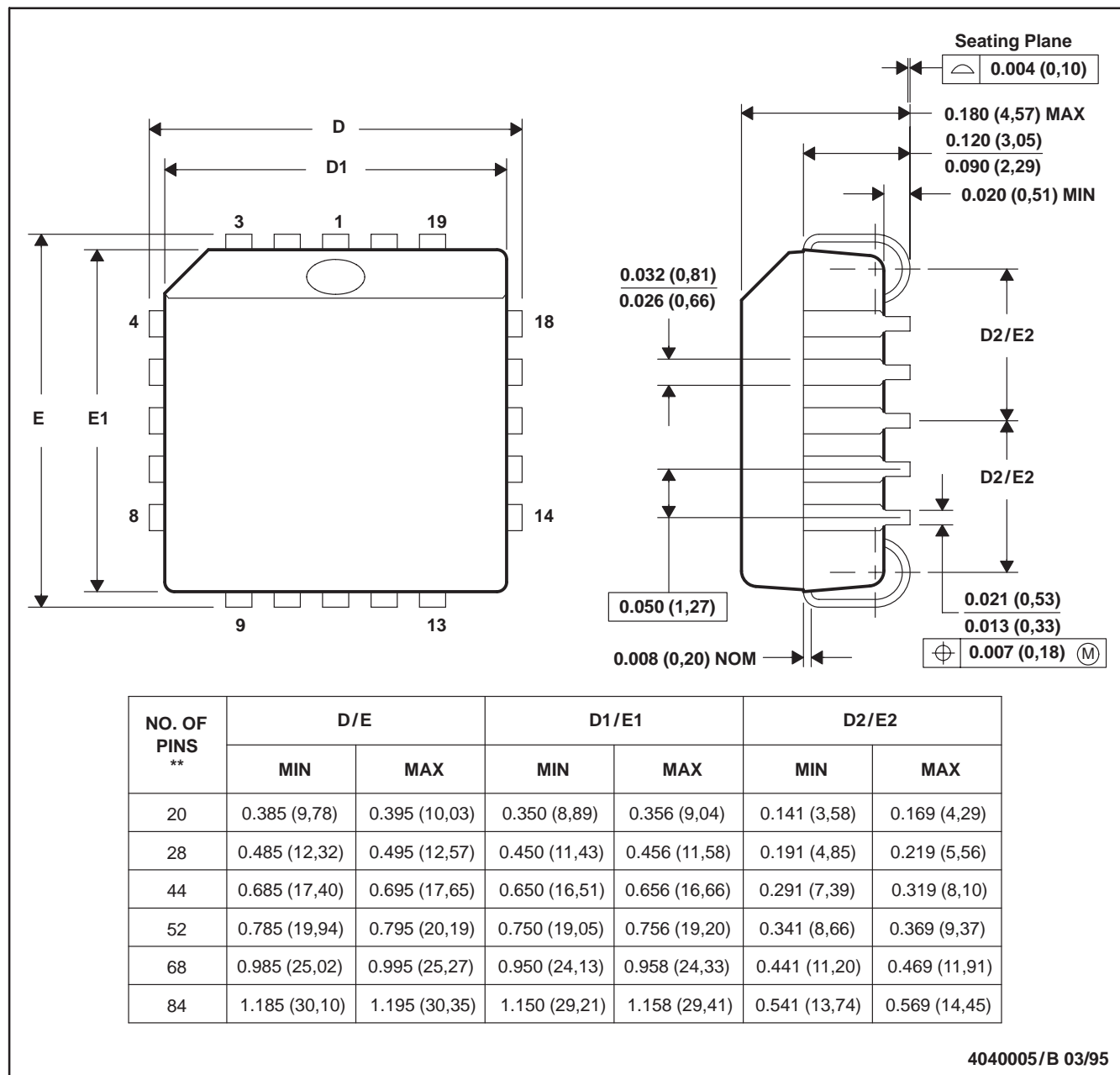


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

DW (R-PDSO-G16)

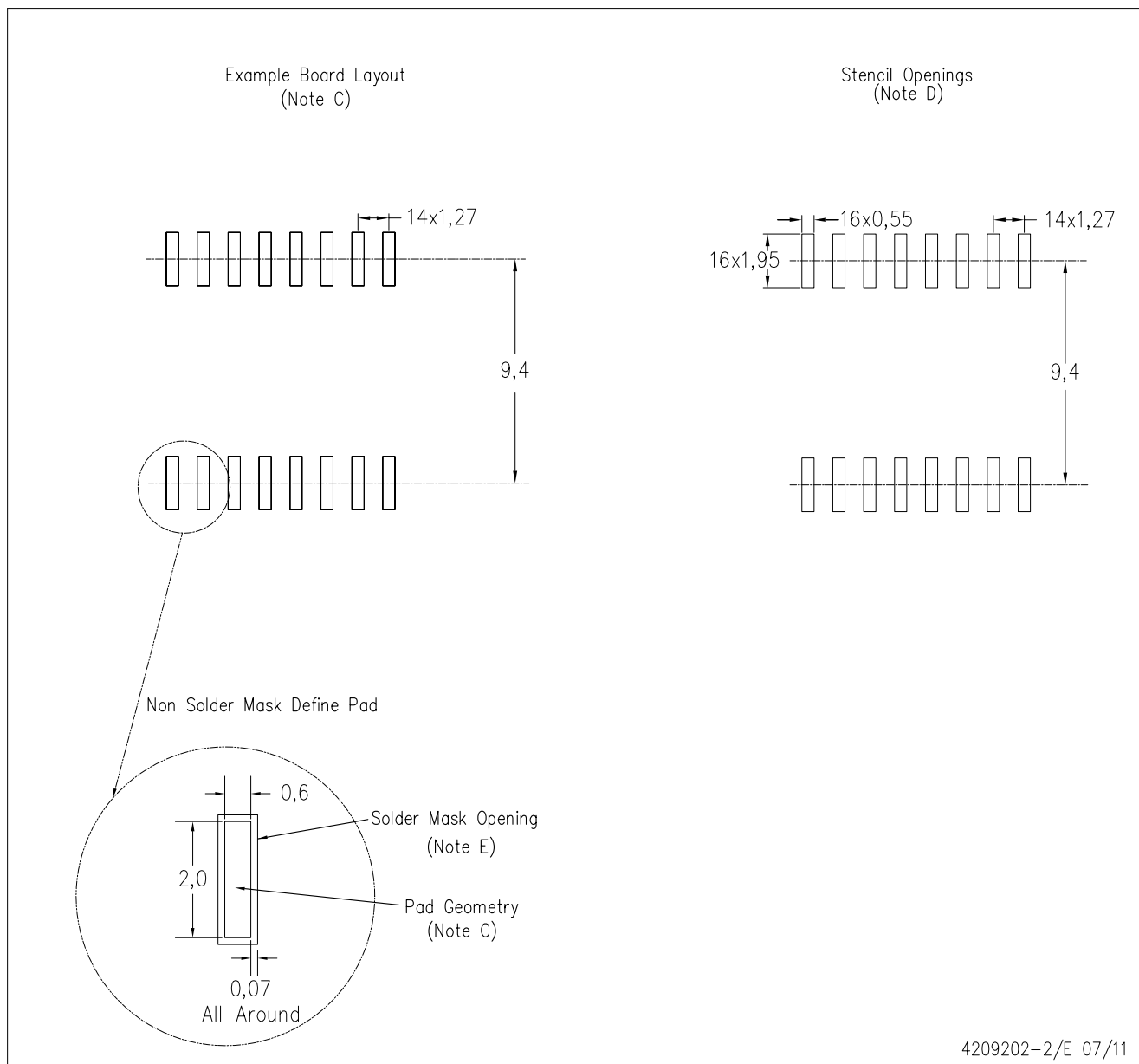
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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