

## P-Channel 60 V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>d</sup>	$Q_g$ (Typ)
- 60	0.060 at $V_{GS} = - 10$ V	- 19	26
	0.077 at $V_{GS} = - 4.5$ V	- 16.8	

### FEATURES

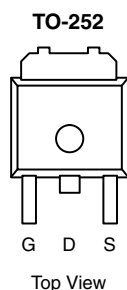
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



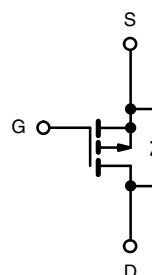
**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- High Side Switch for Full Bridge Converter
- DC/DC Converter for LCD Display



Drain Connected to Tab



P-Channel MOSFET

**Ordering Information:** SUD19P06-60-E3 (Lead (Pb)-free)  
SUD19P06-60-GE3 (Lead (Pb)-free and Halogen free)

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise note)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	A
	$T_C = 125$ °C	- 18.3	
Pulsed Drain Current	$I_{DM}$	- 30	
Avalanche Current, Single Pulse	$I_{AS}$	- 22	
Repetitive Avalanche Energy, Single Pulse <sup>a</sup>	$E_{AS}$	24.2	mJ
Power Dissipation	$T_C = 25$ °C	$P_D$	W
	$T_A = 25$ °C	38.5 <sup>c</sup> 2.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b</sup>	$R_{thJA}$	17	21	°C/W
		45	55	
Maximum Junction-to-Case	$R_{thJC}$	2.7	3.25	

Notes:

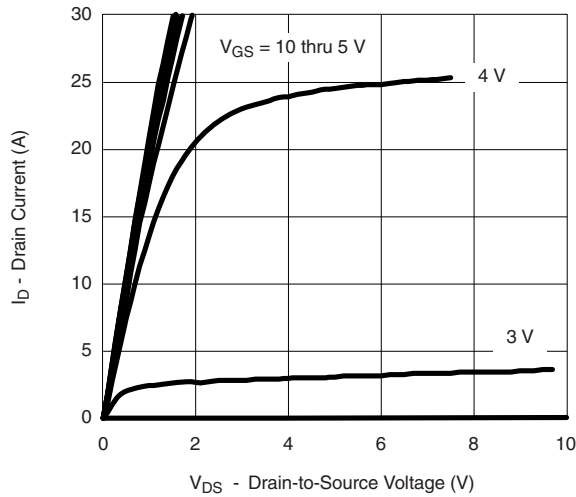
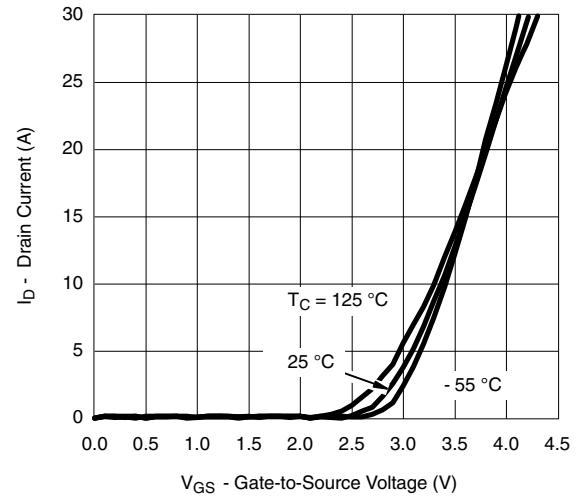
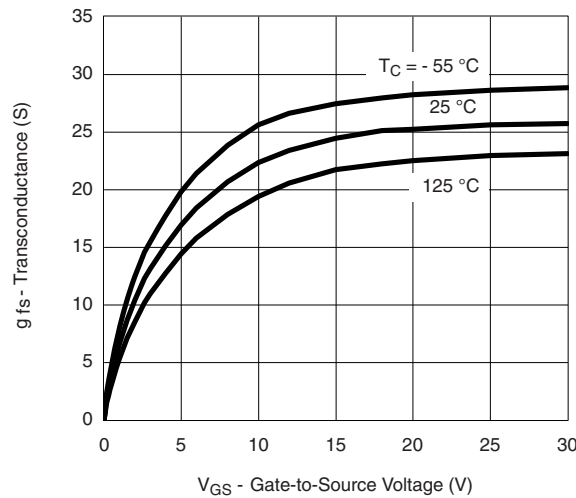
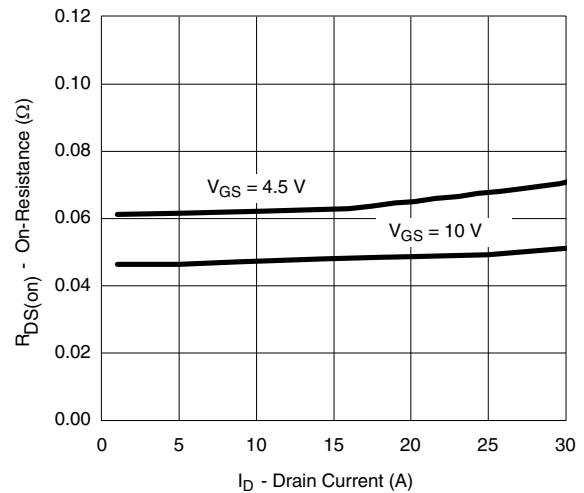
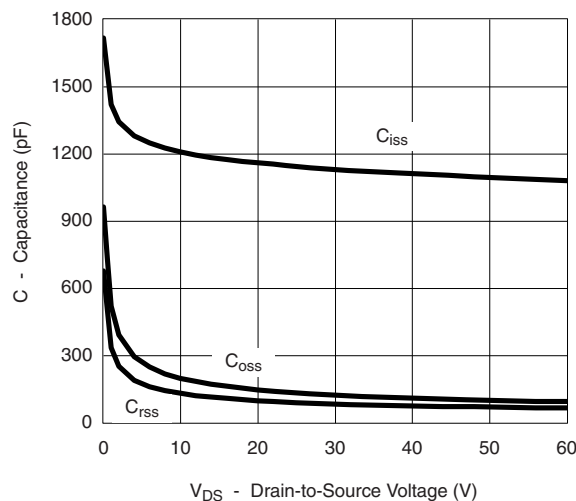
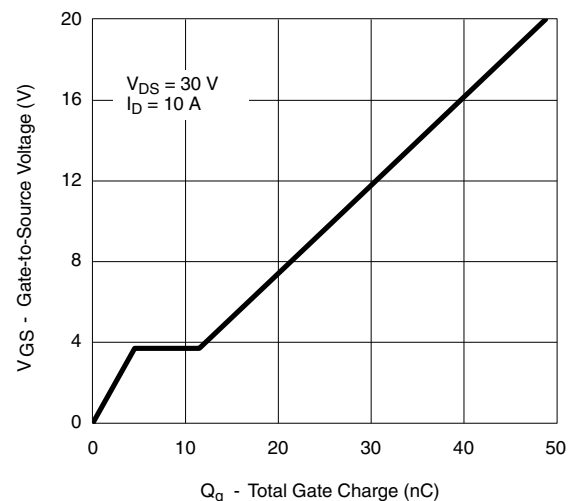
- Duty cycle  $\leq 1$  %.
- When mounted on 1" square PCB (FR-4 material).
- See SOA curve for voltage derating.
- Based up on  $T_C = 25$  °C.

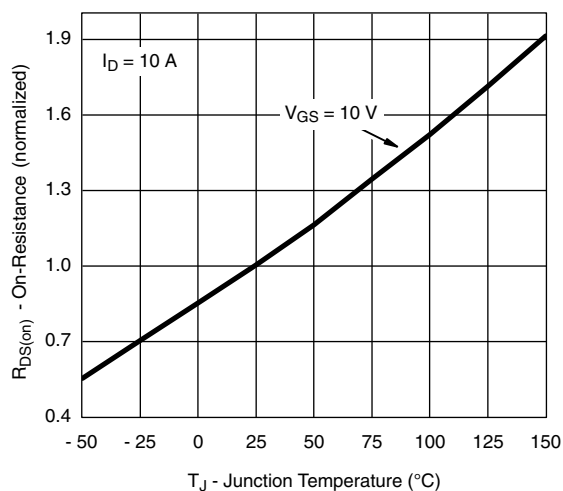
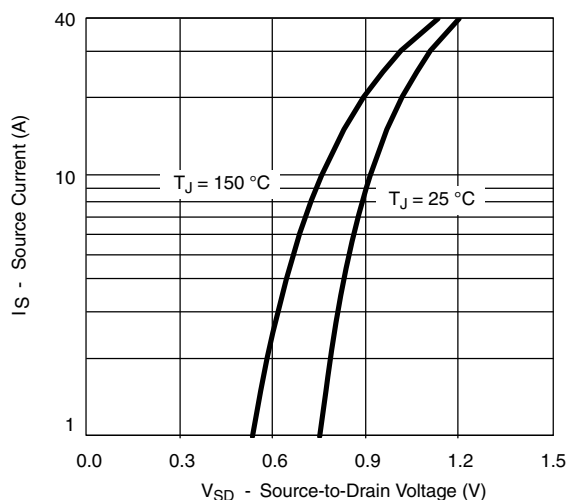
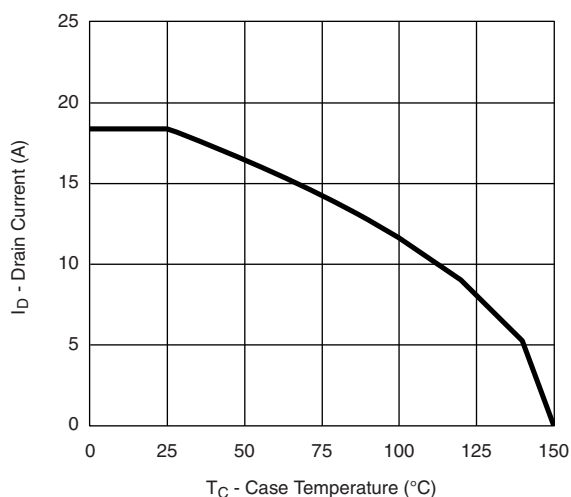
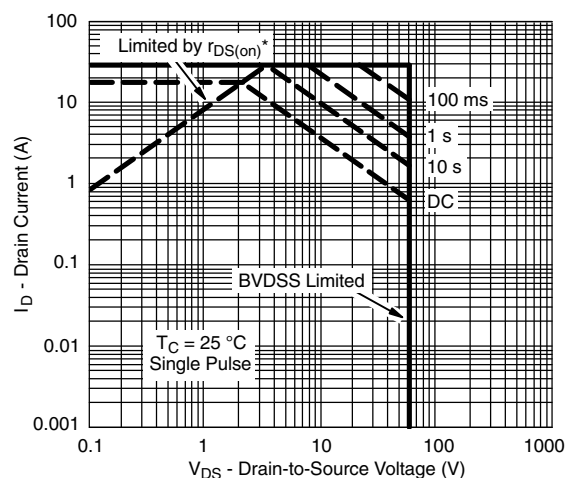
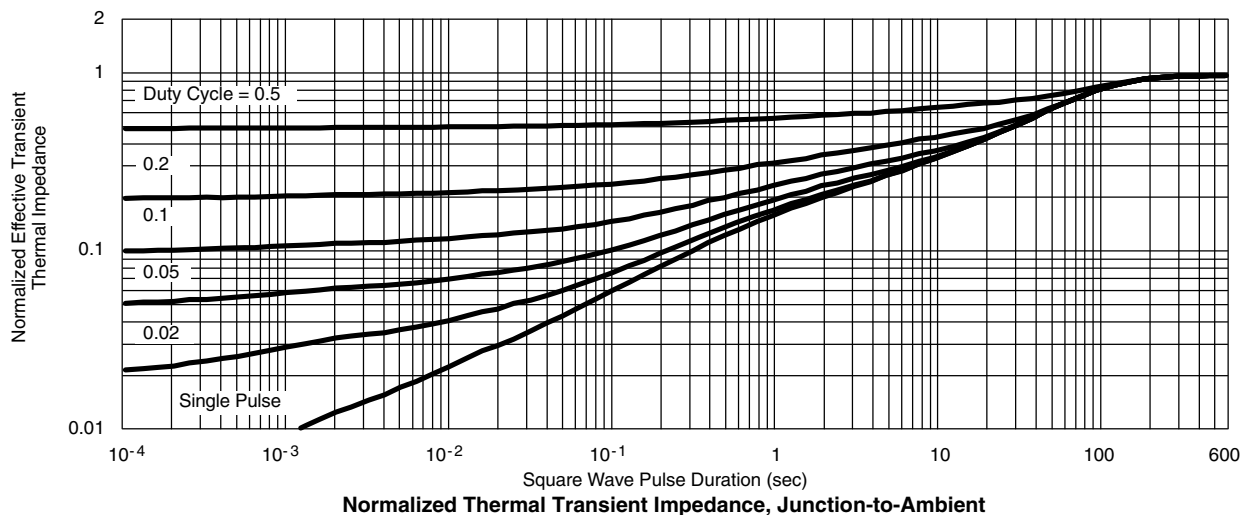
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise note)						
Parameter	Symbol	Test Conditions	Min .	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 1		- 3	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			- 50	
		V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C			- 125	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = - 5 V, V <sub>GS</sub> = - 10 V	- 30			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A		0.048	0.060	Ω
		V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A, T <sub>J</sub> = 125 °C			0.102	
		V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A, T <sub>J</sub> = 150 °C			0.120	
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 5 A		0.061	0.077	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 10 A		22		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = - 25 V, f = 1 MHz		1140	1710	pF
Output Capacitance	C <sub>oss</sub>			130		
Reverse Transfer Capacitance	C <sub>rss</sub>			90		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A		26	40	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			4.5		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			7		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		7		Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = - 30 V, R <sub>L</sub> = 3 Ω I <sub>D</sub> ≡ - 19 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 2.5 Ω		8	15	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			9	15	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			65	100	
Fall Time <sup>c</sup>	t <sub>f</sub>			30	45	
Drain-Source Body Diode and Characteristics (T <sub>C</sub> = 25 °C) <sup>b</sup>						
Continuous Current	I <sub>S</sub>				- 30	A
Pulsed Current	I <sub>SM</sub>				- 30	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = - 19 A, V <sub>GS</sub> = 0 V		- 1	- 1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 19 A, di/dt = 100 A/μs		41	61	ns

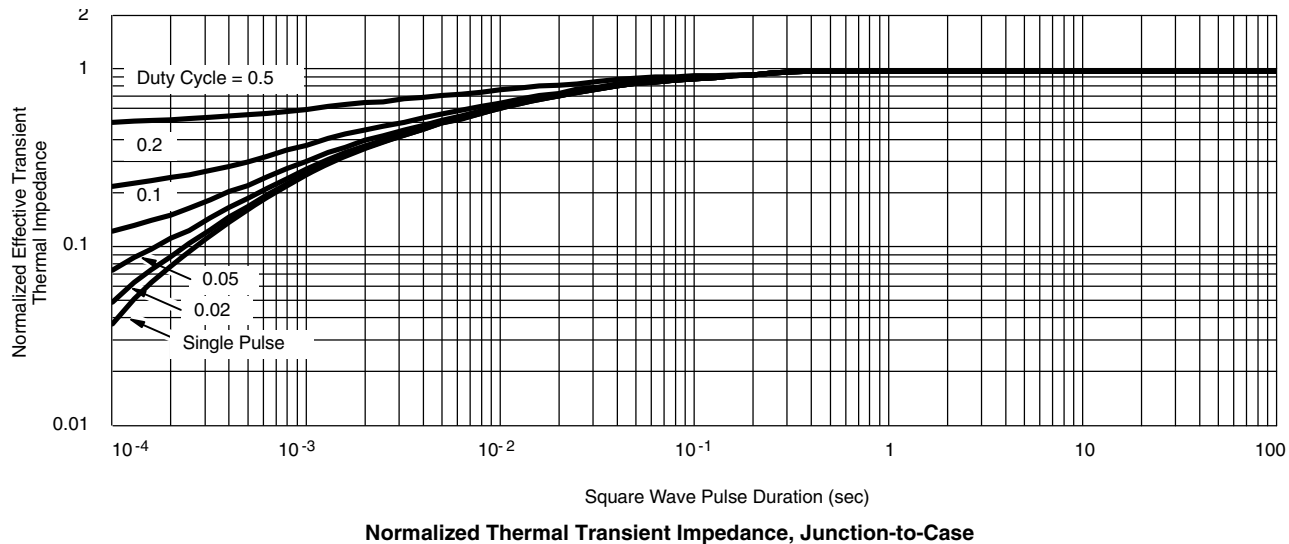
Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

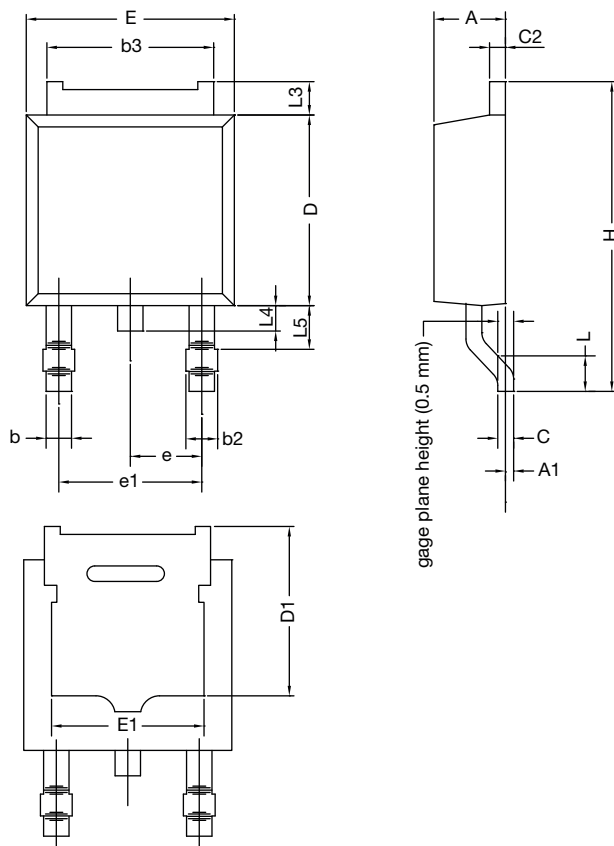
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****THERMAL RATINGS****Maximum Drain Current  
vs. Case Temperature****\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified  
Safe Operating Area**

**THERMAL RATINGS**


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?69253](http://www.vishay.com/ppg?69253).



## TO-252AA Case Outline

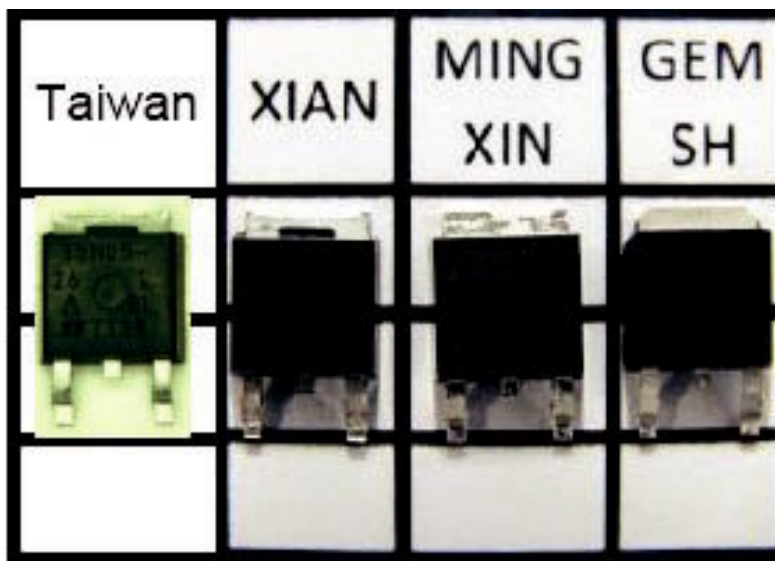


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T13-0359-Rev. O, 03-Jun-13  
DWG: 5347

### Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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