July 2014



FCH170N60

N-Channel SuperFET® II MOSFET

600 V, 22 A, 170 mΩ

Features

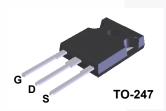
- 650 V @T_J = 150°C
- Typ. R_{DS(on)} = 150 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 42 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 190 pF)
- 100% Avalanche Tested
- · RoHS Compliant

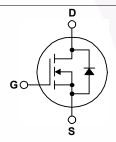
Applications

- Telecom / Sever Power Supplies
- Industrial Power Supplies
- · AC-DC Power Supply

Description

SuperFET[®] II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCH170N60	Unit
V _{DSS}	Drain to Source Voltage			600	V
\/	Cata ta Sauraa Valtaga	- DC		±20	V
V_{GSS}	Gate to Source Voltage	- AC		±30	_ v
	Drain Current	- Continuous (T _C = 25°C)		22	Α
'D	Drain Current	- Continuous (T _C = 100°C)		14	– A
I _{DM}	Drain Current	- Pulsed	(Note 1)	66	Α
E _{AS}	Single Pulsed Avalanche Ene	rgy	(Note 2)	525	mJ
I _{AR}	Avalanche Current		(Note 1)	5	Α
E _{AR}	Repetitive Avalanche Energy	Repetitive Avalanche Energy		2.27	mJ
dv/dt	MOSFET dv/dt		(Note 3)	100	V/ns
uv/ut	Peak Diode Recovery dv/dt			20	V/IIS
D	Dawer Dissipation	$(T_C = 25^{\circ}C)$		227	W
P_{D}	Power Dissipation	- Derate above 25°C		1.82	W/°C
T _J , T _{STG}	Operating and Storage Tempe	erature Range		-55 to +150	°C
T _L	Maximum Lead Temperature 1 1/8" from Case for 5 Seconds	•		300	°C

Thermal Characteristics

Symbol	Parameter	FCH170N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.55	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	*C/VV

Unit

Max.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH170N60	FCH170N60	TO-247	-	-	30

Test Conditions

Min.

Тур.

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted. Parameter

Off Chara	acteristics					
D\/	Drain to Source Breakdown Voltage	$I_D = 10 \text{ mA,V}_{GS} = 0 \text{ V,T}_J = 25^{\circ}\text{C}$	600	-	-	V
BV _{DSS} Drain to Source Breakdown Voltage	$I_D = 10 \text{ mA,V}_{GS} = 0 \text{ V, T}_J = 150^{\circ}\text{C}$	650	-	-	V	
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	-	-	1	μА
DSS	Zero Gate Voltage Brain Gurrent	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	1.2	-	μΑ
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

Symbol

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.5	-	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 11 A	1	150	170	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 11 A	-	17	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 000 V V 0 V	-	2150	2860	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V		60	80	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12	-\	2.65	-	pF
Coss (eff.)	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	-	190	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 11 A,	-	42	55	nC
Q _{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	9	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	11	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.95	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	21	50	ns
t _r		$V_{DD} = 380 \text{ V}, I_D = 11 \text{ A},$	-	12	35	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_g = 4.7 Ω	-/	55	120	ns
t _f	Turn-Off Fall Time	(Note 4)	-	3.8	18	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current			-	22	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current			-	66	Α
V_{SD}	Drain to Source Diode Forward Voltage V _{GS} = 0 V, I _{SD} = 11 A		-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 11 A,	-	346	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	6.2	-	μС

- 1. Repetitive rating: pulse width limited by maximum junction temperature
- 2. I $_{AS}$ = 5 A, R $_{G}$ = 25 Ω , Starting T $_{J}$ = 25°C
- 3. $I_{SD} \leq$ 11 A, di/dt \leq 200 A/ $\mu s,~V_{DD} \leq$ 380 V, Starting T_J = 25°C
- 4. Essentially independent of operating temperature typical characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

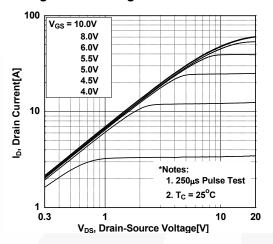


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

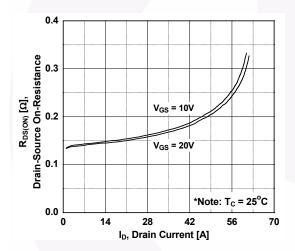


Figure 5. Capacitance Characteristics

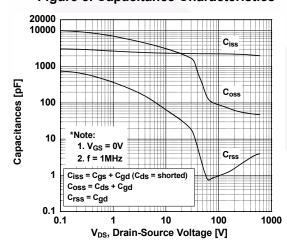


Figure 2. Transfer Characteristics

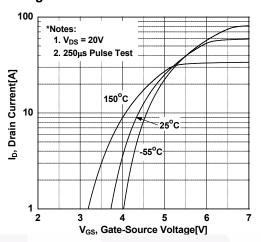


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

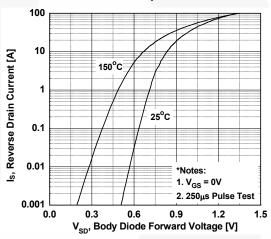
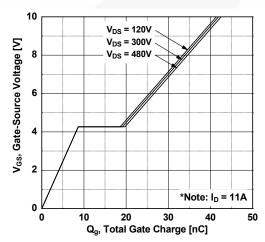


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

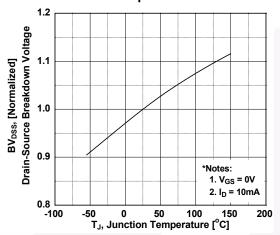


Figure 9. Maximum Safe Operating Area

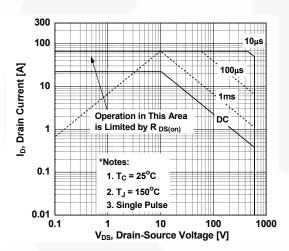


Figure 11. Eoss vs. Drain to Source Voltage

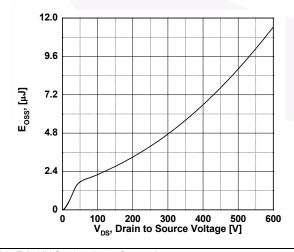


Figure 8. On-Resistance Variation vs. Temperature

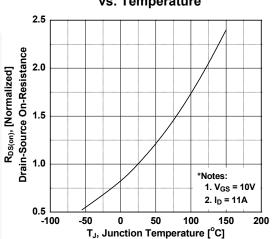
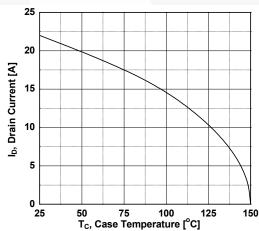
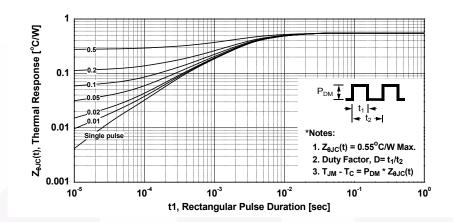


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



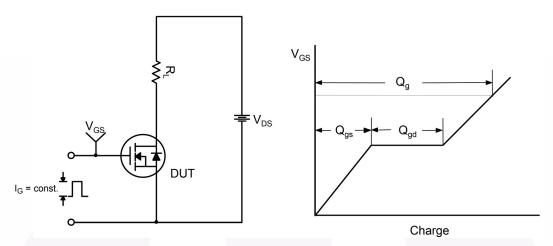


Figure 13. Gate Charge Test Circuit & Waveform

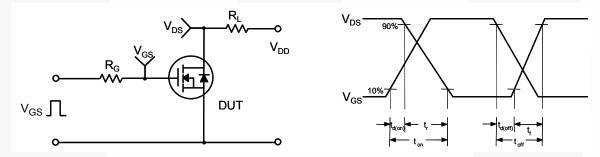


Figure 14. Resistive Switching Test Circuit & Waveforms

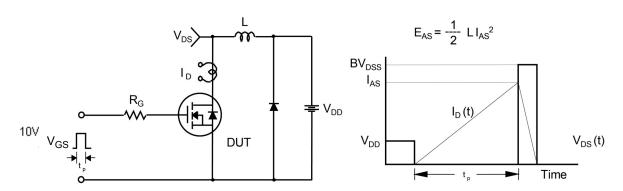


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

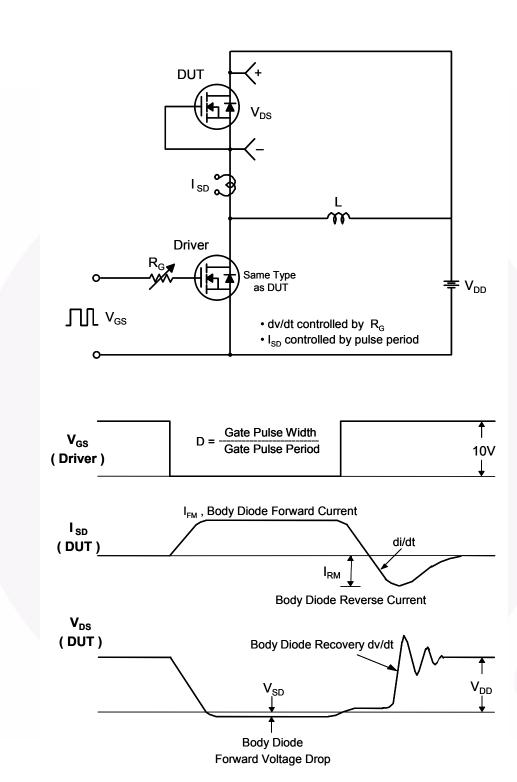
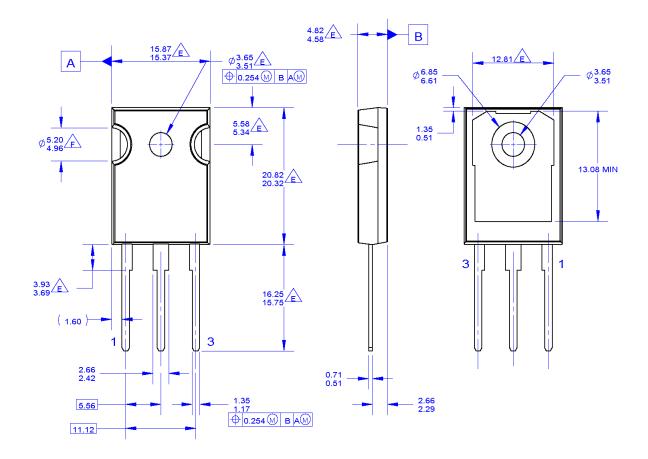


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

TO-247 3L



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
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- E DOES NOT COMPLY JEDEC STANDARD VALUE
- NOTCH MAY BE SQUARE
 G. DRAWING FILENAME: MKT-TO247A03_REV03

Figure 17. TO-247, Molded, 3 Lead, Jedec Variation AB

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Rev. 168

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