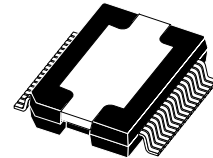


## Multiple linear/switching voltage regulator for car-radio

### Features

- Step-down synchronous switching voltage regulator
  - Internal high-side/ Low-side NDMOS
  - $1.2 < V_{out} < 8\text{ V}$  selectable through external resistors
  - 1.2/2.5 A load current selected through dedicated pin
  - 185 kHz free-run frequency
  - SYNC function ( $220 < f_{sw} < 400\text{ kHz}$ )
- Linear regulators
  - 3.3/5 V @ 150 mA standby regulator selected through dedicated pin (VSTBYSEL)
  - 5/8.5 V @ 350 mA switched linear regulator enabled and selected through I<sup>2</sup>C bus (VLR1)
  - 3.3/10 V @ 1 A switched linear regulator enabled and selected through I<sup>2</sup>C bus (VLR2)
- 2 High side drivers (0.5 V max drop @ 0.5 A) enabled through I<sup>2</sup>C bus and equipped with protection circuit against:
  - short to ground and battery
  - loss of ground and battery
  - unsupplied short to battery
- Reset function with configurable delay (RST, RSTDLY)
- I<sup>2</sup>C bus



**PowerSO36 (slug-up)**

- Enable pin to drive switching regulator and I<sup>2</sup>C bus logic
- Under/over voltage battery detector (VBATVW)
  - Under voltage threshold adjustable through dedicated pin (LVWIN)
- Load dump protection
- Independent thermal protection on all regulators

### Description

L5962 is a very versatile device exploiting BCD technology characteristics to provide a complete set of regulated voltages covering all the needs of a car-radio set.

In standby condition the device guarantees extremely low quiescent current (90  $\mu\text{A}$  max -  $40\text{ }^{\circ}\text{C} < T < 85\text{ }^{\circ}\text{C}$ ) and minimum operating voltage (4.5 V using an external Schottky diode for the back-up function).

**Table 1. Device summary**

| Order code | Package   | Packing       |
|------------|-----------|---------------|
| L5962      | PowerSO36 | Tray          |
| L5962TR    | PowerSO36 | Tape and reel |

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# 1 Block and application diagram

Figure 1. Block diagram

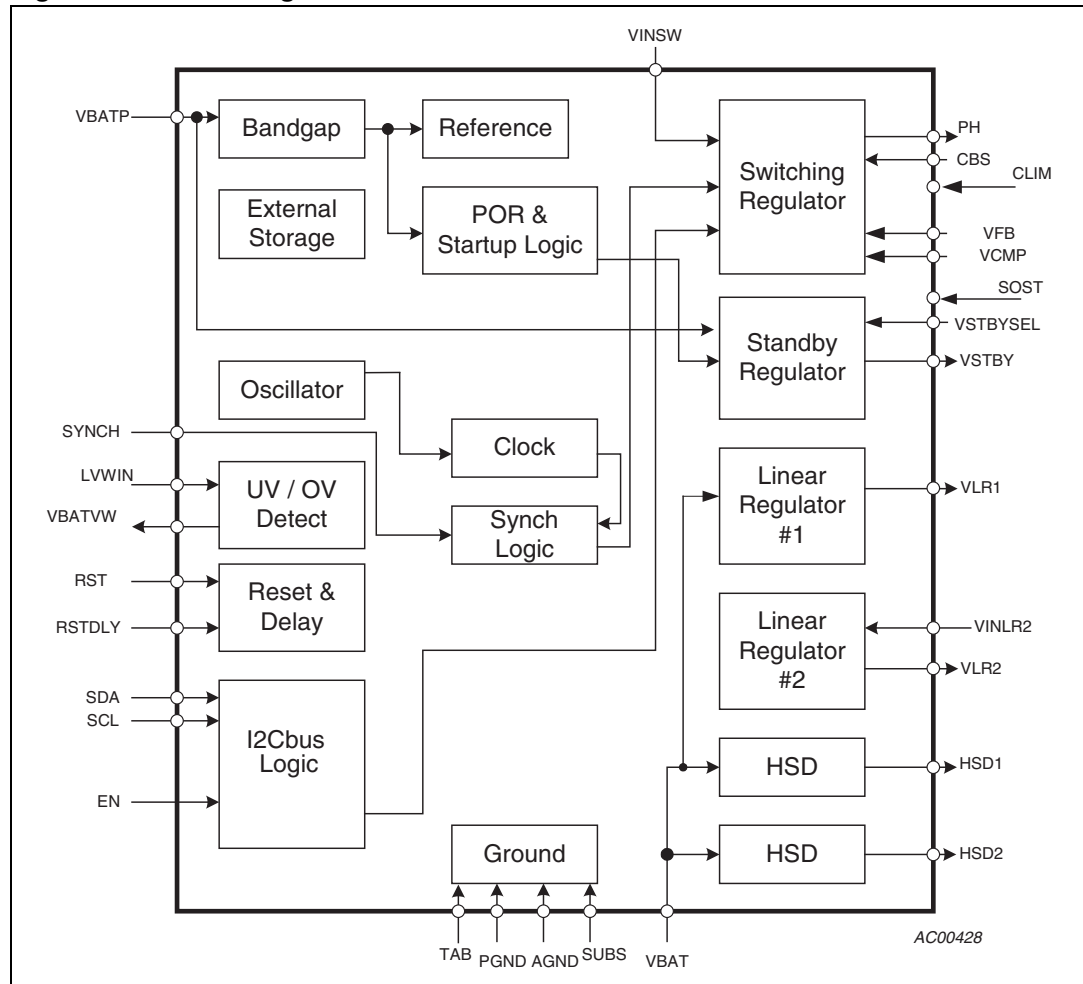
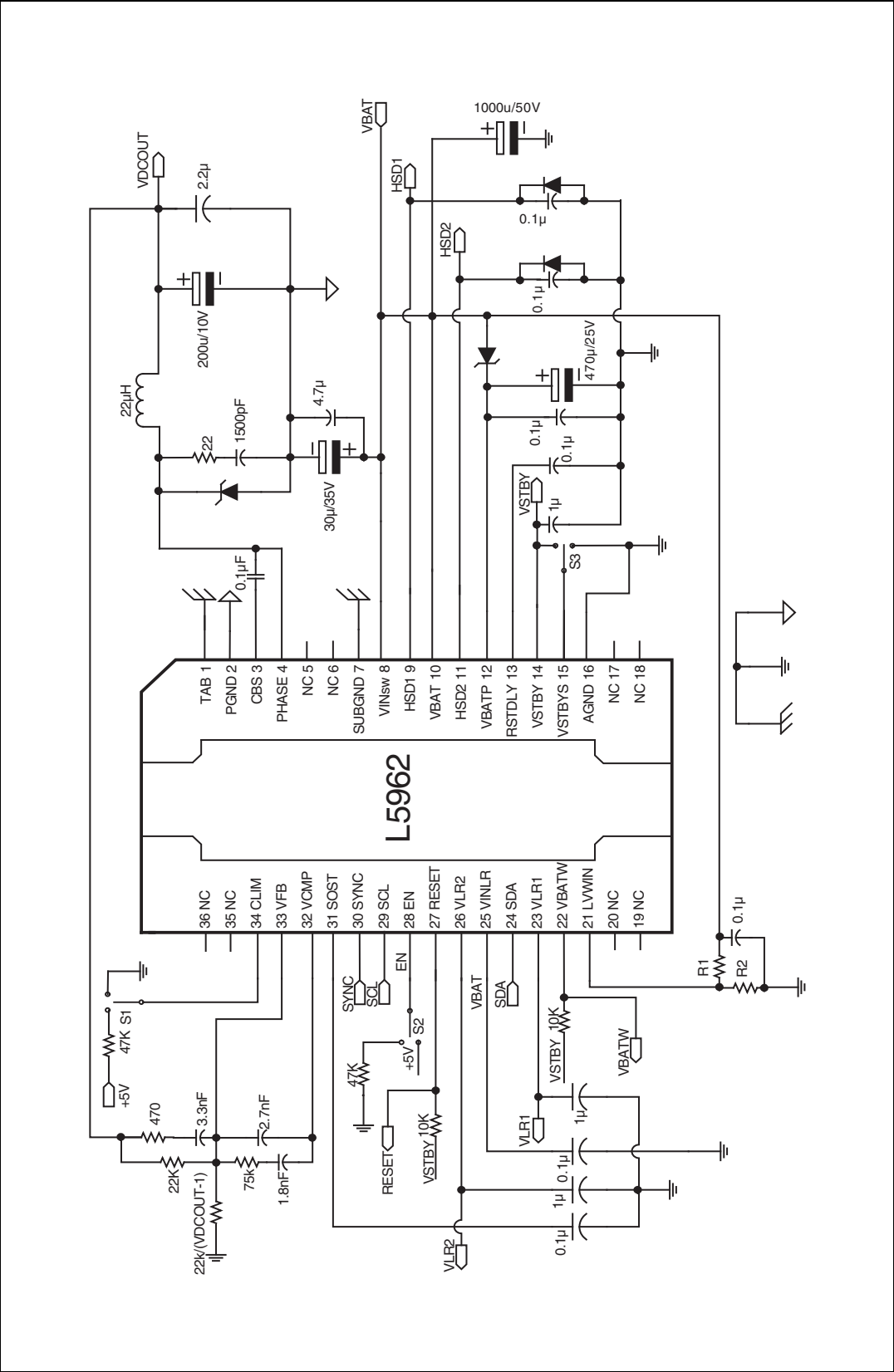
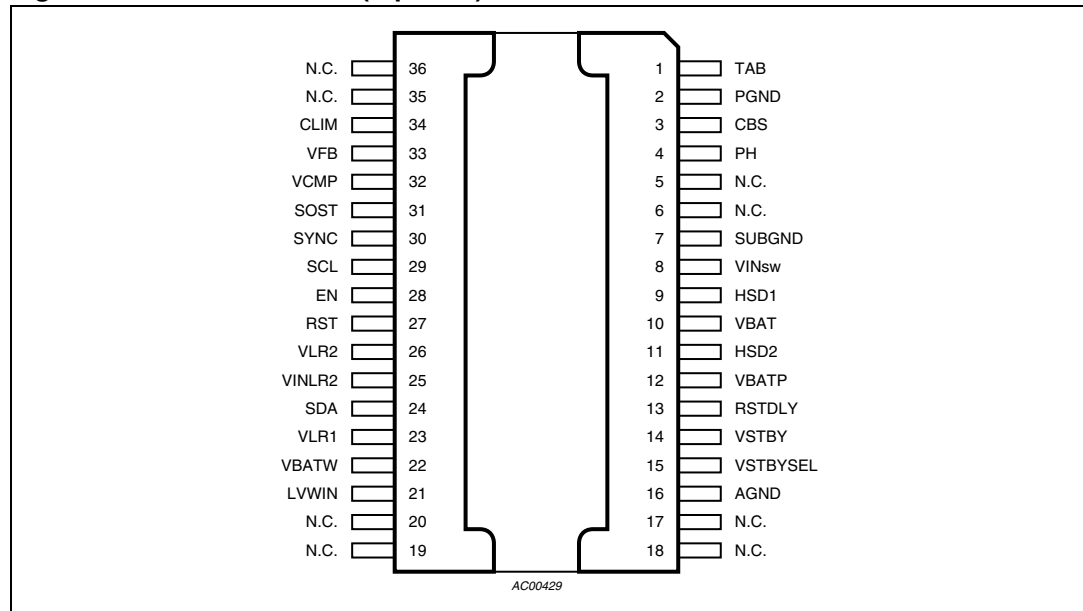


Figure 2. Application diagram



## 2 Pin description

**Figure 3. Pin connection (top view)**



**Table 2. Pin description**

| Pin # | Pad name | Function                           | Description                                                                                                                |
|-------|----------|------------------------------------|----------------------------------------------------------------------------------------------------------------------------|
| 1     | TAB      |                                    | This pin must be connected to GND                                                                                          |
| 2     | PGND     | Switching regulator ground         | It is the power ground reference                                                                                           |
| 3     | CBS      | Bootstrap for switching regulator  | Bootstrap capacitor Input for the switching regulator                                                                      |
| 4     | PH       | Switching stage output             | Phase output. It is the switching output of the switching regulator. It also provides phase reference for bootstrap drive. |
| 5     | N.C.     | Not connected                      | -                                                                                                                          |
| 6     | N.C.     | Not connected                      | -                                                                                                                          |
| 7     | SUBGND   | Substrate ground                   | Substrate ground                                                                                                           |
| 8     | VINsw    | Switching regulator supply voltage | Battery voltage for the switching regulator                                                                                |
| 9     | HSD1     | High side driver 1                 | Output of the 1 <sup>st</sup> high side driver                                                                             |
| 10    | VBAT     | VLR1/HSD1/HSD2 supply voltage      | Voltage input for linear regulator #1 high side driver and battery warnings                                                |
| 11    | HSD2     | High side driver 2                 | Output of the 2 <sup>nd</sup> high side driver                                                                             |
| 12    | VBATP    | Standby regulator supply voltage   | Protected battery input for bias, bandgap, oscillator, and VSTBY regulator                                                 |
| 13    | RSTDLY   | Reset delay function               | Input                                                                                                                      |
| 14    | VSTBY    | Standby regulator output           | Output of the standby regulator                                                                                            |

Table 2. Pin description (continued)

| Pin # | Pad name | Function                                   | Description                                                 |
|-------|----------|--------------------------------------------|-------------------------------------------------------------|
| 15    | VSTBYSEL | Standby regulator selector                 | Selection input for standby regulator output (3.3 V or 5 V) |
| 16    | AGND     | Analog ground                              | Analog voltage reference                                    |
| 17    | N.C.     | Not connected                              | -                                                           |
| 18    | N.C.     | Not connected                              | -                                                           |
| 19    | N.C.     | Not connected                              | -                                                           |
| 20    | N.C.     | Not connected                              | -                                                           |
| 21    | LVWIN    | Battery detector adjustment input          | Low-voltage warning input                                   |
| 22    | VBATW    | Battery detector output (open-drain)       | Battery voltage warning output                              |
| 23    | VLR1     | Switched linear regulator 1                | Output of the 1 <sup>st</sup> linear regulator              |
| 24    | SDA      | I <sup>2</sup> C bus data                  | I <sup>2</sup> C data line                                  |
| 25    | VINLR2   | VLR2 supply voltage                        | Battery supply for the 2 <sup>nd</sup> linear regulator     |
| 26    | VLR2     | Switched linear regulator 2                | Output of the 2 <sup>nd</sup> linear regulator              |
| 27    | RST      | Reset                                      | Output                                                      |
| 28    | EN       | Enable                                     | Active mode enable input. Active high                       |
| 29    | SCL      | I <sup>2</sup> C bus clock                 | I <sup>2</sup> C clock source supplied by the master device |
| 30    | SYNC     | Switching regulator SYNC function          | Synchronization Input                                       |
| 31    | SOST     | Switching regulator soft-start             | Soft start external capacitor                               |
| 32    | VCMP     | Switching regulator compensation           | Feedback compensation input.                                |
| 33    | VFB      | Switching regulator feedback               | Regulated output voltage sense                              |
| 34    | CLIM     | Switching regulator current limit selector | Choose between two current limits                           |
| 35    | N.C.     | Not connected                              | -                                                           |
| 36    | N.C.     | Not connected                              | -                                                           |

## 3 Electrical specification

### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

| Pin name/Symbol         | Parameter                                                                        | Value        | Unit |
|-------------------------|----------------------------------------------------------------------------------|--------------|------|
| $V_{S_{MAX}}$           | Operating supply voltage (VBAT, VBATP, VINSW, VINLR2)                            | -0.3 to 27   | V    |
|                         | Transient supply voltage (VBAT, VBATP, VINSW, VINLR2)                            | -0.3 to 50   | V    |
| $V_{pin_{MAX}}$         | Input pin voltage (EN, RSTDLY, VSTBYSEL, SYNCH, SCL, SDA, VCMF, VFB, CLIM, SOST) | -0.3 to 6    | V    |
| AGND, PGND, SUBGND, TAB | Ground pin voltage                                                               | -0.3 to +0.3 | V    |
| $T_{op}$                | Operating temperature range                                                      | -40 to 85    | °C   |
| $T_{stg}$               | Storage temperature range                                                        | -55 to 150   | °C   |

### 3.2 Thermal data

Table 4. Thermal data

| Symbol           | Parameter                                 | Value | Unit |
|------------------|-------------------------------------------|-------|------|
| $R_{th\ j-case}$ | Thermal resistance junction-to-case (max) | 2     | °C/W |

### 3.3 Electrical characteristics

VBAT= VINSW = VINLR2 = 14.4 V,  $T_{amb}$  = 25 °C unless otherwise specified.

Table 5. Electrical characteristics

| Symbol                | Parameter                   | Test conditions                                                                                                                             | Min. | Typ. | Max.     | Unit    |
|-----------------------|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|------|------|----------|---------|
| <b>Input supplies</b> |                             |                                                                                                                                             |      |      |          |         |
| $V_{min}$             | VBATP operating voltage     | -                                                                                                                                           | 4.1  | -    | -        | V       |
| $I_q$                 | Total quiescent current     | EN = 0; $I_{VSTBY}$ = 100 $\mu$ A<br>@ $T = -40\text{ }^{\circ}\text{C}$<br>@ $25\text{ }^{\circ}\text{C} < T < 85\text{ }^{\circ}\text{C}$ | -    | -    | 90<br>75 | $\mu$ A |
| $V_{OV}$              | Overvoltage shut-down       | VBAT rising                                                                                                                                 | 27   | 29   | 31       | V       |
| $HYS_{OV}$            | Hysteresis on $V_{OV}$      | -                                                                                                                                           | -    | 400  | -        | mV      |
| $V_{UV}$              | VBAT undervoltage threshold | VBAT falling;<br>VBATVW transition to 0 V                                                                                                   | 7    | 7.5  | 8        | V       |

Table 5. Electrical characteristics (continued)

| Symbol               | Parameter                                   | Test conditions                                                                                        | Min. | Typ. | Max.    | Unit               |
|----------------------|---------------------------------------------|--------------------------------------------------------------------------------------------------------|------|------|---------|--------------------|
| $HYS_{UV}$           | Hysteresis on $V_{UV}$                      | -                                                                                                      | -    | 1    | -       | V                  |
| <b>VSTBY (3.3 V)</b> |                                             |                                                                                                        |      |      |         |                    |
| $V_{outVSTBY3}$      | Output voltage                              | $0 < I_{load} < 150 \text{ mA}$                                                                        | 3.2  | 3.3  | 3.4     | V                  |
| $LnR_{VSTBY3}$       | Line regulation                             | $4.1 < V_{BATP} < 18V$<br>$I_{load} = 150 \text{ mA}$                                                  | -10  | -    | +50     | mV                 |
| $LdR_{VSTBY3}$       | Load regulation                             | $0 < I_{load} < 150 \text{ mA}$                                                                        | -    | -    | 20      | mV                 |
| $V_{doVSTBY3}$       | Drop out voltage                            | $I_{load} = 150 \text{ mA}$                                                                            | -    | -    | 600     | mV                 |
| $I_{shortVSTBY3}$    | Short circuit current limit                 | -                                                                                                      | 250  | -    | 450     | mA                 |
| $OS/US_{VSTBY3}$     | Overshoot/Undershoot                        | $I_{load} 0 \leftrightarrow 150 \text{ mA}$ , $t > 50 \mu\text{s}$<br>$C = 1 \mu\text{F}$ ceramic      | -    | -    | $\pm 5$ | %                  |
| $PSRR_{VSTBY3}$      | Power supply rejection ratio                | $I_{load} = 50 \text{ mA}$<br>$120 \text{ Hz} < f < 10 \text{ kHz}$<br>$V_{BATP_{ac}} = 1 \text{ Vpp}$ | 70   | -    | -       | dB                 |
| $n_{VSTBY3}$         | Output noise                                | A-weighted filter<br>$20 \text{ Hz} < f < 20 \text{ kHz}$<br>$I_{load} = 5 \text{ mA}$                 | -    | -    | 200     | $\mu\text{V}$      |
| $TS_{VSTBY3}$        | Thermal shut-down temperature               | Temperature rising                                                                                     | 150  | -    | 190     | $^{\circ}\text{C}$ |
| $HYS_{TS-VSTBY3}$    | Hysteresis on thermal shut-down temperature | -                                                                                                      | 5    | -    | 15      | $^{\circ}\text{C}$ |
| $ESR_{VSTBY3}$       | External filtering capacitor ESR            | $C > 0.5 \mu\text{F}$                                                                                  | -    | -    | 0.2     | $\Omega$           |
| <b>VSTBY (5 V)</b>   |                                             |                                                                                                        |      |      |         |                    |
| $V_{outVSTBY5}$      | Output voltage                              | $0 < I_{load} < 150 \text{ mA}$                                                                        | 4.80 | 5    | 5.15    | V                  |
| $LnR_{VSTBY5}$       | Line regulation                             | $6 < V_{BATP} < 18V$ $I_{load} = 150 \text{ mA}$                                                       | -10  | -    | +60     | mV                 |
| $LdR_{VSTBY5}$       | Load regulation                             | $0 < I_{load} < 150 \text{ mA}$                                                                        | -    | -    | 25      | mV                 |
| $V_{doVSTBY5}$       | Drop out voltage                            | $I_{load} = 150 \text{ mA}$                                                                            | -    | -    | 600     | mV                 |
| $I_{shortVSTBY5}$    | Short circuit current limit                 | -                                                                                                      | 250  | -    | 450     | mA                 |
| $OS/US_{VSTBY5}$     | Overshoot/Undershoot                        | $I_{load} 0 \leftrightarrow 150 \text{ mA}$ , $t > 50 \mu\text{s}$<br>$C = 1 \mu\text{F}$ ceramic      | -    | -    | $\pm 5$ | %                  |
| $PSRR_{VSTBY5}$      | Power supply rejection ratio                | $I_{load} = 50 \text{ mA}$<br>$120 \text{ Hz} < f < 10 \text{ kHz}$<br>$V_{BATP_{ac}} = 1 \text{ Vpp}$ | 70   | -    | -       | dB                 |
| $n_{VSTBY5}$         | Output noise                                | A-weighted filter<br>$20 \text{ Hz} < f < 20 \text{ kHz}$<br>$I_{load} = 5 \text{ mA}$                 | -    | -    | 200     | $\mu\text{V}$      |
| $TS_{VSTBY5}$        | Thermal shut-down temperature               | Temperature rising                                                                                     | 150  | -    | 190     | $^{\circ}\text{C}$ |
| $HYS_{TS-VSTBY5}$    | Hysteresis on thermal shut-down temperature | -                                                                                                      | 5    | -    | 15      | $^{\circ}\text{C}$ |
| $ESR_{VSTBY5}$       | External filtering capacitor ESR            | $C > 0.5 \mu\text{F}$                                                                                  | -    | -    | 0.2     | $\Omega$           |

Table 5. Electrical characteristics (continued)

| Symbol              | Parameter                                   | Test conditions                                                                                       | Min. | Typ. | Max.    | Unit               |
|---------------------|---------------------------------------------|-------------------------------------------------------------------------------------------------------|------|------|---------|--------------------|
| <b>VLR1 (5 V)</b>   |                                             |                                                                                                       |      |      |         |                    |
| $V_{out\_VLR1-5}$   | Output voltage                              | $0 < I_{load} < 350 \text{ mA}$                                                                       | 4.85 | 5    | 5.15    | V                  |
| $LnR_{VLR1-5}$      | Line regulation                             | $6 < V_{BAT} < 18 \text{ V}$ $I_{load} = 350 \text{ mA}$                                              | -25  | -    | +25     | mV                 |
| $LdR_{VLR1-5}$      | Load regulation                             | $0 < I_{load} < 350 \text{ mA}$                                                                       | -90  | -    | -       | mV                 |
| $V_{do\_VLR1-5}$    | Drop out voltage                            | $I_{load} = 350 \text{ mA}$                                                                           | -    | -    | 650     | mV                 |
| $I_{short\_VLR1-5}$ | Short circuit current limit                 | -                                                                                                     | 500  | 650  | 850     | mA                 |
| $OS/US_{VLR1-5}$    | Overshoot/Undershoot                        | $I_{load} 0 \leftrightarrow 350 \text{ mA}$ , $t > 50 \mu\text{s}$<br>$C = 1 \mu\text{F}$ ceramic     | -    | -    | $\pm 3$ | %                  |
| $PSRR_{VLR1-5}$     | Power supply rejection ratio                | $I_{load} = 170 \text{ mA}$<br>$120 \text{ Hz} < f < 10 \text{ kHz}$<br>$V_{BAT\_ac} = 1 \text{ Vpp}$ | 60   | -    | -       | dB                 |
| $n_{VLR1-5}$        | Output noise                                | A-weighted filter<br>$20 \text{ Hz} < f < 20 \text{ kHz}$<br>$I_{load} = 5 \text{ mA}$                | -    | -    | 350     | $\mu\text{V}$      |
| $TS_{VLR1-5}$       | Thermal shut-down temperature               | Temperature rising                                                                                    | 150  | -    | 190     | $^{\circ}\text{C}$ |
| $HYS_{TS-VLR1-5}$   | Hysteresis on thermal shut-down temperature | -                                                                                                     | 5    | -    | 15      | $^{\circ}\text{C}$ |
| $ESR_{VLR1-5}$      | External filtering capacitor ESR            | $C > 0.5 \mu\text{F}$                                                                                 | -    | -    | 0.2     | $\Omega$           |
| <b>VLR1 (8.5 V)</b> |                                             |                                                                                                       |      |      |         |                    |
| $V_{out\_VLR1-8}$   | Output voltage                              | $0 < I_{load} < 350 \text{ mA}$                                                                       | 8.3  | 8.5  | 8.7     | V                  |
| $LnR_{VLR1-8}$      | Line regulation                             | $9.6 < V_{BAT} < 18 \text{ V}$ $I_{load} = 350 \text{ mA}$                                            | -25  | -    | +25     | mV                 |
| $LdR_{VLR1-8}$      | Load regulation                             | $0 < I_{load} < 350 \text{ mA}$                                                                       | -90  | -    | -       | mV                 |
| $V_{do\_VLR1-8}$    | Drop out voltage                            | $I_{load} = 350 \text{ mA}$                                                                           | -    | -    | 650     | mV                 |
| $I_{short\_VLR1-8}$ | Short circuit current limit                 | -                                                                                                     | 500  | 650  | 850     | mA                 |
| $OS/US_{VLR1-8}$    | Overshoot / undershoot                      | $I_{load} 0 \leftrightarrow 350 \text{ mA}$ , $t > 50 \mu\text{s}$<br>$C = 1 \mu\text{F}$ ceramic     | -    | -    | $\pm 3$ | %                  |
| $PSRR_{VLR1-8}$     | Power supply rejection ratio                | $I_{load} = 170 \text{ mA}$<br>$120 \text{ Hz} < f < 10 \text{ kHz}$<br>$V_{BAT\_ac} = 1 \text{ Vpp}$ | 60   | -    | -       | dB                 |
| $n_{VLR1-8}$        | Output noise                                | A-weighted filter<br>$20 \text{ Hz} < f < 20 \text{ kHz}$<br>$I_{load} = 5 \text{ mA}$                | -    | -    | 350     | $\mu\text{V}$      |
| $TS_{VLR1-8}$       | Thermal shut-down temperature               | Temperature rising                                                                                    | 150  | -    | 190     | $^{\circ}\text{C}$ |
| $HYS_{TS-VLR1-8}$   | Hysteresis on thermal shut-down temperature | -                                                                                                     | 5    | -    | 15      | $^{\circ}\text{C}$ |
| $ESR_{VLR1-8}$      | External filtering capacitor ESR            | $C > 0.5 \mu\text{F}$                                                                                 | -    | -    | 0.2     | $\Omega$           |

Table 5. Electrical characteristics (continued)

| Symbol               | Parameter                                   | Test conditions                                                                                            | Min. | Typ. | Max.    | Unit               |
|----------------------|---------------------------------------------|------------------------------------------------------------------------------------------------------------|------|------|---------|--------------------|
| <b>VLR2 (3.3 V)</b>  |                                             |                                                                                                            |      |      |         |                    |
| $V_{out\_VLR2-3}$    | Output voltage                              | $0 < I_{load} < 1 \text{ A}$                                                                               | 3.2  | 3.3  | 3.4     | V                  |
| $LnR_{VLR2-3}$       | Line regulation                             | $4.5 < VIN_{LR2} < 18 \text{ V}$<br>$I_{load} = 1 \text{ A}$                                               | -20  | -    | +20     | mV                 |
| $LdR_{VLR2-3}$       | Load regulation                             | $0 < I_{load} < 1 \text{ A}$                                                                               | -70  | -    | -       | mV                 |
| $V_{do\_VLR2-3}$     | Drop out voltage                            | $I_{load} = 1 \text{ A}$                                                                                   | -    | -    | 1.2     | V                  |
| $I_{short\_VLR2-3}$  | Short circuit current limit                 |                                                                                                            | 1.5  | -    | 2.5     | A                  |
| $OS/US_{VLR2-3}$     | Overshoot / undershoot                      | $I_{load} 0 \leftrightarrow 1 \text{ A}$ , $t > 50 \mu\text{s}$<br>$C = 1 \mu\text{F}$ ceramic             | -    | -    | $\pm 3$ | %                  |
| $PSRR_{VLR2-3}$      | Power supply rejection ratio                | $I_{load} = 500 \text{ mA}$<br>$120 \text{ Hz} < f < 10 \text{ kHz}$<br>$VIN_{LR2\_ac} = 1 \text{ V}_{pp}$ | 60   | -    | -       | dB                 |
| $n_{VLR2-3}$         | Output noise                                | A-weighted filter<br>$20 \text{ Hz} < f < 20 \text{ kHz}$<br>$I_{load} = 5 \text{ mA}$                     | -    | -    | 350     | $\mu\text{V}$      |
| $TS_{VLR2-3}$        | Thermal shut-down temperature               | Temperature rising                                                                                         | 150  | -    | 190     | $^{\circ}\text{C}$ |
| $HYS_{TS-VLR2-3}$    | Hysteresis on thermal shut-down temperature | -                                                                                                          | 5    | -    | 15      | $^{\circ}\text{C}$ |
| $ESR_{VLR2-3}$       | External filtering capacitor ESR            | $C > 0.5 \mu\text{F}$                                                                                      | -    | -    | 0.2     | $\Omega$           |
| <b>VLR2 (10 V)</b>   |                                             |                                                                                                            |      |      |         |                    |
| $V_{out\_VLR2-10}$   | Output voltage                              | $0 < I_{load} < 1 \text{ A}$                                                                               | 9.7  | 10   | 10.3    | V                  |
| $LnR_{VLR2-10}$      | Line regulation                             | $11.4 < V_{BAT} < 18 \text{ V}$<br>$I_{load} = 1 \text{ A}$                                                | -25  | -    | +25     | mV                 |
| $LdR_{VLR2-10}$      | Load regulation                             | $0 < I_{load} < 1 \text{ A}$                                                                               | -70  | -    | -       | mV                 |
| $V_{do\_VLR2-10}$    | Drop out voltage                            | $I_{load} = 1 \text{ A}$                                                                                   | -    | -    | 0.75    | V                  |
| $I_{short\_VLR2-10}$ | Short circuit current limit                 |                                                                                                            | 1.5  | -    | 2.5     | A                  |
| $OS/US_{VLR2-10}$    | Overshoot / undershoot                      | $I_{load} 0 \leftrightarrow 1 \text{ A}$ , $t > 50 \mu\text{s}$<br>$C = 1 \mu\text{F}$ ceramic             | -    | -    | $\pm 3$ | %                  |
| $PSRR_{VLR2-10}$     | Power supply rejection ratio                | $I_{load} = 500 \text{ mA}$<br>$120 \text{ Hz} < f < 10 \text{ kHz}$<br>$VIN_{LR2\_ac} = 1 \text{ V}_{pp}$ | 60   | -    | -       | dB                 |
| $n_{VLR2-10}$        | Output noise                                | A-weighted filter<br>$20 \text{ Hz} < f < 20 \text{ kHz}$<br>$I_{load} = 5 \text{ mA}$                     | -    | -    | 350     | $\mu\text{V}$      |
| $TS_{VLR2-10}$       | Thermal shut-down temperature               | Temperature rising                                                                                         | 150  | -    | 190     | $^{\circ}\text{C}$ |
| $HYS_{TS-VLR2-10}$   | Hysteresis on thermal shut-down temperature | -                                                                                                          | 5    | -    | 15      | $^{\circ}\text{C}$ |
| $ESR_{VLR2-10}$      | External filtering capacitor ESR            | $C > 0.5 \mu\text{F}$                                                                                      | -    | -    | 0.2     | $\Omega$           |

Table 5. Electrical characteristics (continued)

| Symbol                     | Parameter                                       | Test conditions                                                                              | Min.       | Typ. | Max.   | Unit               |
|----------------------------|-------------------------------------------------|----------------------------------------------------------------------------------------------|------------|------|--------|--------------------|
| <b>HSD1</b>                |                                                 |                                                                                              |            |      |        |                    |
| $V_{drop_{HSD1}}$          | Output saturation                               | $I_{load} = 0.5\text{ A}$                                                                    | -          | -    | 500    | mV                 |
| $I_{leak_{HSD1}}$          | Leakage current                                 | HSD off<br>output shorted to GND                                                             | -          | -    | 10     | $\mu\text{A}$      |
| $I_{short_{HSD1}}$         | Short circuit current limit                     | -                                                                                            | 0.75       | -    | 1.5    | A                  |
| $TS_{HSD1}$                | Thermal shut-down temperature                   | Temperature rising                                                                           | 150        | -    | 190    | $^{\circ}\text{C}$ |
| $HYS_{TS-HSD1}$            | Hysteresis on thermal shut-down temperature     | -                                                                                            | 5          | -    | 15     | $^{\circ}\text{C}$ |
| <b>HSD2</b>                |                                                 |                                                                                              |            |      |        |                    |
| $V_{drop_{HSD2}}$          | Output saturation                               | $I_{load} = 0.5\text{ A}$                                                                    | -          | -    | 500    | mV                 |
| $I_{leak_{HSD2}}$          | Leakage current                                 | HSD off<br>output shorted to GND                                                             | -          | -    | 10     | $\mu\text{A}$      |
| $I_{short_{HSD2}}$         | Short circuit current limit                     | -                                                                                            | 0.75       | -    | 1.5    | A                  |
| $TS_{HSD2}$                | Thermal shut-down temperature                   | Temperature rising                                                                           | 150        | -    | 190    | $^{\circ}\text{C}$ |
| $HYS_{TS-HSD2}$            | Hysteresis on thermal shut-down temperature     | -                                                                                            | 5          | -    | 15     | $^{\circ}\text{C}$ |
| <b>Switching regulator</b> |                                                 |                                                                                              |            |      |        |                    |
| $V_{out_{SW}}$             | Output voltage                                  | Selectable through external resistor divider                                                 | 1.2        | -    | 8      | V                  |
| $I_{LOADmax_{SW}}$         | Load current limitation                         | $V_{out_{SW}}$ decreasing of 100 mV <sup>(1)</sup><br>CLIM = 0 V<br>CLIM = 5 V               | 1.2<br>2.5 | -    | 3<br>6 | A                  |
| $f_{sw}$                   | Free-run switching frequency                    | -                                                                                            | 150        | 180  | 210    | kHz                |
| $V_{FB}$                   | FB voltage                                      | -                                                                                            | 970        | -    | 1030   | mV                 |
| $V_{drop_{SW}}$            | Dropout voltage                                 | $V_{out_{SW}} = 8\text{ V}$<br>$I_{load_{SW}} = 2.5\text{ A}$ <sup>(1)</sup>                 | -          | -    | 1.2    | V                  |
| $f_{SYNC}$                 | Switching frequency selectable through SYNC pin | -                                                                                            | 220        | -    | 400    | kHz                |
| $\eta$                     | Efficiency                                      | free run frequency <sup>(1)</sup><br>$V_{out_{SW}} = 8\text{ V}$ ; $I_{load} = 2.5\text{ A}$ | 85         | -    | -      | %                  |
| $SR_{SS}$                  | Soft-start pin slew rate                        | $C_{SOST} = 10\text{ nF}$ <sup>(1)</sup>                                                     | -          | -    | 10     | V/ms               |
| $TS_{SW}$                  | Thermal shut-down temperature                   | Temperature rising                                                                           | 150        | -    | 190    | $^{\circ}\text{C}$ |
| $HYS_{SW}$                 | Hysteresis on thermal shut-down temperature     | -                                                                                            | 5          | -    | 15     | $^{\circ}\text{C}$ |

Table 5. Electrical characteristics (continued)

| Symbol                    | Parameter                              | Test conditions           | Min.  | Typ. | Max.  | Unit |
|---------------------------|----------------------------------------|---------------------------|-------|------|-------|------|
| <b>Reset function</b>     |                                        |                           |       |      |       |      |
| THR <sub>RST</sub>        | Reset threshold on VSTBY               | VSTBY = 3.3 V             | 93    | -    | 98    | %    |
| HYS <sub>RST</sub>        | Hysteresis on RST                      | -                         | 30    | -    | 150   | mV   |
| Vsat <sub>RST</sub>       | RST pin saturation voltage             | I <sub>RST</sub> = 0.5 mA | -     | -    | 0.4   | V    |
| DLY <sub>RST</sub>        | RST delay time                         | C = 100 pF on RSTDLY pin  | 25    | -    | 75    | µs   |
| Tfall <sub>RST</sub>      | RST fall time                          | R = 47 kΩ<br>C = 50 pF    | -     | -    | 1     | µs   |
| Tglitch <sub>RST</sub>    | Glitch filter time for RST             | -                         | 5     | -    | 20    | µs   |
| THR <sub>RSTDLY</sub>     | RSTDLY pin threshold                   | RST falling               | 3     | -    | 3.7   | V    |
| I <sub>RSTDLY</sub>       | RSTDLY output current                  | RSTDLY = Off              | 7     | -    | 13    | µA   |
| <b>Controls</b>           |                                        |                           |       |      |       |      |
| THR <sub>EN</sub>         | EN minimum level recognized as high    | -                         | 2     | -    | -     | V    |
|                           | EN maximum level recognized as low     | -                         |       | -    | 0.8   | V    |
| HYS <sub>EN</sub>         | Hysteresis on EN                       | -                         | 150   | -    | -     | mV   |
| leak <sub>EN</sub>        | EN pin leakage current                 | -                         | -1    | -    | 1     | µA   |
| THR <sub>CLIM</sub>       | CLIM pin threshold                     | -                         | 0.8   | -    | -     | V    |
|                           |                                        | -                         |       | -    | 2     |      |
| leak <sub>CLIM</sub>      | CLIM pin leakage current               | -                         | -1    | -    | 1     | µA   |
| THR <sub>LVWIN</sub>      | LVWIN threshold                        | -                         | 1.225 | -    | 1.275 | V    |
| HYST <sub>LVWIN</sub>     | LVWIN hysteresis                       | -                         | 100   | -    | 200   | mV   |
| <b>I<sup>2</sup>C bus</b> |                                        |                           |       |      |       |      |
| THR <sub>SCL</sub>        | CLOCK minimum level recognized as High | -                         | 2.2   | -    | -     | V    |
|                           | CLOCK maximum level recognized as low  | -                         | -     | -    | 0.8   | V    |
| THR <sub>SDA</sub>        | DATA minimum level recognized as High  | -                         | 2.2   | -    | -     | V    |
|                           | DATA maximum level recognized as low   | -                         | -     | -    | 0.8   | V    |
| f <sub>SCL</sub>          | Clock frequency                        | -                         | -     | -    | 400   | kHz  |

1. by bench characterization

## 4 Device description

The IC includes one standby regulator, always active to guarantee the standby functions; two switched linear regulators, managed by the I<sup>2</sup>C bus and a step-down switching voltage regulator with selectable current limit.

### 4.1 Regulators

The VSTBY regulator is always active when the IC is supplied.

The other regulators can be enabled or disabled. Their outputs are automatically disabled whenever the VBAT voltage exceeds the over-voltage shutdown threshold. Upon return from over-voltage shutdown, the outputs recover without intervention from the system.

#### 4.1.1 Linear regulators

##### VSTBY (3.3 V / 5.0 V standby)

VSTBY is a linearly regulated 3.3/5 V output. This output is enabled on battery connect. It is supplied from the protected battery input (VBATP).

In order to select the 3.3 V output, the VSTBYSEL pin must be connected to ground.

In order to select the 5.0 V output, the VSTBYSEL pin must be connected to 5 V.

When the dropout voltage of the regulator cannot be maintained, the output shall track the VBATP input voltage less the saturation voltage of the regulator pass element.

This regulator has a short circuit protection consisting of current limit, and thermal shutdown. If the local die temperature exceeds the thermal shutdown detection threshold, the output is disabled. The thermal shutdown circuitry has hysteresis such that the output is enabled only after the die temperature falls below the thermal shutdown disable threshold. Thermal shutdown on this output doesn't directly disable any other circuitry.

RST provides an indication that VSTBY is in regulation. It is an open drain output used to indicate that VSTBY is in regulation (below the low-voltage threshold). RST remains low until VSTBY achieves regulation and the RSTDLY input has charged to its threshold. For instance, RST remains low during battery connect and disconnect and under low-voltage battery lockout. The transition from standby mode to active mode (and vice versa) does not cause the RST output to be triggered.

RSTDLY provides a means to delay the releasing of RST once VSTBY has achieved regulation. It is used to delay the release of RST when VSTBY achieves regulation. This input has a current source to charge an external capacitor and an internal pull-down to discharge the external capacitor. The voltage on this capacitor is used to control the operation of the RST output.

The RSTDLY pull-down is activated when a loss of regulation is detected. The input remains low until VSTBY once again achieves regulation.

When the RSTDLY is released the current source charges the external capacitor. When the voltage exceeds the pin's threshold, RST pin is also released, disabling its pull-down.

**VLR1 (5.0 V /8.5 V) and VLR2 (3.3 V, 5.0 V, 5.5 V, 6.0 V, 7.0 V, 7.5 V, 8.0 V, 10.0 V)**

The output of these two regulators can be selected through the I<sup>2</sup>C bus.

When the dropout voltage of the regulator cannot be maintained, the output tracks the VBAT input voltage less the saturation voltage of the regulator pass element.

This regulator has a short circuit protection consisting of current limit and thermal shutdown. If the local die temperature exceeds the thermal shutdown detection threshold, the output is disabled. The thermal shutdown circuitry has hysteresis such that the output is enabled only after the die temperature falls below the thermal shutdown disable threshold. Thermal shutdown on this output doesn't directly disable any other circuitry.

VLR2 has its own power supply (VINLR2) because of its high current capability.

**4.1.2 Switching regulator**

The IC contains an independent, step-down, synchronous switching regulator, which is used to produce an output voltage that is adjustable in the system by means of an external resistor divider.

The switching regulator functionality is guaranteed in the 1.2-8.0 V output voltage range. The switching frequency is externally synchronizable. The switcher has its own supply input pin (VINSW) and is enabled by the EN input.

The regulator contains soft-start control to protect external devices from excessive in-rush currents. This control is independent of the presence of a synchronizing signal on the SYNCH input.

The switching cycle is synchronized to the internal oscillator unless a signal is present on the SYNC input. The signal present on the SYNCH input overrides the internal oscillator to control the switching of the regulator if its frequency gets inside the allowed range (220-400 kHz). The IC detects a small number of edges (e.g. 2-5) prior to recognize a valid input signal and synchronizing internal operation to the external signal.

It is designed to operate in continuous conduction mode (CCM), where the inductor current remains continuous throughout the entire load range of the output. It can also work in DCM mode.

This regulator has short circuit protection consisting of cycle-by-cycle duty-cycle limitation.

Upon return from over-voltage shutdown this regulator employs the soft-start.

An external bootstrap capacitor must be connected between the output (PH, phase output pin) and the CBS pin.

The switching regulator output slew rate can be controlled with an external capacitor on the SOST (soft start) pin. This protects the device against excessive dV/dt transients, lowering the stress of the internal components. A maximum slews rate of 10 V/ms is suggested.

Two separate current limits for the switching regulator can be chosen in order to guarantee a proper protection for the device at the desired load current rating. The CLIM pin should be tied to ground for the low limit (max 3 A) or to 5.0 V for the high limit (max 6 A).

The VFB pin is the voltage feedback from the regulated output for the switching regulator; the VCMP one is the compensation feedback for the switching regulator.

## 4.2 High side drivers

The device embeds fully-protected high-side drivers for use outside of the car-radio module.

### HSD1, HSD2

These high side driver outputs have short circuit protections consisting of current limit and independent thermal shutdown. If the local die temperature exceeds the thermal shutdown detection threshold, the output is disabled. The thermal shutdown circuitry has hysteresis such that the output is enabled only after the die temperature falls below the thermal shutdown disable threshold. Thermal shutdown on any one output doesn't directly disable any other circuitry.

HSD1 and HSD2 are protected from shorts to ground and shorts to battery (0-18 V) during a loss of car-radio module battery.

## 5 Operating mode

When a power source is connected to the IC, the internal circuitry begins to establish internal bias, the bandgap reference voltage, and other related functions. The standby (VSTBY) regulator and battery detection are functional.

The standby mode is activated when the enable (EN) input is asserted low.

When the enable (EN) input is set high (EN = 1: active mode.), the IC exits the standby mode and enters the active mode.

During active mode, I2C interface is activated and all functions are operational. The IC remains in active mode until either the standby regulator falls out of regulation (where the IC enters the low-voltage reset state) or until the enable (EN) input is brought back to 0 V (where the IC enters the standby state).

### 5.1 Battery detection

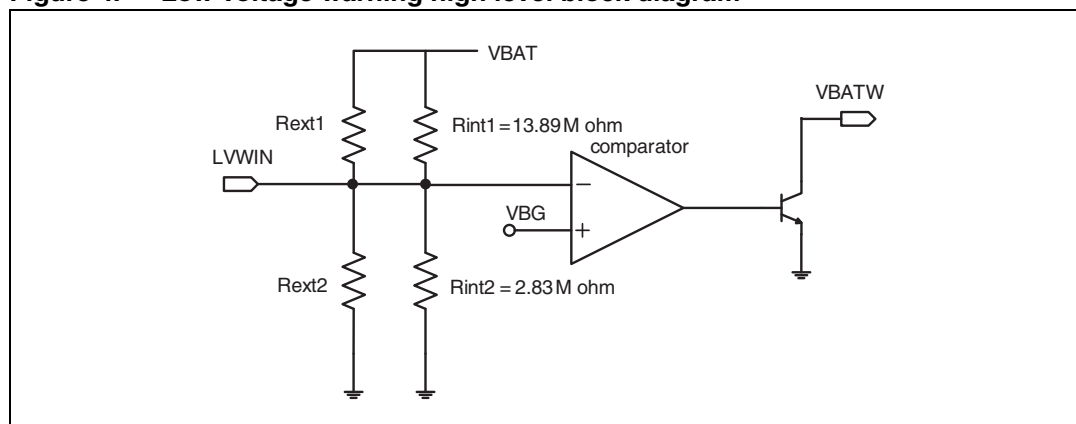
The operating voltage for VLR1, high side drivers and battery warnings is provided by VBAT pin. This input is also used as reference to detect an over-voltage or an under-voltage condition. When such condition is detected, the VBATVW output is pulled down. The overvoltage detection circuit has hysteresis for noise rejection.

Two external resistors (Rext1, Rext2), whose values are lower than 100 kohm, are connected to the LVWIN (low warning input) pin to give the possibility to trim the threshold at which the low voltage warning comparator triggers. When LVWIN voltage is below the input voltage threshold (1.25 V typ), the VBATW (battery voltage warning) output is pulled down and a low-voltage warning is indicated. When no external resistor network is connected to LVWIN, the detector sets the threshold to a nominal 7.5 V.

No external interaction is required to reset the output state, because it is automatically reset when the fault condition is removed.

*Figure 4* shows an high level block diagram of the low-voltage warning circuit. VBAT is divided by two internal resistors (Rint1, Rint2) and two external programming resistors (Rext1, Rext2). When VBAT decreases so that LVWIN voltage gets lower than the internal reference (VBG), VBATW is pulled down to ground.

**Figure 4. Low voltage warning high level block diagram**



## 6 I<sup>2</sup>C bus interface

Data transmission from microprocessor to the L5962 and viceversa takes place through the 2 wires I<sup>2</sup>C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

### 6.1 Data validity

As shown by [Figure 5](#), the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

### 6.2 Start and stop conditions

As shown by [Figure 6](#) a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

### 6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

### 6.4 Acknowledge

The transmitter\* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see [Figure 6](#)). The receiver\*\* the acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

\* Transmitter

- master (μP) when it writes an address to the L5962
- slave (L5962) when the μP reads a data byte from L5962

\*\* Receiver

- slave (L5962) when the μP writes an address to the L5962
- master (μP) when it reads a data byte from L5962

**Figure 5. Data validity on the I<sup>2</sup>C bus**

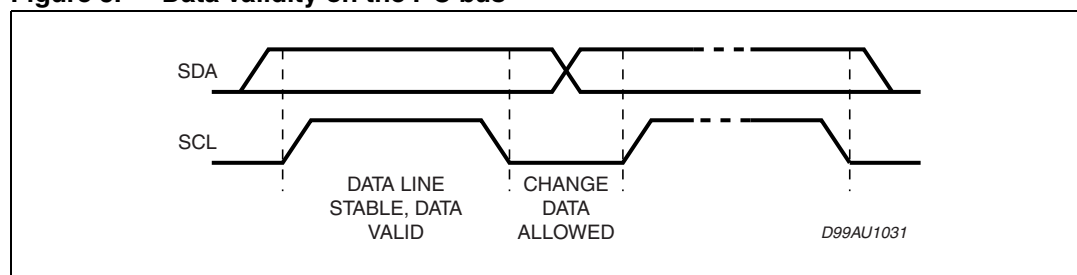


Figure 6. Timing diagram on the I<sup>2</sup>C bus

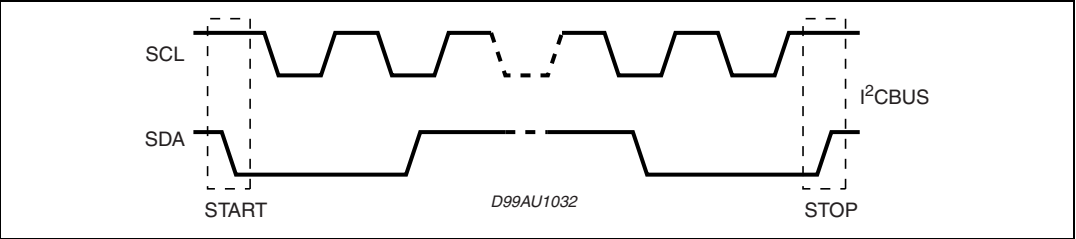
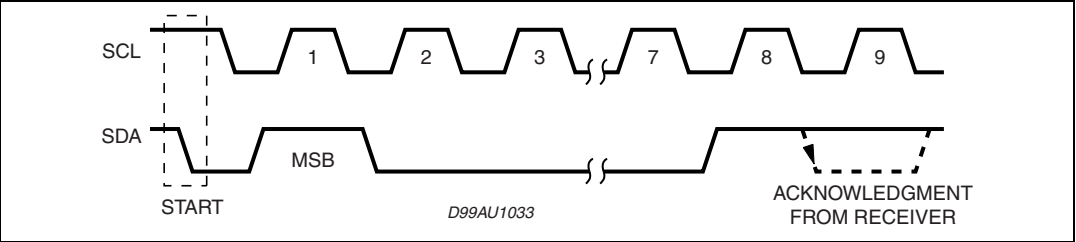


Figure 7. Acknowledge on the I<sup>2</sup>C bus



## 7 Software specifications

**Table 6. Chip address**

| D7 (MSB) |   |   |   |   |   |   | D0 (LSB) | 10 Hex |
|----------|---|---|---|---|---|---|----------|--------|
| 0        | 0 | 0 | 1 | 0 | 0 | 0 | R/W      |        |

IC functions can be driven sending one data byte IB1

**Table 7. IB1 data byte**

| Bit position | Bit name | Function description |
|--------------|----------|----------------------|
| D7           | VLR2EN   | VLR2 enable          |
| D6           | VLR2SEL2 | VLR2 selection       |
| D5           | VLR2SEL1 |                      |
| D4           | VLR2SEL0 |                      |
| D3           | VLR1EN   | VLR1 enable          |
| D2           | VLR1SEL  | VLR1 selection       |
| D1           | HSD2EN   | HSD2 enable          |
| D0           | HSD1EN   | HSD1 enable          |

Bits D6-D4 are used to select VLR2 output voltage according to the following table

**Table 8. VLR2 output level selection**

| VLR2SEL2 | VLR2SEL1 | VLR2SEL0 | VLR2 output voltage |
|----------|----------|----------|---------------------|
| 0        | 0        | 0        | 3.3V                |
| 0        | 0        | 1        | 5.0V                |
| 0        | 1        | 0        | 5.5V                |
| 0        | 1        | 1        | 6.0V                |
| 1        | 0        | 0        | 7.0V                |
| 1        | 0        | 1        | 7.5V                |
| 1        | 1        | 0        | 8.0V                |
| 1        | 1        | 1        | 10.0V               |

## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

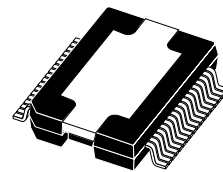
ECOPACK<sup>®</sup> is an ST trademark.

**Figure 8. PowerSO36 (slug-up) mechanical data and package dimensions**

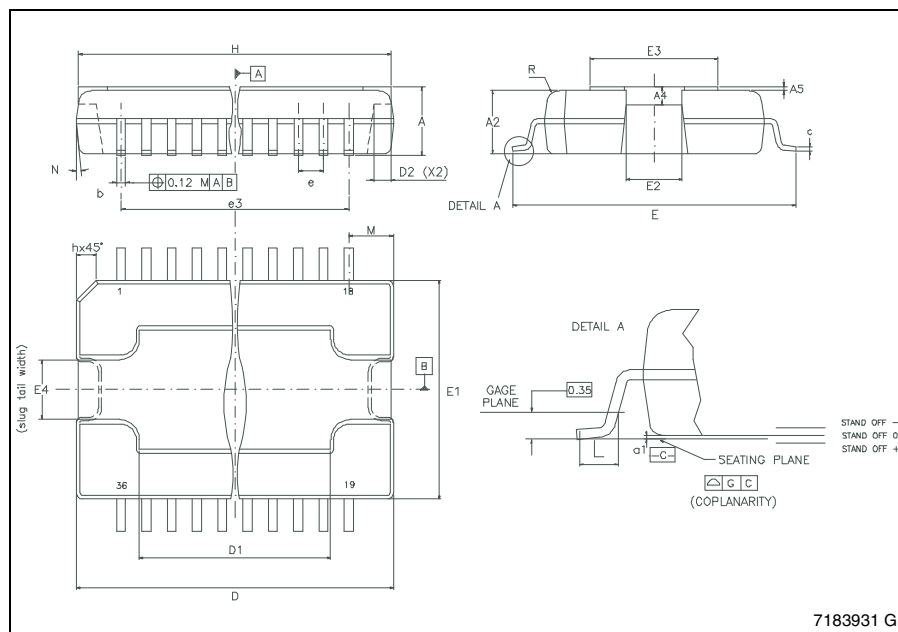
| DIM. | mm     |        |        | inch   |        |         |
|------|--------|--------|--------|--------|--------|---------|
|      | MIN.   | TYP.   | MAX.   | MIN.   | TYP.   | MAX.    |
| A    | 3.270  | -      | 3.410  | 0.1287 | -      | 0.1343  |
| A2   | 3.100  | -      | 3.180  | 0.1220 | -      | 0.1252  |
| A4   | 0.800  | -      | 1.000  | 0.0315 | -      | 0.0394  |
| A5   | -      | 0.200  | -      | -      | 0.0079 | -       |
| a1   | 0.030  | -      | -0.040 | 0.0012 | -      | -0.0016 |
| b    | 0.220  | -      | 0.380  | 0.0087 | -      | 0.0150  |
| c    | 0.230  | -      | 0.320  | 0.0091 | -      | 0.0126  |
| D    | 15.800 | -      | 16.000 | 0.6220 | -      | 0.6299  |
| D1   | 9.400  | -      | 9.800  | 0.3701 | -      | 0.3858  |
| D2   | -      | 1.000  | -      | -      | 0.0394 | -       |
| E    | 13.900 | -      | 14.500 | 0.5472 | -      | 0.5709  |
| E1   | 10.900 | -      | 11.100 | 0.4291 | -      | 0.4370  |
| E2   | -      | -      | 2.900  | -      | -      | 0.1142  |
| E3   | 5.800  | -      | 6.200  | 0.2283 | -      | 0.2441  |
| E4   | 2.900  | -      | 3.200  | 0.1142 | -      | 0.1260  |
| e    | -      | 0.650  | -      | -      | 0.0256 | -       |
| e3   | -      | 11.050 | -      | -      | 0.4350 | -       |
| G    | 0      | -      | 0.075  | 0      | -      | 0.0031  |
| H    | 15.500 | -      | 15.900 | 0.6102 | -      | 0.6260  |
| h    | -      | -      | 1.100  | -      | -      | 0.0433  |
| L    | 0.800  | -      | 1.100  | 0.0315 | -      | 0.0433  |
| N    | -      | -      | 10°    | -      | -      | 10°     |
| s    | -      | -      | 8°     | -      | -      | 8°      |

- (1) "D and E1" do not include mold flash or protrusions.  
Mold flash or protrusions shall not exceed 0.15mm (0.006").  
(2) No intrusion allowed inwards the leads.

### OUTLINE AND MECHANICAL DATA



### PowerSO36 (SLUG UP)



## 9 Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                                                         |
|-------------|----------|-------------------------------------------------------------------------------------------------|
| 24-Nov-2009 | 1        | Initial release.                                                                                |
| 10-Dec-2009 | 2        | Updated <i>Figure 8: PowerSO36 (slug-up) mechanical data and package dimensions on page 22.</i> |
| 18-Sep-2013 | 3        | Updated Disclaimer.                                                                             |

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