

October 2013

FQP4N20L

N-Channel QFET® MOSFET

200 V, 3.8 A, 1.35 Ω

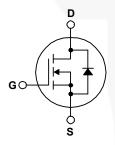
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation modes. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, and motor control.

Features

- 3.8 A, 200 V, $\rm R_{DS(on)}$ = 1.35 Ω (Max.) @ $\rm V_{GS}$ = 10 V, $\rm I_D$ = 1.9 A
- Low Gate Charge (Typ. 4.0 nC)
- Low Crss (Typ. 6.0 pF)
- · 100% Avalanche Tested





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	0.19	FQP4N20L	Unit
V _{DSS}	Drain-Source Voltage		200	V
I _D	Drain Current - Continuous (T _C = 25°C)		3.8	Α
	- Continuous (T _C = 100°C)		2.4	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	15.2	А
V _{GSS}	Gate-Source Voltage		± 20	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	52	mJ
I _{AR}	Avalanche Current	(Note 1)	3.8	A
E _{AR}	Repetitive Avalanche Energy	(Note 1)	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	5.5	V/ns
P_{D}	Power Dissipation (T _C = 25°C)		45	W
	- Derate above 25°C		0.36	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQP4N20L	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.78	°C/W	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP4N20L	FQP4N20L	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	racteristics					
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		0.16		V/°C
I _{DSS}	Zana Oata Vallana Basis Oursel	V _{DS} = 200 V, V _{GS} = 0 V			1	μΑ
	Zero Gate Voltage Drain Current	V _{DS} = 160 V, T _C = 125°C			10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
On Cha	racteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1.0		2.0	V
R _{DS(on)}	Static Drain-Source	V _{GS} = 10 V, I _D = 1.9 A		1.10	1.35	
DO(011)	On-Resistance	$V_{GS} = 5 \text{ V}, I_D = 1.9 \text{ A}$	-	1.13	1.40	Ω
g _{FS}	Forward Transconductance	V _{DS} = 25 V, I _D = 1.9 A		3.2		S
Dynam	ic Characteristics					
C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		240	310	pF
C _{oss}	Output Capacitance	f = 1.0 MHz		36	45	pF
C _{rss}	Reverse Transfer Capacitance			6	8	pF
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V 400 V I 0.0 A		7	25	ns
t _r	Turn-On Rise Time	$V_{DD} = 100 \text{ V}, I_{D} = 3.8 \text{ A},$ $R_{G} = 25 \Omega$		70	150	ns
t _{d(off)}	Turn-Off Delay Time	NG - 20 12		15	40	ns
t _f	Turn-Off Fall Time	(Note 4		40	90	ns
Qg	Total Gate Charge	$V_{DS} = 160 \text{ V}, I_{D} = 3.8 \text{ A},$		4.0	5.2	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 5 V	/	1.0		nC
Q _{gd}	Gate-Drain Charge	(Note 4)		1.9		nC
Drain-S	ource Diode Characteristics ar	nd Maximum Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				3.8	Α
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				15.2	Α
V_{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 3.8 A)	1.5	V
t _{rr}	Reverse Recovery Time	00 1 7 0 1 1		90	//	ns
Q _{rr}	Reverse Recovery Charge			0.25		μС

- **Notes:**1. Repetitive rating : pulse-width limited by maximum junction temperature.
 2. L = 5.4 mH, I_{AS} = 3.8 A, V_{DD} = 50 V, R_{G} = 25 Ω_{c} starting T_{J} = 25°C.
 3. I_{SD} ≤ 3.8 A, di/dt ≤ 300 A/ μ s, V_{DD} ≤ BV $_{DSS}$, starting T_{J} = 25°C.
 4. Essentially independent of operating temperature.

Typical Characteristics

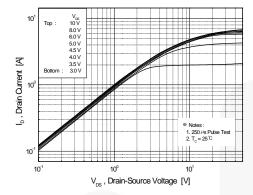


Figure 1. On-Region Characteristics

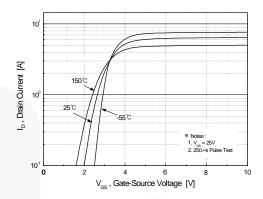


Figure 2. Transfer Characteristics

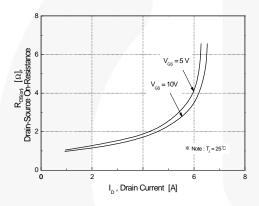


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

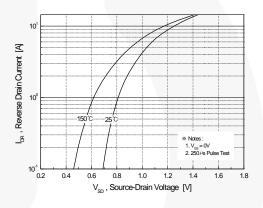


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

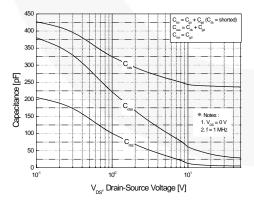


Figure 5. Capacitance Characteristics

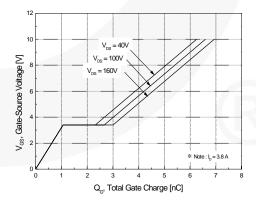


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

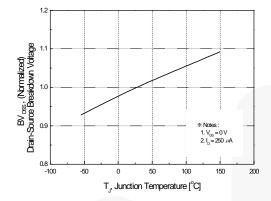


Figure 7. Breakdown Voltage Variation vs. Temperature

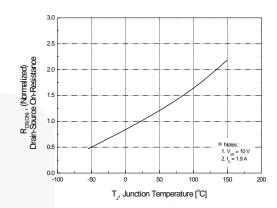


Figure 8. On-Resistance Variation vs. Temperature

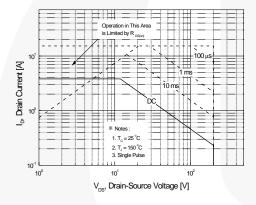


Figure 9. Maximum Safe Operating Area

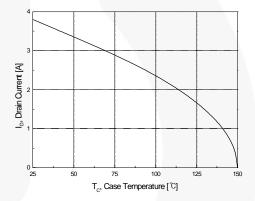


Figure 10. Maximum Drain Current vs. Case Temperature

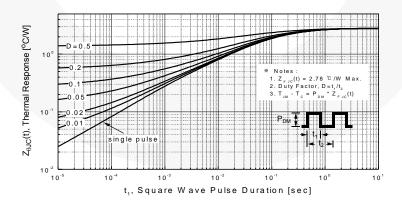


Figure 11. Transient Thermal Response Curve

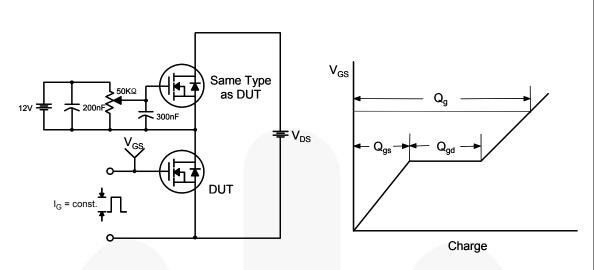


Figure 12. Gate Charge Test Circuit & Waveform

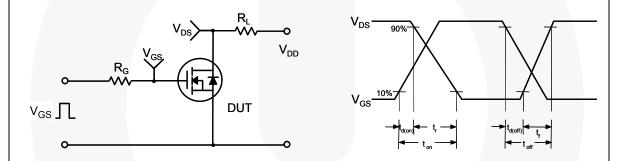


Figure 13. Resistive Switching Test Circuit & Waveforms

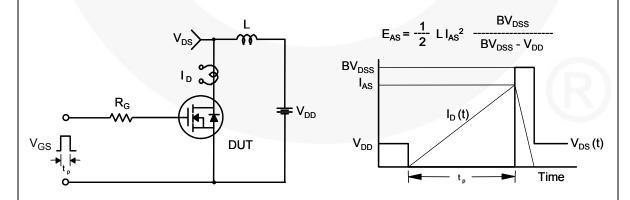
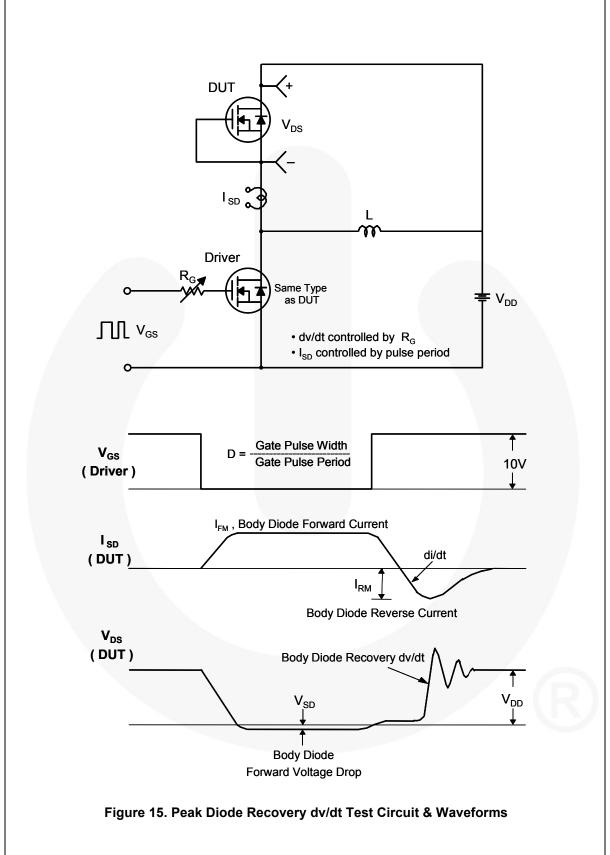


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions

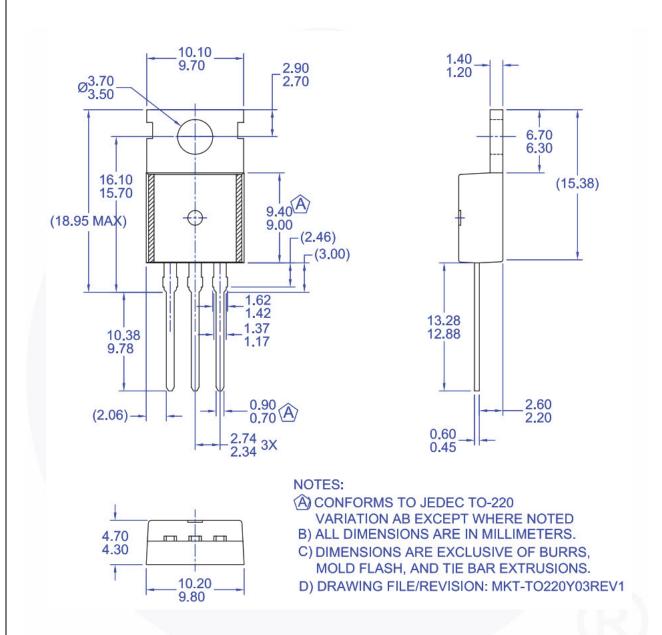


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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