NCP51460

20 mA Micropower Precision Voltage Reference

The NCP51460 is a high performance, low power precision voltage reference. This device combines very high accuracy, low power dissipation and small package size. It can supply output current up to 20 mA at a 3.3 V fixed output voltage with excellent line and load regulation characteristics making it ideal for precision regulator applications. It is designed to be stable with or without an output capacitor. The protective features include Short Circuit and Reverse Input Voltage Protection. The NCP51460 is packaged in a 3−lead surface mount SOT−23 package.

Features

- Fixed Output Voltage 3.3 V
- V_{OUT} Accuracy 1% over 0 to +100°C
- Wide Input Voltage Range up to 28 V
- Low Quiescent Current
- Low Noise
- Reverse Input Voltage Protection
- Stable Without an Output Capacitor
- Available in 3 leads SOT−23 Package
- Pb−Free Package is Available

Typical Applications

- Handheld Instruments
- Precision Regulators
- Data Acquisition Systems
- High Accuracy Micropower Supplies

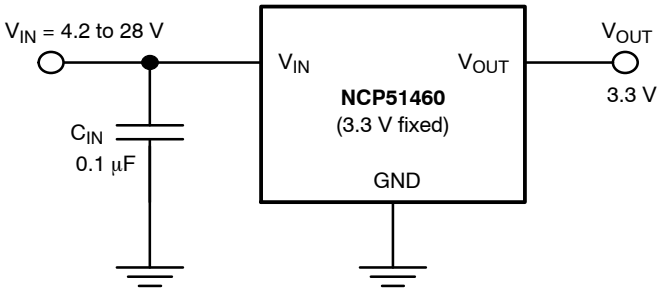

Figure 1. Typical Application Schematics

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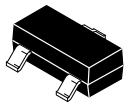
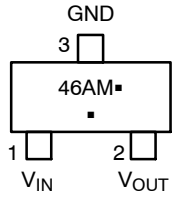
http://onsemi.com



SOT−23
SN1 SUFFIX
CASE 318

MARKING DIAGRAM AND PIN ASSIGNMENT



(Top View)

46A = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V_{IN}	Positive Input Voltage
2	V_{OUT}	Regulated Output Voltage
3	GND	Power Supply Ground; Device Substrate

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	30	V
Reverse Input Voltage	V_{IN}	−15	V
Output Short Circuit Duration, T_A = 25°C $V_{IN} \le 27$ V $V_{IN} > 27$ V	t_{SC}	 ∞ 50	sec
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latch up Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT−23 package Thermal Resistance, Junction−to−Ambient (Note 3)	$R_{\theta JA}$	246	°C/W

3. Soldered on 1 oz 50 mm^2 FR4 copper area.

Table 4. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Operating Input Voltage (Note 4)	V_{IN}	V_{OUT} + 0.9	28	V
Operating Ambient Temperature Range	T_A	0	100	°C

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS (V_{IN} = V_{OUT} + 2.5 V, I_{OUT} = 0, C_{IN} = 0.1 μF, C_{OUT} = 0 μF; For typical values T_A = 25°C, for min/max values 0°C ≤ T_A ≤ 100°C unless otherwise noted.) (Note 5).

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Output Voltage		V_{OUT}	3.267 (–1%)	3.3	3.333 (+1%)	V
Line Regulation	V_{IN} = V_{OUT} + 0.9 V to V_{OUT} + 2.5 V V_{IN} = V_{OUT} + 2.5 V to V_{OUT} + 20 V	Reg_{LINE}	– –	150 65	500 130	ppm/V
Load Regulation	I_{OUT} = 0 to 100 μA I_{OUT} = 0 to 10 mA I_{OUT} = 0 to 20 mA	Reg_{LOAD}	– – –	1100 150 120	4000 300 300	ppm/mA
Dropout Voltage	Measured at V_{OUT} – 2% I_{OUT} = 0 mA I_{OUT} = 10 mA	V_{DO}	 – –	 0.65 0.9	 0.9 1.4	V
Quiescent Current	I_{OUT} = 0 mA, T_A = 25°C I_{OUT} = 0 mA, 0°C ≤ T_A ≤ 100°C	I_Q	– –	140	200 220	μA
Output Short Circuit Current	V_{OUT} = 0 V, T_A = 25°C	I_{SC}	–	80	–	mA
Reverse Leakage	V_{IN} = – 15 V, T_A = 25°C	I_{LEAK}	–	0.1	10	μA
Output Noise Voltage (Note 6)	f = 0.1 Hz to 10 Hz f = 10 Hz to 1 kHz	V_N	–	12 18	–	μV_{PP} μV_{rms}
Output Voltage Temperature Coefficient	0°C ≤ T_A ≤ 100°C	T_{CO}	–	18	–	ppm/°C

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization, tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. The noise spectral density from 0.1 Hz to 10 Hz is measured, then the integral output noise voltage in this range is calculated. Finally the peak to peak noise is calculated as 5x integral output noise.

TYPICAL CHARACTERISTICS

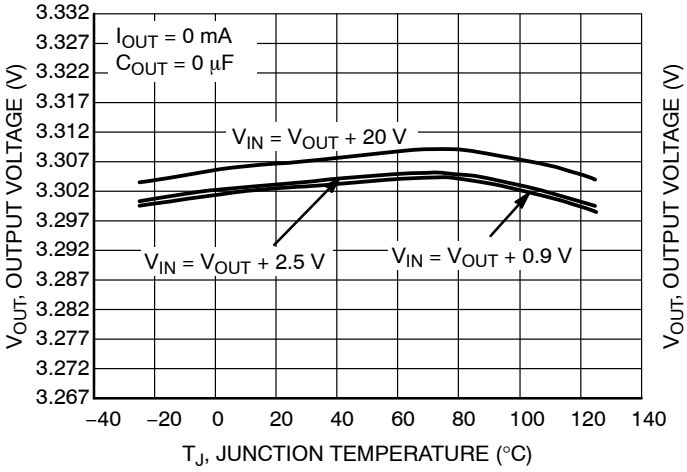


Figure 2. Output Voltage vs. Temperature

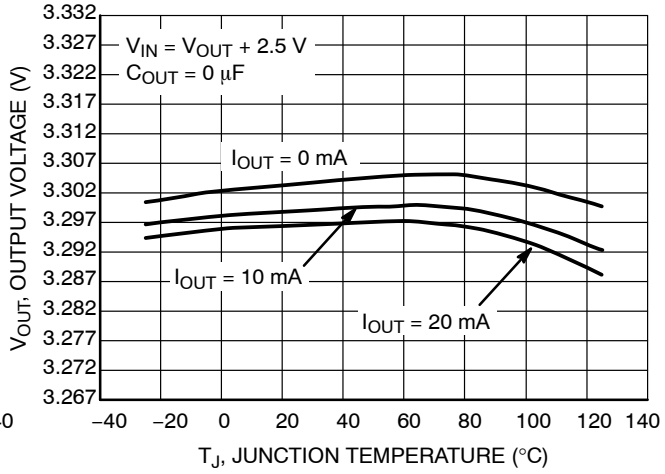


Figure 3. Output Voltage vs. Temperature

TYPICAL CHARACTERISTICS

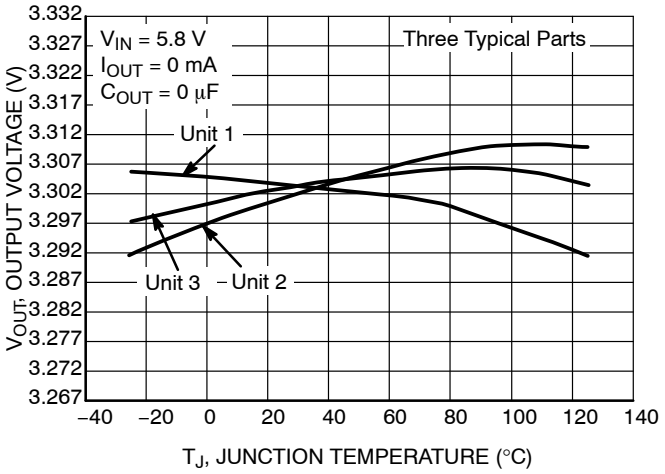


Figure 4. Output Voltage vs. Temperature

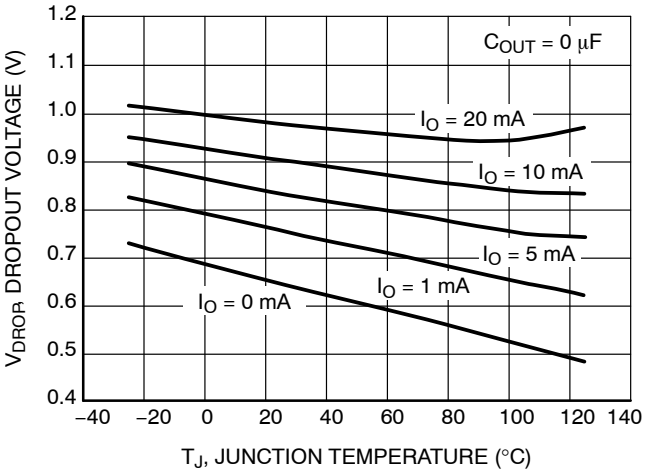


Figure 5. Dropout Voltage

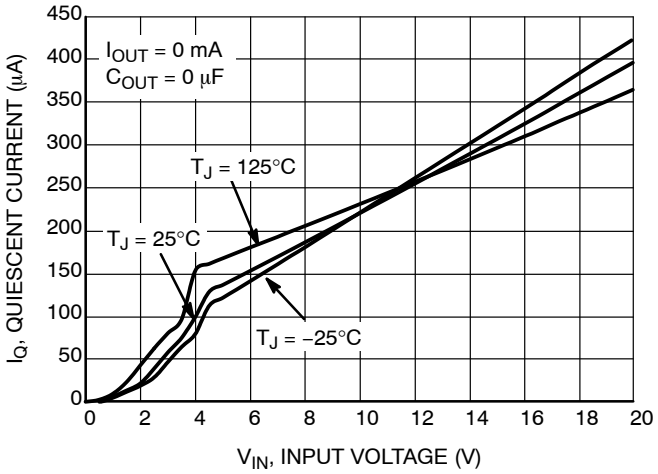


Figure 6. Quiescent Current

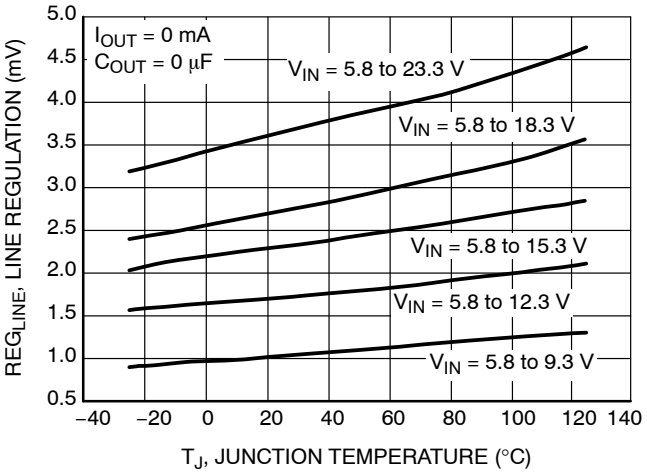


Figure 7. Line Regulation

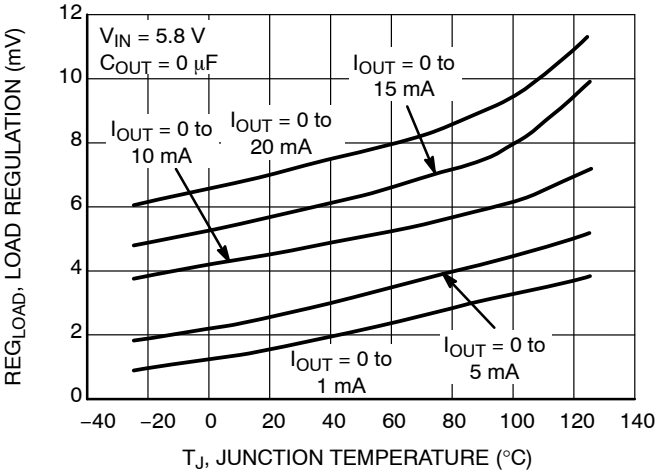


Figure 8. Load Regulation Sourcing

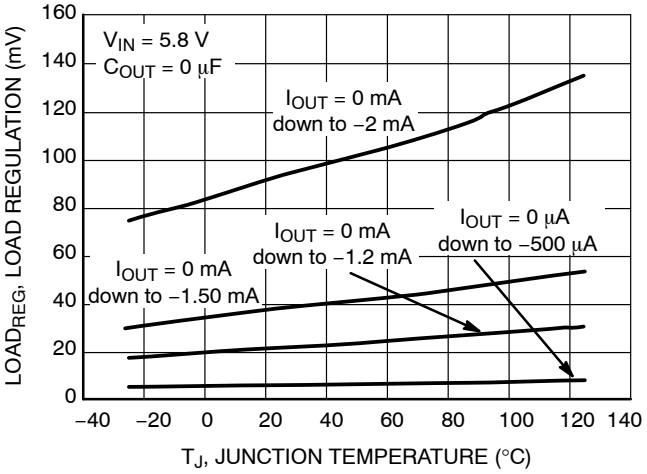


Figure 9. Load Regulation Sinking

TYPICAL CHARACTERISTICS

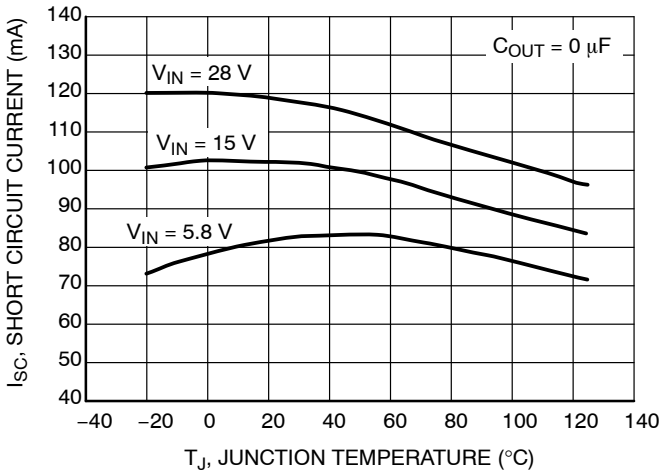


Figure 10. Short Circuit Current

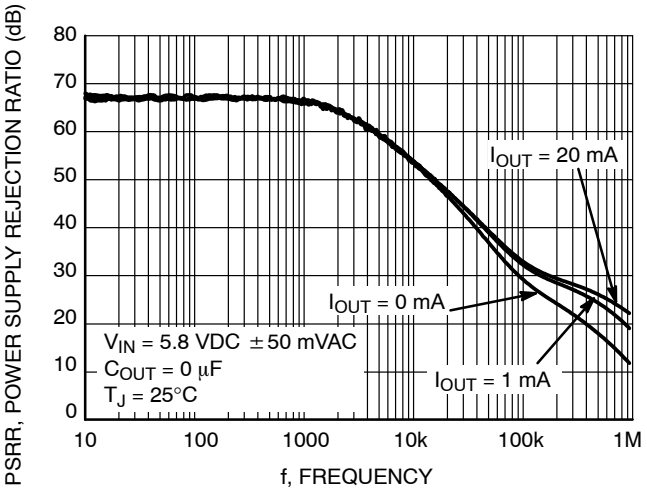


Figure 11. Power Supply Rejection Ratio C_{out} = 0 μF

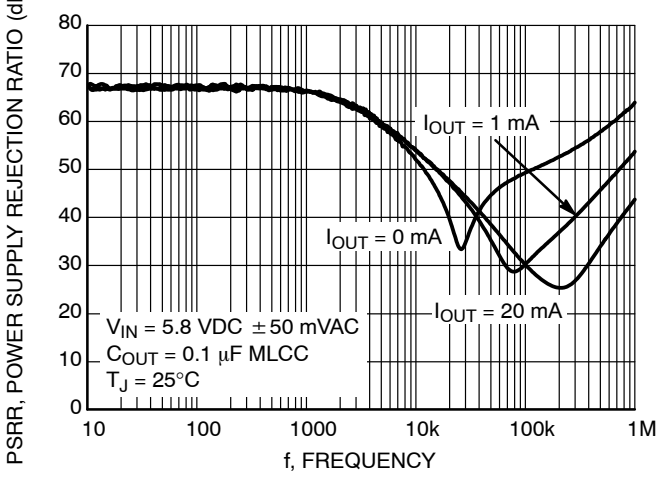


Figure 12. Power Supply Rejection Ratio C_{out} = 0.1 μF

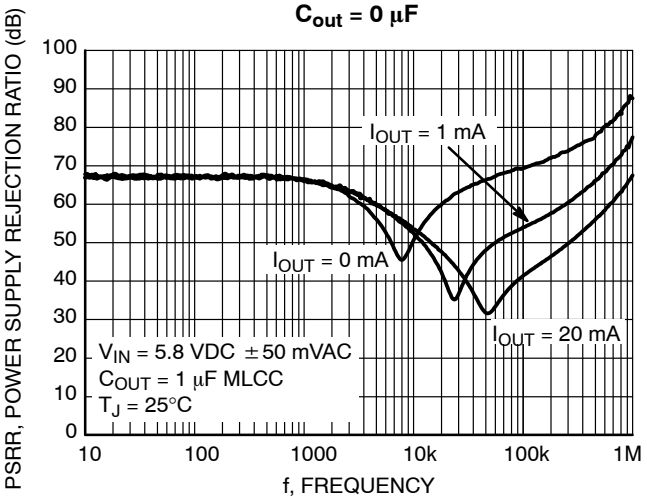


Figure 13. Power Supply Rejection Ratio C_{out} = 1 μF

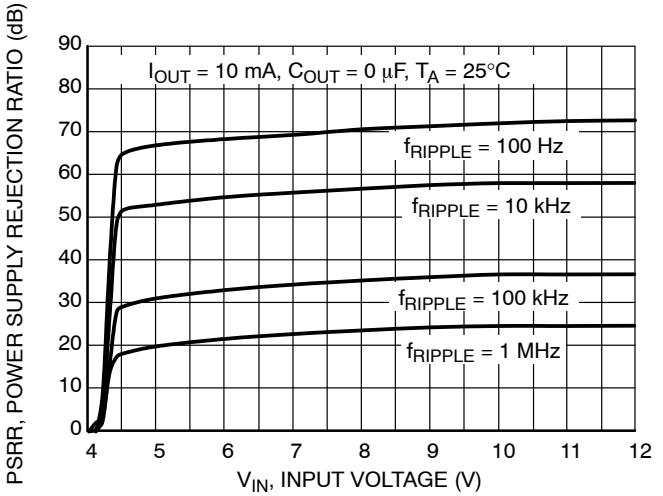


Figure 14. Power Supply Rejection Ratio vs. Input Voltage

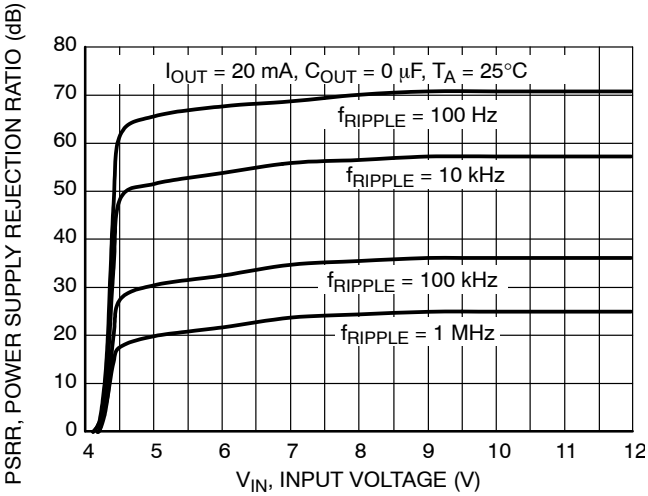


Figure 15. Power Supply Rejection Ratio vs. Input Voltage

TYPICAL CHARACTERISTICS

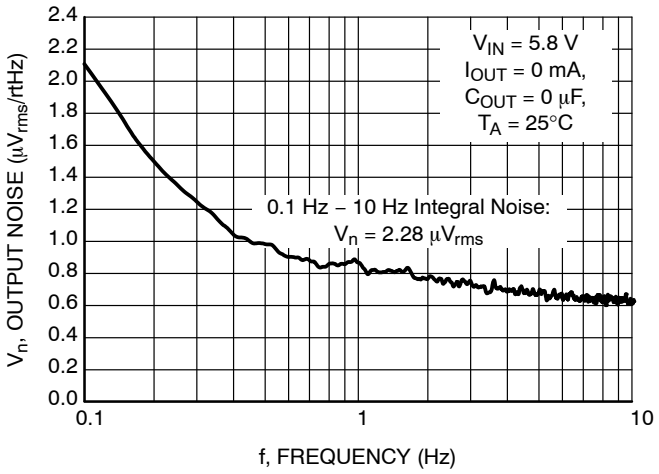


Figure 16. Output Voltage Noise 0.1 Hz – 10 Hz

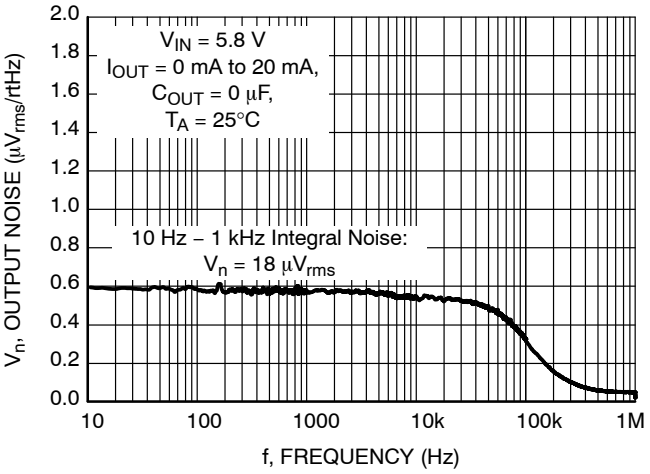


Figure 17. Output Voltage Noise 10 Hz – 1 MHz

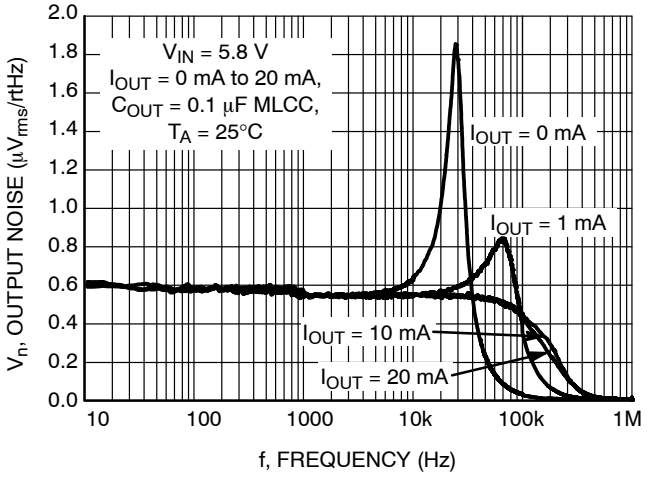


Figure 18. Output Voltage Noise 10 Hz – 1 MHz
C_{OUT} = 0.1 μF

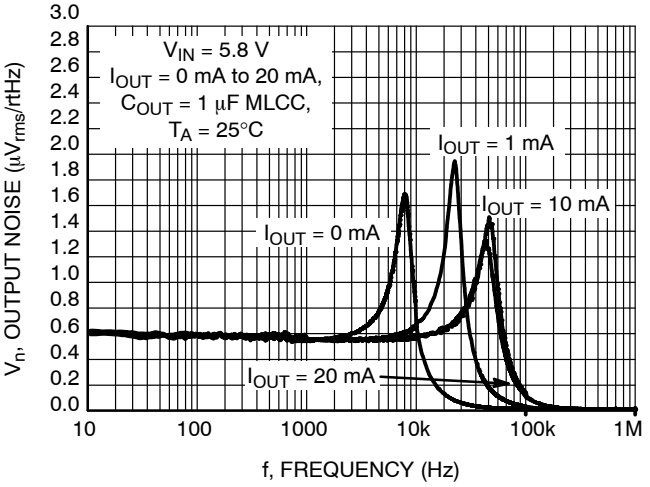


Figure 19. Output Voltage Noise 10 Hz – 1 MHz
C_{OUT} = 1 μF

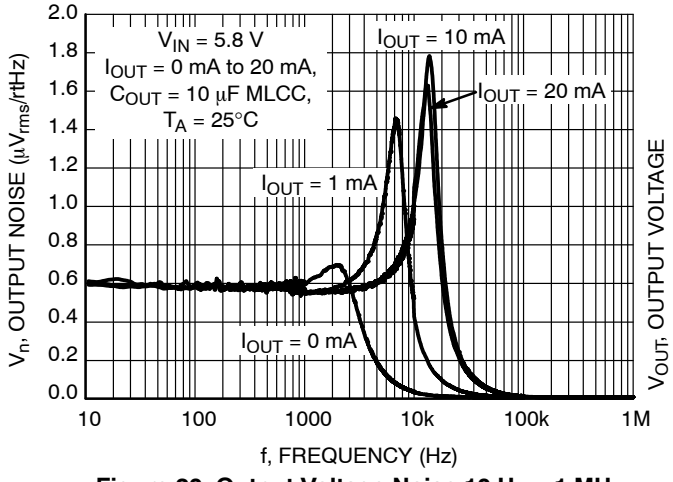


Figure 20. Output Voltage Noise 10 Hz – 1 MHz
C_{OUT} = 10 μF

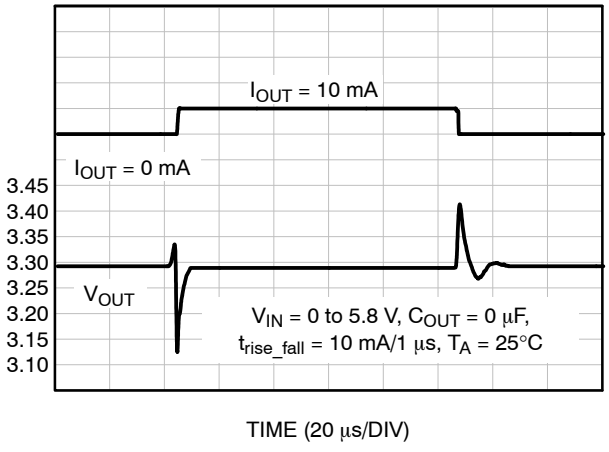


Figure 21. Load Transient Response 0 – 10 mA

TYPICAL CHARACTERISTICS

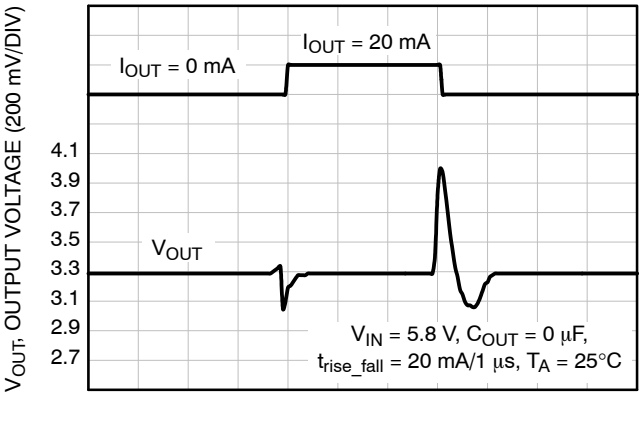


Figure 22. Load Transient Response 0 – 20 mA

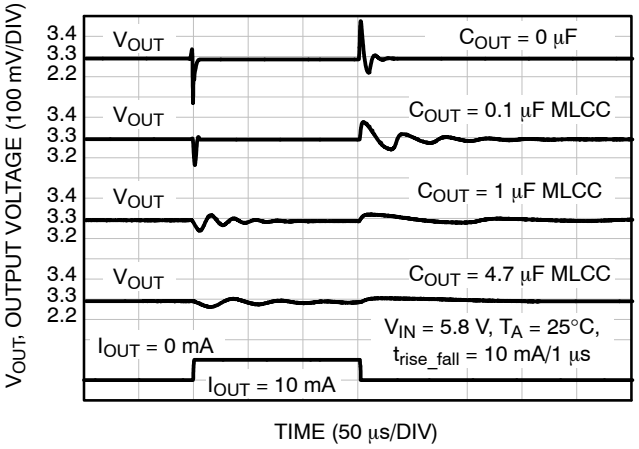


Figure 23. Load Transient Responses C_{OUT} = 0 – 4.7 μF

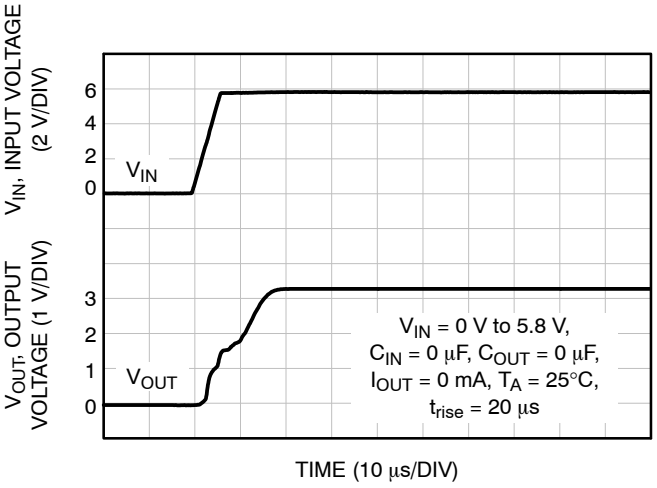


Figure 24. Turn−On

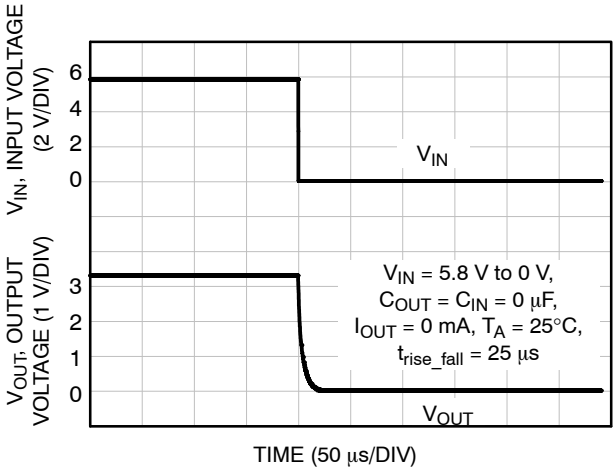


Figure 25. Turn−Off

APPLICATIONS INFORMATION

Input Decoupling Capacitor (C_{IN})

It is recommended to connect a 0.1 μF Ceramic capacitor between V_{IN} and GND pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise present on the input voltage. The input capacitor will also limit the influence of input trace inductances and Power Supply resistance during sudden load current changes. Higher capacitances will improve the Power Supply Rejection Ratio and line transient response.

Output Decoupling Capacitor (C_{OUT})

The NCP51460 was designed to be stable without an additional output capacitor. Without the output capacitor the V_{OUT} settling times during Reference Turn−on or Turn−off can be as short as 20 μs (Refer to Figure 24 and 25). The Load Transient Responses without C_{OUT} (Figure 21 and 22) show good stability of NCP51460 even for fast output current changes from 0 mA to full load. If smaller V_{OUT} deviations during load current changes are required, it is possible to add some external capacitance as shown on Figure 26.

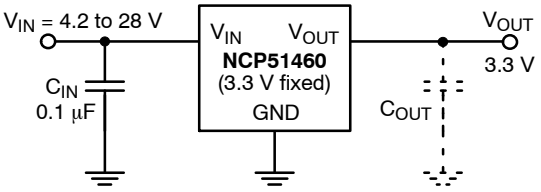


Figure 26. Output Capacitor Connection

The C_{OUT} will reduce the overshoot and undershoot but will increase the settling time and can introduce some ringing of the output voltage during fast load transients. NCP51460 behavior for different values of ceramic X7R output capacitors is depicted on Figure 23.

The Output Voltage ringing and settling times can be reduced by using some additional resistance in series with the Ceramic Capacitor or by using Tantalum or Aluminum Capacitors which have higher ESR values. Figure 27 below shows the Load Transient improvement after adding an additional 2 Ω series resistor to a 1 μF Ceramics Capacitor.

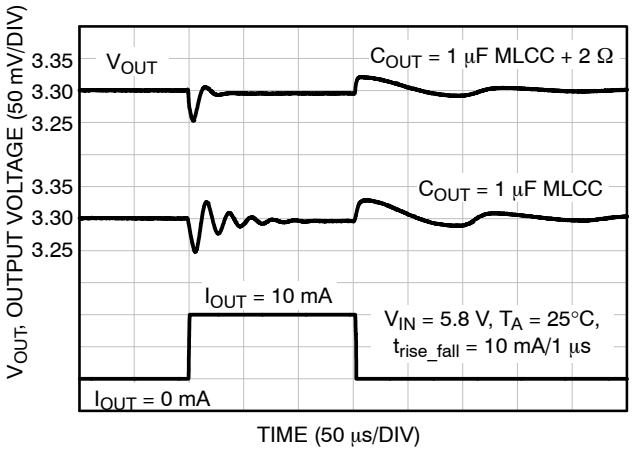


Figure 27.

The device was determined to be stable with Aluminum, Ceramic and Tantalum Capacitors with capacitances ranging from 0 to 100 μF at T_A = 25°C.

Turn−On Response

It is possible to achieve very fast Turn−On time when fast V_{IN} ramp is applied to NCP51460 input as shown on Figure 24. However if the Input Voltage change from 0 V to nominal Input Voltage is extremely fast, the Output Voltage settling time will increase. Figure 28 below shows this effect when the Input Voltage change is 5.8 V / 2 μs.

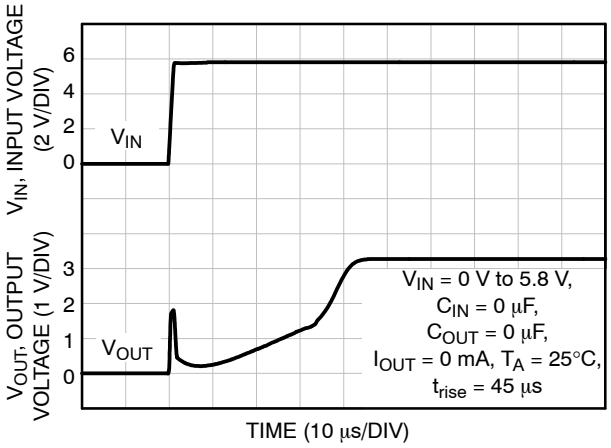


Figure 28.

A 0.1 μF or larger input capacitor will help to decrease the dv/dt of the input voltage and improve stability during large load current changes.

During the Turn−On for certain conditions the output voltage can exhibit an overshoot. The amount of the overshoot strongly depends on application conditions i.e. input voltage level, slew rate, input and output capacitors, and output current. The maximum value of the overshoot isn't guaranteed for this device.

The figure below shows an example of the Turn−On overshoot.

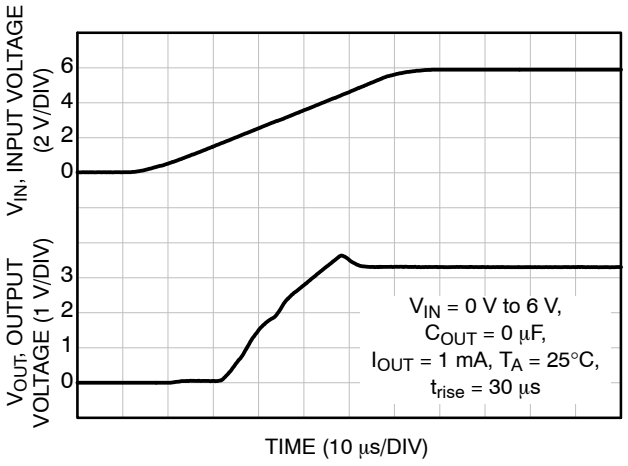


Figure 29.

Turn−Off Response

The Turn−Off response time is directly proportional to the output capacitor value and inversely proportional to the load value.

The NCP51460 device does not have any dedicated internal circuitry to discharge the output capacitor when the input voltage is turned−off or disconnected. This is why when large output capacitors are used and very small output current is drawn, it can take a considerable amount of time to discharge the capacitor. If short turn−off times are required, the output capacitor value should be minimized i.e. with no output capacitor a 20 μs turn−off time can be achieved.

Protection Features

The NCP51460 device is equipped with reverse input voltage protection which will help to protect the device when Input voltage polarity is reversed. In this circumstance the Input current will be minimized to typically less than 0.1 μA.

The short circuit protection will protect the device under the condition that the V_{OUT} is suddenly shorted to ground. The short circuit protection will work properly up to an Input Voltage of 27 V at T_A = 25°C. Depending on the PCB trace width and thickness, air flow and process spread this value can be slightly different and should be confirmed in the end application.

No external voltage source should be connected directly to the V_{OUT} pin of NCP51460 regulator. If the external source forces the output voltage to be greater than the nominal output voltage level, the current will start to flow from the Voltage Source to the V_{OUT} pin. This current will increase with the Output Voltage applied and can cause damage to the device if V_{OUT} > 10 V Typ. at 25°C (Figure 30).

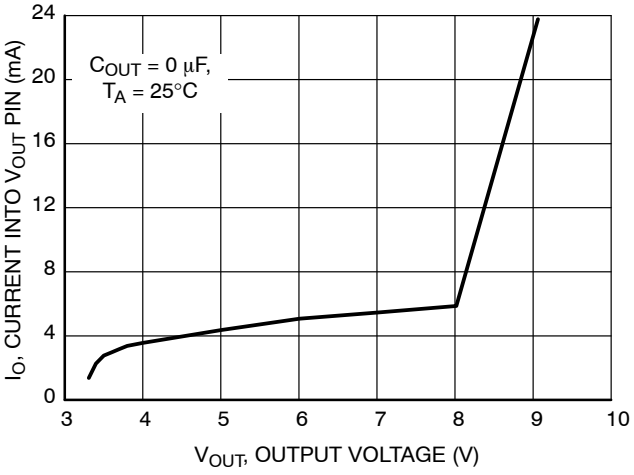


Figure 30.

Output Noise

The NCP51460 Output Voltage Noise strongly depends on the output capacitor value and load value. This is caused by the fact that the bandwidth of the Reference is inversely proportional to the capacitor value and directly proportional to the output current. The Reference bandwidth directly determines the point where the output voltage noise starts to fall. This can be observed at the Figure 31 below.

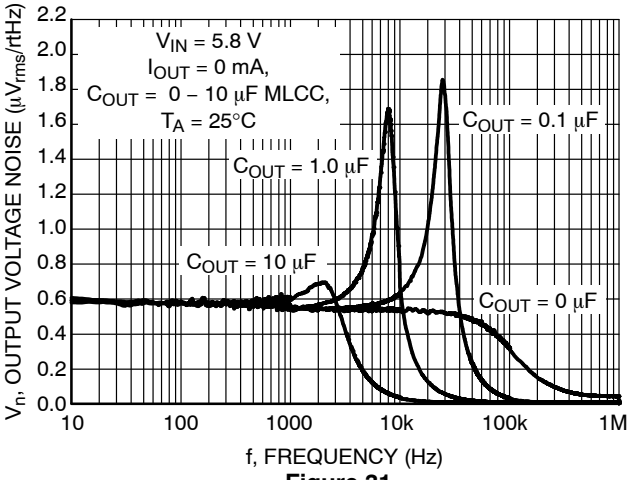


Figure 31.

The peaks which are visible on the noise spectrum are reflecting the stability of the NCP51460 device. In the comparison in Figure 31 it can be noticed that 0 μF and 10 μF cases represents the best stability.

Thermal Characteristics

As power dissipation in the NCP51460 increases, it may become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. The board material and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the NCP51460 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 100°C ($T_{J(MAX)}$), then the NCP51460 can dissipate up to 305 mW when the ambient temperature (T_A) is 25°C.

The power dissipated by the NCP51460 can be calculated from the following equations:

$$P_D \approx V_{IN}(I_Q@I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + (V_{OUT} \cdot I_{OUT})}{I_{OUT} + I_Q} \quad \text{(eq. 3)}$$

PCB Layout Recommendations

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise and cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP51460, and make traces as short as possible.

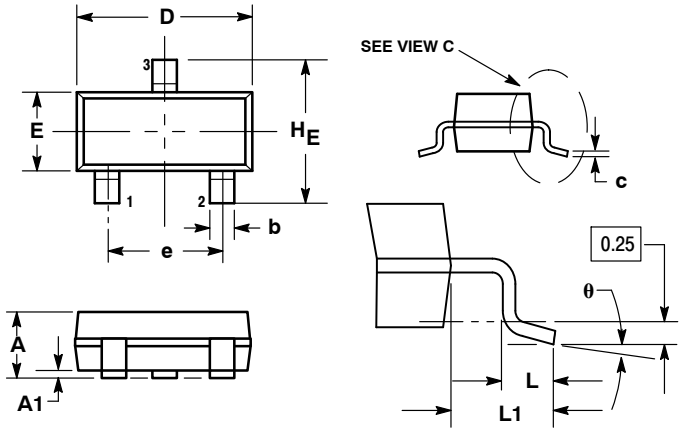
ORDERING INFORMATION

Device	Marking Code	Package	Shipping†
NCP51460SN33T1G	46A	SOT−23 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

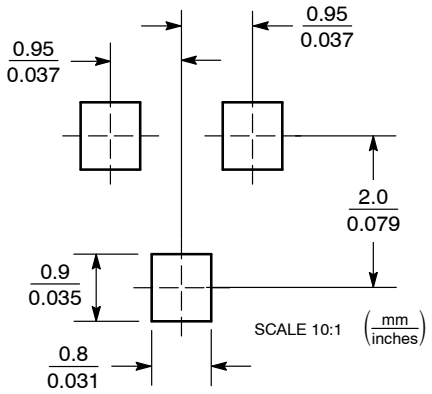
SOT−23 (TO−236)
CASE 318−08
ISSUE AP



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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