NX3DV42

Dual high-speed USB 2.0 double-pole double-throw analog switch

Rev. 3 — 13 February 2013 Product data sheet

1. General description

The NX3DV42 is a double-pole double-throw analog switch suitable for use as an analog or digital multiplexer/demultiplexer. Its wide bandwidth and low bit-to-bit skew allows the NX3DV42 to pass high-speed differential signals with good signal integrity. Its high channel to channel crosstalk rejection results in minimal noise interference. The bandwidth is wide enough to pass high-speed USB 2.0 differential signals (480 Mb/s). It consist of two switches, each with two independent input/outputs (HSDn+ and HSDn−) and a common input/output (D+ or D−). One digital input (S) is used to select the switch position. When pin $\overline{OE}$ is HIGH, the switches are turned off. Schmitt trigger action at the select input (S) and output enable input ($\overline{OE}$) makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 3.0 V to 4.3 V.

2. Features and benefits

- Supply voltage range from 3.0 V to 4.3 V
- 4 Ω typical ON resistance
- 7.3 pF typical ON capacitance
- 950 MHz typical bandwidth or data frequency
- Low crosstalk of −30 dB at 240 MHz
- Break-before-make switching
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4000 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
  - HBM exceeds 12000 V for power to GND protection
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Specified from −40 °C to +125 °C

3. Applications

- Cell phone, PDA, digital camera and notebook
- LCD monitor, TV and set-top box

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX3DV42GM	–40 °C to +125 °C	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.55 × 2.00 × 0.5 mm	SOT1049-3
NX3DV42GU	–40 °C to +125 °C	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm	SOT1160-1
NX3DV42GU10	–40 °C to +125 °C	XQFN10	plastic extremely thin small outline package; no leads; 10 terminals; body 1.3 x 1.6 x 0.5 mm	SOT1337-1

5. Marking

Table 2. Marking

Type number	Marking code
NX3DV42GM	x4
NX3DV42GU	x4
NX3DV42GU10	x4

6. Functional diagram

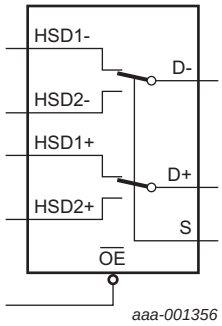


Fig 1. Logic symbol

7. Pinning information

7.1 Pinning

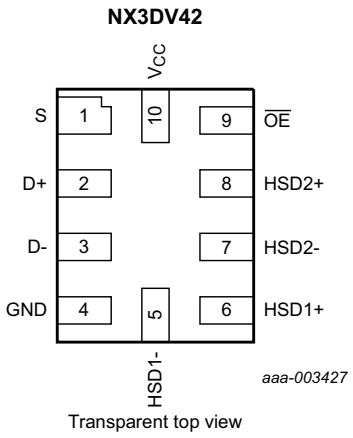


Fig 2. Pin configuration SOT1049-3 (XQFN10)

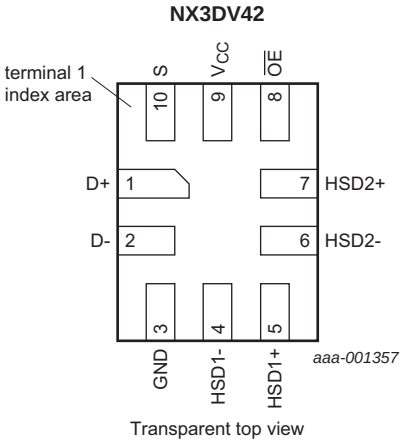


Fig 3. Pin configuration SOT1160-1 and SOT1337-1 (XQFN10)

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT1049-3	SOT1160-1, SOT1337-1	
HSD1–, HSD2–	5, 7	4, 6	independent input or output
HSD1+, HSD2+	6, 8	5, 7	independent input or output
D+, D–	2, 3	1, 2	common output or input
GND	4	3	ground (0 V)
$\overline{OE}$	9	8	output enable input (active LOW)
S	1	10	select input
V_{CC}	10	9	supply voltage

8. Functional description

Table 4. Function table[1]

Input		Channel on
S	$\overline{OE}$	
L	L	HSD1+ and HSD1–
H	L	HSD2+ and HSD2–
X	H	switch off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+5.5	V
V_I	input voltage	pins S and $\overline{OE}$	[1]	–0.5	+5.5	V
V_{SW}	switch voltage			–0.5	+5.5	V
I_{IK}	input clamping current	V_I < –0.5 V		–50	-	mA
I_{SK}	switch clamping current	V_I < –0.5 V		–50	-	mA
I_{SW}	switch current			-	±100	mA
I_{CC}	supply current			-	+50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For XQFN10 packages: above 100 °C derate linearly with 4 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			3.0	4.3	V
V_I	input voltage	pins S and $\overline{OE}$		0	4.5	V
V_{SW}	switch voltage		[1]	0	V_{CC}	V
T_{amb}	ambient temperature			–40	+125	°C

[1] To avoid sinking GND current from terminals D+ and D– when switch current flows in terminals HSDn+ and HSDn–, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals D+ and D–, no GND current will flow from terminals HSDn+ and HSDn–. In this case, there is no limit for the voltage drop across the switch.

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 3.0 V to 3.6 V	1.3	-	-	1.3	-	V
		V_{CC} = 4.3 V	1.7	-	-	1.7	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 V to 3.6 V	-	-	0.5	-	0.5	V
		V_{CC} = 4.3 V	-	-	0.7	-	0.7	V
V_{IK}	input clamping voltage	V_{CC} = 3.0 V; I_I = –18 mA	-	-	–1.2	-	–1.2	V
I_I	input leakage current	pins S and $\overline{OE}$; V_I = GND to 4.3 V; V_{CC} = 4.3 V; see Figure 5	-	-	±1	-	±10	µA

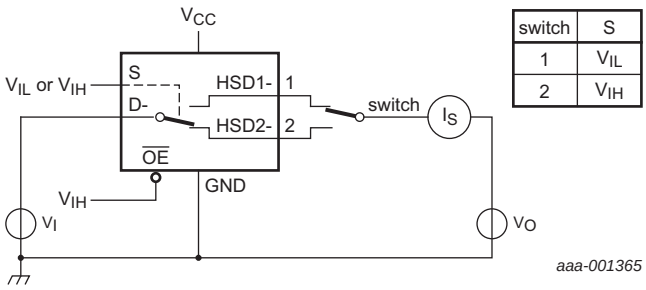
Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 4.3 V; see Figure 4 and Figure 7	-	-	±1	-	±2	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 4.3 V; V_{CC} = 0 V; see Figure 8	-	-	±1	-	±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{CC} = 4.3 V; V_{SW} = GND or V_{CC}; see Figure 6	-	-	1	-	10	µA
ΔI_{CC}	additional supply current	V_I = 2.6 V; V_{CC} = 4.3 V; V_{SW} = GND or V_{CC}	-	-	10	-	10	µA
		V_I = 1.8 V; V_{CC} = 4.3 V; V_{SW} = GND or V_{CC}	-	-	15	-	15	µA
C_I	input capacitance	pins S and OE	-	1.0	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance	pins HSDn+ and HSDn–; V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	2.8	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	pins D+ and D–; V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	7.3	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

11.1 Test circuit and graphs

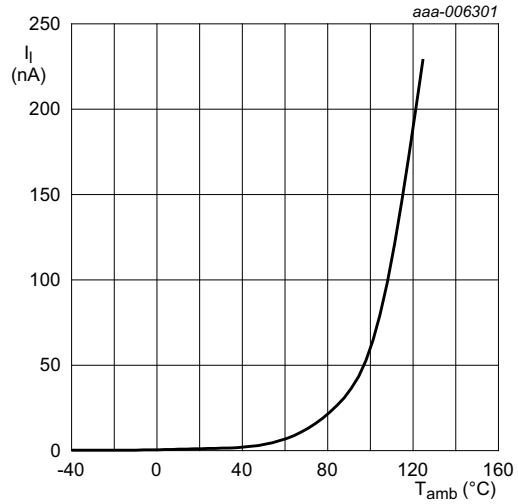


switch	S
1	V_{IL}
2	V_{IH}

V_I = V_{CC} or GND and V_O = GND or V_{CC}.

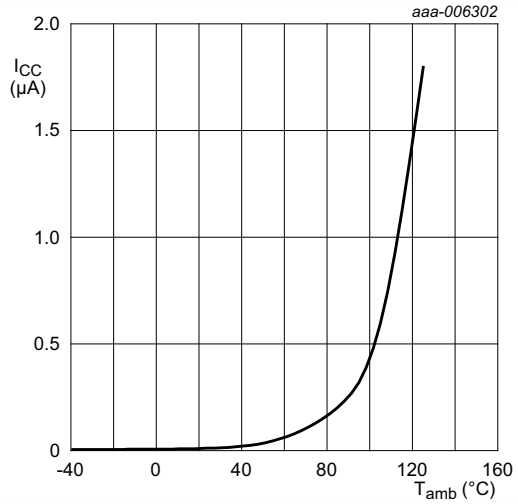
Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 4. Test circuit for measuring OFF-state leakage current



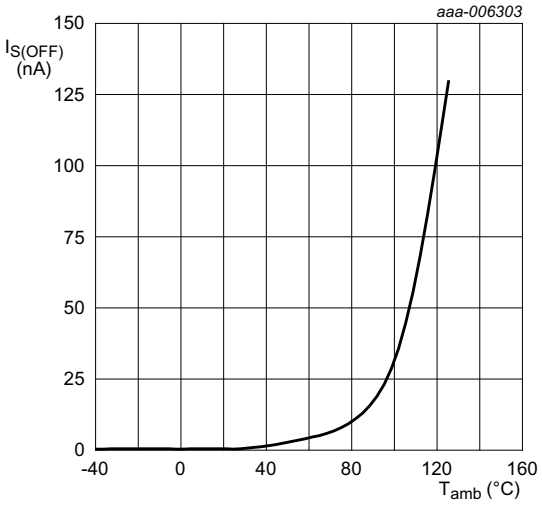
V_{CC} = 4.3 V.

Fig 5. Waveform showing the typical input leakage current versus temperature



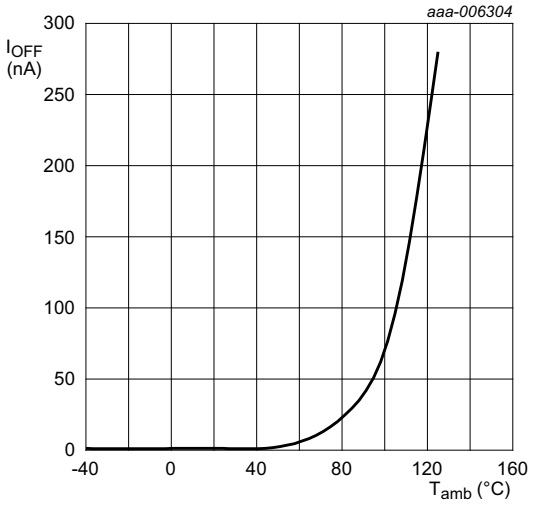
V_{CC} = 4.3 V.

Fig 6. Waveform showing the typical supply current versus temperature



V_{CC} = 4.3 V.

Fig 7. Waveform showing the typical OFF-state leakage current versus temperature



V_{CC} = 4.3 V.

Fig 8. Waveform showing the typical power-off leakage current versus temperature

11.2 ON resistance

Table 8. ON resistance

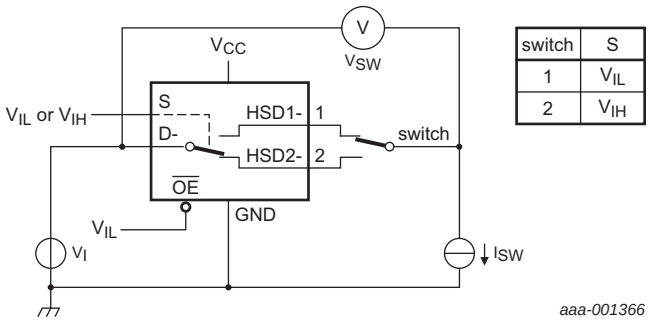
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R_{ON}	ON resistance	V_I = 0.4 V; I_{SW} = 8 mA; see Figure 9						
		V_{CC} = 3.0 V	-	3.9	6.5	-	10	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = 0.4 V; I_{SW} = 8 mA [2]						
		V_{CC} = 3.0 V	-	0.65	-	-	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

[2] Measured at identical V_{CC}, temperature and input voltage.

11.3 ON resistance test circuit



switch	S
1	V_{IL}
2	V_{IH}

$R_{ON} = V_{SW} / I_{SW}$.

Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 9. Test circuit for measuring ON resistance

12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	HSDn+ to D+ or HSDn– to D– or D+ to HSDn+ or D– to HSDn–; see Figure 10 [2][3]						
		V_{CC} = 3.3 V	-	0.25	-	-	-	ns
t_{en}	enable time	S or $\overline{OE}$ to D+ or D–; see Figure 11 [4]						
		V_{CC} = 3.0 V to 3.6 V	-	11.2	30	-	40	ns

Table 9. Dynamic characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			T_{amb} = –40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{dis}	disable time	S or $\overline{OE}$ to D+ or D–; see Figure 11	[5]						
		V_{CC} = 3.0 V to 3.6 V		-	3.9	25	-	30	ns
t_{b-m}	break-before-make time	see Figure 12	[3]						
		V_{CC} = 3.0 V to 3.6 V		2.0	5.9	-	2.0	-	ns
$t_{sk(p)}$	pulse skew time	see Figure 10							
		V_{CC} = 3.0 V to 3.6 V	[3]	-	20	-	-	-	ps
t_{jit}	jitter time	R_L = 50 Ω; C_L = 5 pF; t_r, t_f = 500 ps (10 % to 90 %) at 480 Mbs (PRBS = $2^{15} - 1$)	[3]	-	200	-	-	-	ps

[1] Typical values are measured at T_{amb} = 25 °C, C_L = 5 pF and V_{CC} = 3.3 V.

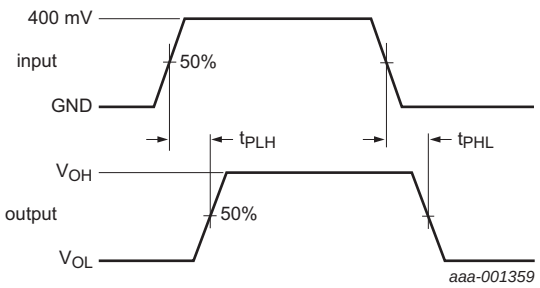
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Guaranteed by design.

[4] t_{en} is the same as t_{PZH}.

[5] t_{dis} is the same as t_{PHZ}.

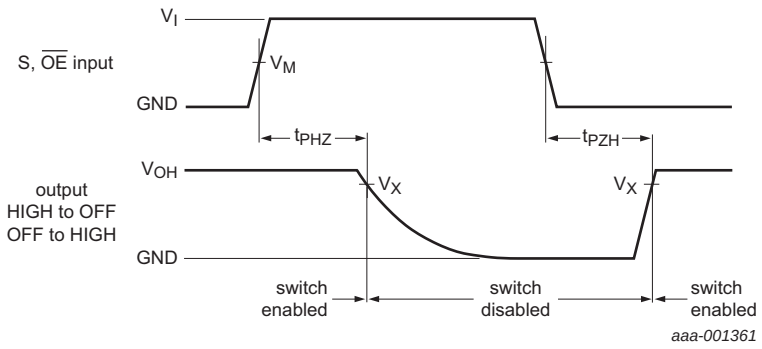
12.1 Waveforms and test circuits



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

$t_{sk(p)} = |t_{PHL} - t_{PLH}|$.

Fig 10. The data input to output propagation delay times and pulse skew time



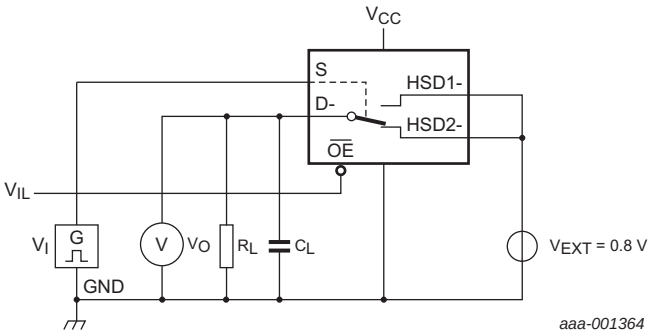
Measurement points are given in Table 10.

Logic level: V_{OH} is the typical output voltage level that occurs with the output load.

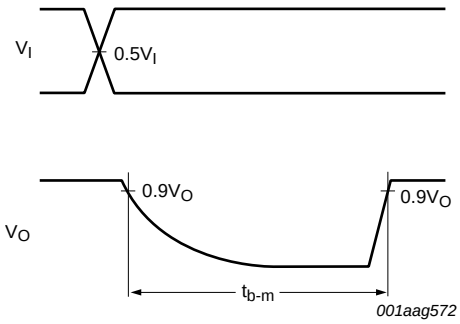
Fig 11. Enable and disable times

Table 10. Measurement points

Supply voltage	Input		Output
V_{CC}	V_M	V_I	V_X
3.0 V to 3.6 V	$0.5V_{CC}$	V_{CC}	$0.9V_{OH}$



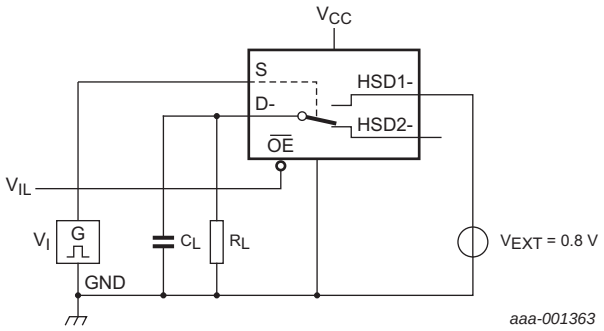
a. Test circuit.



b. Input and output measurement points.

Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 12. Test circuit for measuring break-before-make timing



Test circuit also applies for D+, HSD1+ and HSD2+.

Test data is given in Table 11.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

V_I may be connected to S or $\overline{OE}$.

Fig 13. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
3.0 V to 3.6 V	V_{CC}	≤ 2.5 ns	5 pF	50 Ω

12.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

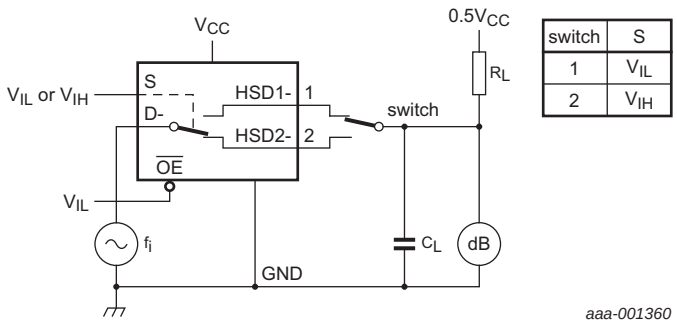
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			Unit
				Min	Typ[2]	Max	
$f_{(-3dB)}$	−3 dB frequency response	R_L = 50 Ω; see Figure 14	[1]				
		C_L = 0 pF; V_{CC} = 3.0 V to 3.6 V		-	950	-	MHz
		C_L = 5 pF; V_{CC} = 3.0 V to 3.6 V		-	450	-	MHz
α_{iso}	isolation (OFF-state)	f_i = 240 MHz; R_L = 50 Ω; see Figure 15	[1]				
		V_{CC} = 3.0 V to 3.6 V		-	−30	-	dB
Xtalk	crosstalk	between switches; f_i = 240 MHz; R_L = 50 Ω; see Figure 16	[1]				
		V_{CC} = 3.0 V to 3.6 V		-	−30	-	dB

[1] f_i is biased at $0.5V_{CC}$.

[2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

12.3 Test circuits

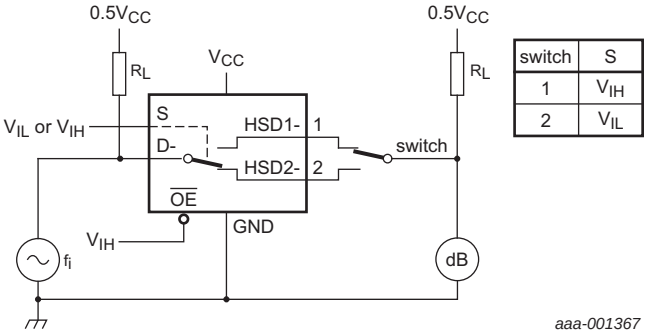


switch	S
1	V_{IL}
2	V_{IH}

Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads −3 dB.

Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 14. Test circuit for measuring the frequency response when channel is in ON-state

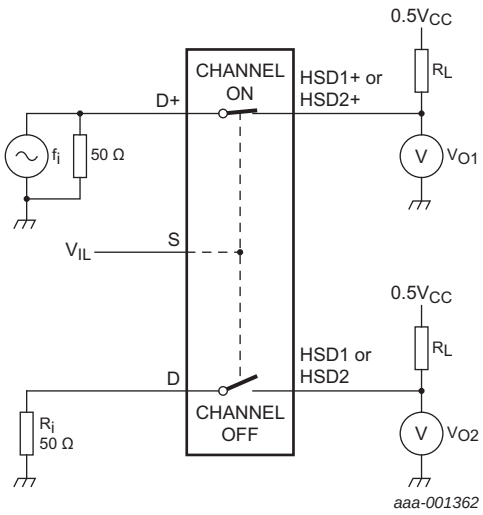


switch	S
1	V_{IH}
2	V_{IL}

Adjust f_i voltage to obtain 0 dBm level at input.

Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 15. Test circuit for measuring isolation (OFF-state)

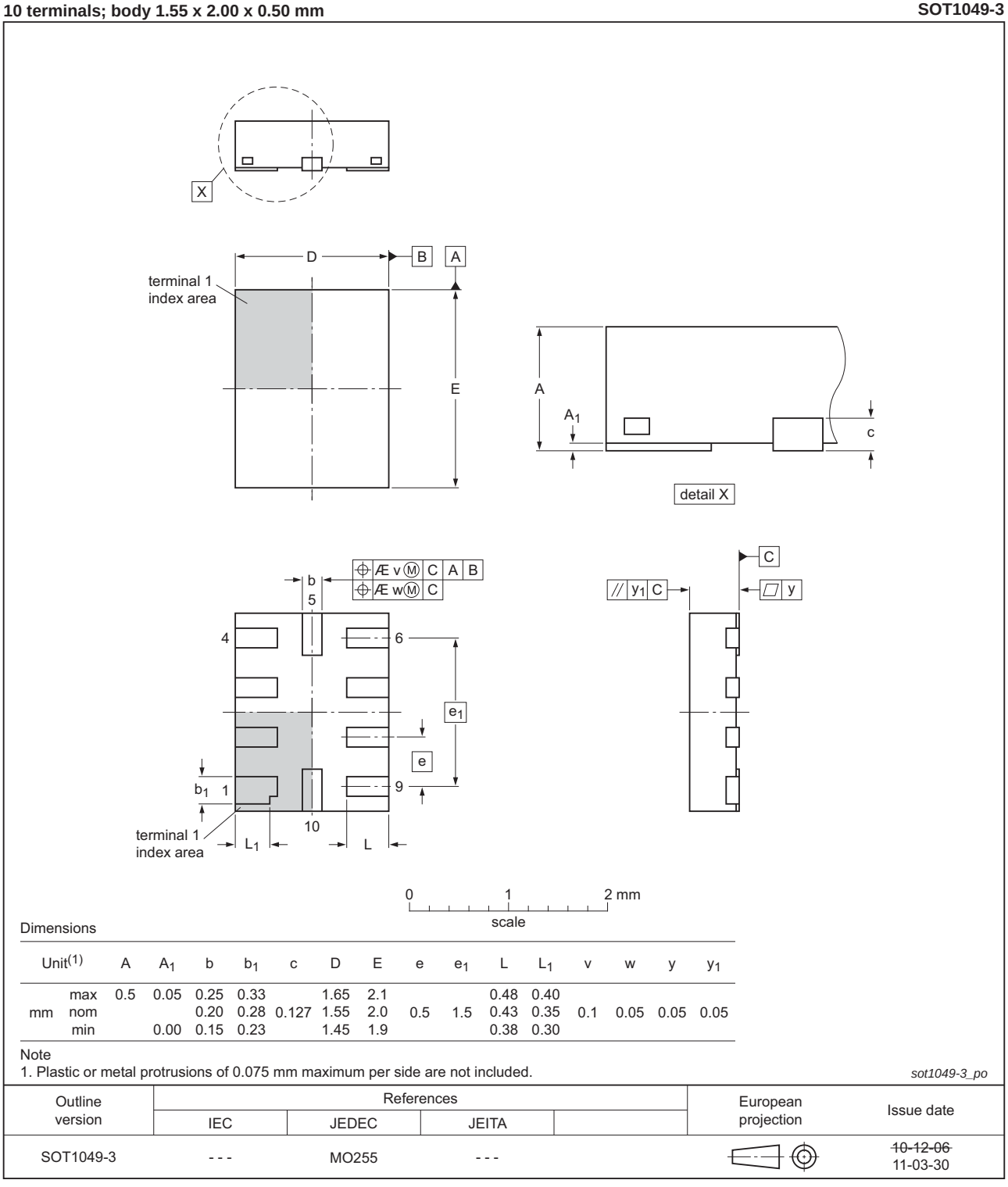


20 $\log_{10}$ (V_{O2}/V_{O1}) or 20 $\log_{10}$ (V_{O1}/V_{O2}).

Fig 16. Test circuit for measuring crosstalk between switches

13. Package outline

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.55 x 2.00 x 0.50 mm **SOT1049-3**



Dimensions

Unit(1)		A	A1	b	b1	c	D	E	e	e1	L	L1	v	w	y	y1
mm	max	0.5	0.05	0.25	0.33		1.65	2.1			0.48	0.40				
	nom			0.20	0.28	0.127	1.55	2.0	0.5	1.5	0.43	0.35	0.1	0.05	0.05	0.05
	min		0.00	0.15	0.23		1.45	1.9			0.38	0.30				

Note

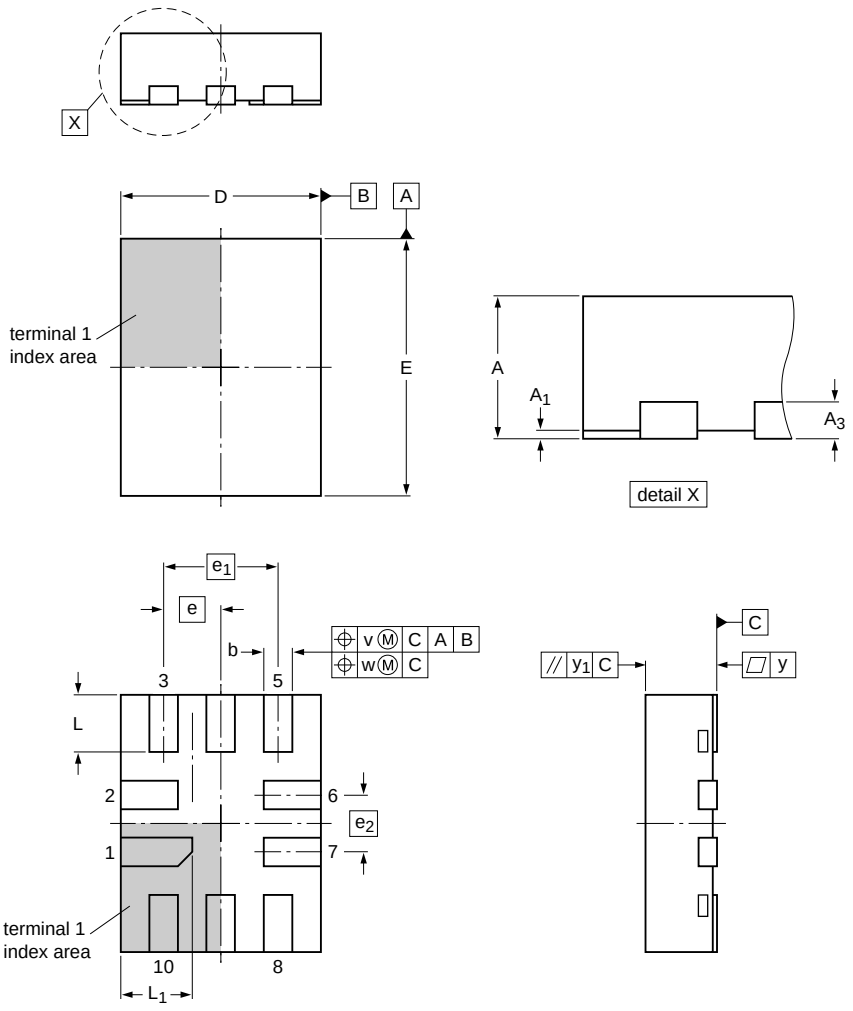
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1049-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1049-3	- - -	MO255	- - -			~~10-12-06~~ 11-03-30

Fig 17. Package outline SOT1049-3 (XQFN10)

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm **SOT1160-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
	max	0.5	0.05		0.25	1.5	1.9				0.45	0.55				
mm	nom			0.127	0.20	1.4	1.8	0.4	0.8	0.4	0.40	0.50	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.3	1.7				0.35	0.45				

Note

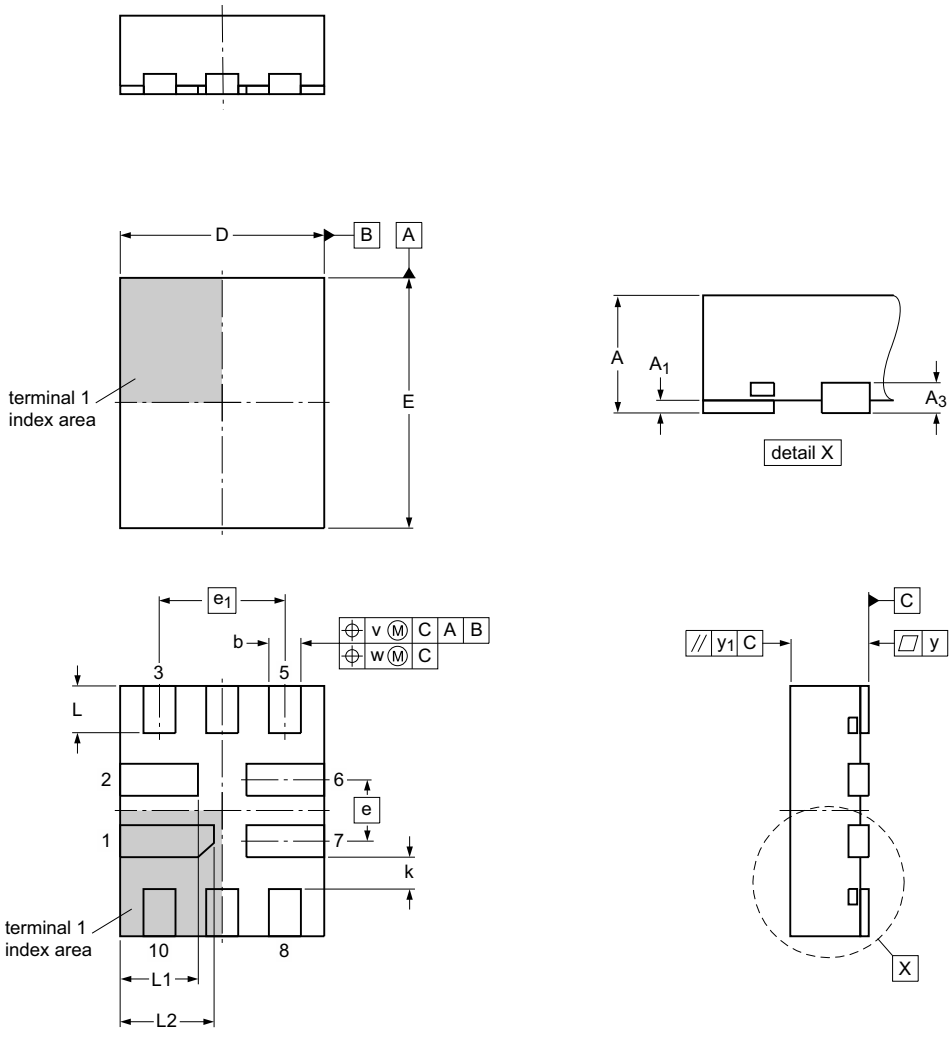
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1160-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1160-1	- - -	- - -	- - -		~~09-12-28~~ 09-12-29

Fig 18. Package outline SOT1160-1 (XQFN10)

XQFN10: plastic extremely thin small outline package; no leads; 10 terminals; body 1.3 x 1.6 x 0.5 mm **SOT1337-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_3	b	D	E	e	e_1	k	L	L_1	L_2	v	w	y	y_1
	max	0.5	0.05	0.127	0.25	1.35	1.65				0.35	0.55	0.65				
mm	nom				0.20	1.30	1.60	0.4	0.8		0.30	0.50	0.60	0.1	0.05	0.05	0.05
	min		0.00	0.050	0.15	1.25	1.55			0.2	0.25	0.45	0.55				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1337-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1337-1	- - -	MO-288	- - -			~~12-08-28~~ 12-09-11

Fig 19. Package outline SOT1337-1 (XQFN10)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
LCD	Liquid Crystal Display
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3DV42 v.3	20130213	Product data sheet	-	NX3DV42 v.2
Modifications:	• Values added for T_{amb} = +125 °C throughout the data sheet. • Type number NX3DV42GU10 added (Table 1). • Marking code for type number NX3DV42GU10 added (Table 2). • Package outline drawing SOT1337-1 added (Figure 19).			
NX3DV42 v.2	20120618	Product data sheet	-	NX3DV42 v.1
Modifications:	• Package outline drawing SOT1049-2 changed to SOT1049-3 (Figure 17).			
NX3DV42 v.1	20120103	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

1 General description 1
2 Features and benefits 1
3 Applications 1
4 Ordering information 2
5 Marking 2
6 Functional diagram 2
7 Pinning information 3
7.1 Pinning 3
7.2 Pin description 3
8 Functional description 3
9 Limiting values 4
10 Recommended operating conditions 4
11 Static characteristics 4
11.1 Test circuit and graphs 5
11.2 ON resistance 7
11.3 ON resistance test circuit 7
12 Dynamic characteristics 7
12.1 Waveforms and test circuits 8
12.2 Additional dynamic characteristics 10
12.3 Test circuits 11
13 Package outline 13
14 Abbreviations 16
15 Revision history 16
16 Legal information 17
16.1 Data sheet status 17
16.2 Definitions 17
16.3 Disclaimers 17
16.4 Trademarks 18
17 Contact information 18
18 Contents 19

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 February 2013
Document identifier: NX3DV42

AMEYA360
Components Supply Platform

Authorized Distribution Brand :

Website :

Welcome to visit www.ameya360.com

Contact Us :

- ### Address :

  401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
  Minhang District, Shanghai , China

- ### Sales :

  Direct +86 (21) 6401-6692

  Email amall@ameya360.com

  QQ 800077892

  Skype ameyasales1 ameyasales2

- ### Customer Service :

  Email service@ameya360.com

- ### Partnership :

  Tel +86 (21) 64016692-8333

  Email mkt@ameya360.com