

MM74HC14

Hex Inverting Schmitt Trigger

Features

- Typical propagation delay: 13ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20µA maximum (74HC Series)
- Low input current: 1µA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at $V_{CC} = 4.5V$

General Description

The MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Ordering Information

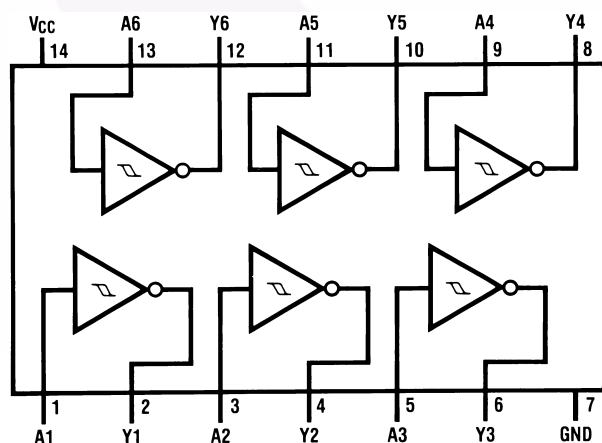
Order Number	Package Number	Package Description
MM74HC14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

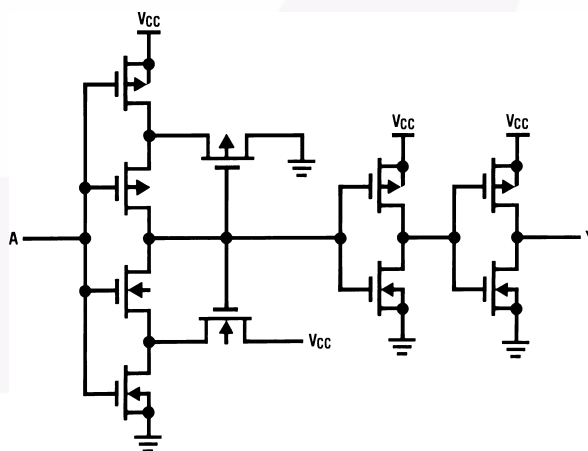
Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Logic Diagram



Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5 to +7.0V
V_{IN}	DC Input Voltage	−1.5 to $V_{CC}+1.5V$
V_{OUT}	DC Output Voltage	−0.5 to $V_{CC}+0.5V$
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	−65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: −12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−55	+125	°C

DC Electrical Characteristics⁽³⁾

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Units
				Typ.	Guaranteed Limits			
V _{T+}	Positive Going Threshold Voltage	2.0	Minimum	1.2	1.0	1.0	1.0	V
		4.5		2.7	2.0	2.0	2.0	
		6.0		3.2	3.0	3.0	3.0	
		2.0	Maximum	1.2	1.5	1.5	1.5	
		4.5		2.7	3.15	3.15	3.15	
		6.0		3.2	4.2	4.2	4.2	
V _{T-}	Negative Going Threshold Voltage	2.0	Minimum	0.7	0.3	0.3	0.3	V
		4.5		1.8	0.9	0.9	0.9	
		6.0		2.2	1.2	1.2	1.2	
		2.0	Maximum	0.7	1.0	1.0	1.0	
		4.5		1.8	2.2	2.2	2.2	
		6.0		2.2	3.0	3.0	3.0	
V _H	Hysteresis Voltage	2.0	Minimum	0.5	0.2	0.2	0.2	V
		4.5		0.9	0.4	0.4	0.4	
		6.0		1.0	0.5	0.5	0.5	
		2.0	Maximum	0.5	1.0	1.0	1.0	
		4.5		0.9	1.4	1.4	1.4	
		6.0		1.0	1.5	1.5	1.5	
V _{OH}	Minimum HIGH Level Output Voltage	2.0	V _{IN} = V _{IL} , I _{OUT} = 20μA	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	V _{IN} = V _{IL} , I _{OUT} = 4.0mA	4.2	3.98	3.84	3.7	
		6.0	V _{IN} = V _{IL} , I _{OUT} = 5.2mA	5.7	5.48	5.34	5.2	
V _{OL}	Maximum LOW Level Output Voltage	2.0	V _{IN} = V _{IH} , I _{OUT} = 20μA	0	0.1	0.1	0.1	V
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	V _{IN} = V _{IH} , I _{OUT} = 4.0mA	0.2	0.26	0.33	0.4	
		6.0	V _{IN} = V _{IH} , I _{OUT} = 5.2mA	0.2	0.26	0.33	0.4	
I _{IN}	Maximum Input Current	6.0	V _{IN} = V _{CC} or GND		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	6.0	V _{IN} = V _{CC} or GND, I _{OUT} = 0μA		2.0	20	40	μA

Note:

3. For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics
 $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15pF$, $t_r = t_f = 6ns$

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay		12	22	ns

AC Electrical Characteristics
 $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50pF$, $t_r = t_f = 6ns$ (unless otherwise specified)

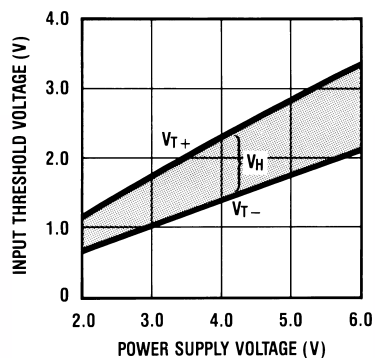
Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C		T _A = −40°C to 85°C	T _A = −55°C to 125°C	Units
				Typ.	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay	2.0		60	125	156	188	ns
		4.5		13	25	31	38	
		6.0		11	21	26	32	
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time	2.0		30	75	95	110	ns
		4.5		8	15	19	22	
		6.0		7	13	16	19	
C _{PD}	Power Dissipation Capacitance ⁽⁴⁾		(per gate)	27				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note:

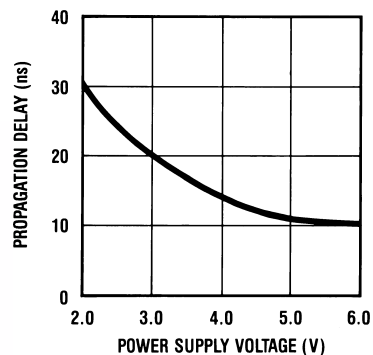
4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Typical Performance Characteristics

Input Threshold, V_{T+} , V_{T-} , vs Power Supply Voltage

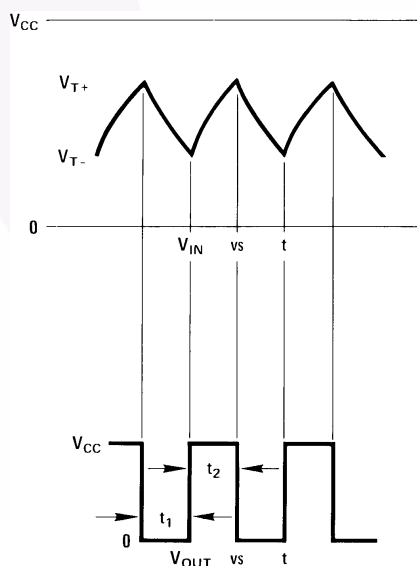
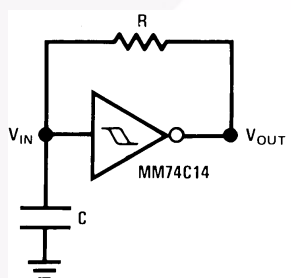


Propagation Delay vs. Power Supply



Typical Applications

Low Power Oscillator



$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}}$$

Note:

The equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$

Physical Dimensions

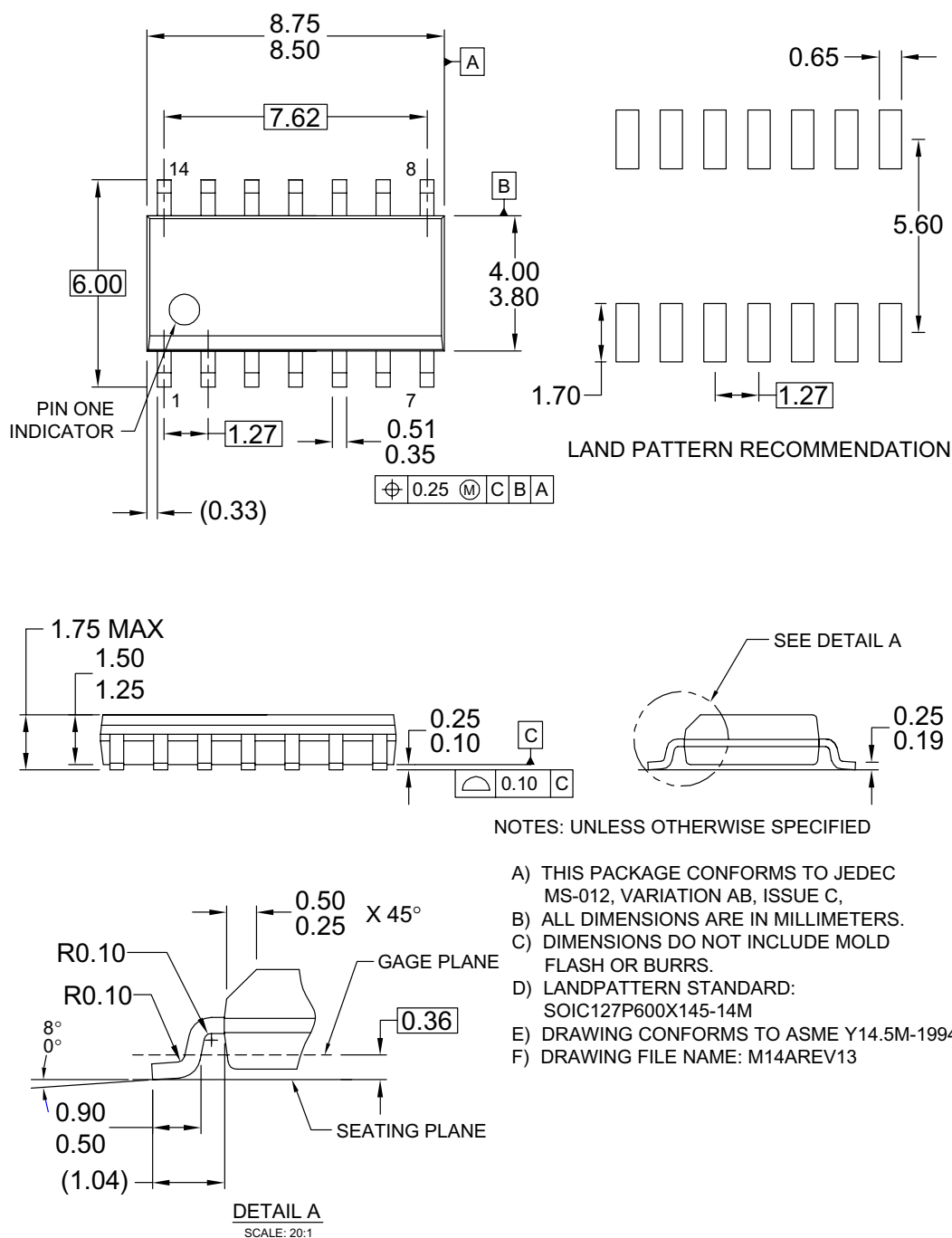


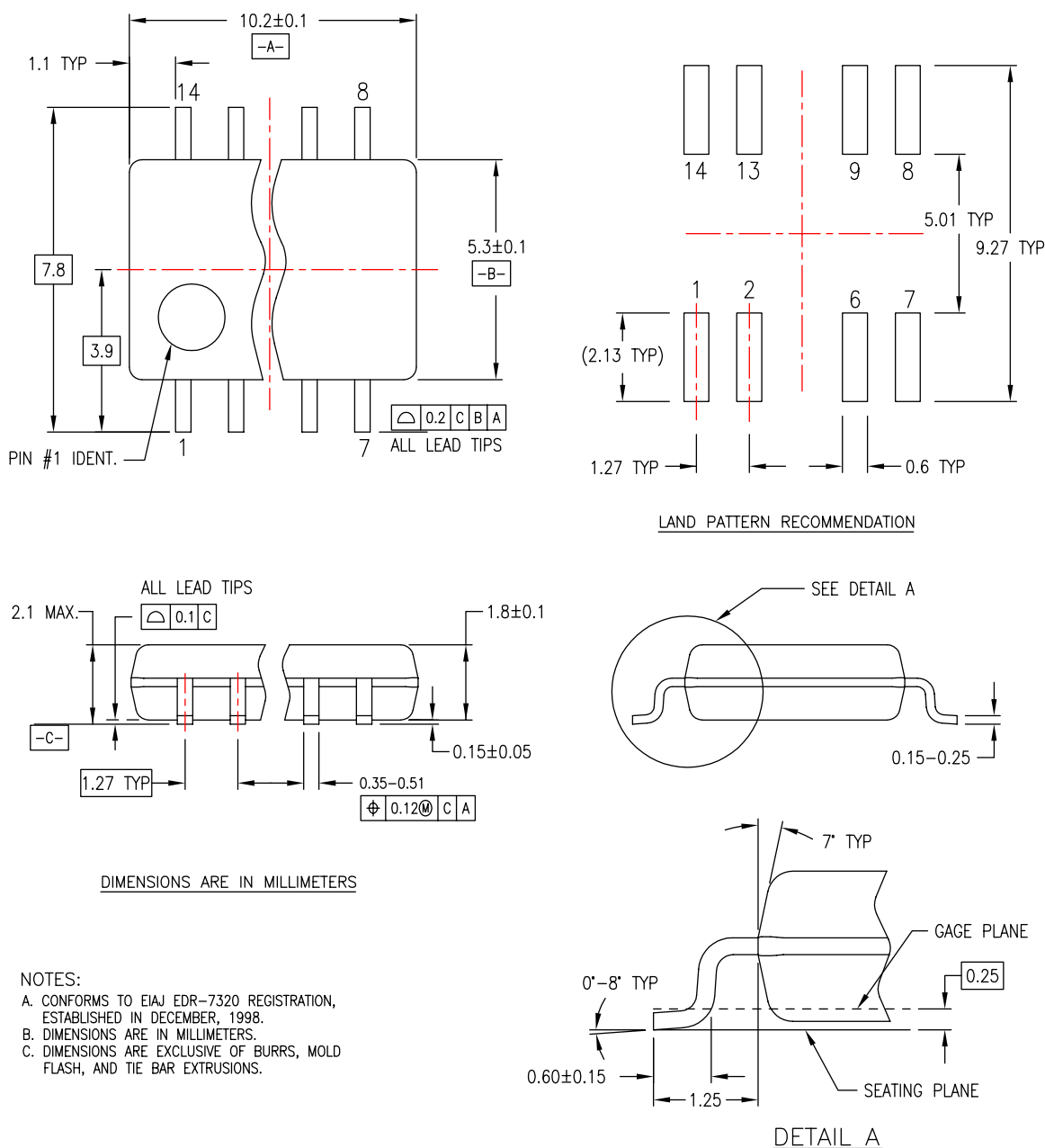
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



M14DREVC

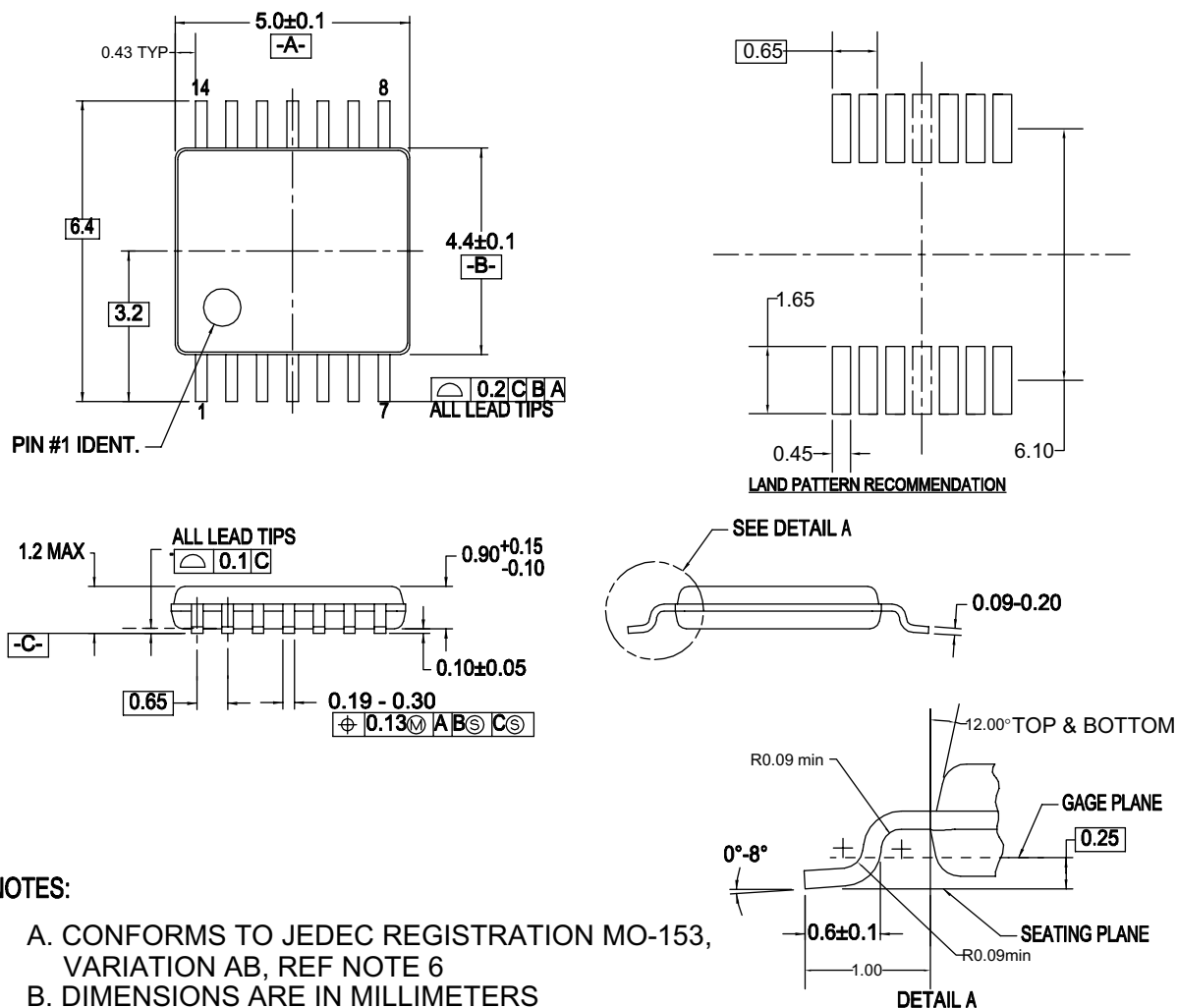
Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)



NOTES:

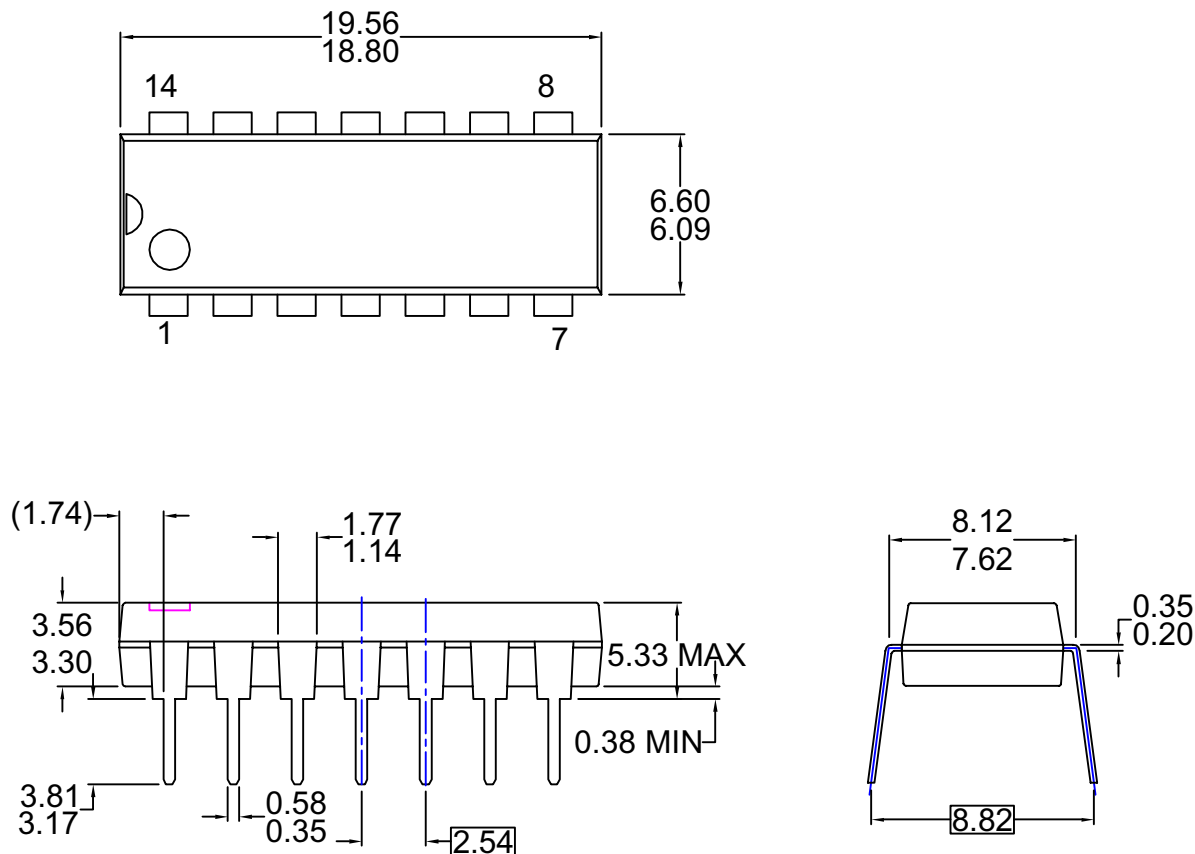
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>

Physical Dimensions (Continued)**NOTES: UNLESS OTHERWISE SPECIFIED**

THIS PACKAGE CONFORMS TO

A) JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

DIMENSIONS ARE EXCLUSIVE OF BURRS,
C) MOLD FLASH, AND TIE BAR EXTRUSIONS.D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5-1994

E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.



Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx [®]	FPS [™]	PDP-SPM [™]	SupreMOS [™]
Build it Now [™]	FRFET [®]	Power220 [®]	SyncFET [™]
CorePLUS [™]	Global Power Resource SM	POWEREDGE [®]	SYSTEM [®]
CROSSVOLT [™]	Green FPS [™]	Power-SPM [™]	GENERAL
CTL [™]	Green FPS [™] e-Series [™]	PowerTrench [®]	The Power Franchise [®]
Current Transfer Logic [™]	GTO [™]	Programmable Active Droop [™]	the power [®]
EcoSPARK [®]	i-Lo [™]	QFET [®]	franchise
EZSWITCH [™] *	IntelliMAX [™]	QS [™]	TinyBoost [™]
	ISOPLANAR [™]	QT Optoelectronics [™]	TinyBuck [™]
	MegaBuck [™]	Quiet Series [™]	TinyLogic [®]
Fairchild [®]	MICROCOUPLER [™]	RapidConfigure [™]	TINYOPTO [™]
Fairchild Semiconductor [®]	MicroFET [™]	SMART START [™]	TinyPower [™]
FACT Quiet Series [™]	MicroPak [™]	SPM [®]	TinyPWM [™]
FACT [®]	MillerDrive [™]	STEALTH [™]	TinyWire [™]
FAST [®]	Motion-SPM [™]	SuperFET [™]	μSerDes [™]
FastvCore [™]	OPTOLOGIC [®]	SuperSOT [™] 3	UHC [®]
FlashWriter [®] *	OPTOPLANAR [®]	SuperSOT [™] 6	Ultra FRFET [™]
		SuperSOT [™] 8	UniFET [™]
			VCX [™]

* EZSWITCH[™] and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I33

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692
Email amall@ameya360.com
QQ 800077892
Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333
Email mkt@ameya360.com