



TS3A4751 0.9-Ω Low-Voltage, Single-Supply, 4-Channel SPST Analog Switch

1 Features

- Low ON-State Resistance (R_{ON})
 - 0.9 Ω Max (3-V Supply)
 - 1.5 Ω Max (1.8-V Supply)
- R_{ON} Flatness: 0.4 Ω Max (3-V)
- R_{ON} Channel Matching
 - 0.05 Ω Max (3-V Supply)
 - 0.15 Ω Max (1.8-V Supply)
- 1.6-V to 3.6-V Single-Supply Operation
- 1.8-V CMOS Logic Compatible (3-V Supply)
- High Current-Handling Capacity (100 mA Continuous)
- Fast Switching: $t_{ON} = 5$ ns, $t_{OFF} = 4$ ns
- Supports Both Digital and Analog Applications
- ESD Protection Exceeds JESD-22
 - ±4000-V Human Body Model (A114-A)
 - 300-V Machine Model (A115-A)
 - ±1000-V Charged-Device Model (C101)

2 Applications

- Power Routing
- Battery-Powered Systems
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- PCMCIA Cards
- Cellular Phones
- Modems
- Hard Drives

3 Description

The TS3A4751 device is a bidirectional, 4-channel, normally open (NO) single-pole single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

The TS3A4751 device has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in space-saving 14-pin VQFN (RGY) and micro X2QFN (RUC) packages.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A4751	TSSOP (14)	5.00 mm × 4.40 mm
	VQFN (14)	3.50 mm × 3.50 mm
	X2QFN (14)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

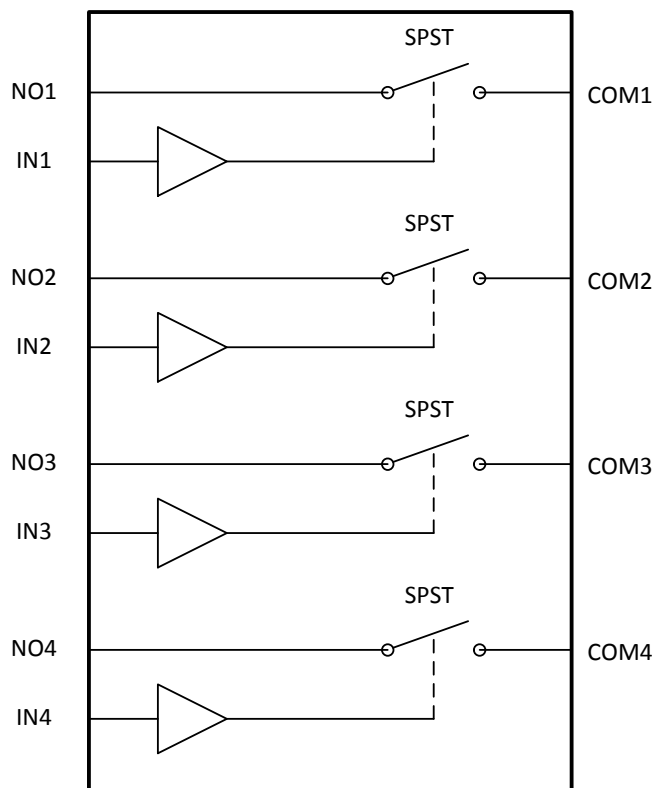


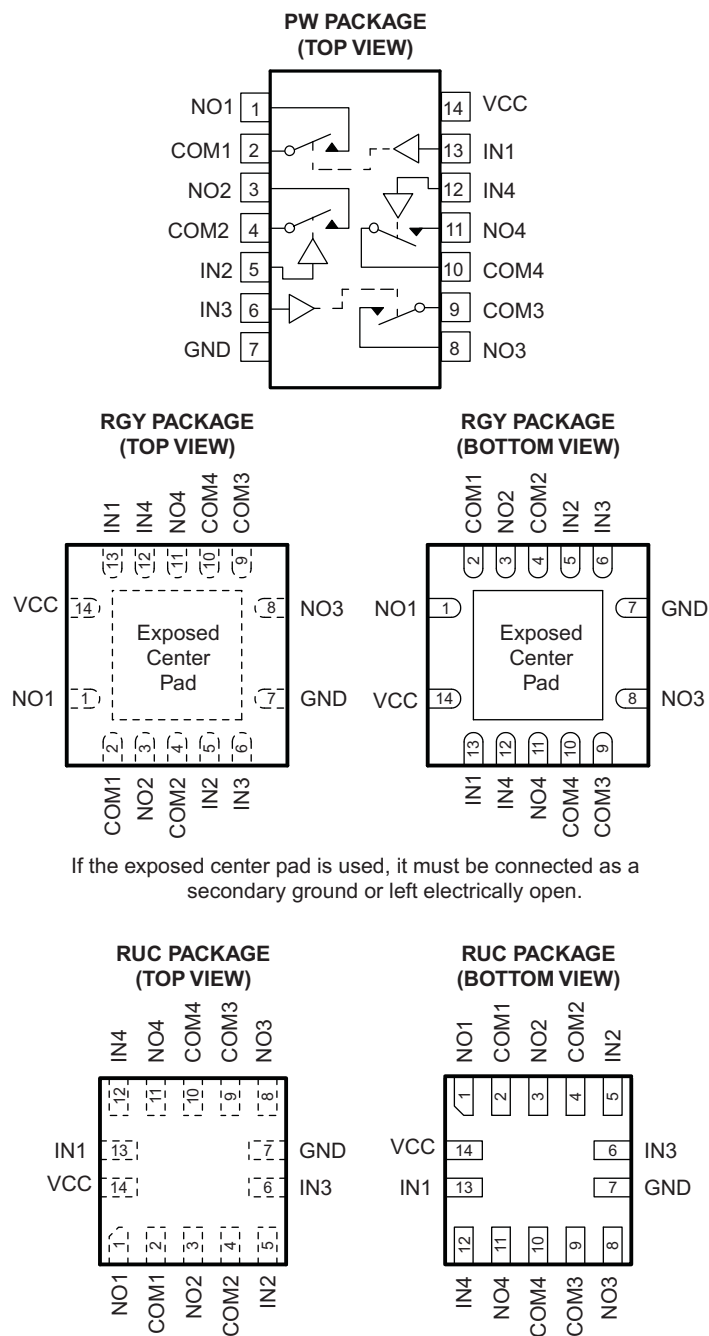
Table of Contents

1 Features	1	7.2 Functional Block Diagram	13
2 Applications	1	7.3 Feature Description	13
3 Description	1	7.4 Device Functional Modes	13
4 Revision History	2	8 Application and Implementation	14
5 Pin Configuration and Functions	3	8.1 Application Information	14
6 Specifications	4	8.2 Typical Application	14
6.1 Absolute Maximum Ratings	4	9 Power Supply Recommendations	16
6.2 ESD Ratings	4	10 Layout	16
6.3 Recommended Operating Conditions	5	10.1 Layout Guidelines	16
6.4 Thermal Information	5	10.2 Layout Example	16
6.5 Electrical Characteristics for 1.8-V Supply	6	11 Device and Documentation Support	17
6.6 Electrical Characteristics for 3-V Supply	7	11.1 Trademarks	17
6.7 Typical Characteristics	10	11.2 Electrostatic Discharge Caution	17
7 Detailed Description	13	11.3 Glossary	17
7.1 Overview	13	12 Mechanical, Packaging, and Orderable Information	17

4 Revision History

Changes from Revision D (July 2008) to Revision E	Page
<ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NO1	I/O	Normally open signal path
2	COM1	I/O	Common signal path
3	NO2	I/O	Normally open signal path
4	COM2	I/O	Common signal path
5	IN2	I	Logic control input
6	IN3	I	Logic control input
7	GND	—	Ground
8	NO3	I/O	Normally open signal path
9	COM3	I/O	Common signal path
10	COM4	I/O	Common signal path
11	NO4	I/O	Normally open signal path
12	IN4	I	Logic control input
13	IN1	I	Logic control input
14	V _{CC}	I	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage referenced to GND ⁽²⁾	−0.3	4	V
V _{NO} V _{COM} V _{IN}	Analog and digital voltage	−0.3	V _{CC} + 0.3	V
I _{NO} I _{COM}	On-state switch current	V _{NO} , V _{COM} = 0 to V _{CC}		−100 100 mA
I _{CC} I _{GND}	Continuous current through V _{CC} or GND		±100	mA
V	Peak current pulsed at 1 ms, 10% duty cycle	COM, V _{I/O}		±200 mA
T _A	Operating temperature	−40	85	°C
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Signals on COM or NO exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
		Machine Model	±300

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.3	V
V_{NO} V_{COM} V_{IN}	Analog and digital voltage range	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS3A4751			UNIT
		PW	RGY	RUC	
		14 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	132.3	68.5	196.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	60.6	83.1	73.9	
R _{θJB}	Junction-to-board thermal resistance	74.2	44.6	130.7	
ψ _{JT}	Junction-to-top characterization parameter	11.2	7.8	2.1	
ψ _{JB}	Junction-to-board characterization parameter	73.6	44.7	130.6	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	24.6	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics for 1.8-V Supply

 $V_{CC} = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$, $V_{IH} = 1\text{ V}$, $V_{IL} = 0.4\text{ V}$ (unless otherwise noted)^{(1) (2)}

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP ⁽³⁾	MAX	UNIT
ANALOG SWITCH								
V _{COM} , V _{NO}	Analog signal range				0		V _{CC}	V
R _{on}	ON-state resistance	V _{CC} = 1.8 V, I _{COM} = −10 mA, V _{NO} = 0.9 V		25°C	1	1.5	2	Ω
				Full				
ΔR _{on}	ON-state resistance match between channels ⁽⁴⁾	V _{CC} = 1.8 V, I _{COM} = −10 mA, V _{NO} = 0.9 V		25°C	0.09	0.15	0.25	Ω
				Full				
R _{on(flat)}	ON-state resistance flatness ⁽⁵⁾	V _{CC} = 1.8 V, I _{COM} = −10 mA, 0 ≤ V _{NO} ≤ V _{CC}		25°C	0.7	0.9	1.5	Ω
				Full				
I _{NO(OFF)}	NO OFF leakage current ⁽⁶⁾	V _{CC} = 1.95 V, V _{COM} = 0.15 V, 1.65 V, V _{NO} = 1.8 V, 0.15 V		25°C	−1	0.5	1	nA
				Full	−10	10		
I _{COM(OFF)}	COM OFF leakage current ⁽⁶⁾	V _{CC} = 1.95 V, V _{COM} = 0.15 V, 1.65 V, V _{NO} = 1.65 V, 0.15 V		25°C	−1	0.5	1	nA
				Full	−10	10		
I _{COM(ON)}	COM ON leakage current ⁽⁶⁾	V _{CC} = 1.95 V, V _{COM} = 0.15 V, 1.65 V, V _{NO} = 0.15 V, 1.65 V, or floating		25°C	−1	0.01	1	nA
				Full	−3	3		
DYNAMIC								
t _{ON}	Turn-on time	V _{NO} = 1.5 V, R _L = 50 Ω, C _L = 35 pF, See Figure 1		25°C	6	18	20	ns
				Full				
t _{OFF}	Turn-off time	V _{NO} = 1.5 V, R _L = 50 Ω, C _L = 35 pF, See Figure 1		25°C	5	10	12	ns
				Full				
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, See Figure 5		25°C	3.2			pC
C _{NO(OFF)}	NO OFF capacitance	f = 1 MHz, See Figure 2		25°C	23			pF
C _{COM(OFF)}	COM OFF capacitance	f = 1 MHz, See Figure 2		25°C	20			pF
C _{COM(ON)}	COM ON capacitance	f = 1 MHz, See Figure 2		25°C	43			pF
BW	Bandwidth	R _L = 50 Ω, Switch ON		25°C	123			MHz
O _{ISO}	OFF isolation ⁽⁷⁾	R _L = 50 Ω, C _L = 5 pF, See Figure 3	f = 1 MHz	25°C	−61		−36	dB
			f = 10 MHz					
X _{TALK}	Crosstalk	R _L = 50 Ω, C _L = 5 pF, See Figure 3	f = 10 MHz	25°C	−95		−73	dB
			f = 100 MHz					
THD	Total harmonic distortion	f = 20 Hz to 20 kHz, V _{COM} = 2 V _{P-P}	R _L = 32 Ω	25°C	0.14%		0.013%	
			R _L = 600 Ω					
DIGITAL CONTROL INPUTS (IN1–IN4)								
V _{IH}	Input logic high			Full	1			V
V _{IL}	Input logic low			Full			0.4	V
I _{IN}	Input leakage current	V _I = 0 or V _{CC}		25°C	0.1	5	10	nA
				Full	−10			
SUPPLY								
V _{CC}	Power-supply range				1.6	3.6		V
I _{CC}	Positive-supply current	V _I = 0 or V _{CC}		25°C		0.05	0.5	μA
				Full				

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.

(3) Typical values are at $T_A = 25^\circ\text{C}$.

(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$

(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.

(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at $T_A = 25^\circ\text{C}$.

(7) OFF isolation = $20_{\log} 10 (V_{COM}/V_{NO})$, V_{COM} = output, V_{NO} = input to OFF switch

6.6 Electrical Characteristics for 3-V Supply

 $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$, $V_{IH} = 1.4 \text{ V}$, $V_{IL} = 0.5 \text{ V}$ (unless otherwise noted).^{(1) (2)}

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP ⁽³⁾	MAX	UNIT
ANALOG SWITCH							
V_{COM} , V_{NO}	Analog signal range			0		V_{CC}	V
R_{on}	ON-state resistance	$V_{CC} = 2.7 \text{ V}$, $I_{COM} = -100 \text{ mA}$, $V_{NO} = 1.5 \text{ V}$	25°C	0.7	0.9		Ω
			Full		1.1		
ΔR_{on}	ON-state resistance match between channels ⁽⁴⁾	$V_{CC} = 2.7 \text{ V}$, $I_{COM} = -100 \text{ mA}$, $V_{NO} = 1.5 \text{ V}$	25°C	0.03	0.05		Ω
			Full		0.15		
$R_{on(Flat)}$	ON-state resistance flatness ⁽⁵⁾	$V_{CC} = 2.7 \text{ V}$, $I_{COM} = -100 \text{ mA}$, $V_{NO} = 1 \text{ V}, 1.5 \text{ V}, 2 \text{ V}$	25°C	0.23	0.4		Ω
			Full		0.5		
$I_{NO(OFF)}$	NO OFF leakage current ⁽⁶⁾	$V_{CC} = 3.6 \text{ V}$, $V_{COM} = 0.3 \text{ V}, 3 \text{ V}$, $V_{NO} = 3 \text{ V}, 0.3 \text{ V}$	25°C	-2	1	2	nA
			Full	-18		18	
$I_{COM(OFF)}$	COM OFF leakage current ⁽⁶⁾	$V_{CC} = 3.6 \text{ V}$, $V_{COM} = 0.3 \text{ V}, 3 \text{ V}$, $V_{NO} = 3 \text{ V}, 0.3 \text{ V}$	25°C	-2	1	2	nA
			Full	-18		18	
$I_{COM(ON)}$	COM ON leakage current ⁽⁶⁾	$V_{CC} = 3.6 \text{ V}$, $V_{COM} = 0.3 \text{ V}, 3 \text{ V}$, $V_{NO} = 0.3 \text{ V}, 3 \text{ V}$, or floating	25°C	-2.5	0.01	2.5	nA
			Full	-5		5	
DYNAMIC							
t_{ON}	Turn-on time	$V_{NO} = 1.5 \text{ V}$, $R_L = 50 \Omega$, $C_L = 35 \text{ pF}$, See Figure 1	25°C	5	14		ns
			Full		15		
t_{OFF}	Turn-off time	$V_{NO} = 1.5 \text{ V}$, $R_L = 50 \Omega$, $C_L = 35 \text{ pF}$, See Figure 1	25°C	4	9		ns
			Full		10		
Q_C	Charge injection	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1 \text{ nF}$, See Figure 5	25°C	3			pC
$C_{NO(OFF)}$	NO OFF capacitance	$f = 1 \text{ MHz}$, See Figure 2	25°C	23			pF
$C_{COM(OFF)}$	COM OFF capacitance	$f = 1 \text{ MHz}$, See Figure 2	25°C	20			pF
$C_{COM(ON)}$	COM ON capacitance	$f = 1 \text{ MHz}$, See Figure 2	25°C	43			pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON	25°C	125			MHz
O_{ISO}	OFF isolation ⁽⁷⁾	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, See Figure 3	f = 10 MHz f = 1 MHz	25°C	-40 -62		dB
X_{TALK}	Crosstalk	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, See Figure 3	f = 10 MHz f = 1 MHz	25°C	-73 -95		dB
THD	Total harmonic distortion	f = 20 Hz to 20 kHz, $V_{COM} = 2 V_{P-P}$	$R_L = 32 \Omega$ $R_L = 600 \Omega$	25°C	0.04% 0.003%		
DIGITAL CONTROL INPUTS (IN1–IN4)							
V_{IH}	Input logic high		Full	1.4			V
V_{IL}	Input logic low		Full		0.5		V
I_{IN}	Input leakage current	$V_I = 0 \text{ or } V_{CC}$	25°C	0.5	1		nA
			Full	-20		20	
SUPPLY							
V_{CC}	Power-supply range			1.6		3.6	V
I_{CC}	Positive-supply current	$V_{CC} = 3.6 \text{ V}$, $V_{IN} = 0 \text{ or } V_{CC}$	25°C		0.075		μA
			Full		0.75		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.

(3) Typical values are at $V_{CC} = 3 \text{ V}$, $T_A = 25^\circ\text{C}$.

(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$

(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.

(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at $T_A = 25^\circ\text{C}$.

(7) OFF isolation = $20_{\log 10} (V_{COM}/V_{NO})$, V_{COM} = output, V_{NO} = input to OFF switch

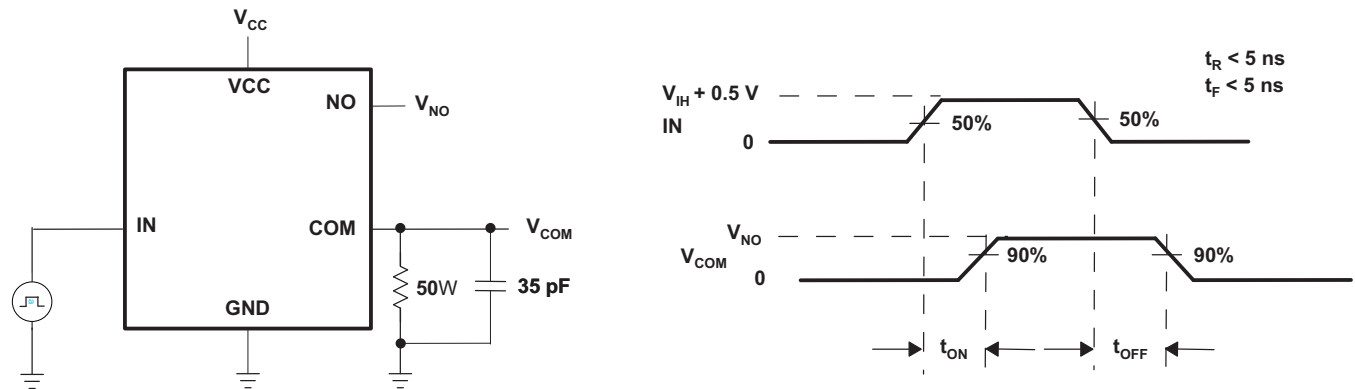


Figure 1. Switching Times

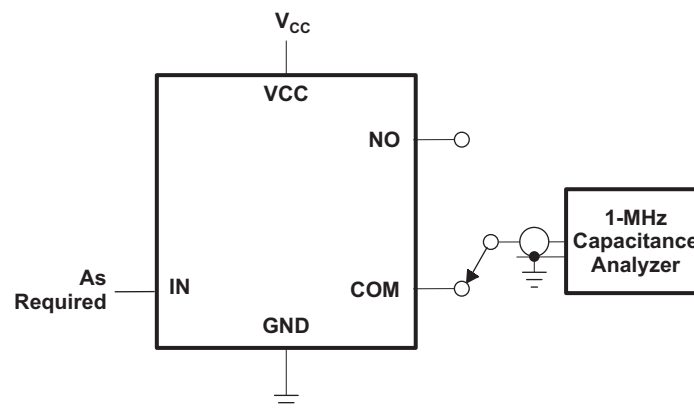
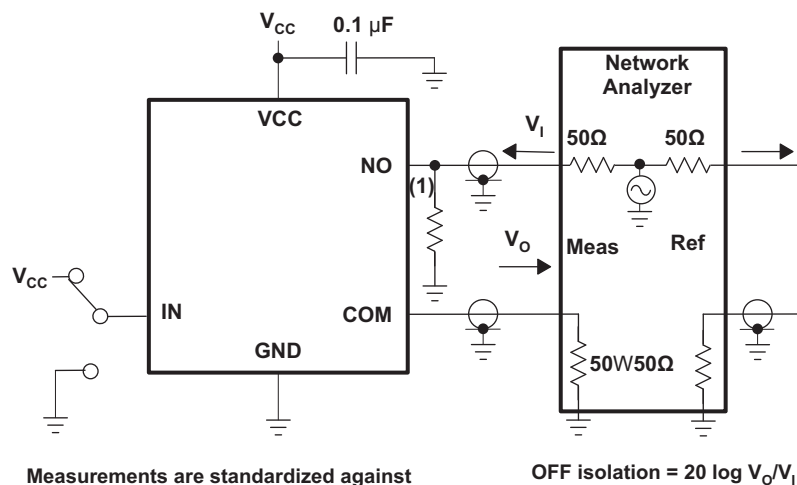


Figure 2. NO and COM Capacitance



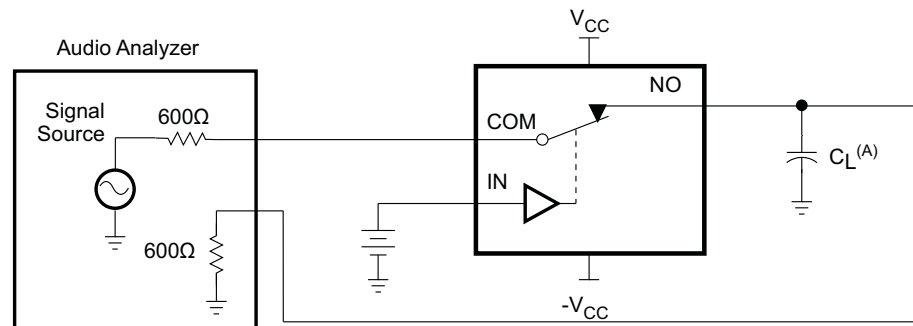
Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. Bandwidth is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF isolation} = 20 \log V_O/V_I$$

(1) Add 50-Ω termination for OFF isolation

Figure 3. OFF Isolation, Bandwidth, and Crosstalk

Channel ON: COM to NO $V_I = V_{CC}$ $C_L = 50 \text{ pF}$
 $V_{SOURCE} = V_{CC} \text{ P-P}$ $f_{SOURCE} = 20 \text{ Hz to } 20 \text{ kHz}$ $R_L = 600\Omega$



A. C_L includes probe and jig capacitance.

Figure 4. Total Harmonic Distortion (THD)

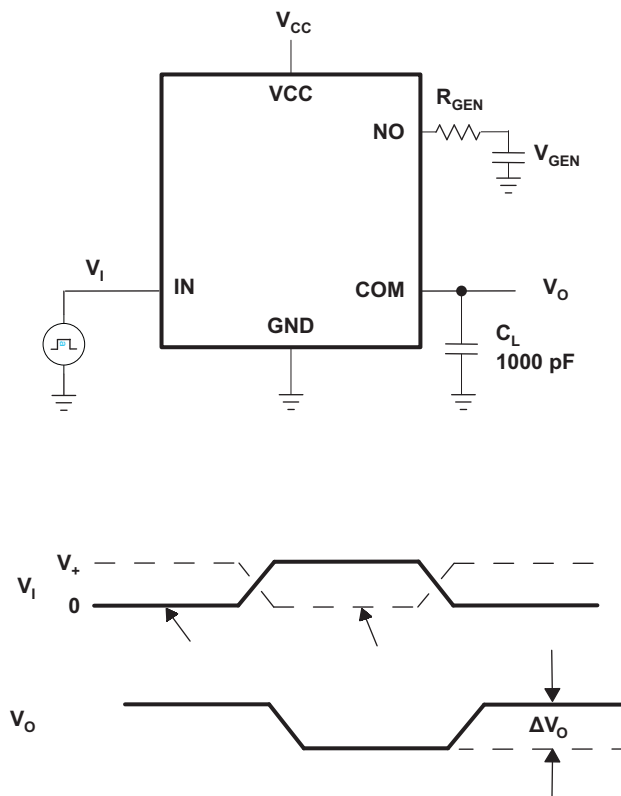
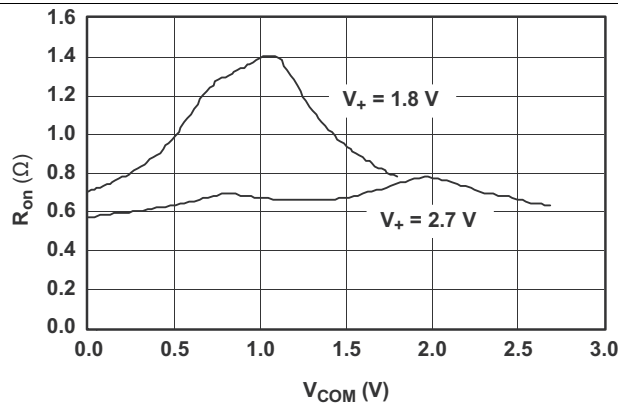
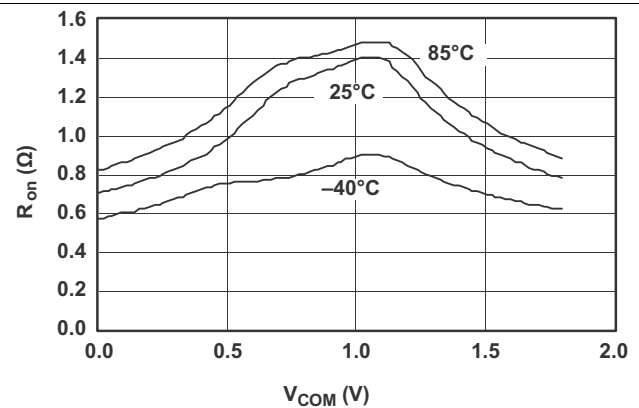
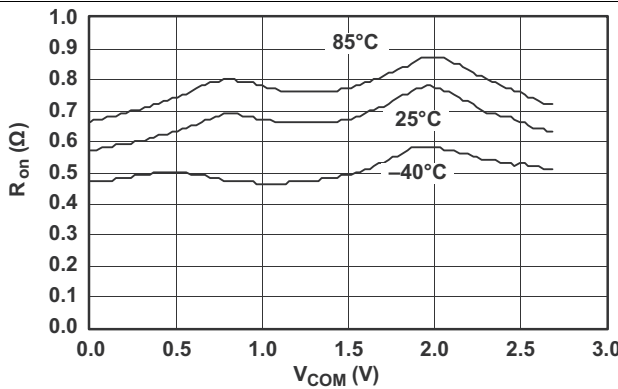
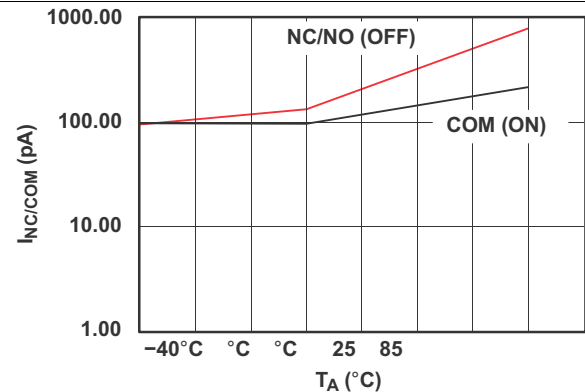
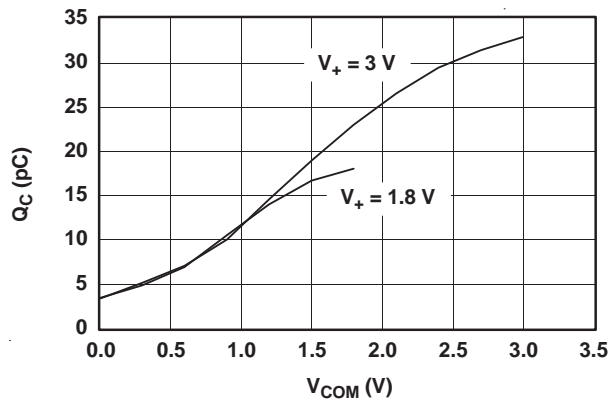
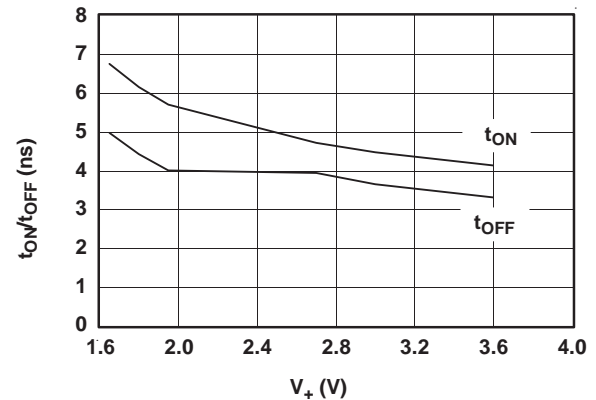


Figure 5. Charge Injection (Q_C)

6.7 Typical Characteristics


Figure 6. R_{on} vs V_{COM}

Figure 7. R_{on} vs V_{COM} ($V_{CC} = 1.8$ V)

Figure 8. R_{on} vs V_{COM} ($V_{CC} = 2.7$ V)

Figure 9. I_{ON} and I_{OFF} vs Temperature ($V_{CC} = 3.6$ V)

Figure 10. Q_C vs V_{COM}

Figure 11. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

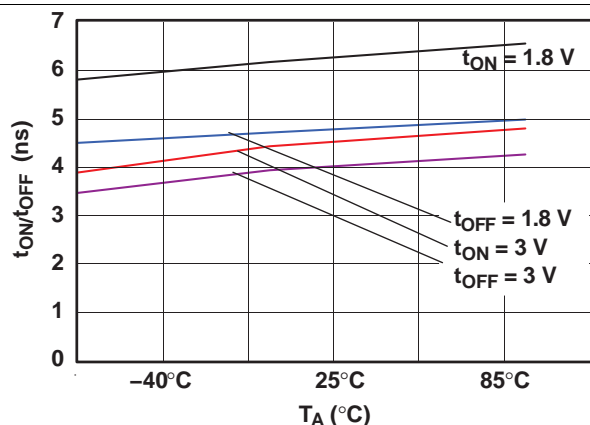


Figure 12. t_{ON} and t_{OFF} vs Temperature

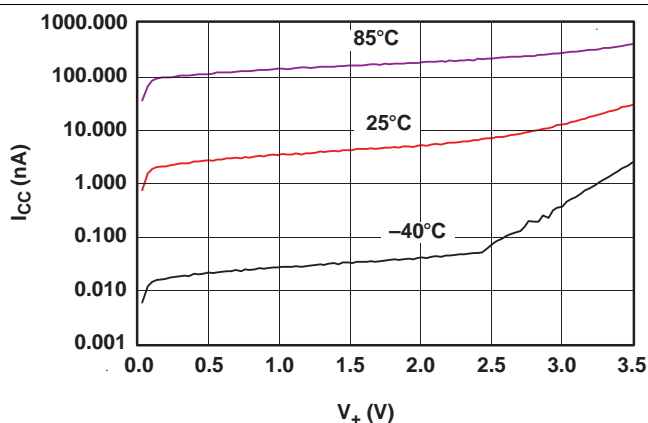


Figure 13. I_{CC} vs V_{CC}

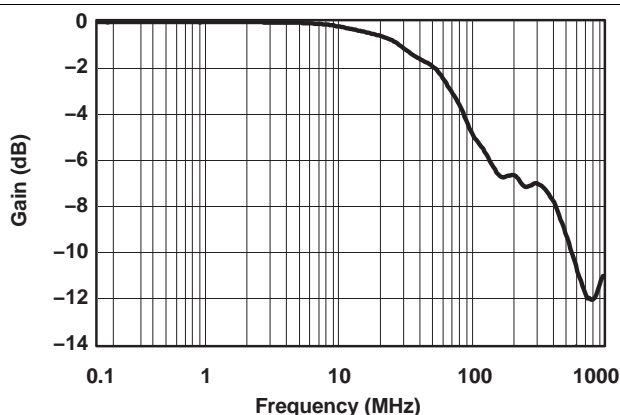


Figure 14. Gain vs Frequency
($V_{CC} = 3$ V)

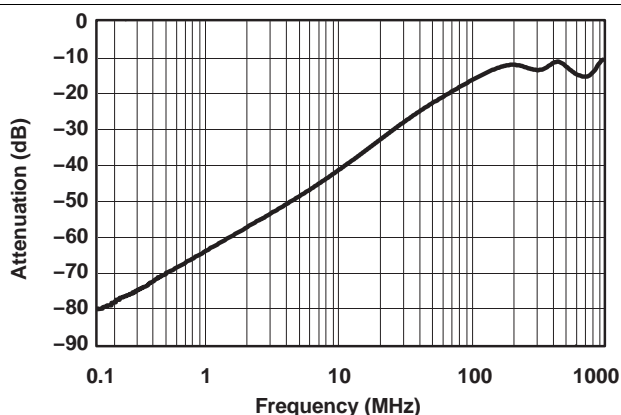


Figure 15. OFF Isolation vs Frequency
($V_{CC} = 3$ V)

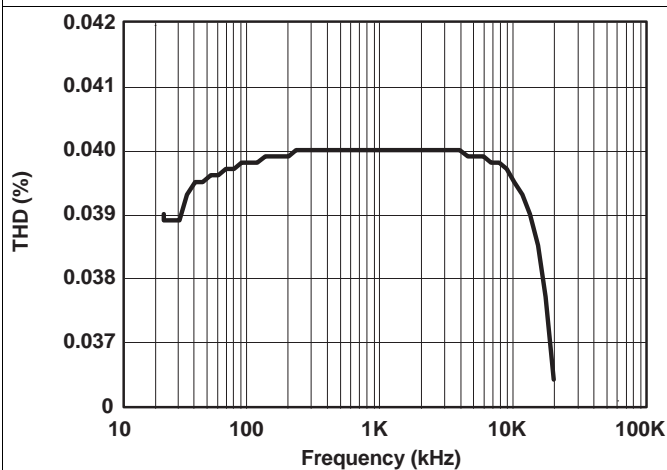


Figure 16. Total Harmonic Distortion vs Frequency
($R_L = 32 \Omega$)

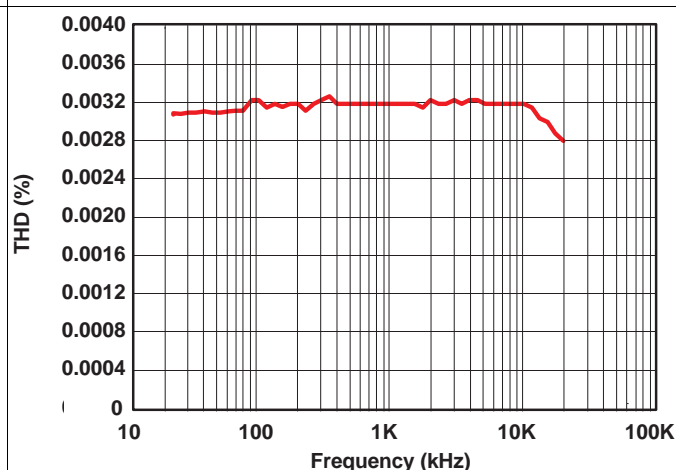


Figure 17. Total Harmonic Distortion vs Frequency
($R_L = 600 \Omega$)

Typical Characteristics (continued)

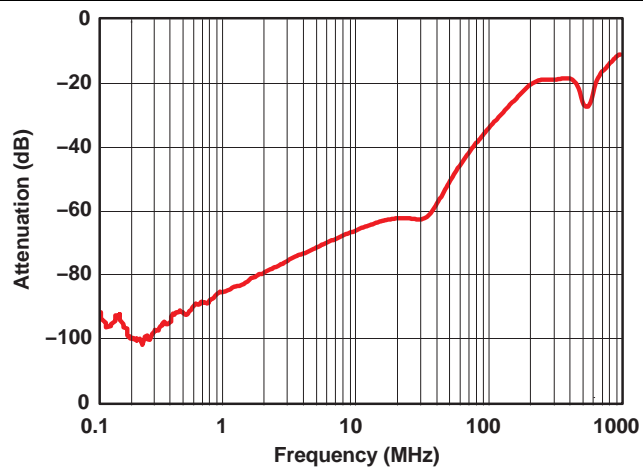


Figure 18. Crosstalk vs Frequency ($V_{CC} = 3\text{ V}$)

7 Detailed Description

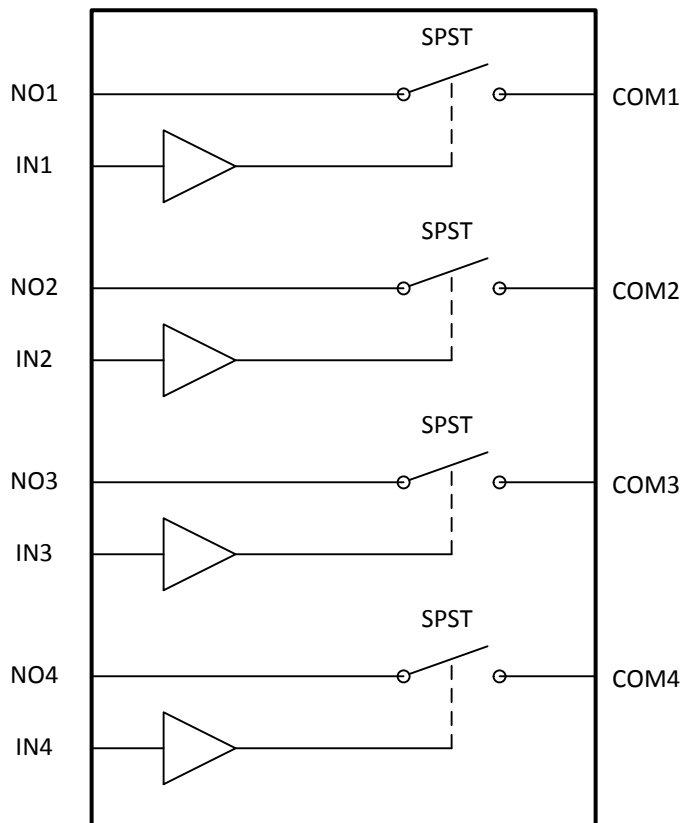
7.1 Overview

The TS3A4751 is a bidirectional, 4-channel, normally open (NO) single-pole single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

The TS3A4751 has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in space-saving 14-pin VQFN (RGY) and micro X2QFN (RUC) packages.

7.2 Functional Block Diagram



7.3 Feature Description

This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V TTL/CMOS compatible when using a 3-V supply.

7.4 Device Functional Modes

Table 1. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Logic Inputs

The TS3A4751 logic inputs can be driven up to 3.6 V, regardless of the supply voltage. For example, with a 1.8-V supply, IN may be driven low to GND and high to 3.6 V. Driving IN rail to rail minimizes power consumption.

8.1.2 Analog Signal Levels

Analog signals that range over the entire supply voltage (V_{CC} to GND) can be passed with very little change in R_{on} (see [Typical Characteristics](#)). The switches are bidirectional, so NO and COM can be used as either inputs or outputs.

8.2 Typical Application

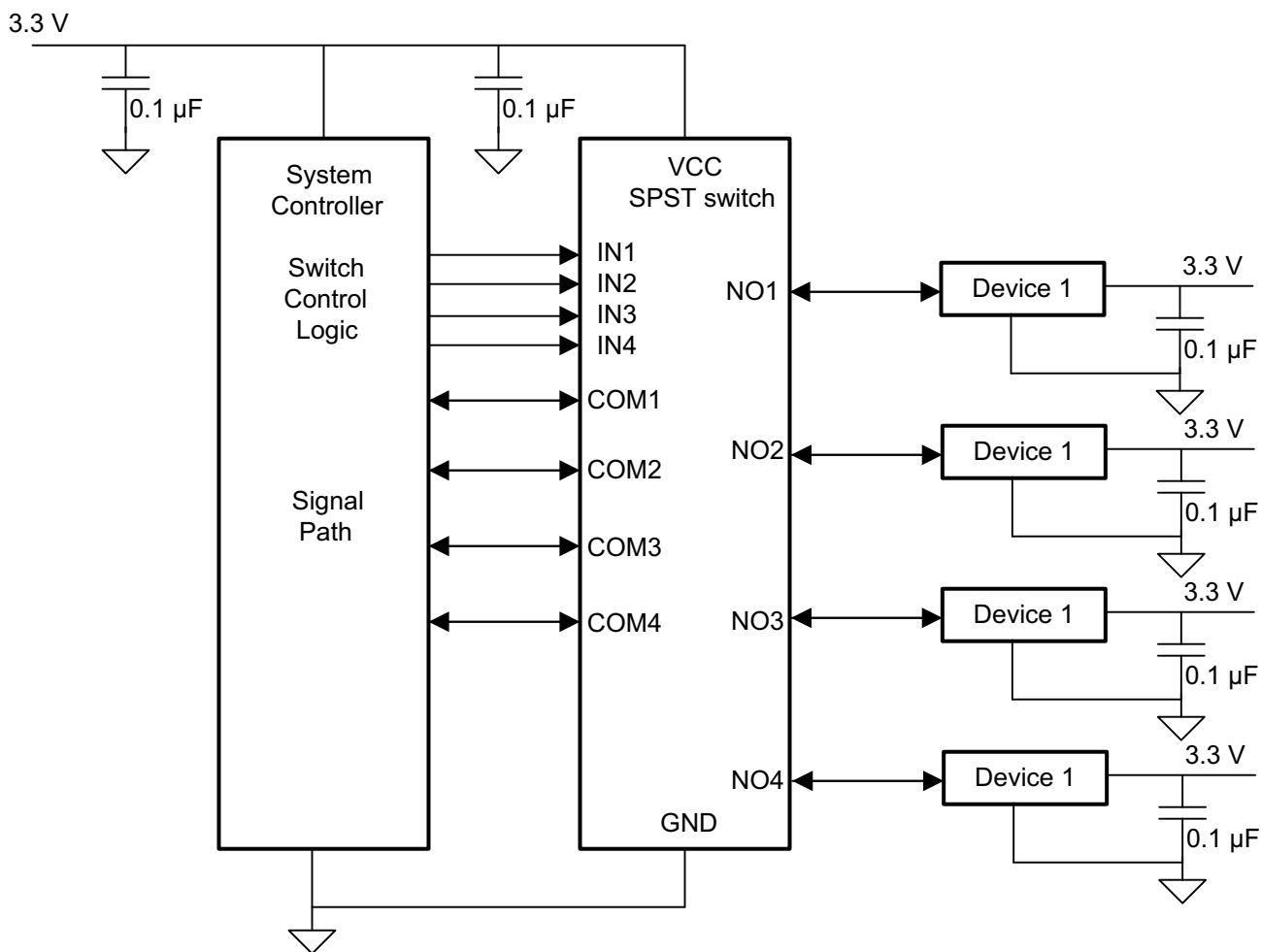


Figure 19. Typical Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

Ensure that all of the signals passing through the switch are within the specified ranges to ensure proper performance.

8.2.2 Detailed Design Procedure

The TS3A4751 can be properly operated without any external components. However, it is recommended that unused pins should be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. It is also recommended that the digital control pins (INX) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

8.2.3 Application Curve

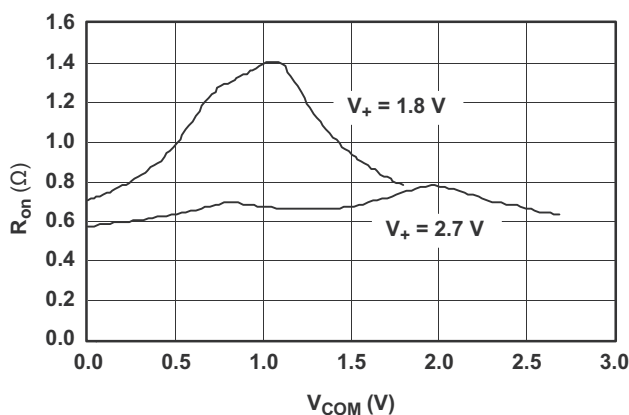


Figure 20. R_{on} vs V_{COM}

9 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1- μF capacitor, connected from V_{CC} to GND, is adequate for most applications.

10 Layout

10.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance.

Reduce stray inductance and capacitance by keeping traces short and wide.

Ensure that bypass capacitors are as close to the device as possible.

Use large ground planes where possible.

10.2 Layout Example

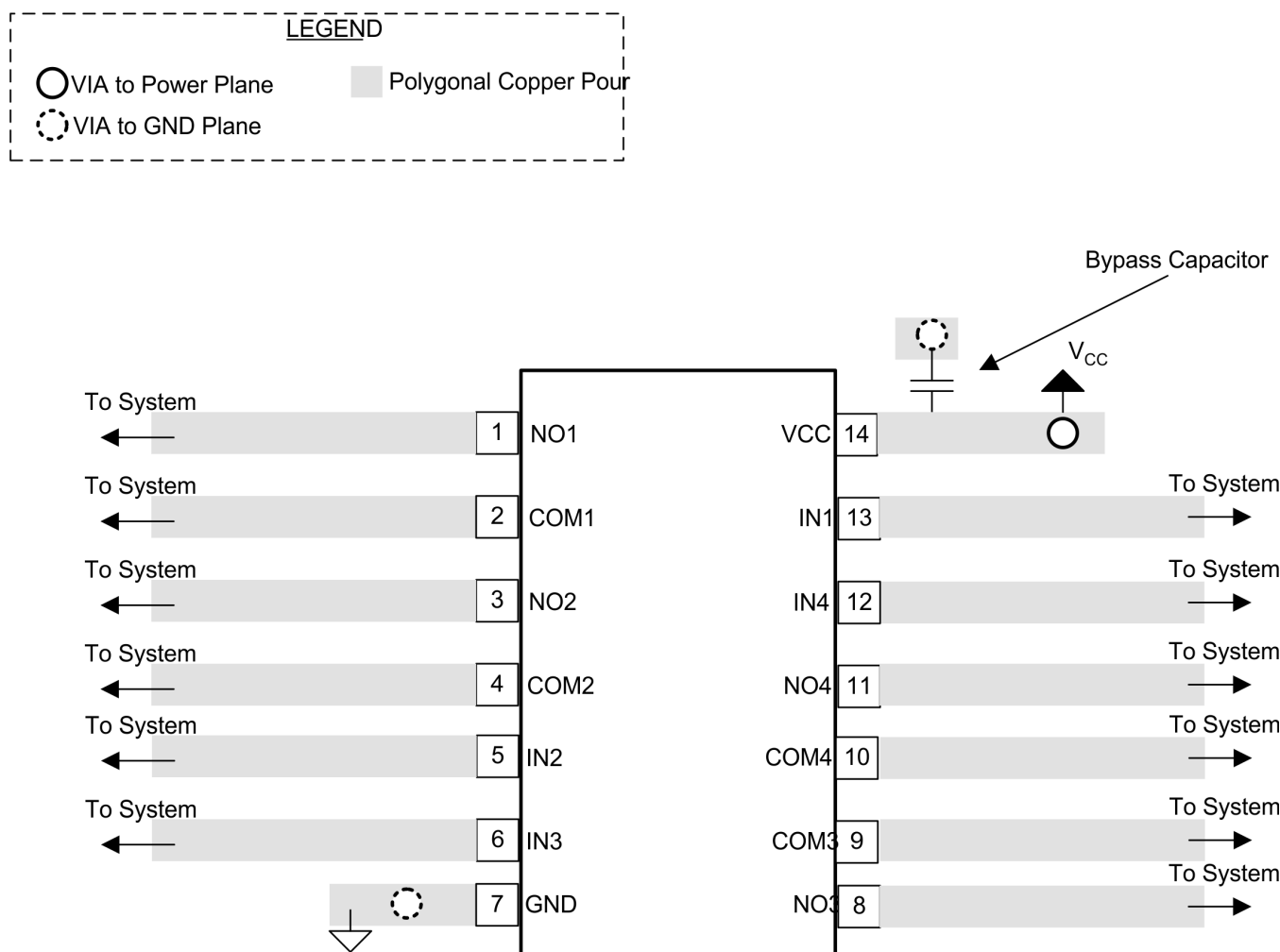


Figure 21. Layout Schematic

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A4751PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC751	Samples
TS3A4751PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC751	Samples
TS3A4751RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YC751	Samples
TS3A4751RUCR	ACTIVE	QFN	RUC	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3MO	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A4751PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A4751RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TS3A4751RUCR	QFN	RUC	14	3000	179.0	8.4	2.25	2.25	0.55	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A4751PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TS3A4751RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
TS3A4751RUCR	QFN	RUC	14	3000	203.0	203.0	35.0

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

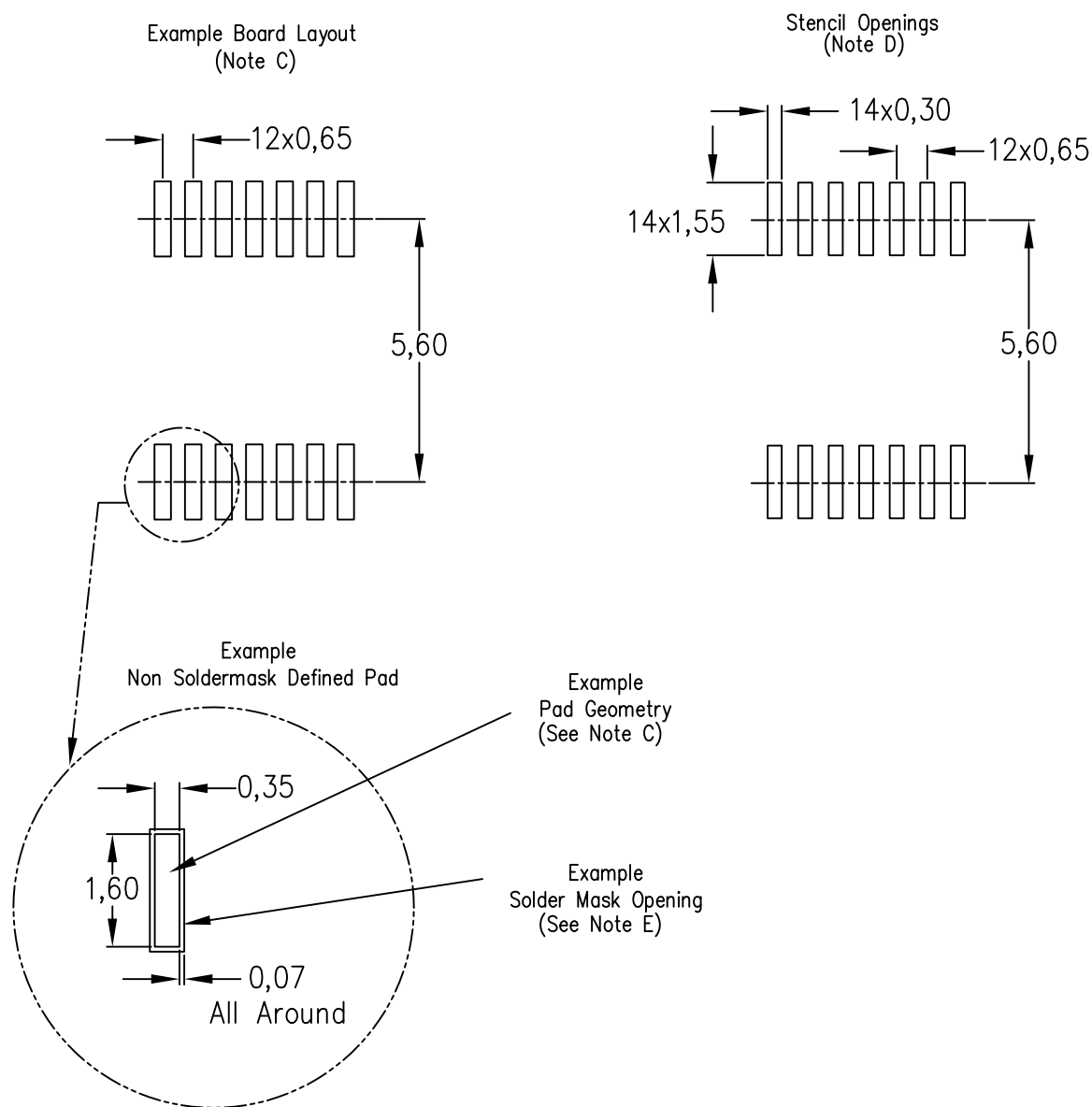


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

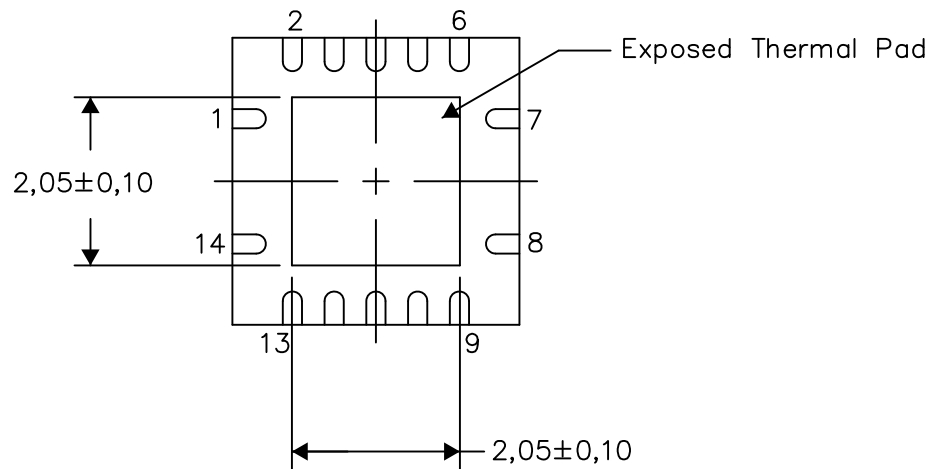
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

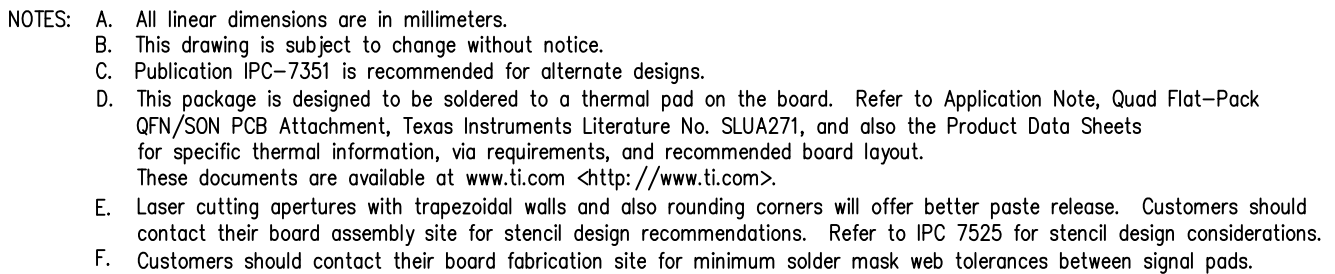


Bottom View

Exposed Thermal Pad Dimensions

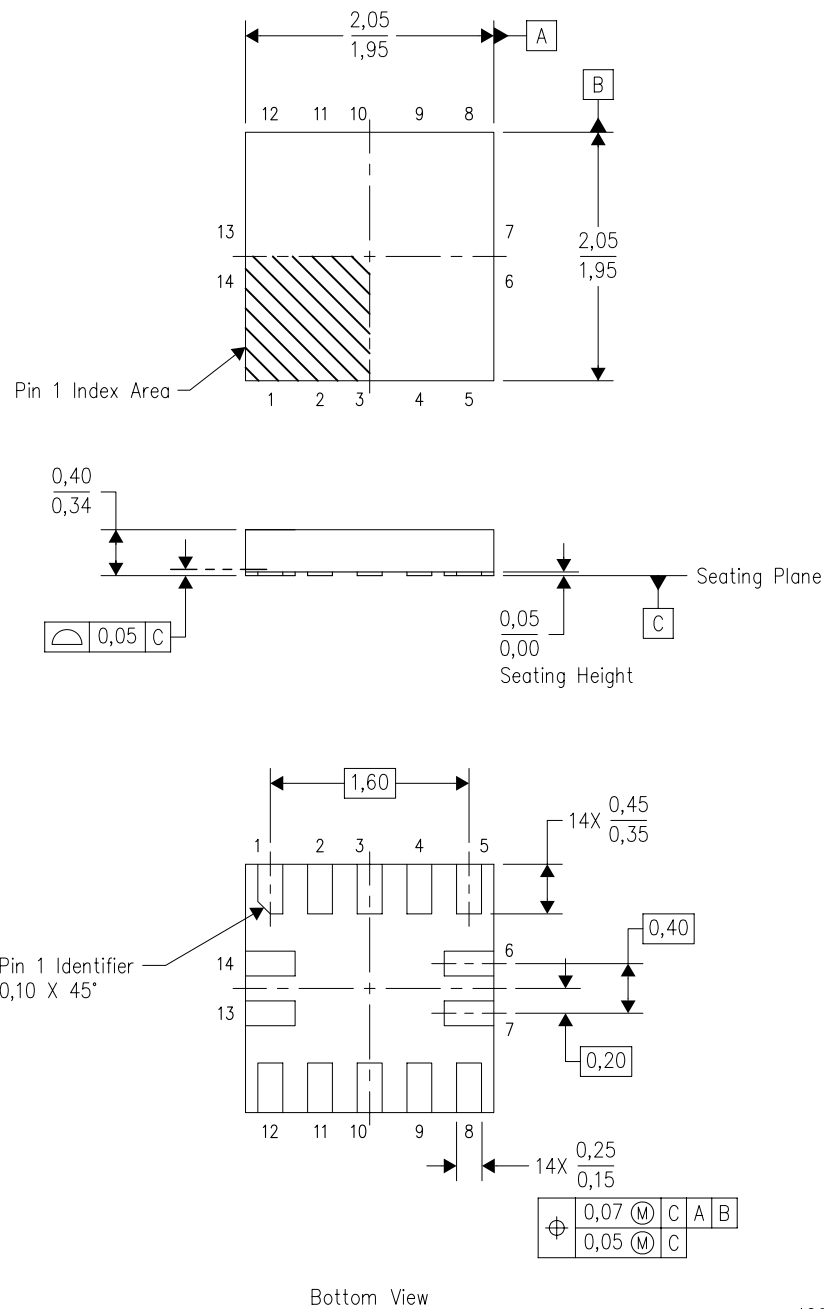
4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters



RUC (S-PX2QFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



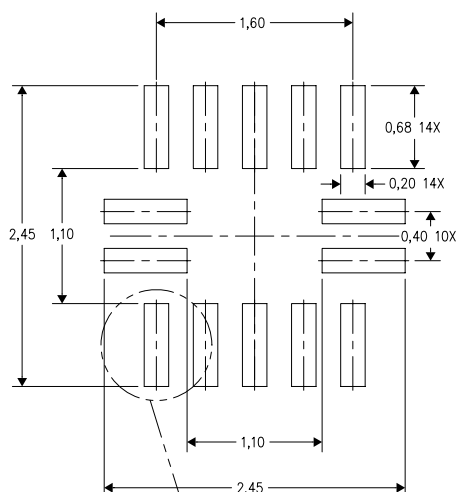
4208447/C 08/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation X2GFE.

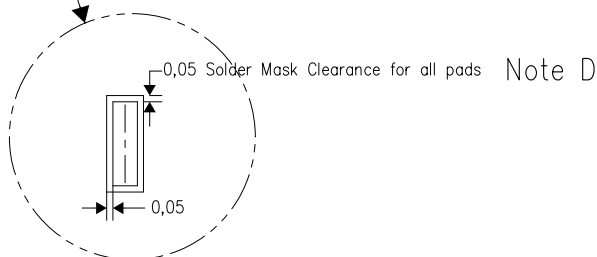
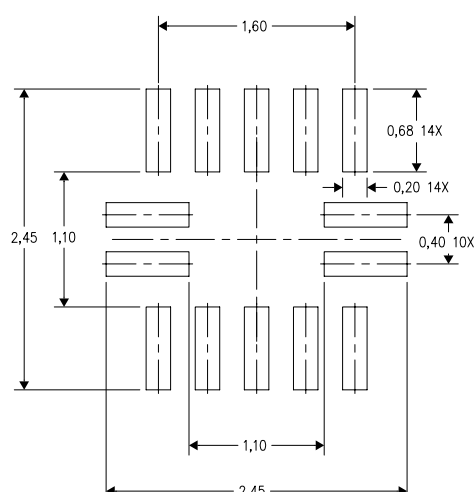
RUC (S-PX2QFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout



Example Stencil Design
(Note E)



4211124/A 06/10

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com

AMEYA360

Components Supply Platform

Authorized Distribution Brand :



Website :

Welcome to visit www.ameya360.com

Contact Us :

➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd
Minhang District, Shanghai , China

➤ Sales :

Direct +86 (21) 6401-6692
Email amall@ameya360.com
QQ 800077892
Skype ameyasales1 ameyasales2

➤ Customer Service :

Email service@ameya360.com

➤ Partnership :

Tel +86 (21) 64016692-8333
Email mkt@ameya360.com