IRS2552D

CCFL/EEFL BALLAST CONTROLLER IC

Features

- Drives up to two IGBT/MOSFET power devices
- Integrated programmable oscillator
- Soft start function
- 15.6 V voltage clamp on V_{CC}
- Micro-power startup
- 0 V to 5 V input analog dimming
- Programmable ignition frequency
- Programmable ignition time
- Lamp current control
- Programmable deadtime
- Supports multi-lamp operation
- Burst dimming with soft start at every burst
- Latched open circuit protection
- Integrated bootstrap functionality
- Excellent latch immunity on all inputs & outputs
- Integrated ESD protection on all pins

Typical Application

- CCFL/EEFL inverter

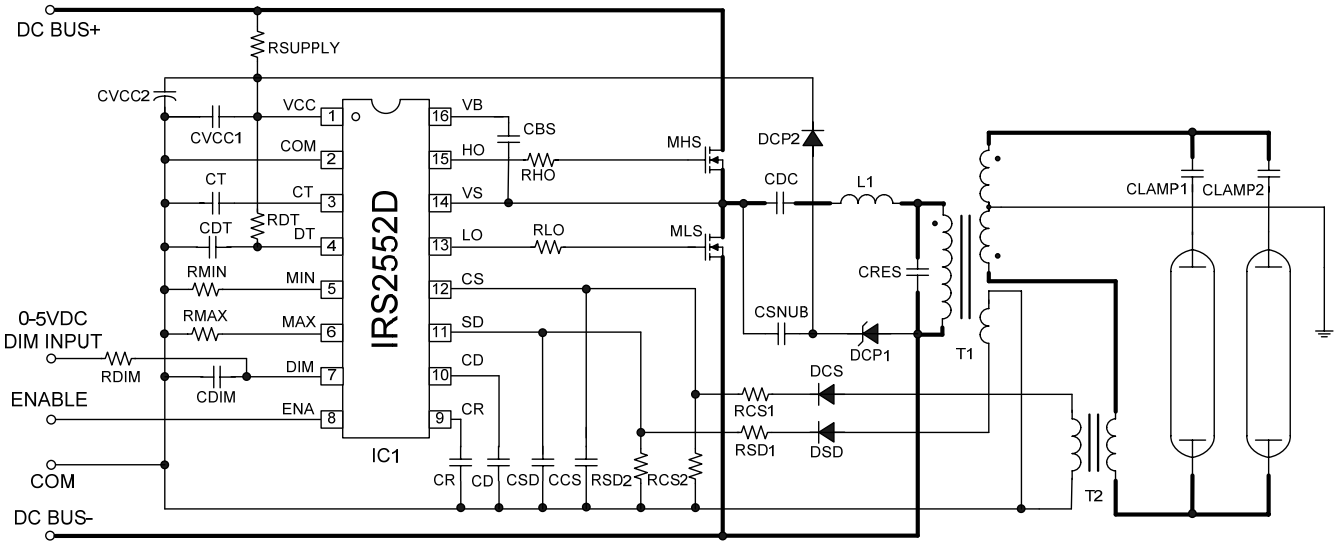
Product Summary

Topology	Half-Bridge
V_{OFFSET}	600 V
V_{OUT}	V_{CC}
I_{O+} & I_{O-} (typical)	300 mA & 450 mA
Deadtime (programmable)	500ns ~ 2µs

Package Options

16-Lead PDIP
16-Lead SOIC (Narrow Body)

Typical Application Diagram



Description

The IRS2552D incorporates a high voltage half-bridge gate driver with a front end that incorporates full control functionality for CCFL/EEFL ballasts. Includes a programmable ignition and supports dimming via analog or PWM control voltage. HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. Noise immunity is achieved with low di/dt peak of the gate drivers, and with an undervoltage lockout hysteresis of approximately 1 V. The IRS2552D also includes protection features for over-current and over-voltage of the lamps.

Qualification Information†

Qualification Level		Industrial†† (per JEDEC JESD 47E)	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC16	MSL3††† (per IPC/JEDEC J-STD-020C)
		PDIP16	Not applicable (non-surface mount package style)
ESD	Machine Model	Class C (per JEDEC standard EIA/JESD22-A115-A)	
	Human Body Model	Class 3A (per EIA/JEDEC standard JESD22-A114-B)	
IC Latch-Up Test		Class I, Level A (per JESD78A)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating supply voltage		-0.3	625	V
V_S	High-side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_H	High-side floating output voltage		V_S – 0.3	V_B + 0.3	
V_L	Low-side output voltage		-0.3	V_{CC} + 0.3	
V_{CO}	VCO pin voltage		-0.3	V_{CC} + 0.3	
V_{CT}	CT pin voltage		-0.3	V_{CC} + 0.3	
V_{DT}	DT pin voltage		-0.3	V_{CC} + 0.3	
MIN	MIN pin voltage		-0.3	V_{CC} + 0.3	
DIM	DIM pin voltage		-0.3	V_{CC} + 0.3	
CR	CR pin voltage		-0.3	V_{CC} + 0.3	
CD	CD pin voltage		-0.3	V_{CC} + 0.3	
SD	SD pin voltage		-0.3	V_{CC} + 0.3	
CS	CS pin voltage		-0.3	V_{CC} + 0.3	
I_{CC}	Supply current†		---	25	mA
dV_S/dt	Allowable offset voltage slew rate		-50	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ ºC	16L-PDIP	---	1.3	W
		16L-SOIC	---	1.4	
$R_{\Theta JA}$	Thermal resistance, junction to ambient	16L-PDIP	---	70	ºC/W
		16L-SOIC	---	82	
T_J	Junction temperature		-55	150	ºC
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		---	300	

† This IC contains a voltage clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6 V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{BS}	High-side floating supply voltage	V_{CC} – 0.7	V_{CLAMP}	V
V_S	Steady-state high-side floating supply offset voltage	-3.0†	600	
V_{CC}	Supply voltage	V_{CCUV+} +0.1V	V_{CLAMP}	
I_{CC}	Supply current	††	10	mA
T_J	Junction temperature	-40	125	ºC

† Care should be taken to avoid output switching conditions where the V_S node flies inductively below ground by more than 5 V.

†† Enough current should be supplied to the V_{CC} pin of the IC to keep the internal 15.6 V zener diode clamping the voltage at this pin.

Recommended Component Values

Symbol	Component	Min.	Max.	Units
R_{MIN}	MIN pin resistor value	5	---	kΩ
R_{MAX}	MAX pin resistor value	5		
R_{DT}	DT pin resistor value	22		
C_T	CT pin capacitor value	330	---	pF
C_{DT}	DT pin capacitor value	47		
C_R	CR pin capacitor value	1	---	nF
C_D	CD pin capacitor value	1		

Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 14 V, C_T = 1 nF and T_A = 25 °C unless otherwise specified. The input parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Voltage Supply Characteristics						
V_{CCUV+}	Rising V_{CC} undervoltage lockout threshold	9.5	10.5	11.5	V	N/A
V_{CCUV-}	Falling V_{CC} undervoltage lockout threshold	8.5	9.5	10.5		
$V_{CCUVHYS}$	V_{CC} undervoltage lockout hysteresis	0.5	1	1.5		
I_{QCCUV}	Micropower startup V_{CC} supply current	---	300	350	µA	V_{CC} = V_{CCUV+} -100 mV rising
I_{QCC}	Quiescent V_{CC} supply current	---	4.0	4.5	mA	R_{MIN} = 12 kΩ, RUN MODE CT = 0 V
I_{QCCFLT}	V_{CC} supply current	---	0.9	1.3		Fault mode
$I_{CC,FMIN}$	V_{CC} current @ f_{osc} = fMIN	---	4.7	5.3		R_{MIN} = 12 kΩ, RUN MODE
V_{CLAMP}	V_{CC} clamp voltage	14.6	15.6	16.6	V	I_{CC} = 19 mA
Floating Supply Characteristics						
I_{QBSUV}	Micropower startup V_{BS} supply current	---	6	20	µA	$V_{CC} \le V_{CCUV-}$, $V_{CC} = V_{BS}$
I_{BS}	V_{BS} supply current	---	1000	1200		HO oscillating
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	6.5	7.5	8.5	V	N/A
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	6.0	7.0	8.0		
I_{LK}	Offset supply leakage current	---	---	50	µA	$V_B = V_S$ = 600 V
Oscillator I/O Characteristics						
f_{MIN}	Minimum oscillator frequency	36.5	39	42.5	kHz	R_{MIN} = 12 kΩ, RUN MODE
f_{MAX}	Maximum oscillator frequency	67	69	71		R_{MAX} = 6.8 kΩ, IGNITION MODE
V_{CT+}	Upper CT ramp voltage threshold	4.8	5.0	5.2	V	N/A
V_{CT-}	Lower CT ramp voltage threshold	---	0	---		
I_{CT}	CT pin source current	350	410	470	µA	R_{MIN} =12 kΩ, RUN MODE
V_{MIN}	VMIN pin voltage	4.8	5.0	5.2	V	N/A
V_{MAX}	VMAX pin voltage	4.8	5.0	5.2		
$V_{MIN,FLT}$	VMIN voltage in fault mode	---	0	---		
$V_{MAX,FLT}$	VMAX voltage in fault mode	---	0	---		

Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 14 V, C_T = 1 nF and T_A = 25 °C unless otherwise specified. The input parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

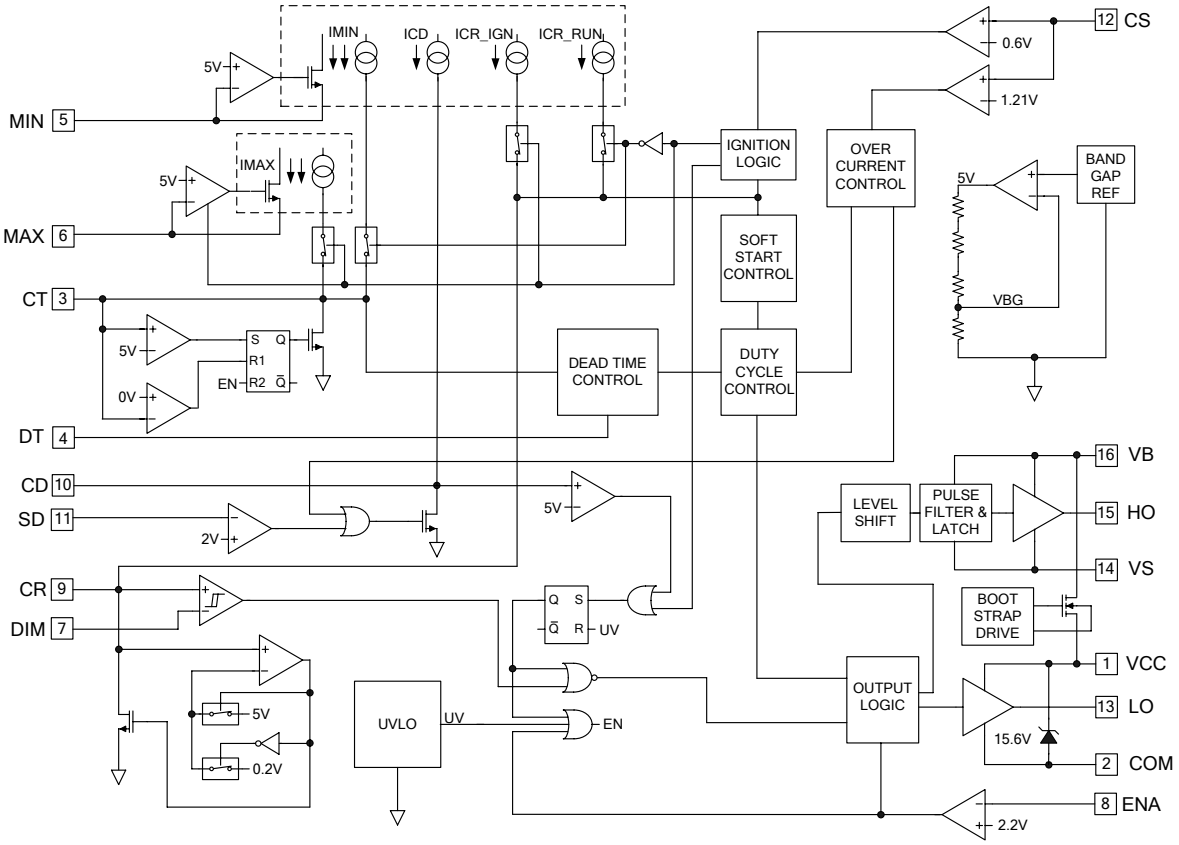
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Ignition						
$I_{CR,IGN}$	Source current at CR pin in IGN mode	3.7	4.5	5.3	µA	R_{MIN} = 12 kΩ, IGNITION MODE
$V_{CS,IGN}$	Ignition detection threshold	0.57	0.6	0.63	V	N/A
Gate Driver Output Characteristics						
V_{OH}	High-level output voltage, V_{BIAS} – V_O	---	V_{CC}	---	V	I_O = 0 A
V_{OL}	Low-level output voltage, VO	---	COM	---	mV	I_O = 0 A
$V_{OL,UV}$	UV-mode output voltage, VO	---	COM	---	mV	I_O = 0 A, $V_{CC} \le V_{CCUV-}$
t_R	Output rise time	---	80	150	ns	N/A
t_F	Output fall time	---	45	100	ns	N/A
t_D	Output deadtime (HO or LO)	1.0	1.1	1.2	µs	R_{DT} = 2.2 kΩ, C_{DT} = 1 nF
I_{O+}	Output source current	---	300	---	mA	N/A
I_{O-}	Output sink current	---	450	---	mA	N/A
Bootstrap FET Characteristics						
$V_{B,ON}$	V_B when the bootstrap FET is on	13.2	13.5	---	V	N/A
$I_{B,CAP}$	V_B source current when FET is on	40	55	---	mA	C_{BS} = 0.1 µF
$I_{B,10V}$	V_B source current when FET is on	9	12	---	mA	V_B = 10 V
Shutdown						
$V_{SD,TH}$	Shutdown threshold at SD pin	1.9	2.0	2.1	V	N/A
$I_{CD,source}$	CD pin source current	3.7	4.5	5.3	µA	V_{SD}>$V_{SD,TH}$, R_{MIN} = 12 kΩ
$V_{CD,TH}$	Threshold at which CD triggers shutdown	4.8	5.0	5.2	V	V_{CC} = 14 V

Electrical Characteristics

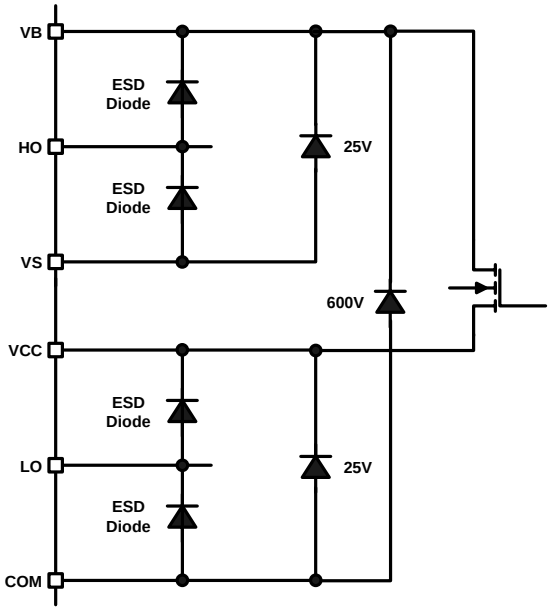
V_{BIAS} (V_{CC}, V_{BS}) = 14 V, C_T = 1 nF and T_A = 25 °C unless otherwise specified. The input parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

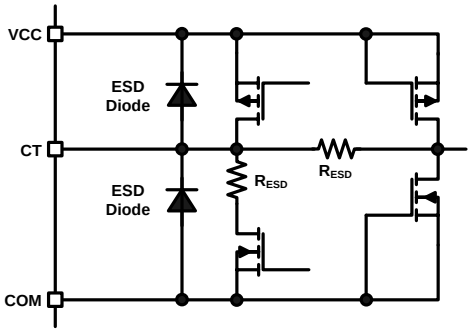
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Over-Current Compensation						
$V_{CS,TH}$	Current compensation threshold at CS pin	1.15	1.21	1.27	V	N/A
$I_{CD,OC}$	Source current at CD pin when the IC is in current compensation mode	3.7	4.5	5.3	µA	V_{CS}>$V_{CS,TH}$, R_{MIN} = 12 kΩ
$V_{CD,oc}$	Voltage on CD where duty cycle reaches minimum	4.8	5.0	5.2	V	N/A
DC_{MIN}	Minimum HO duty cycle	---	10%	---	---	V_{CD} = 4.7 V, RUN MODE
Dimming						
V_{CR+}	CR pin upper threshold voltage	4.8	5.0	5.2	V	N/A
V_{CR-}	CR pin lower threshold voltage	---	0.2	---		
$I_{CR,RUN}$	Source current at CR pin in RUN mode	125	150	175	µA	R_{MIN} = 12 kΩ
f_{CR}	Frequency at CR pin	240	310	370	Hz	C_R = 100 nF, RUN MODE, R_{MIN} = 12 kΩ
Soft Start						
DC_{MIN}	Minimum HO duty cycle	---	10%	---	---	V_{CR} = 0 V, V_{DIM} < $V_{DIM,SS}$
$V_{CR,SS}$	End of soft start voltage	0.88	0.96	1.04	V	V_{DIM} < $V_{DIM,SS}$
$V_{DIM,SS}$	Soft start disable threshold	---	4.8	---		N/A
Enable						
V_{ENATH}	Enable threshold	1.9	2.2	2.5	V	N/A
V_{ENAHYS}	Enable hysteresis	---	200	---	mV	

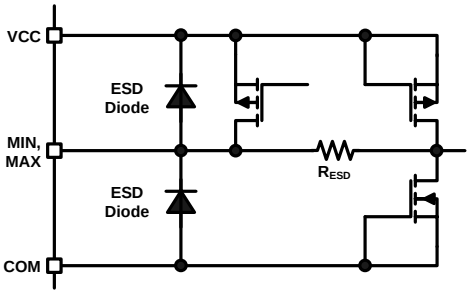
Functional Block Diagram

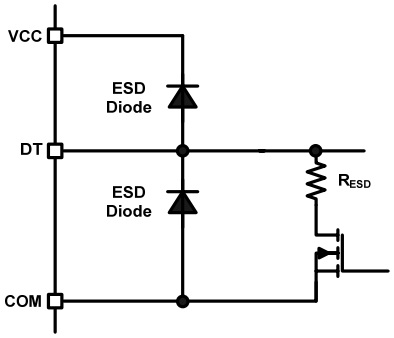


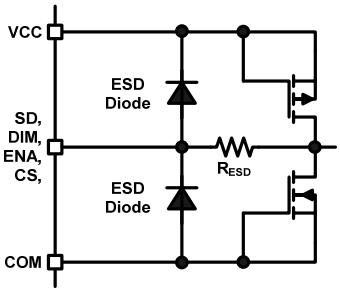
Input/Output Pin Equivalent Circuit Diagrams: IRS2552D

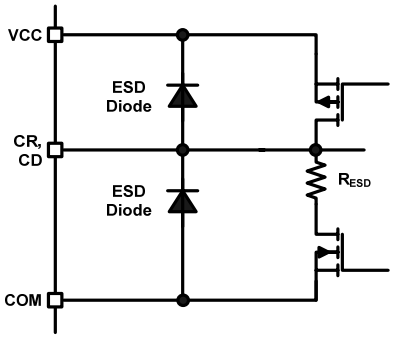








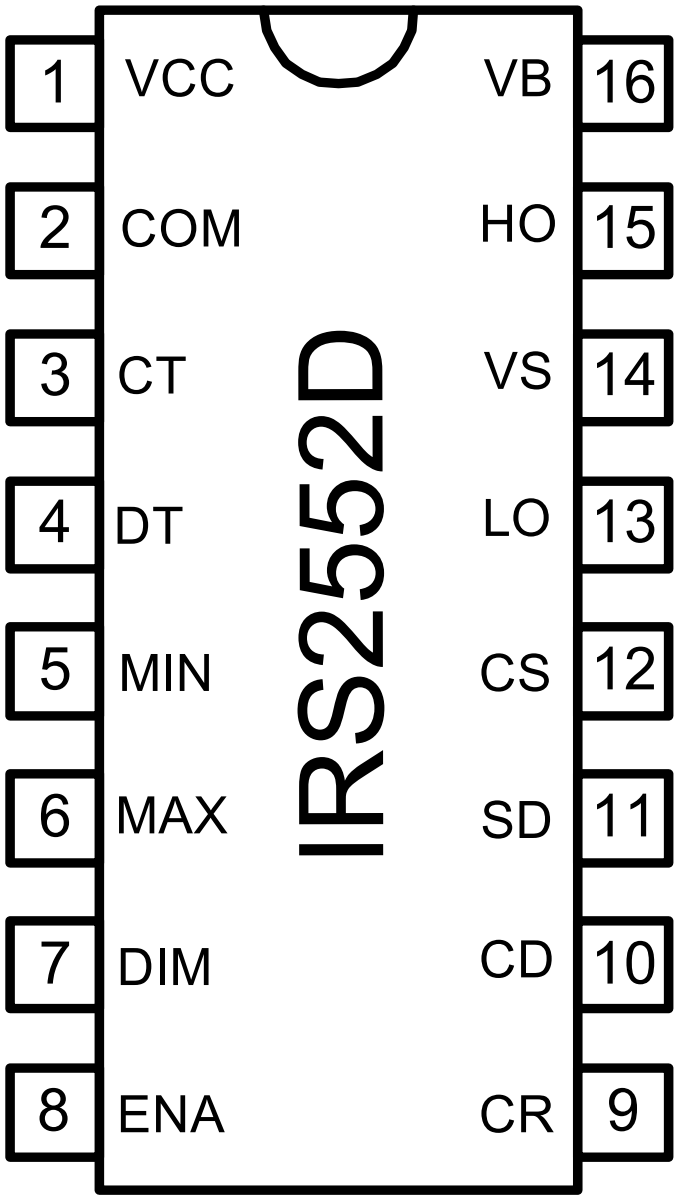




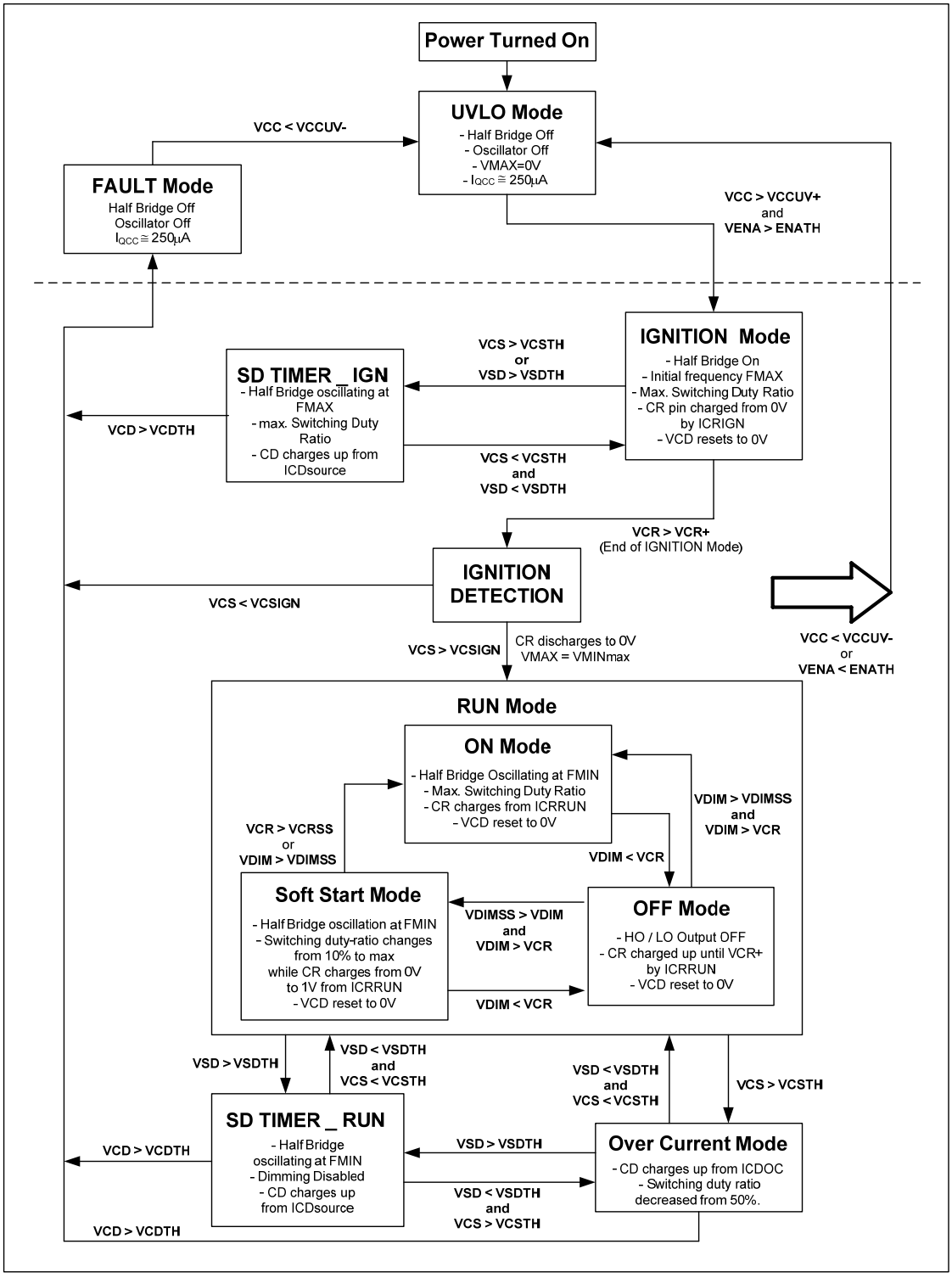
Lead Definitions

Symbol	Description
VCC	Logic and internal gate drive supply voltage
COM	IC power and signal ground
CT	Oscillator timing capacitor
DT	Independent dead time R and C
MIN	RFMIN sets running frequency
MAX	RFMAX sets ignition mode frequency
DIM	0 to 5 V DC burst mode dimming control input
ENA	Chip Enable (2 V logic threshold)
CR	Burst dimming ramp
CD	Shutdown delay timing
SD	Open load detection
CS	Ignition detection (0.6 V threshold), over-current (1.2 V threshold)
LO	Low side output
VS	Half bridge
HO	High side output
VB	High side floating supply

Lead Assignments



State Diagram†



† All values are typical. Applies to application circuit on page 1.

Application Information and Additional Details

Information regarding the following topics is included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Undervoltage Lockout Protection
- Oscillator
- Deadtime
- Ignition
- Run Mode
- Lamp Current Control
- Frequency, Current and Deadtime Calculation
- Dimming Function
- Soft Start
- PCB Layout Tips
- Additional Documentation

IGBT/MOSFET Gate Drive

The IRS2552D HVICs are designed to drive up to two MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

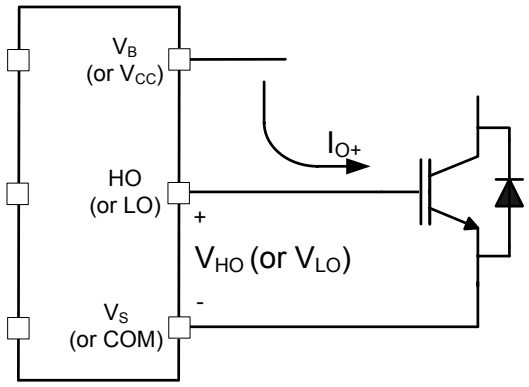


Figure 1: HVIC sourcing current

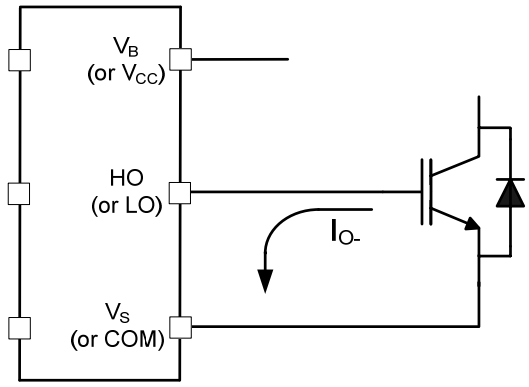


Figure 2: HVIC sinking current

Undervoltage Lock-Out

The IRS2552D includes an under voltage lockout circuit such that it remains in micro-power mode until the voltage at VCC pin exceeds the V_{CCUV+} threshold. When V_{CC} exceeds the V_{CCUV+} threshold the IRS2552D oscillator starts up and gate drive signals appear at the LO and HO outputs, provided the ENABLE pin is connected to a voltage source above V_{ENATH}. The LO output will always go high first in order to pre-charge the bootstrap capacitor before the IRS2552D begins normal operation.

Oscillator

During UVLO and shutdown and the voltage at the MIN and MAX pins remain at 0 V. When V_{CC} is raised above V_{CCUV+} the oscillator will start and LO and HO will produce output drive waveforms at frequency F_{MAX}. The MAX pin sources 5 V and the resistance connected from this point to COM determines the C_T charging current and consequently the frequency. R_{MIN} is always connected from the MIN pin to COM, which sets the RUN mode frequency. In IGNITION mode the MAX pin supplies 5 V to R_{MAX}, which is connected to COM setting a higher C_T charging current and consequently a higher ignition frequency, as R_{MAX} is smaller than R_{MIN}. In RUN mode the MAX pin is no longer active and the voltage will drop to 0V. C_T charges until the voltage reaches the 5 V threshold and then it is discharged rapidly to V_{CT-}. It then begins to charge again, repeating this sequence and producing a saw tooth waveform. The MIN pin sources 5 V during IGNITION and RUN modes. The current flowing through F_{MIN} to COM determines the charging current of C_T during RUN mode and also serves as a current reference for the currents supplied from the CD and CR pins.

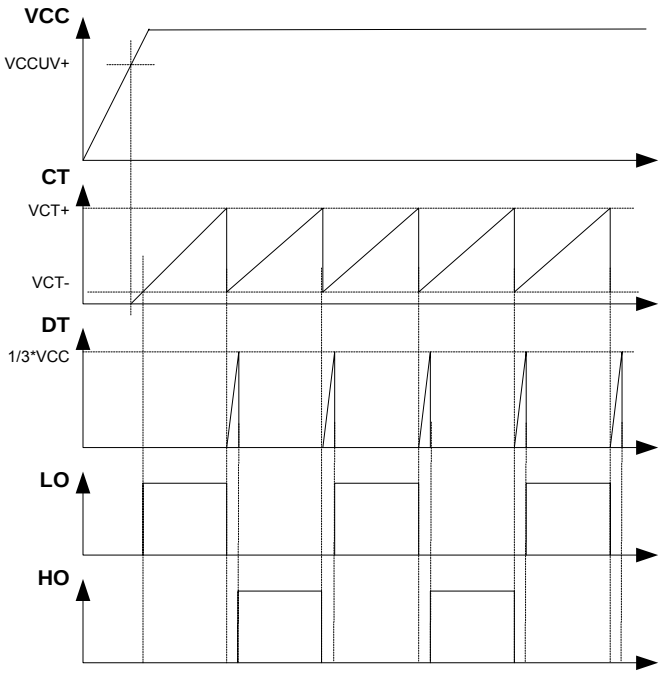


Figure 3: Oscillator waveforms

Deadtime

In the IRS2552D the dead time is determined by an independent external timing circuit comprising of R_{DT} and C_{DT} and is not affected by the values of C_T, R_{MIN} or R_{MAX}. The DT pin voltage is held at COM when LO or HO is high. C_{DT} is charged through R_{DT}, which is connected to VCC, when DT is internally disconnected from COM at the start of the dead time. The dead time ends when C_{DT} has charged to 1/3 V_{CC}. This allows the dead time to remain consistent over the working range of V_{CC}, i.e. from UVLO+ to the clamp voltage of 15.6 V.

Ignition

During the IGNITION phase the C_R capacitor is charged through an internal current source ICR_IGN. When C_R reaches V_{CR+} then if the voltage at CS is greater than VCS_{IGN}, the IRS2552D will enter RUN mode. If the voltage at the CS pin is less than VCS_{IGN} the IRS2552D will enter FAULT mode whereby LO and HO will both go low and the IRS2552D will shut down until V_{CC} is reduced below V_{CCUV-} and then increased above V_{CCU+}. The ignition function is achieved by applying a frequency somewhat above resonance to the output step up transformer and resonant load. This should develop sufficient voltage across the lamps to allow partial ignition and some arc current to flow. The combined lamp current is fed back to the CS pin through a suitable isolating network to determine whether the lamps have ignited successfully. If a successful ignition is detected after the voltage at C_R has reached V_{CR+} then R_{MAX} is disconnected inside the IRS2552D and the frequency will switch immediately to

to F_{MIN}, therefore applying maximum power to the lamps. At this point the burst mode dimming function will be enabled.

Run Mode

In RUN mode an additional current source ICR_RUN is also switched into the circuit. This causes C_R to ramp up to V_{CR+} much more rapidly than before. The C_R pin is used to provide ignition timing as well as the burst mode dimming low frequency ramp.

If the output is open circuit a very large voltage develops at the output. This is fed back to the SD pin through some suitable isolated sensing network such that the voltage at the SD pin will exceed VSDTH during an over-voltage condition. At this stage the capacitor C_D begins to charge through a current source. When VSD > VSDTH the burst mode dimming function is disabled and the output will be continuous.

If the voltage at SD drops below VSDTH the capacitor C_D will be discharged to 0V again. If SD remains above VSDTH long enough for the C_D capacitor voltage to reach VCDMAX or about 5 V then the IRS2552D will shut down and go into fault mode.

Lamp Current Control

Additionally the half bridge current is monitored at the CS pin so that during running if too much power is supplied to the lamps the IRS2552D is able to compensate by reducing the oscillator duty cycle while maintaining the same run frequency. This prevents the lamps from being over driven preventing premature end of life. When VCS > VCSTH the C_D capacitor will begin to charge and the CD pin voltage will rise. As this occurs the duty cycle will begin to adjust, i.e. the HO on time will become gradually shorter and the LO on time will become gradually longer. The dead time will remain constant at all times. In this way the power to the output will be reduced while the frequency remains at f_{MIN}. As the CD voltage rises, the duty cycle will be further reduced. If VCS then drops below VCSTH then the duty cycle will be regulated at that point and thus the current will be maintained at this limit. If VCS remains above VCSTH then the voltage will continue to rise on C_D until it reaches VCDMAX, at which point the duty cycle reaches its minimum limit DC_{MIN} and the IRS2552D will enter FAULT mode, requiring V_{CC} to fall below UVLO- and then rise above UVLO+ in order to re-start.

Frequency, Current, and Dead Time Calculation

The running frequency of the IRS2552D is given by the following formula:

$$f_{MIN} = \frac{1}{2.09 \cdot C_T \cdot R_{MIN}}$$

where V_{MIN} = 5 V, i.e. When the ignition ramp is complete and R_{MAX} has no further effect on the oscillator.

The ignition frequency given by:

$$f_{MAX} = \frac{1}{2.09 \cdot C_T \cdot R_{MAX}}$$

and the dead time is calculated by:

$$t_{DT} = R_{DT} \cdot C_{DT} \cdot \ln(1.5)$$

$$t_{DT} = 0.405 \cdot R_{DT} \cdot C_{DT}$$

Maximum duty cycle

$$DC_{MAX} = 0.5 - (t_{DT} * f)$$

The ICR charging current during ignition mode and the ICD charging current are given by:

$$ICR_{IGN} = \frac{0.06}{R_{MIN}}$$

$$ICD = \frac{0.06}{R_{MIN}}$$

The ICR charging current and frequency during run mode are given by:

$$ICR_{RUN} = \frac{1.8}{R_{MIN}}$$

$$f_{CR} = \frac{0.36}{R_{MIN} \cdot C_{CR}}$$

Dimming Function

The IRS2552D supports burst mode dimming, meaning that the output drive to the lamps is pulsed on and off at a low frequency and the burst duty cycle is adjusted to control the average current and therefore the light output of the lamps. The IRS2552D contains a low frequency oscillator that generates a ramp waveform at the CR pin from 0 V to 5 V. The ramp frequency is dependent on the value of the external C_R capacitor. A DC dimming control voltage is fed into the DIM pin which is compared with the dimming ramp by means of an internal comparator, which generates the PWM signal that is used internally to switch the outputs on and off. Thus when the DIM voltage is at 5 V the outputs will be on all of the time and when it is at 0 V the outputs will be off all of the time. Alternatively a PWM dimming control signal from 0 V to 5 V can be fed directly into the DIM pin to allow external PWM control independent of the dimming ramp. During the off period the LO and HO outputs are both low.

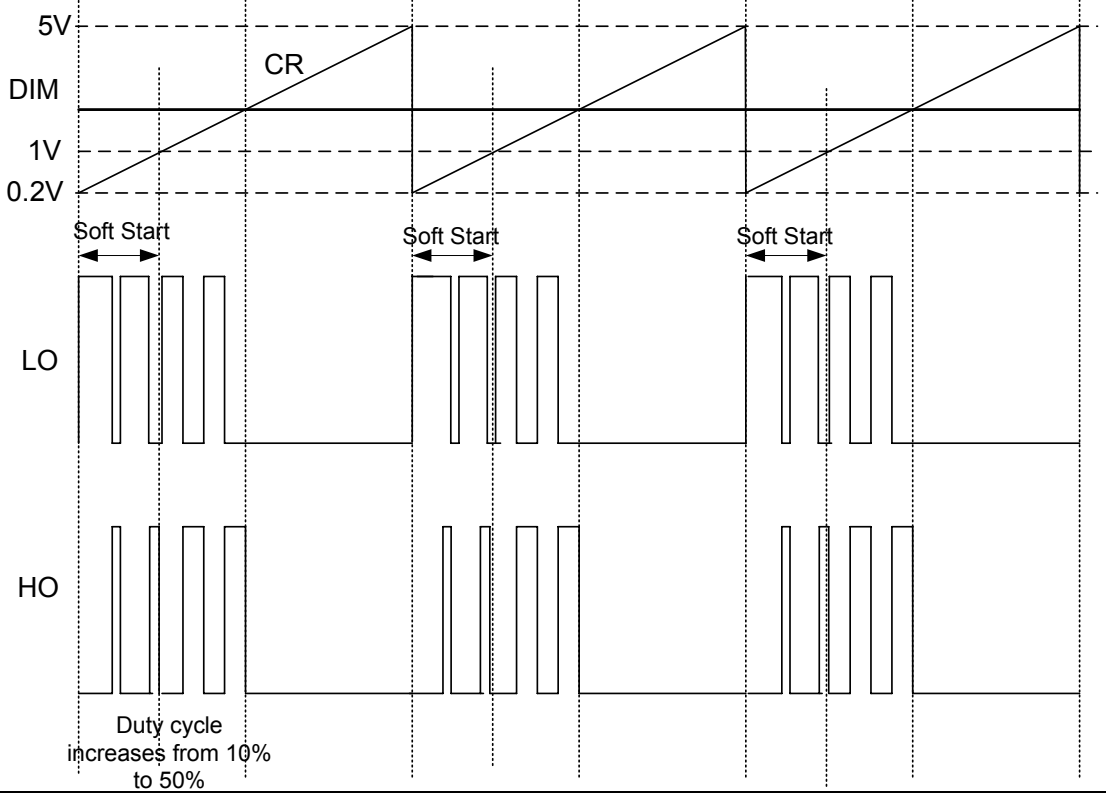


Figure 4: Dimming waveform

RUN MODE ICCRUN charges CR up to VCR+. CR oscillates at fCR (sawtooth) Half-bridge oscillates at FMIN. VDC reset to 0V			
	SOFT START	**ON**	**OFF**
	DC increases from DC min to DC max	DC=DCmax	DC=0
VDIM <VCRSS	**VCR**<VCRSS		**VCR**>VDIM
VCRSS <VDIM<VDIMSS	**VCR**<VCRSS	**VCR**<VDIM	**VCR**>VDIM
VDIM>VDIMSS		**VCR**<VDIM	**VCR**>VDIM

Soft start

In addition the IRS2552D includes a soft start function that operates at the start of each burst, during dimming operation when VDIM < $VDIM_{SS}$. The soft start will operate during the portion of the dimming ramp CR at the start of each burst from CR = 0 V to CR = VCR_{SS}. When VCR = 0 the duty cycle will be at minimum (DCMIN) and will linearly increase to 50% (minus the dead time) when VCR reaches VCR_{SS}. This function is enabled only in RUN mode and allows inrush currents to be eliminated during burst mode dimming, while always maintaining the frequency at F_{MIN}.

PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 5). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

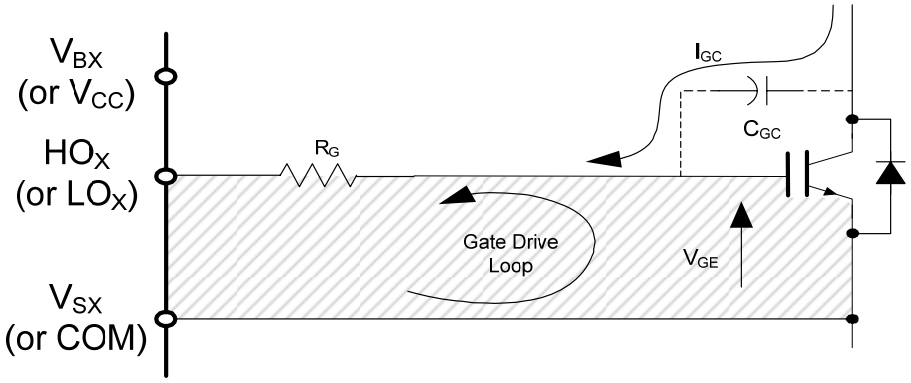


Figure 5: Antenna Loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and V_{SS} pins. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients as the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 6), and in some cases using a clamping diode between V_{SS} and V_S (see Figure 7). See DT04-4 at www.irf.com for more detailed information.

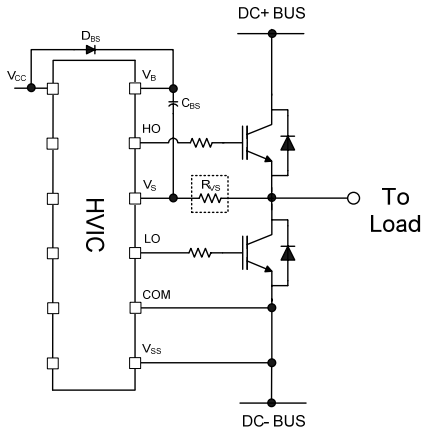


Figure 6: V_S resistor

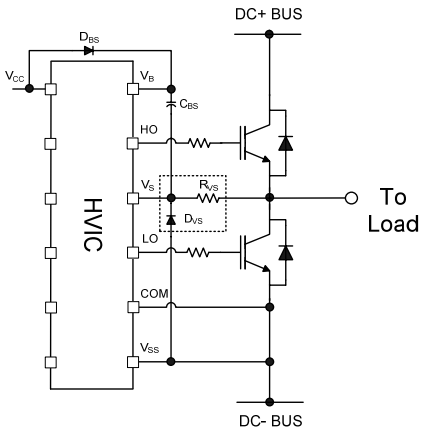


Figure 7: V_S clamping diode

Additional Documentation

Several technical documents related to the use of HVICs are available at www.irf.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Programmable parameter characteristics

Figure 7 to 12 provide the characteristics of the programmable parameters as a function of the value of the programming components.

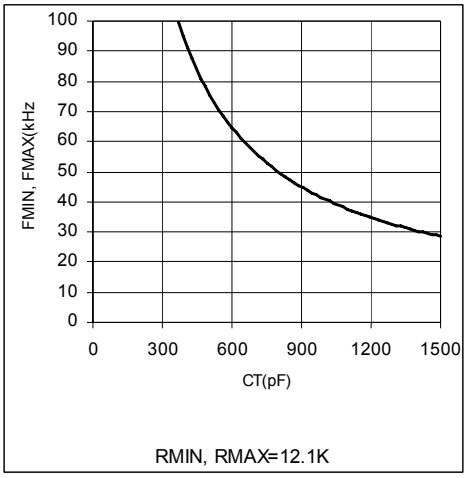


Figure 7: FMIN, FMAX vs. CT

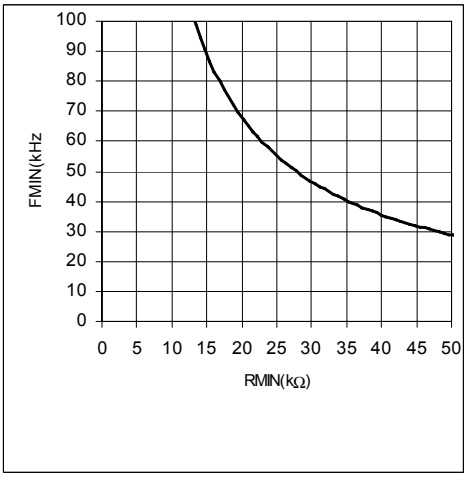


Figure 8: FMIN vs. RMIN

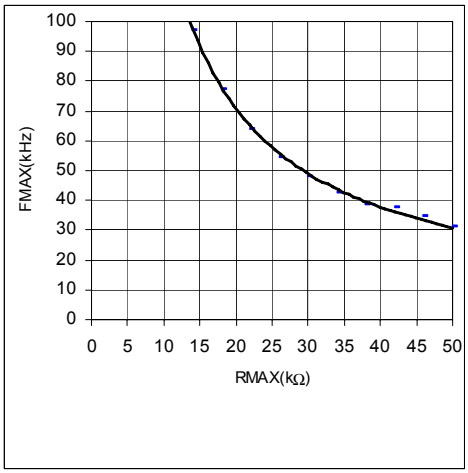


Figure 9: FMAX vs. RMAX

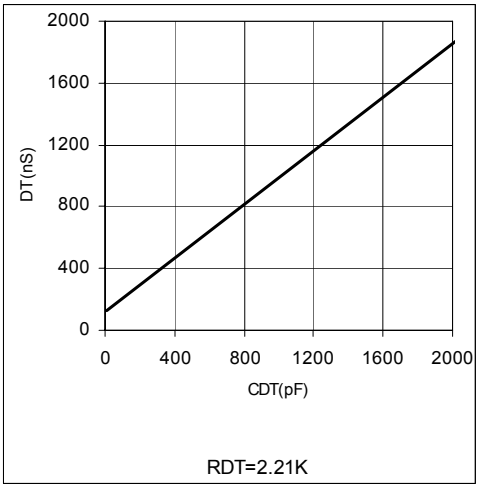


Figure 10: DT vs. CDT

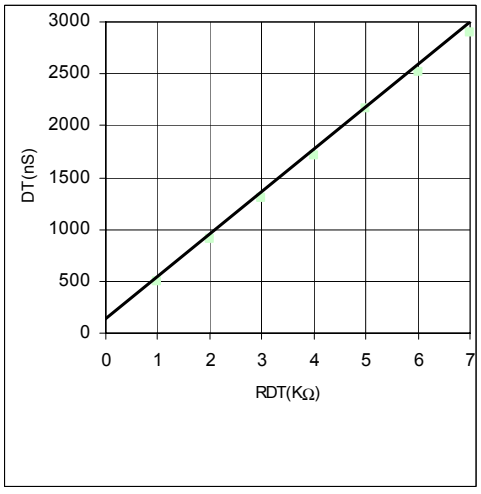


Figure 11: DT vs. RDT

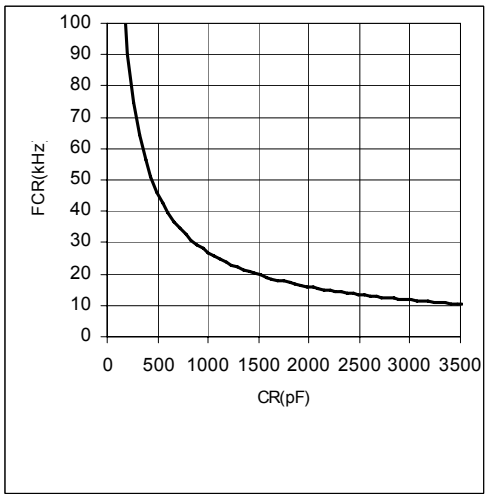


Figure 12: FCR vs. CR

Parameter characteristics

Figure 13 to 18 provide the characteristics of the main parameters as a function of VCC or the oscillator frequency

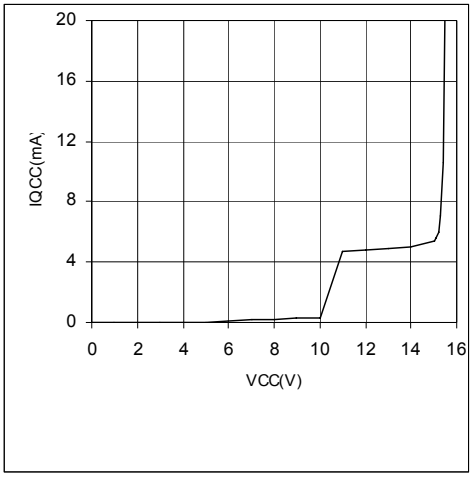


Figure 13: ICC vs. VCC

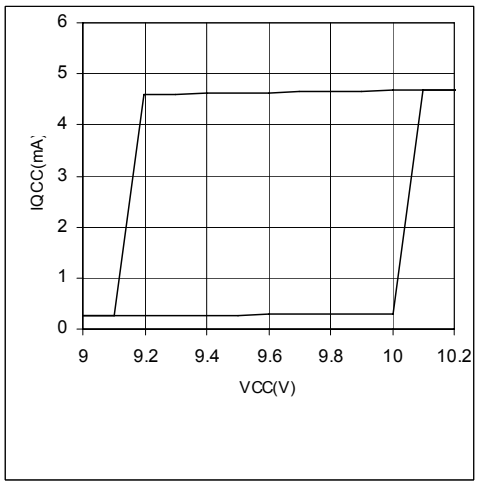


Figure 14: IQCC vs. VCC (VCC raising and falling

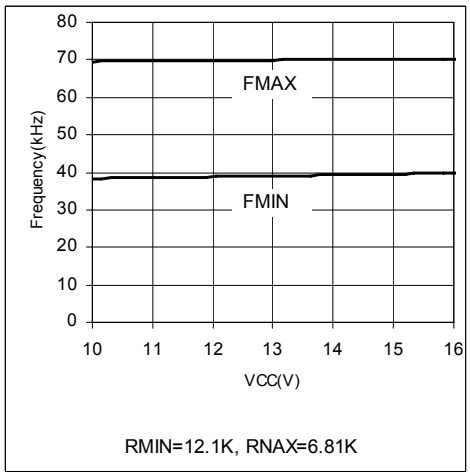


Figure15: FMIN, FMAX vs. VCC

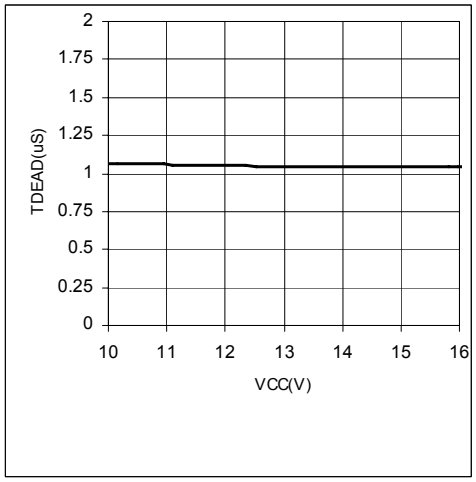


Figure 16: td vs. VCC

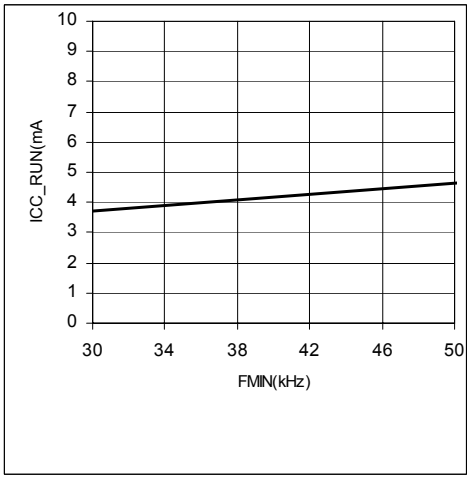


Figure 17: ICC RUN vs. FMIN

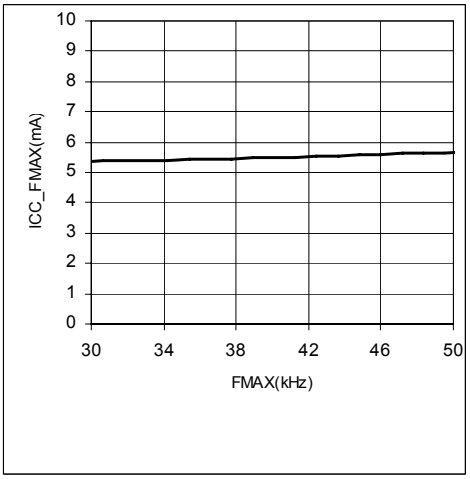


Figure 18: ICC FMAX vs. FMAX

Parameter Temperature Trends

Figures 38-58 provide the characteristics of the main parameters over temperature based on three temperatures (-40 ºC, 25 ºC, and 125 ºC) average testing.

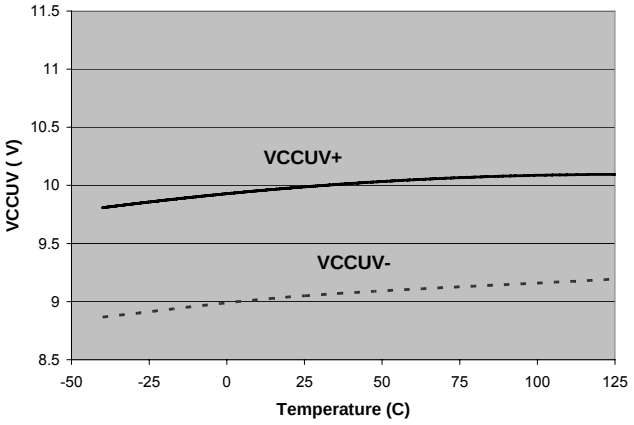


Figure 19: VCCUV vs. temperature

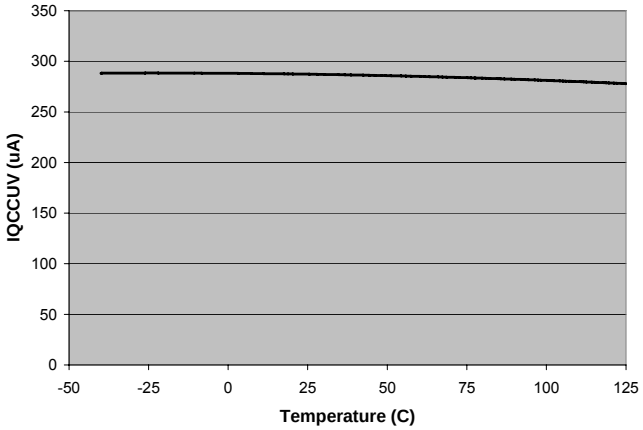


Figure 20: IQCCUV vs. temperature

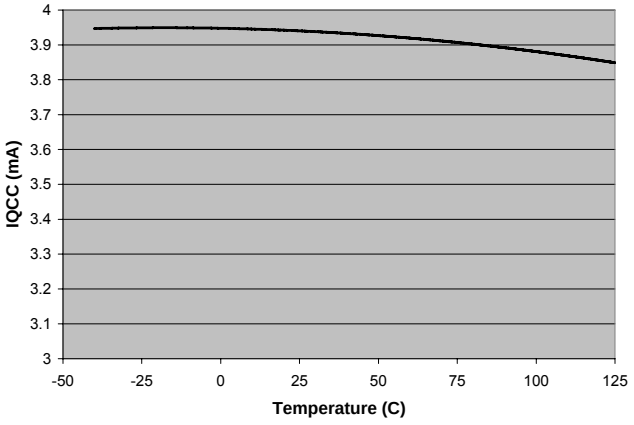


Figure 21: IQCC vs. temperature

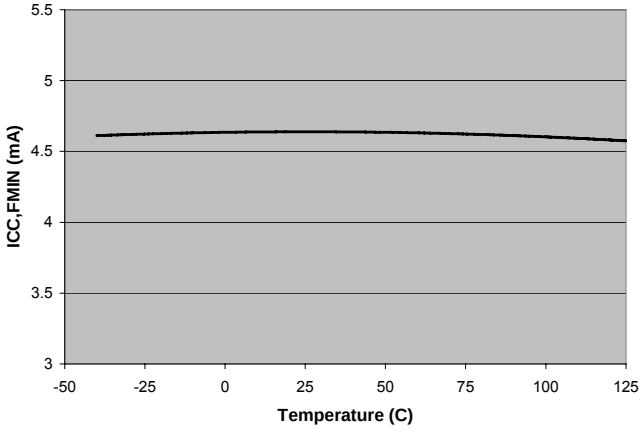


Figure 22: ICC,FMIN vs. temperature

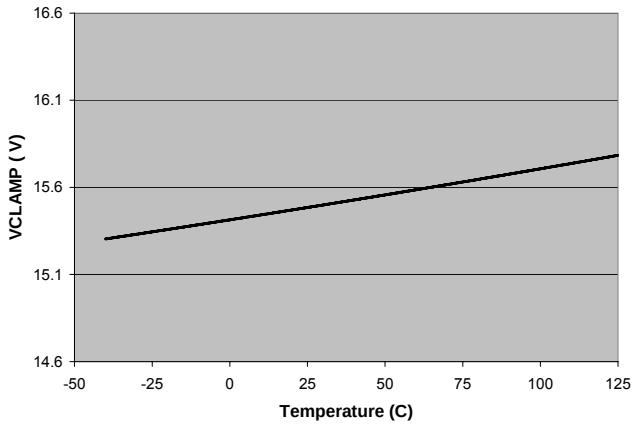


Figure 23: VCLAMP vs. temperature

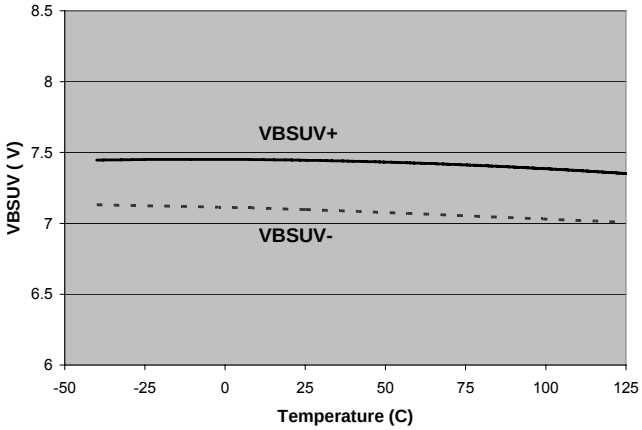


Figure 24: VBSUV vs. temperature

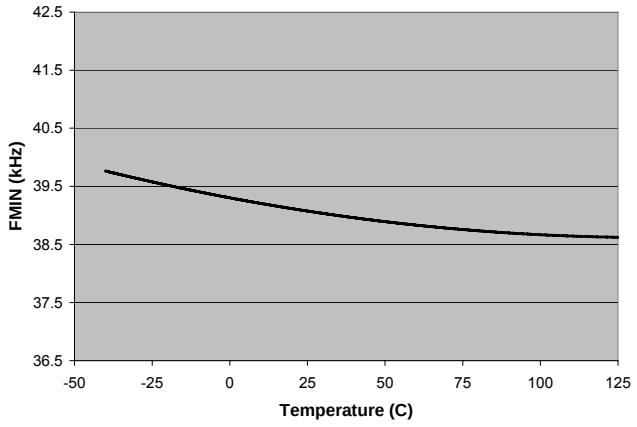


Figure 25: fMIN vs. temperature

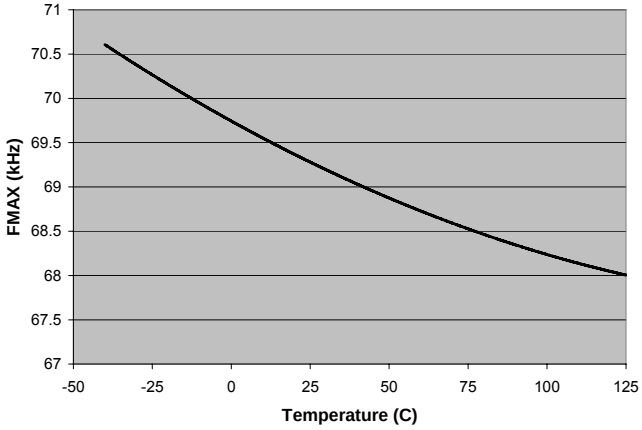


Figure 26: fMAX vs. temperature

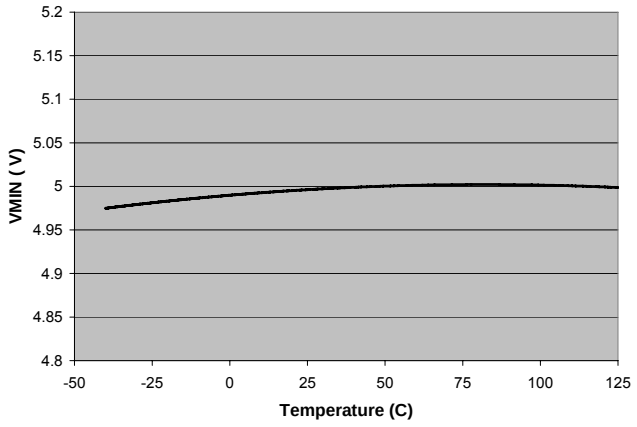


Figure 27: V_{MIN}vs. temperature

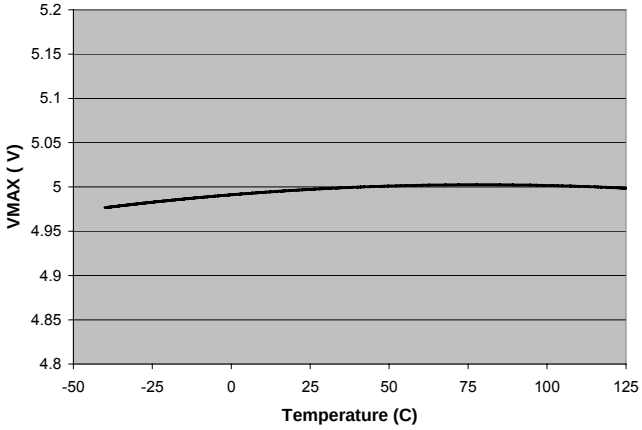


Figure 28: VMAX vs. temperature

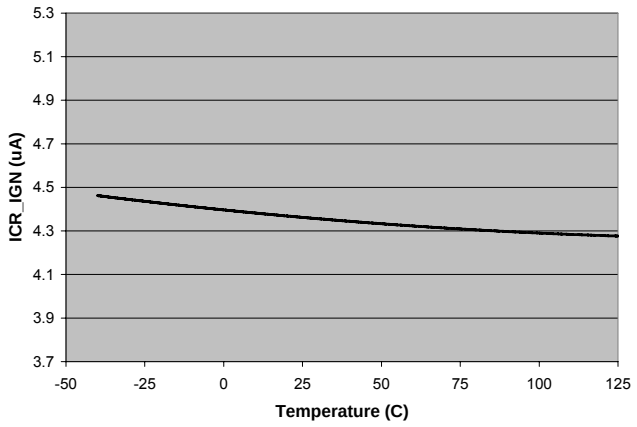


Figure 29: $I_{CR,IGN}$ vs. temperature

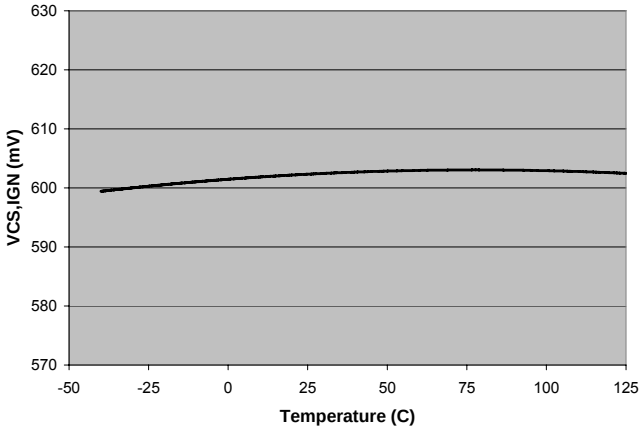


Figure 30: $V_{cs,ign}$ vs. temperature

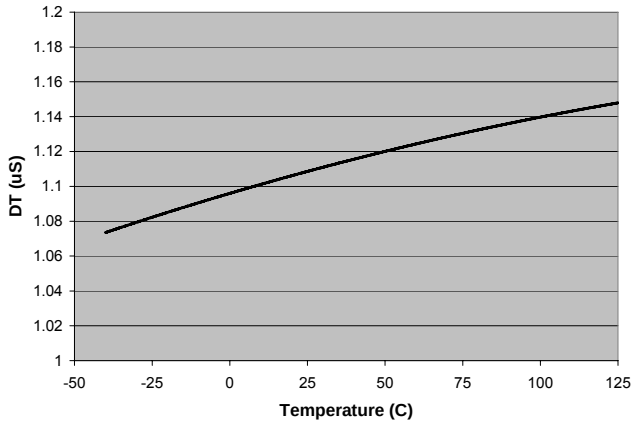


Figure 31: t_D vs. temperature

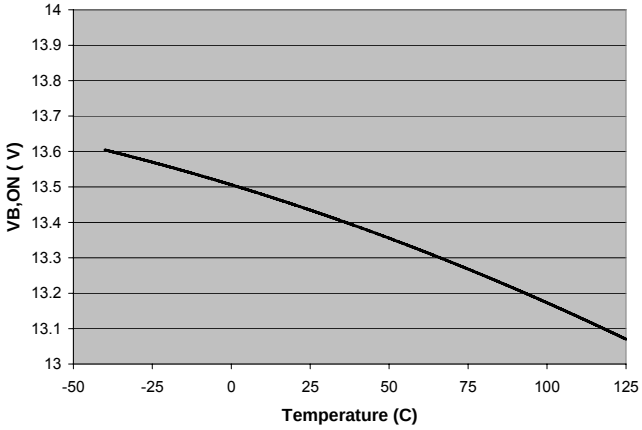


Figure 32: $V_{B,ON}$ vs. temperature

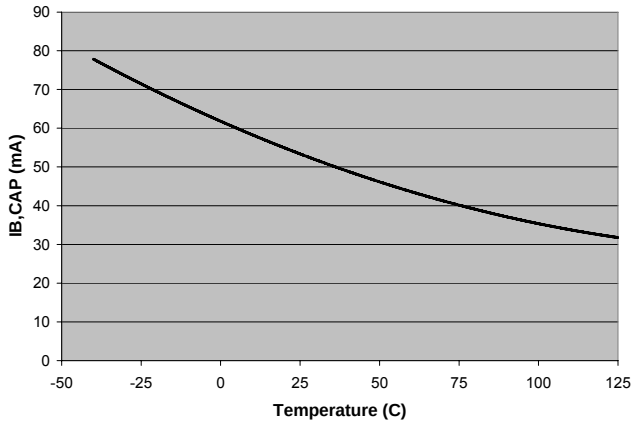


Figure 33: $I_{B,CAP}$ vs. temperature

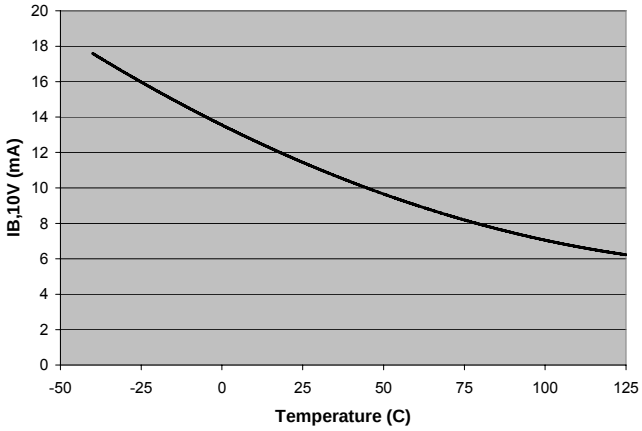


Figure 34: $I_{B,10V}$ vs. temperature

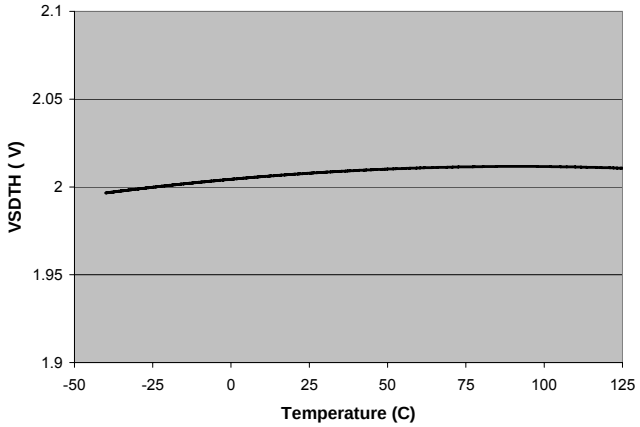


Figure 35: $V_{SD,TH}$ vs. temperature

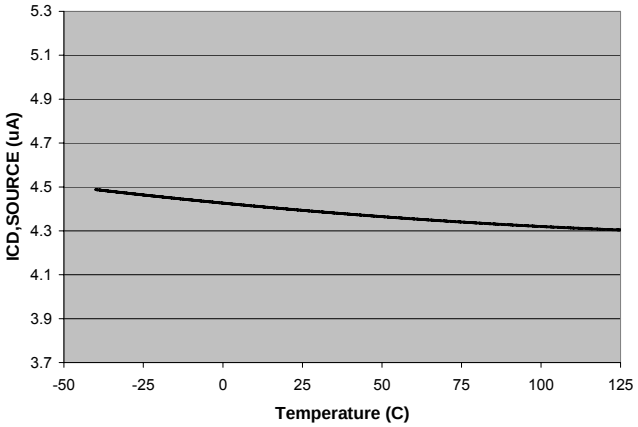


Figure 36: $V_{CD,SOURCE}$vs. temperature

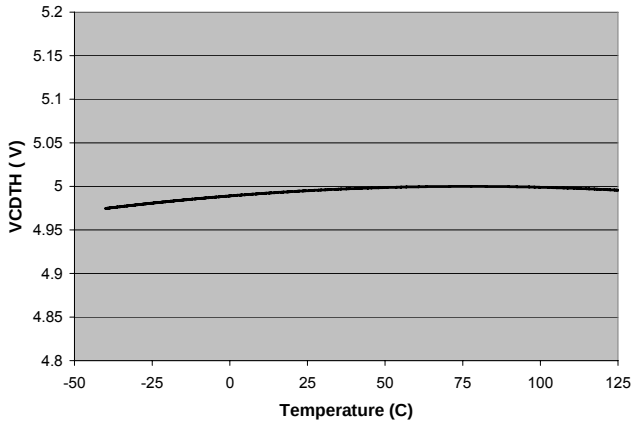


Figure 37: $V_{CD,TH}$ vs. temperature

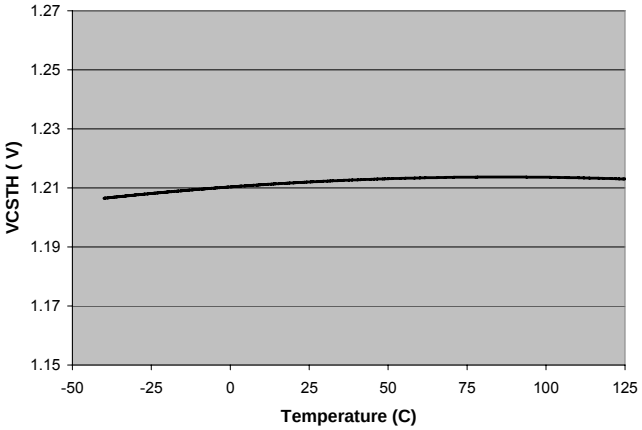


Figure 38: V_{CDSTH} vs. temperature

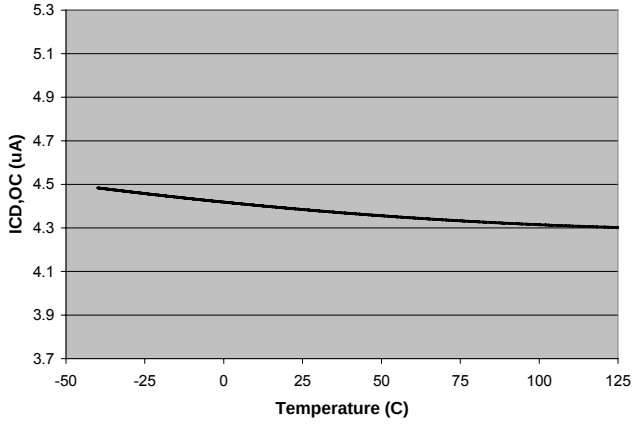


Figure 39: $I_{CD,OC}$ vs. temperature

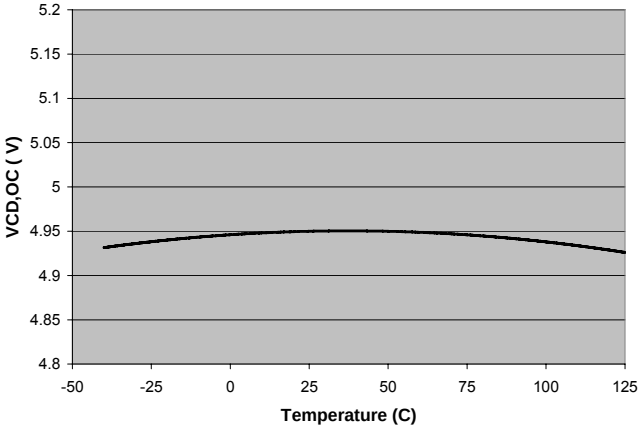


Figure 40: $V_{CD,OC}$ vs. temperature

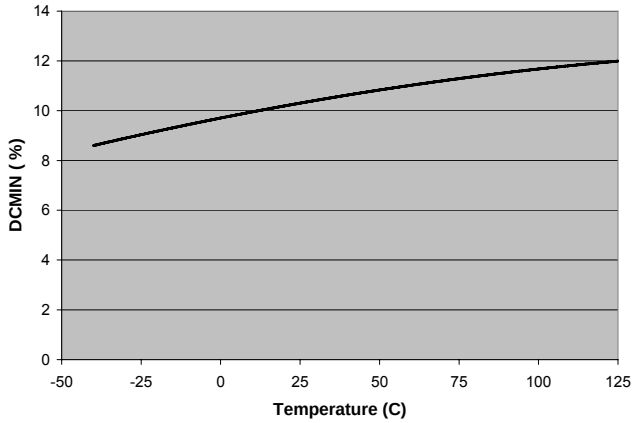


Figure 41: DC_{MIN} vs. temperature

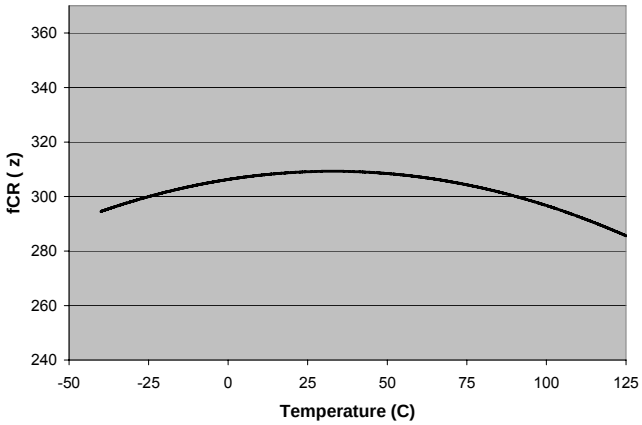


Figure 42: f_{CR} vs. temperature

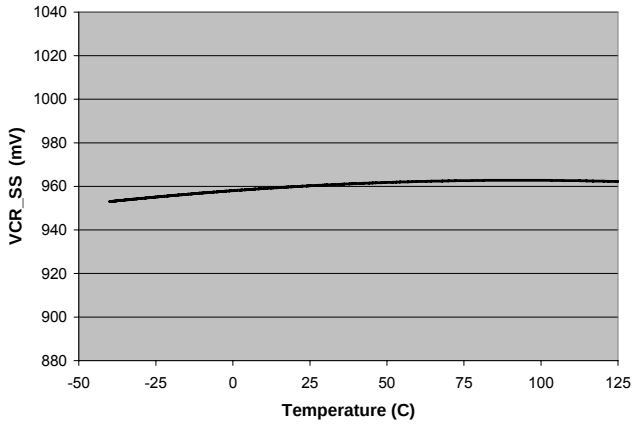


Figure 43: $V_{CR,SS}$ vs. temperature

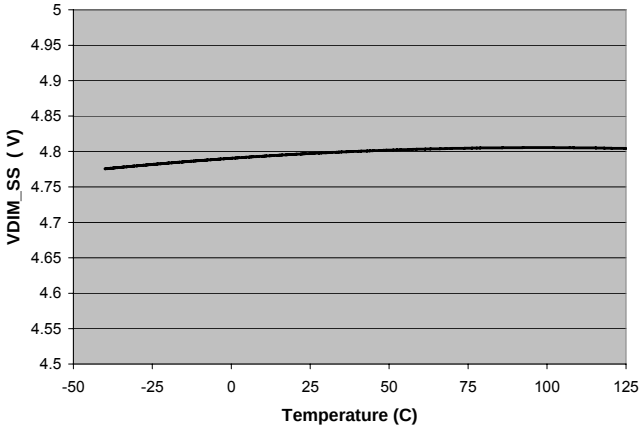


Figure 44: $V_{DIM,SS}$ vs. temperature

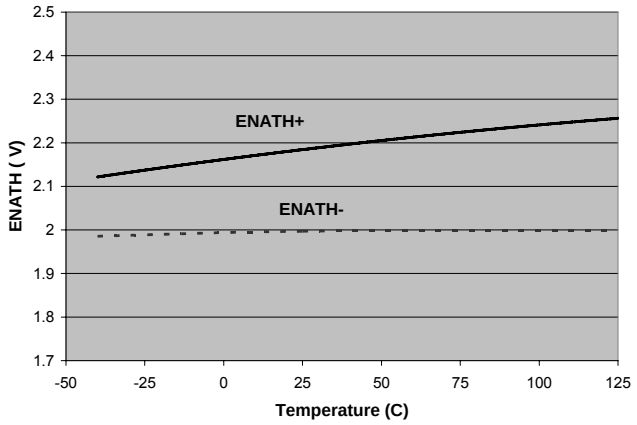


Figure 45: V_{ENA} vs. temperature

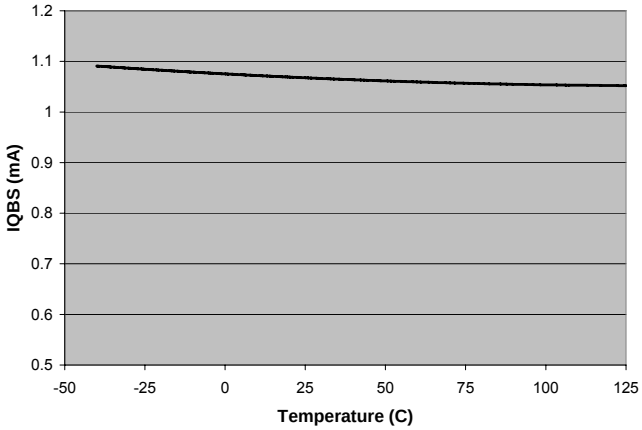
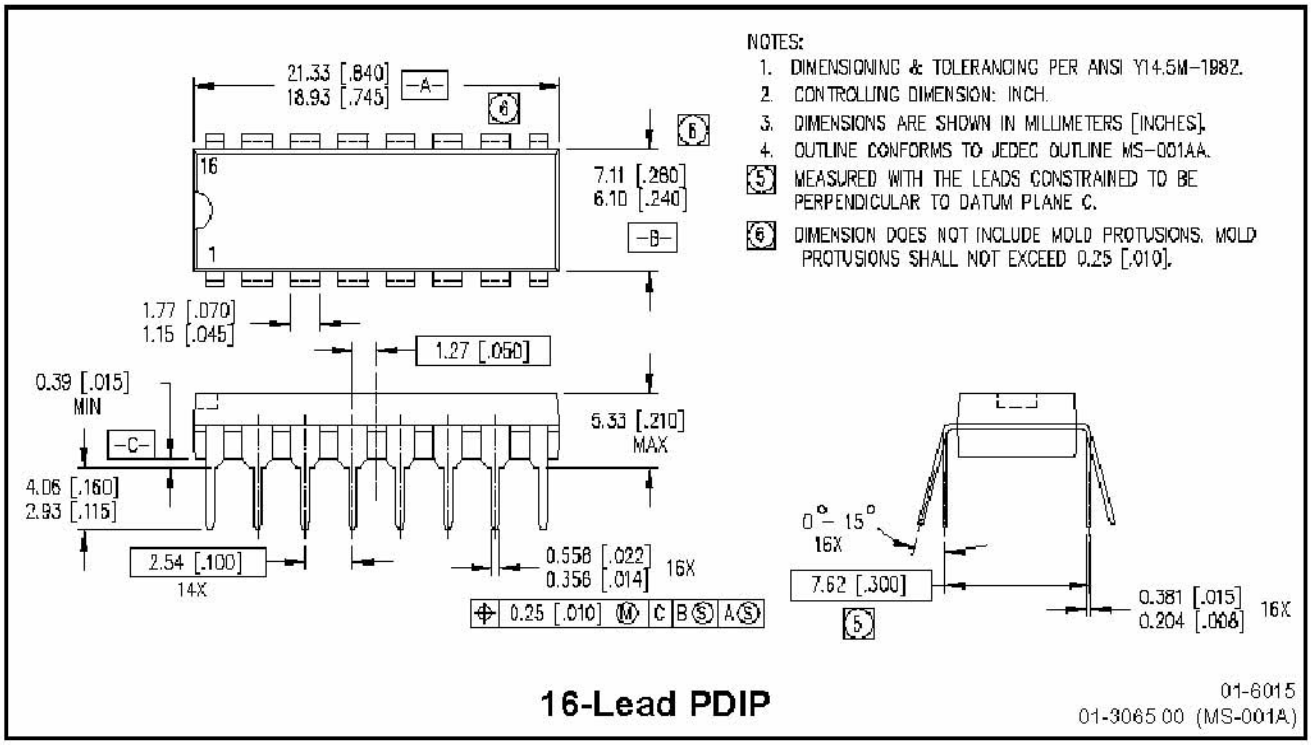
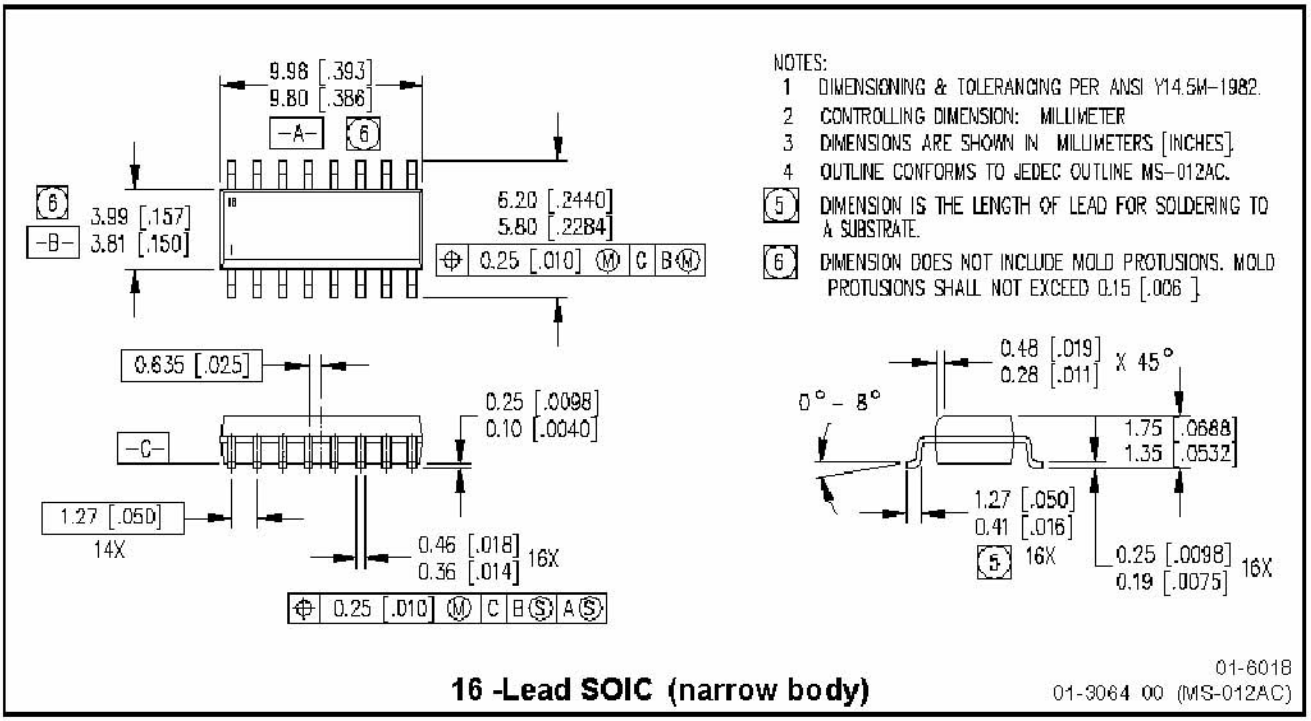


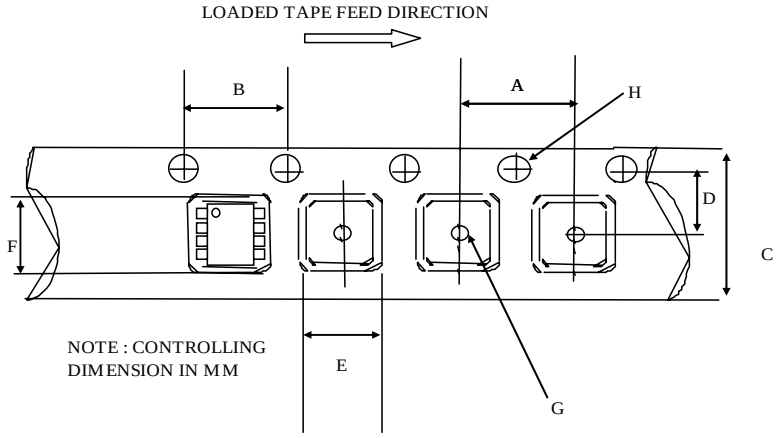
Figure 46: IBS vs. temperature

Package Details: PDIP16 and S016N



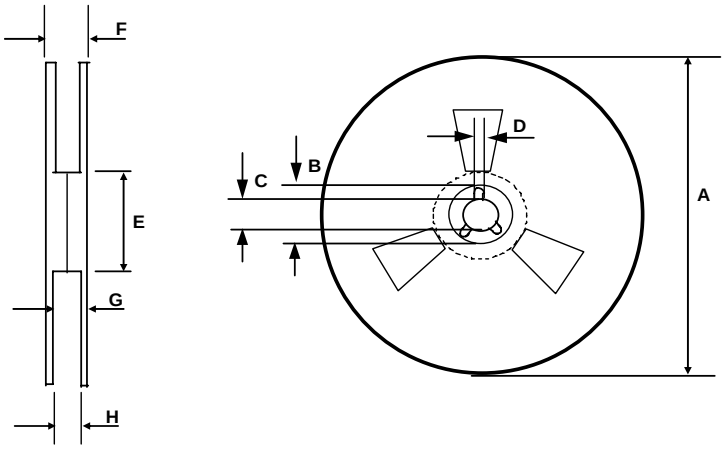


Package Details: SOIC16N, Tape and Reel



CARRIER TAPE DIMENSION FOR 16SOICN

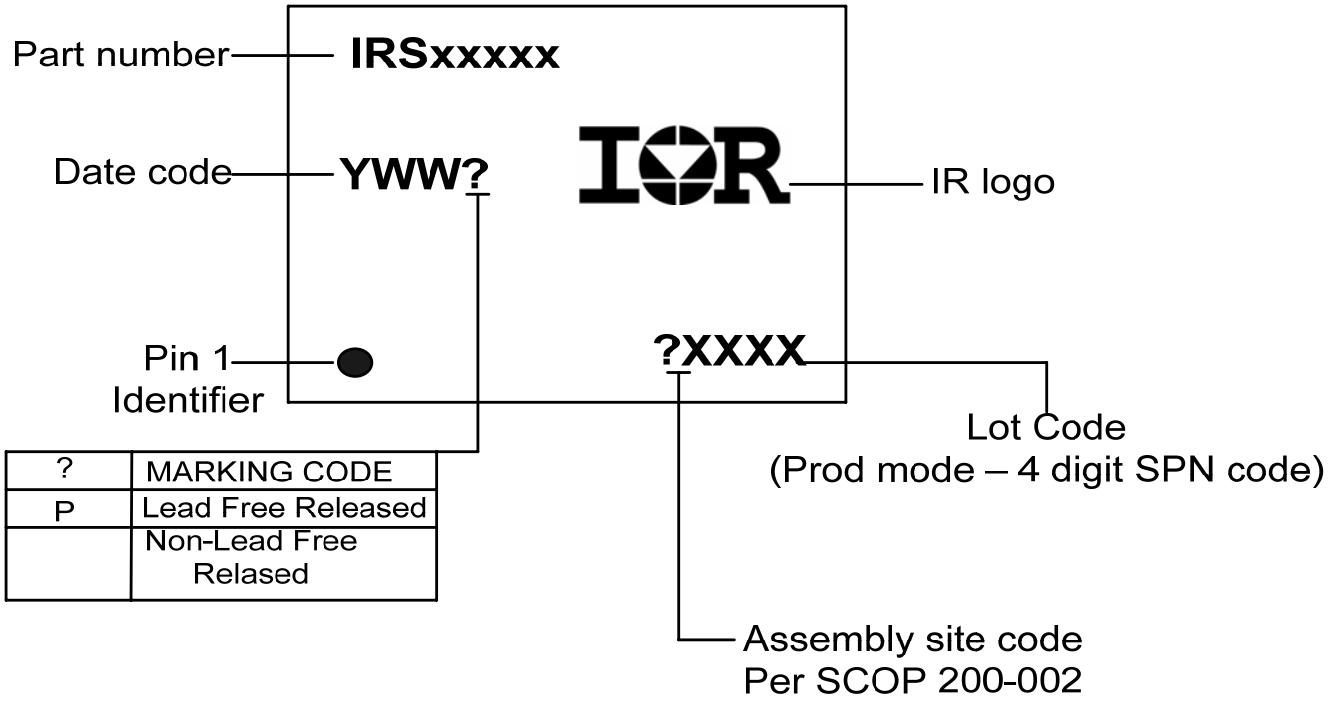
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2552D	PDIP16	Tube/Bulk	25	IRS2552DPBF
	SOIC16N	Tube/Bulk	45	IRS2552DSPBF
		Tape and Reel	2500	IRS2552DSTRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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Components Supply Platform

Authorized Distribution Brand :

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Welcome to visit www.ameya360.com

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