

SN74LVC1G125 Single Bus Buffer Gate With 3-State Output

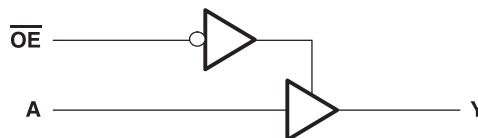
1 Features

- Available in the Ultra Small 0.64-mm² Package (DPW) With 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V_{CC}
- Max t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Cable Modem Termination System
- High-Speed Data Acquisition and Generation
- Military: Radar and Sonar
- Motor Control: High-Voltage
- Power Line Communication Modem
- SSD: Internal or External
- Video Broadcasting and Infrastructure: Scalable Platform
- Video Broadcasting: IP-Based Multi-Format Transcoder
- Video Communications System

4 Simplified Schematic



3 Description

This bus buffer gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G125 device is a single line driver with a 3-state output. The output is disabled when the output-enable (\overline{OE}) input is high.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The SN74LVC1G125 device is available in a variety of packages including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

Device Information⁽¹⁾

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
SN74LVC1G125	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
	SON (6)	1.45 mm × 1.00 mm
	DSBGA (5)	1.40 mm × 0.90 mm
	X2SON (4)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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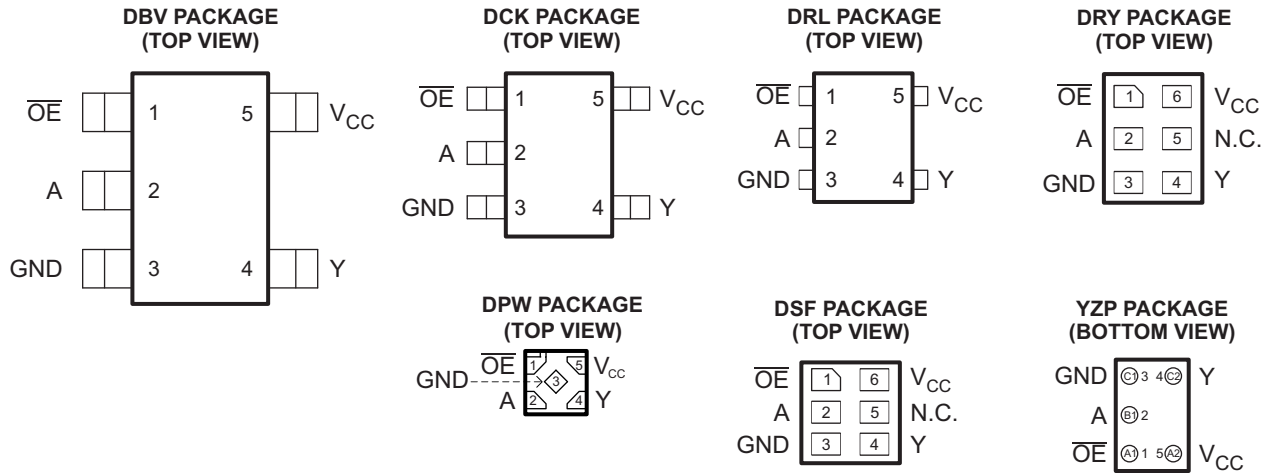
5 Revision History

Changes from Revision S (April 2014) to Revision T	Page
• Updated Device Information table.	1
• Removed PREVIEW status from DPW Pin Out drawing.	3

Changes from Revision R (April 2013) to Revision S	Page
• Added Applications.	1
• Added Pin Functions table.	3
• Updated Handling Ratings table.	4
• Added Thermal Information table.	5
• Added Typical Characteristics.	7
• Added Detailed Description section.	10
• Added Application and Implementation section.	11
• Added Power Supply Recommendations section.	12
• Added Layout section.	12

Changes from Revision Q (November 2012) to Revision R	Page
• Added Device Information table.	1
• Moved T_{stg} to Handling Ratings table.	4
• Added -40°C to 125°C Temperature range to Electrical Characteristics	6
• Added Switching Characteristics for -40°C to 125°C temperature range.	7

6 Pin Configuration and Functions



N.C. – No internal connection

See mechanical drawings for dimensions.

Pin Functions

NAME	PIN				DESCRIPTION
	DRL, DCK, DBV	DRY, DSF	DPW	YZP	
\overline{OE}	1	1	1	A1	Input
A	2	2	2	B1	Input
GND	3	3	3	C1	Ground
Y	4	4	4	C2	Output
V _{CC}	5	6	5	A2	Power pin
NC	–	5	–	–	Not connected

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating* table.

7.2 Handling Ratings

		MIN	MAX	UNIT	
T_{stg}	Storage temperature range	-65	150	°C	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V		–4	mA
		V _{CC} = 2.3 V		–8	
		V _{CC} = 3 V		–16	
				–24	
		V _{CC} = 4.5 V		–32	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
				24	
		V _{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	
T _A	Operating free-air temperature	–40	125	°C	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G125						UNIT	
	DBV	DCK	DRL	DRY	YZP	DPW		
	5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	229	278	243	439	130	340	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	164	93	78	277	54	215	
R _{θJB}	Junction-to-board thermal resistance	62	65	78	271	51	294	
Ψ _{JT}	Junction-to-top characterization parameter	44	2	10	84	1	41	
Ψ _{JB}	Junction-to-board characterization parameter	62	64	77	271	50	294	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	–	–	–	–	–	250	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	–40 °C to 85 °C			–40 °C to 125 °C			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1			V
	I _{OH} = –4 mA	1.65 V	1.2			1.2			
	I _{OH} = –8 mA	2.3 V	1.9			1.9			
	I _{OH} = –16 mA	3 V	2.4			2.4			
	I _{OH} = –24 mA		2.3			2.3			
	I _{OH} = –32 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V	0.1			0.1			V
	I _{OL} = 4 mA	1.65 V	0.45			0.45			
	I _{OL} = 8 mA	2.3 V	0.3			0.3			
	I _{OL} = 16 mA	3 V	0.4			0.4			
	I _{OL} = 24 mA		0.55			0.55			
	I _{OL} = 32 mA	4.5 V	0.55			0.55			
I _I	A or \overline{OE} inputs	V _I = 5.5 V or GND	0 to 5.5 V			±5			μA
I _{off}	V _I or V _O = 5.5 V	0	±10			±10			μA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V	10			10			μA
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V	10			10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500			500			μA
C _I	V _I = V _{CC} or GND	3.3 V	4			4			pF

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

7.6 Switching Characteristics, C_L = 15 pF

 over recommended operating free-air temperature range of –40°C to 85°C, C_L = 15 pF (unless otherwise noted)

 (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.9	6.9	0.7	4.6	0.6	3.7	0.5	3.4	ns

7.7 Switching Characteristics, –40°C to 85°C

 over recommended operating free-air temperature range –40°C to 85°C, C_L = 30 pF or 50 pF (unless otherwise noted)

 (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2.8	9	1.2	5.5	1	4.5	1	4	ns
t _{en}	\overline{OE}	Y	3.3	10.1	1.5	6.6	1	5.3	1	5	ns
t _{dis}	\overline{OE}	Y	1.3	9.2	1	5	1	5	1	4.2	ns

7.8 Switching Characteristics, –40°C to 125°C

over recommended operating free-air temperature range –40°C to 125°C, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

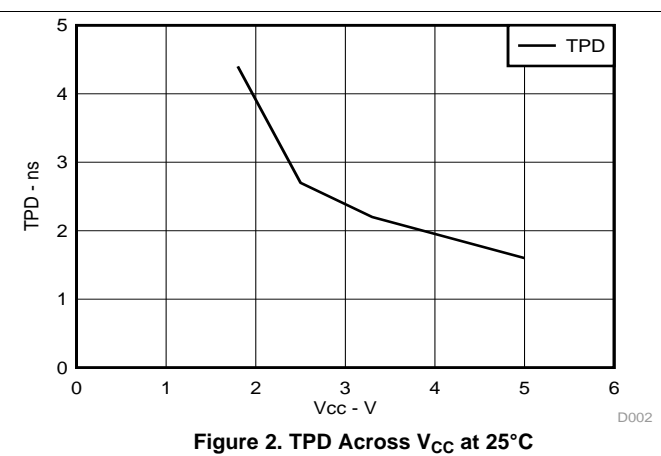
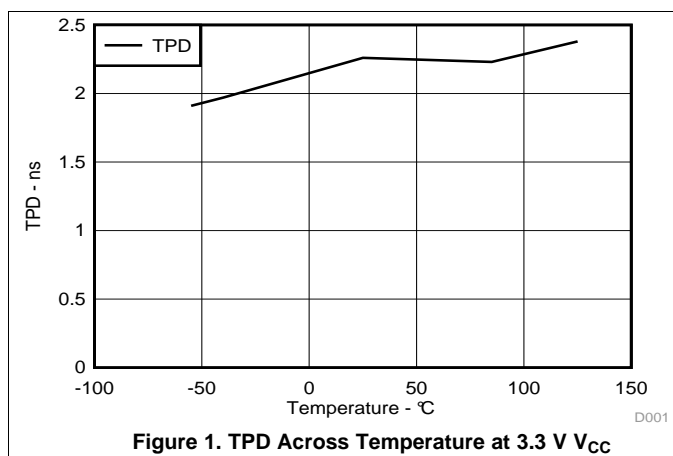
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2.8	9.3	1.2	5.8	1	4.7	1	4.2	ns
t _{en}	\overline{OE}	Y	3.3	10.4	1.5	6.9	1	5.6	1	5.2	ns
t _{dis}	\overline{OE}	Y	1.3	9.3	1	5.2	1	5.2	1	4.4	ns

7.9 Operating Characteristics

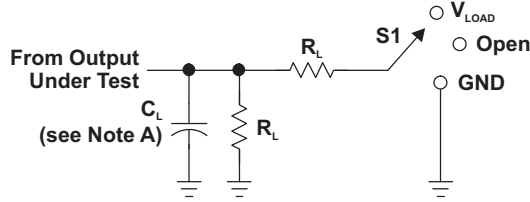
T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
				TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	18	18	19	21	pF
		Outputs disabled		2	2	2	4	

7.10 Typical Characteristics



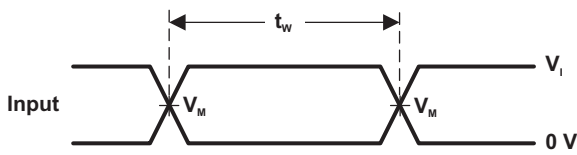
8 Parameter Measurement Information



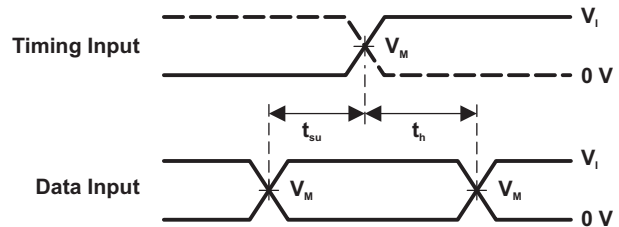
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

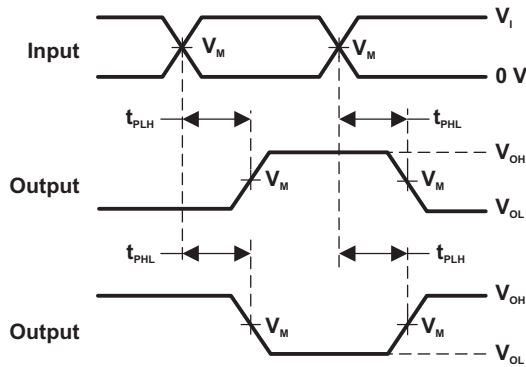
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_i	t_i/t_r					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



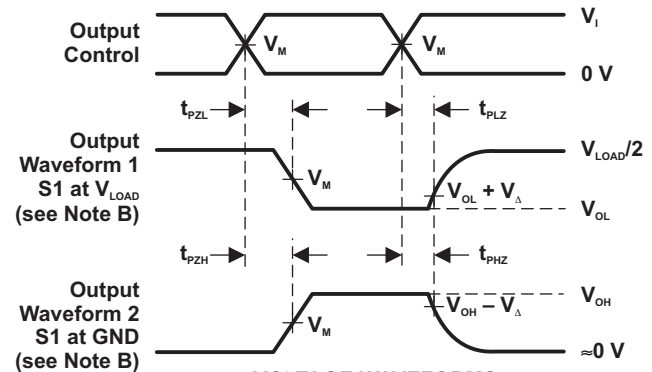
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

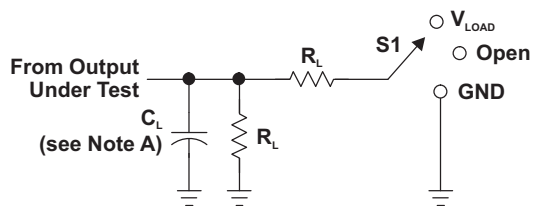


VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

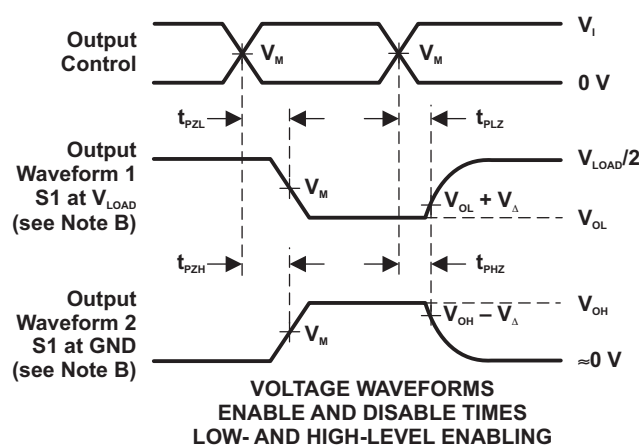
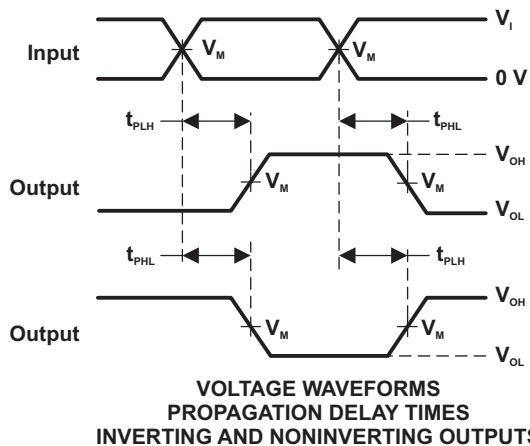
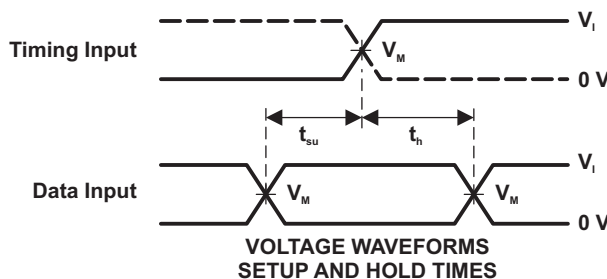
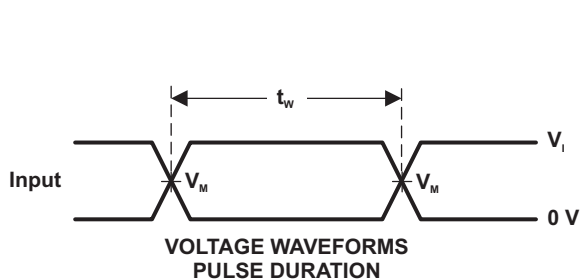
Parameter Measurement Information (continued)



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_f/t_r					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{on} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

9 Detailed Description

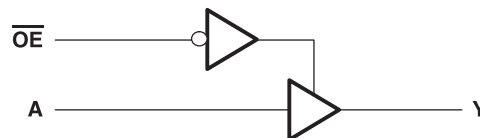
9.1 Overview

The SN74LVC1G125 device contains one buffer gate device with output enable control and performs the Boolean function $Y = A$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

9.2 Functional Block Diagram



9.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 5.5 V
- Allows down voltage translation
- Inputs accept voltages to 5.5 V
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V

9.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

10 Application and Implementation

10.1 Application Information

The SN74LVC1G125 device is a high drive CMOS device that can be used as an output enabled buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC} .

10.2 Typical Application

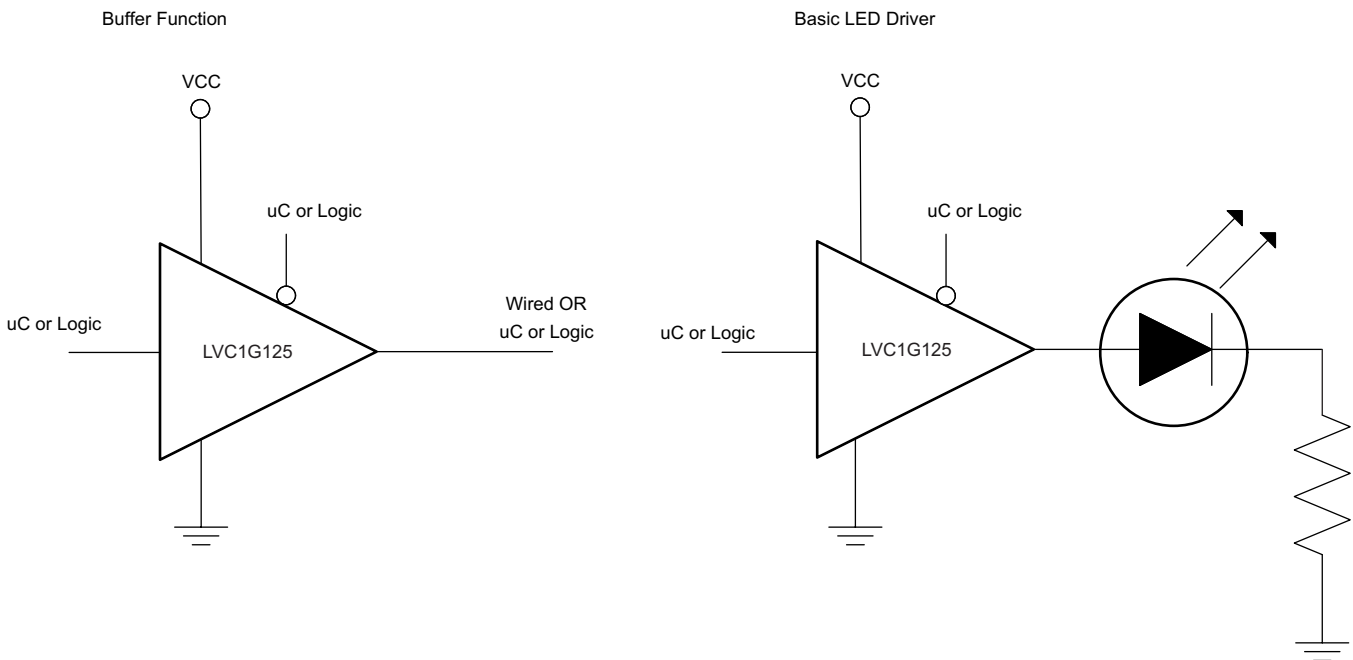


Figure 5. Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the [Recommended Operating Conditions](#) table at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves

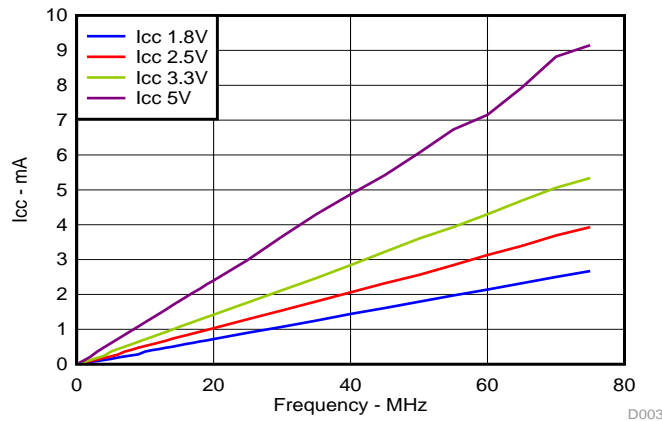


Figure 6. I_{CC} vs Frequency

11 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1- μ F capacitor is recommended and if there are multiple VCC pins then a 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 7](#) shows the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient.

12.2 Layout Example

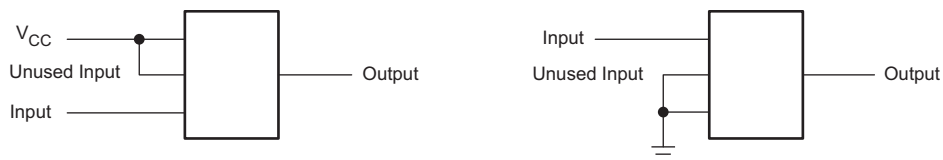


Figure 7. Package Layout

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

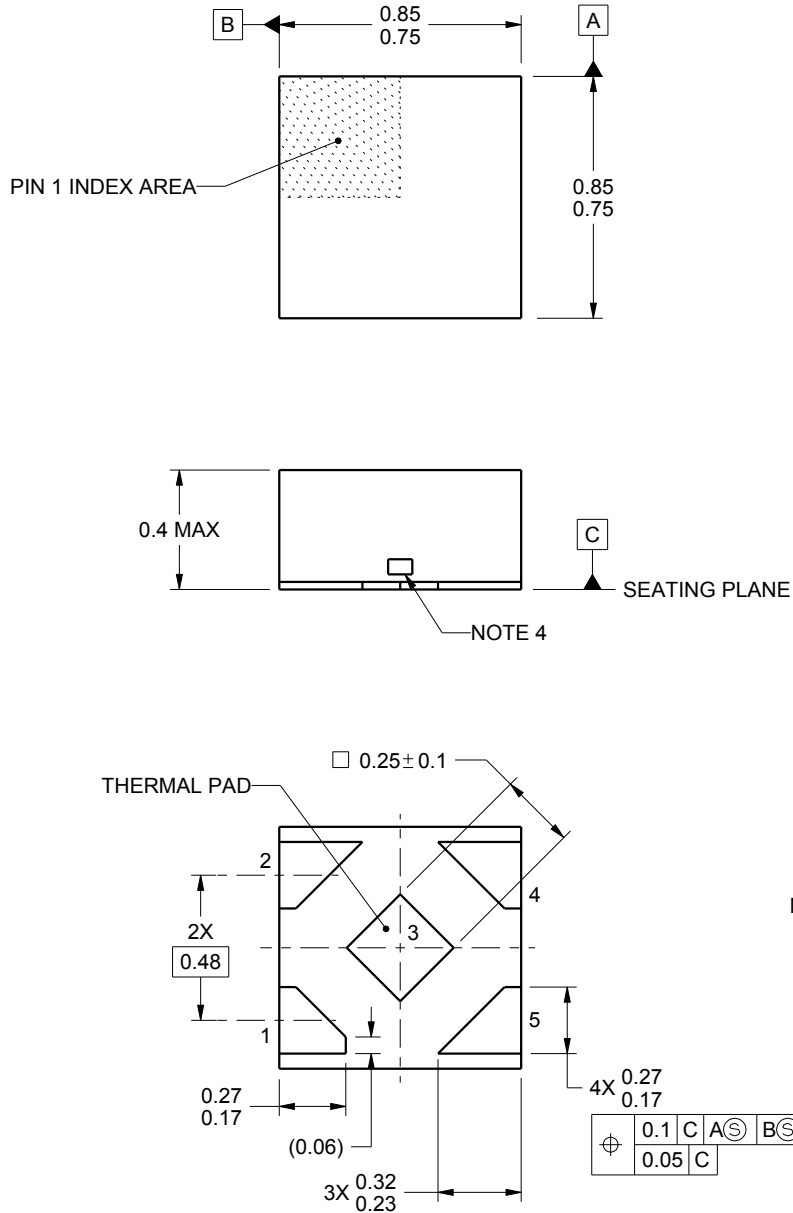
13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

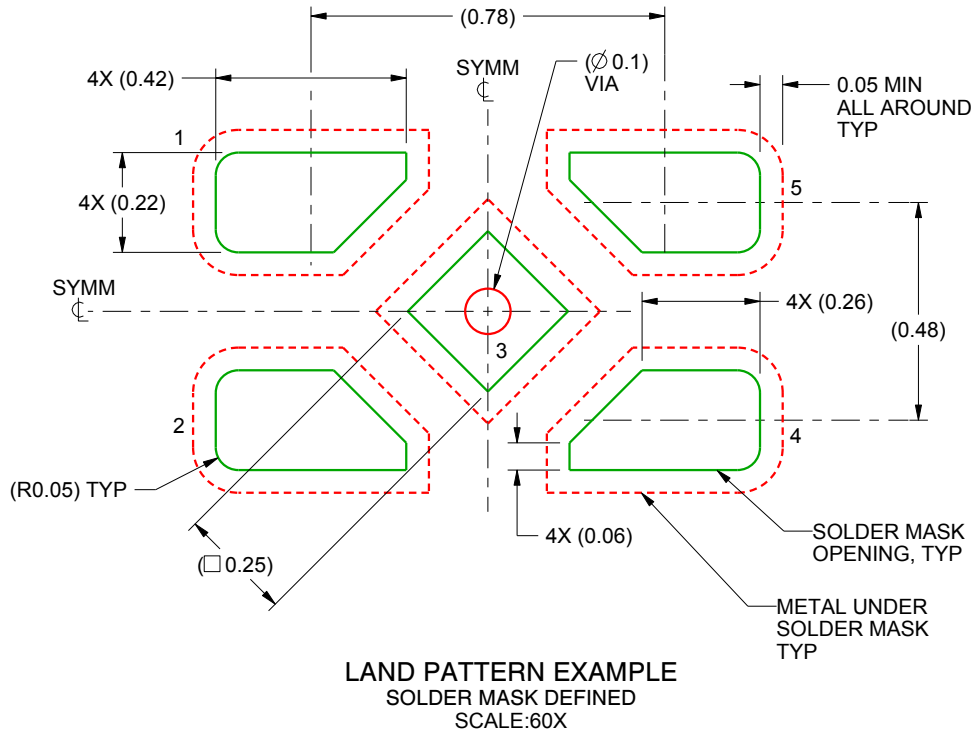
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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NOTES:

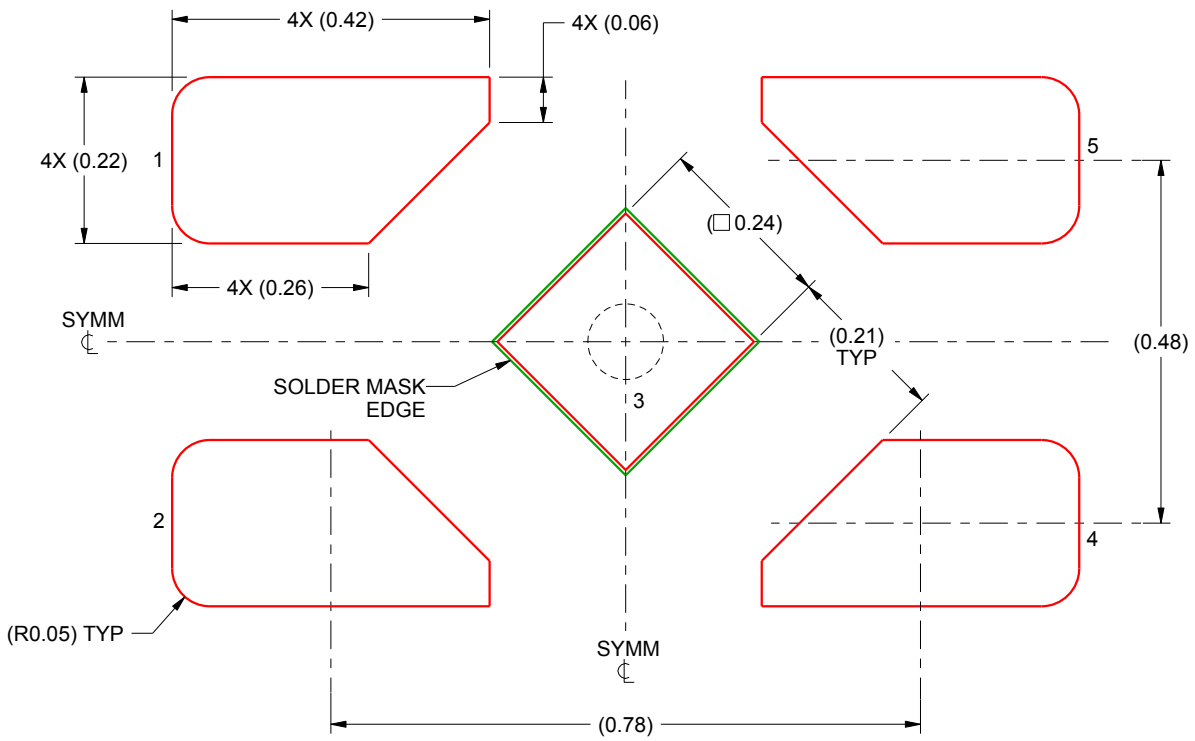
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.



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NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sluea271).



SOLDER PASTE EXAMPLE
 BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
 92% PRINTED SOLDER COVERAGE BY AREA
 SCALE:100X




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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC1G125DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C252 ~ C255 ~ C25F ~ C25K ~ C25R ~ C25T)	Samples
74LVC1G125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C252 ~ C255 ~ C25F ~ C25K ~ C25R ~ C25T)	Samples
74LVC1G125DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255 ~ C25F ~ C25K ~ C25R)	Samples
74LVC1G125DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
74LVC1G125DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
74LVC1G125DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
74LVC1G125DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
74LVC1G125DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM7 ~ CMR)	Samples
SN74LVC1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C252 ~ C255 ~ C25F ~ C25K ~ C25R ~ C25T)	Samples
SN74LVC1G125DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C255 ~ C25F ~ C25K ~ C25R)	Samples
SN74LVC1G125DCKJ	ACTIVE	SC70	DCK	5	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM5	Samples
SN74LVC1G125DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
SN74LVC1G125DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
SN74LVC1G125DPWR	ACTIVE	X2SON	DPW	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4	Samples
SN74LVC1G125DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CM7 ~ CMR)	Samples
SN74LVC1G125DRY2	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	-40 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G125DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CM	
SN74LVC1G125DSF2	PREVIEW	SON	DSF	6	5000	TBD	Call TI	Call TI	-40 to 85		
SN74LVC1G125DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CM	
SN74LVC1G125YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CM2 ~ CM7 ~ CMN)	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G125 :

- Automotive: [SN74LVC1G125-Q1](#)
- Enhanced Product: [SN74LVC1G125-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G125DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G125DCKJ	SC70	DCK	5	10000	330.0	8.4	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G125DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G125DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G125DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G125DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G125DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G125DPWR	X2SON	DPW	4	3000	180.0	8.4	0.91	0.91	0.5	4.0	8.0	Q3
SN74LVC1G125DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G125DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G125DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G125DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G125YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G125DCKJ	SC70	DCK	5	10000	338.0	343.0	30.0
SN74LVC1G125DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G125DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G125DPWR	X2SON	DPW	4	3000	205.0	200.0	33.0
SN74LVC1G125DRLR	SOT	DRL	5	4000	184.0	184.0	19.0
SN74LVC1G125DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G125DRYR	SON	DRY	6	5000	203.0	203.0	35.0
SN74LVC1G125DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G125YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

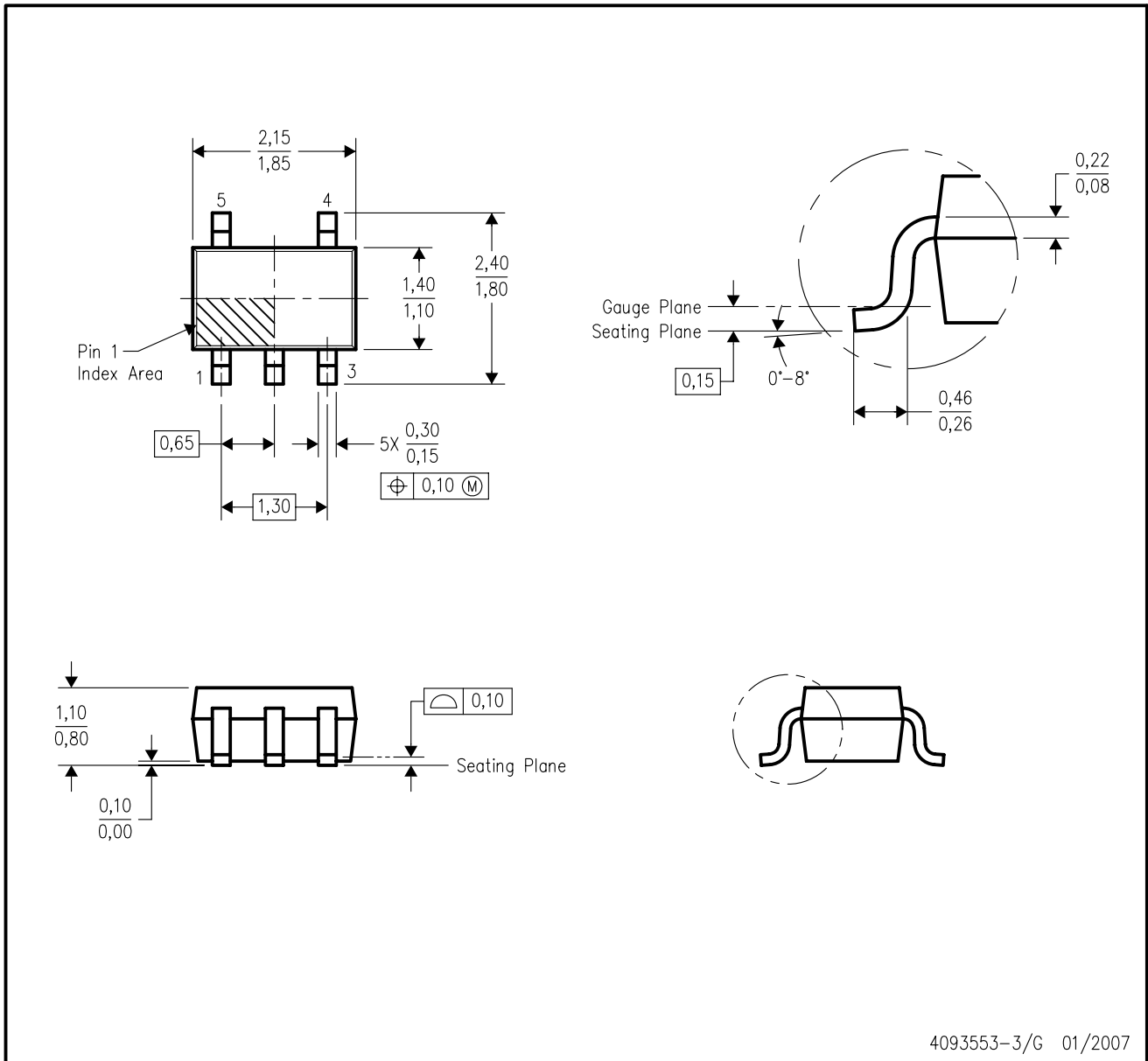


4209593-3/C 08/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



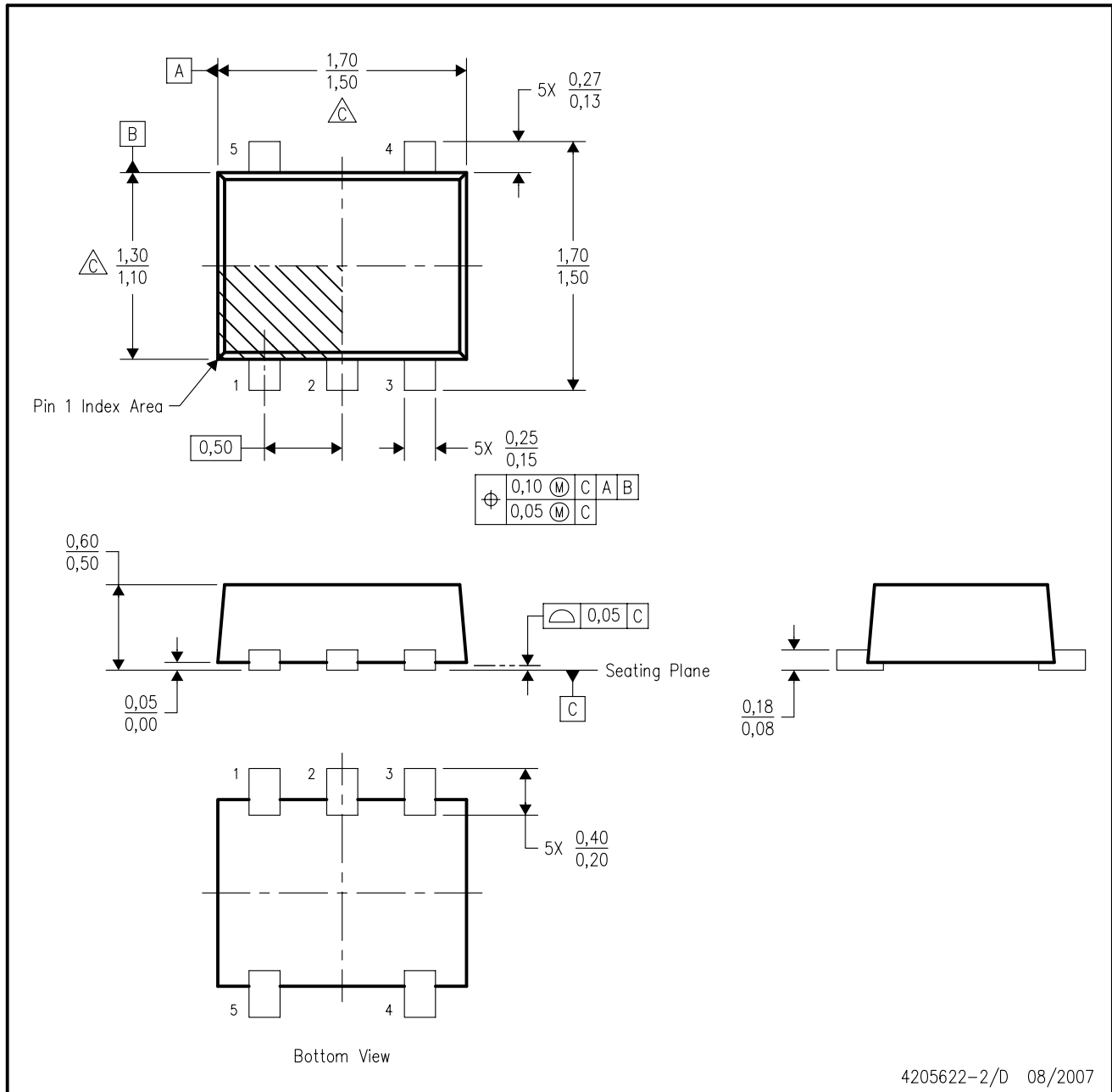
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

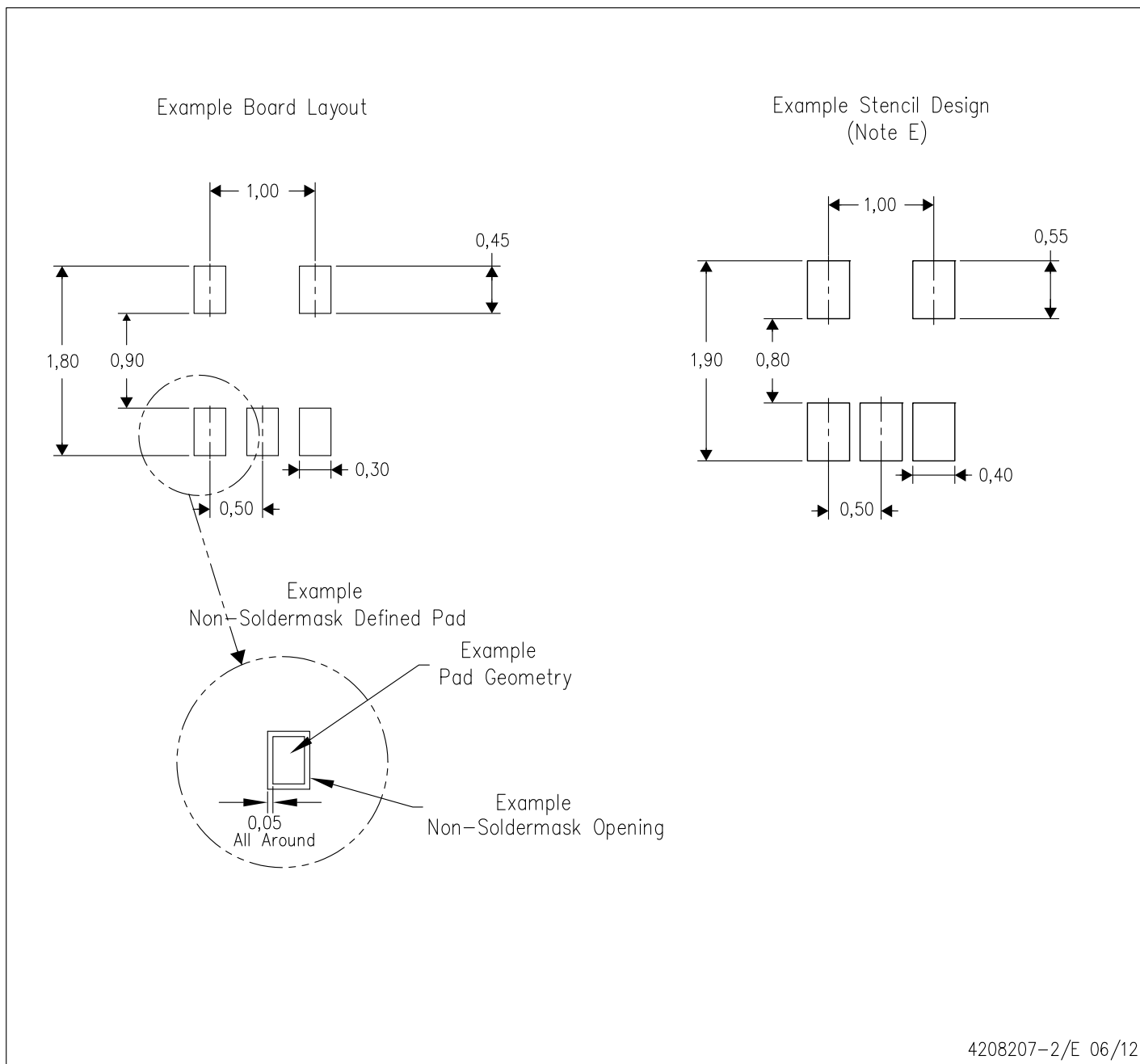
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



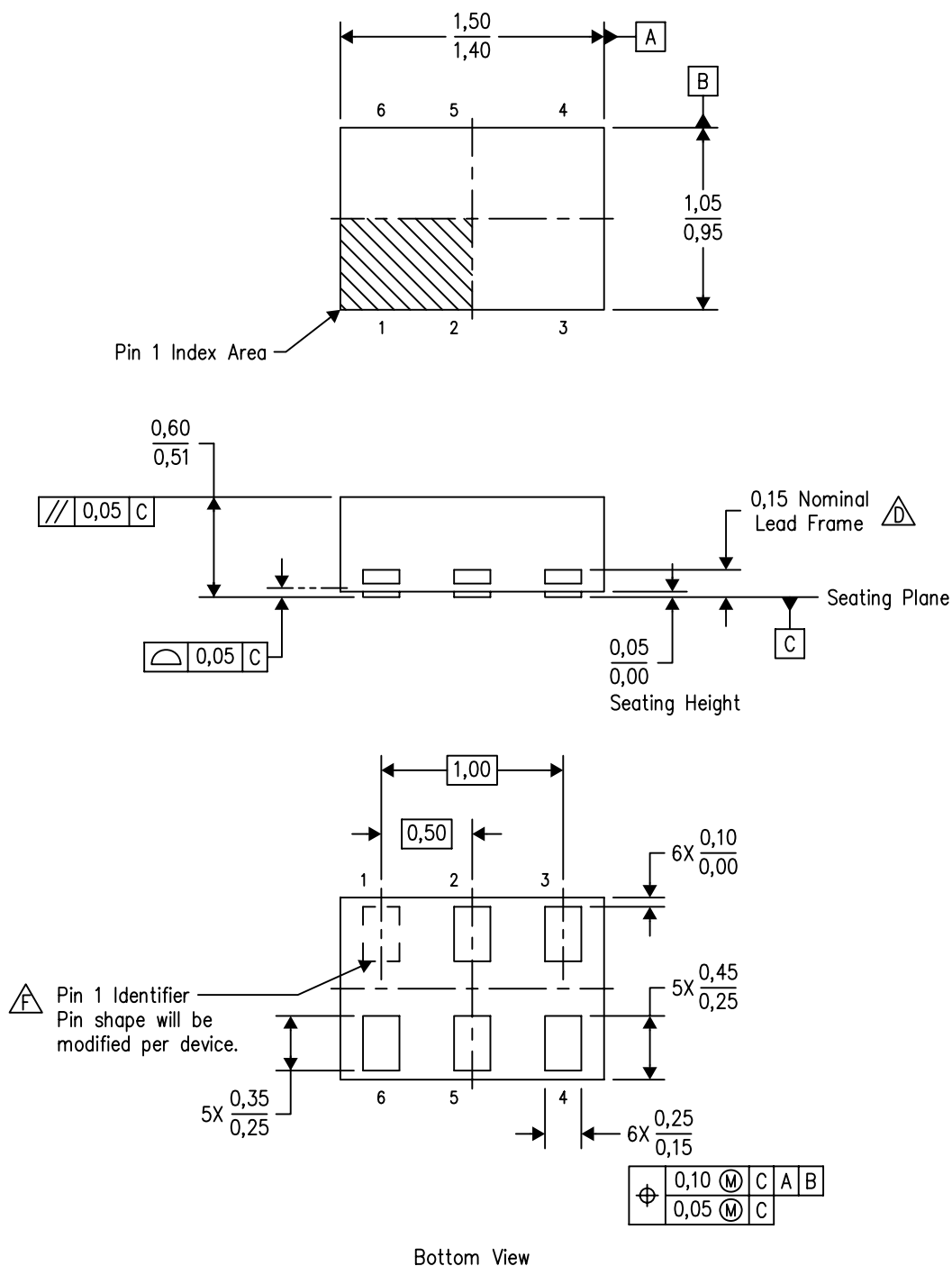
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

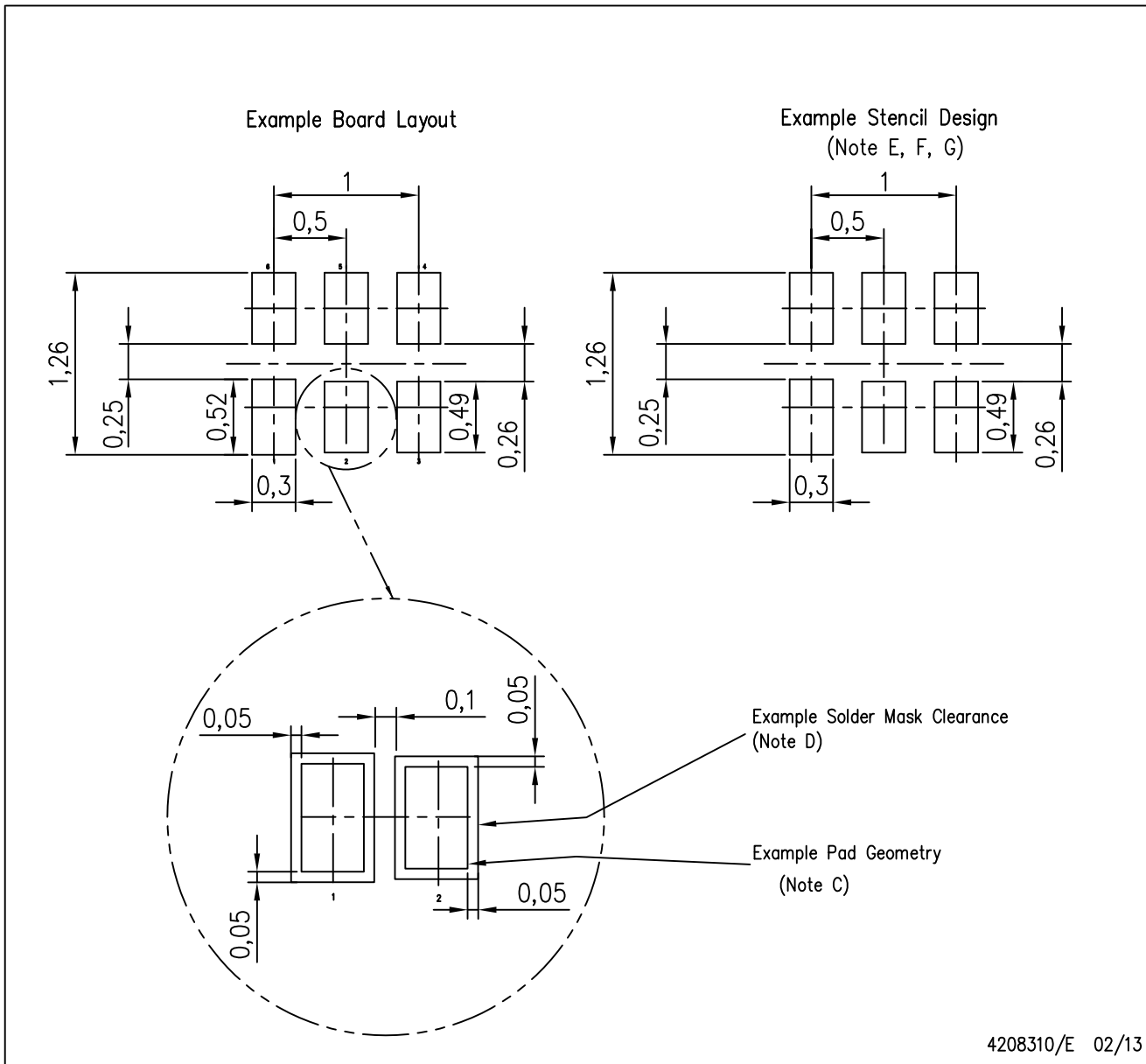


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
 - E. This package complies to JEDEC MO-287 variation UFAD.
 - See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

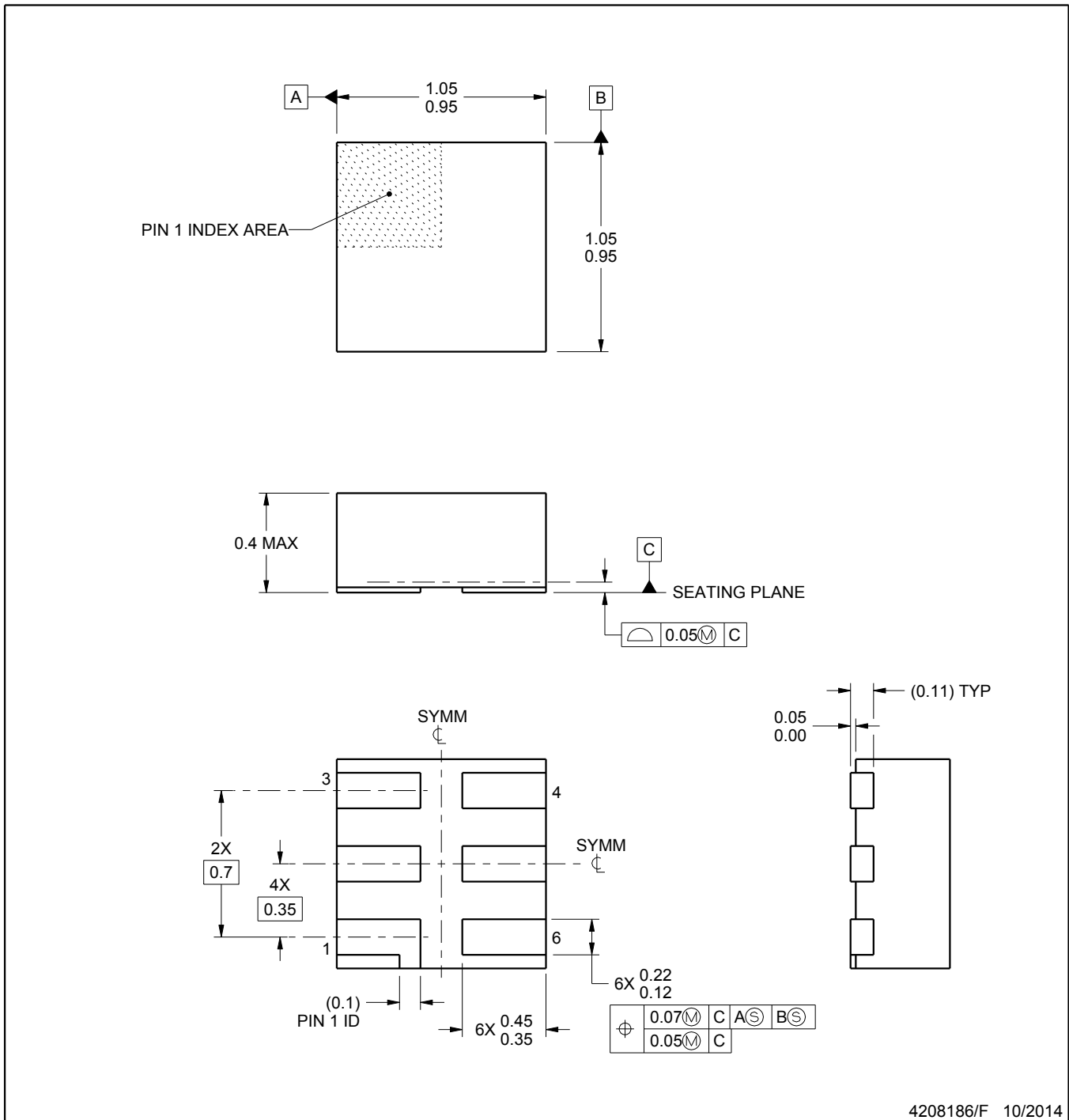


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

MECHANICAL DATA

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



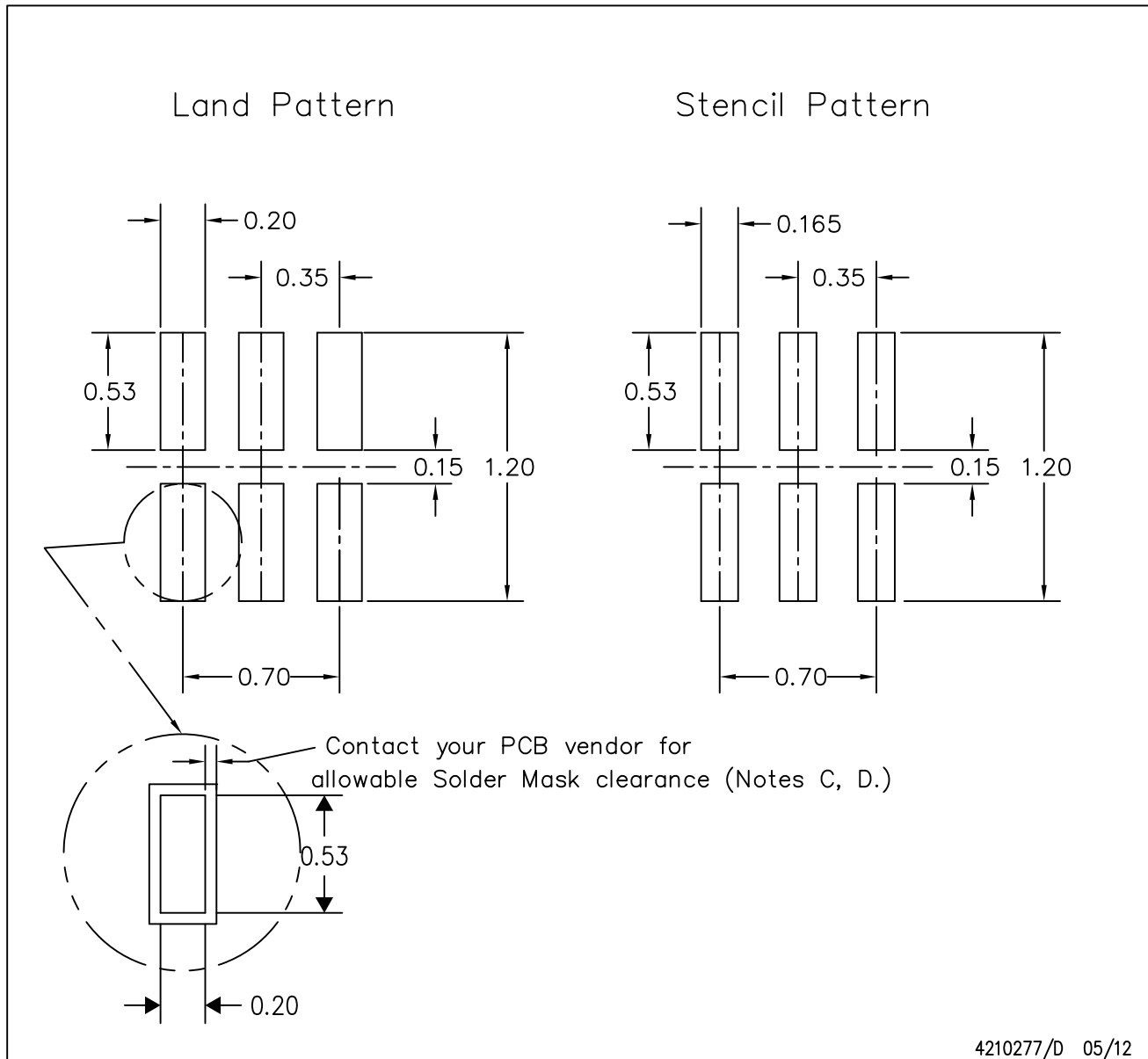
4208186/F 10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

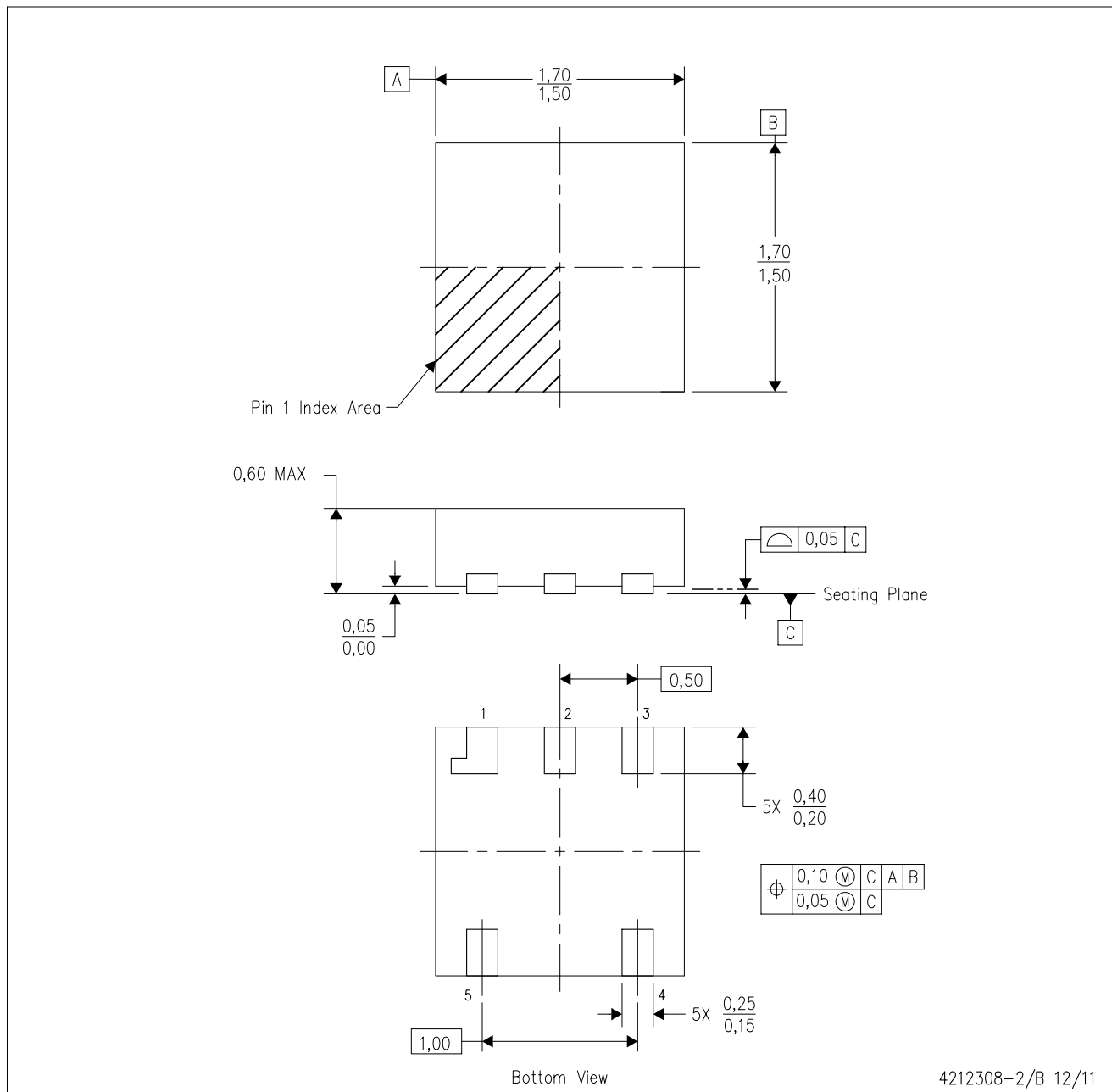


4210277/D 05/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 - Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - Component placement force should be minimized to prevent excessive paste block deformation.

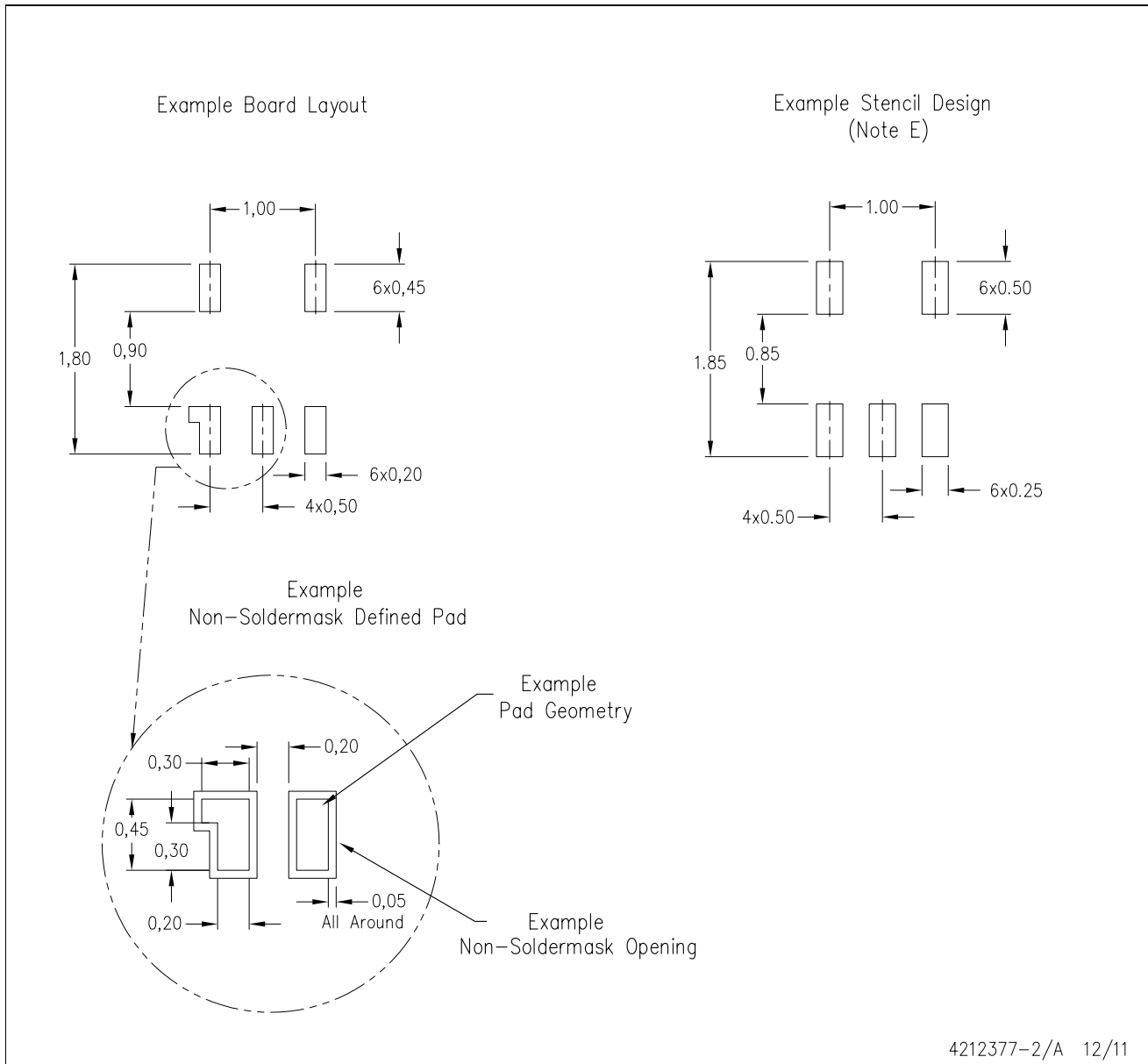
DPK (S-PUSON-N5)

PLASTIC SMALL OUTLINE NO-LEAD



4212308-2/B 12/11

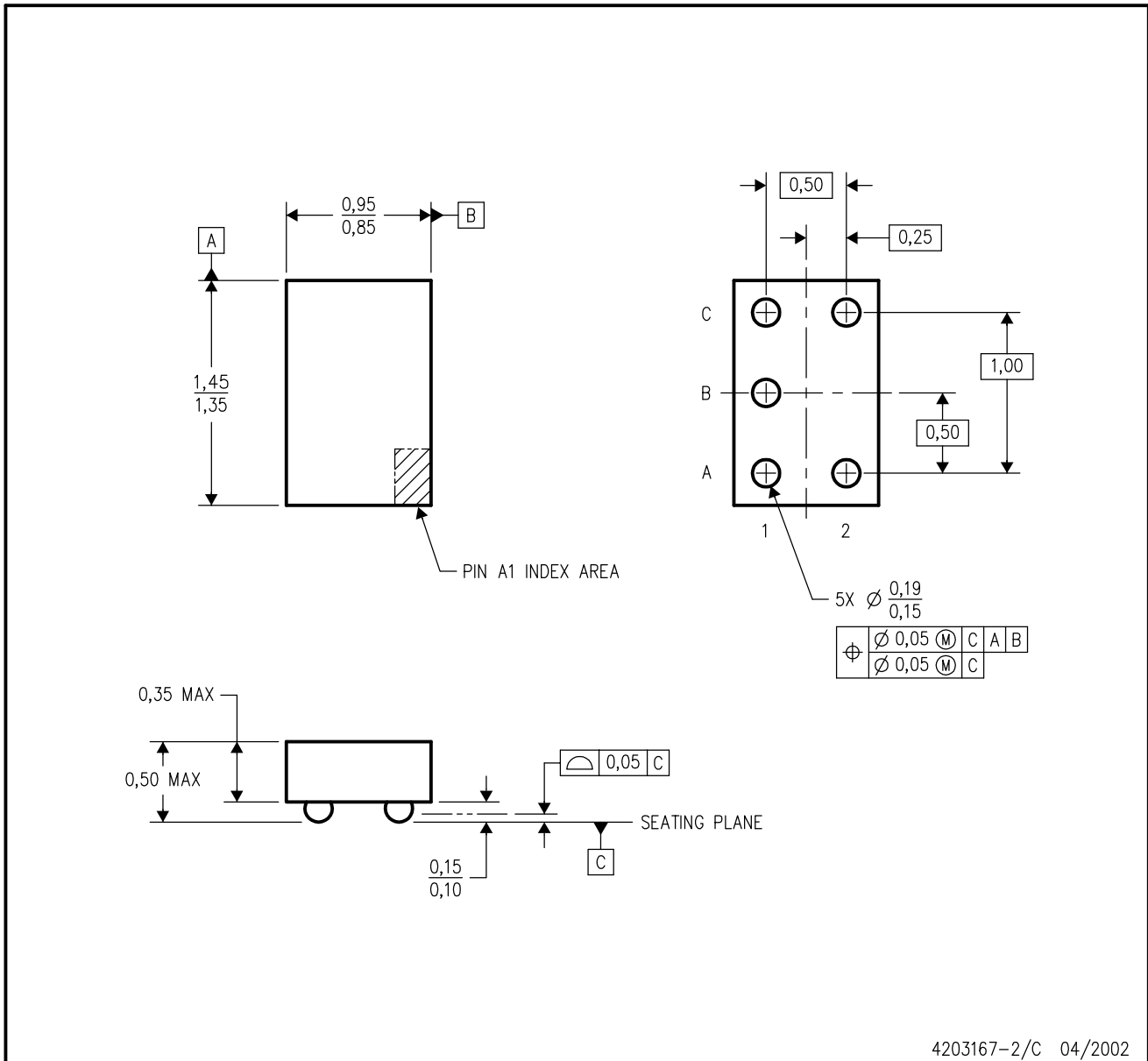
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

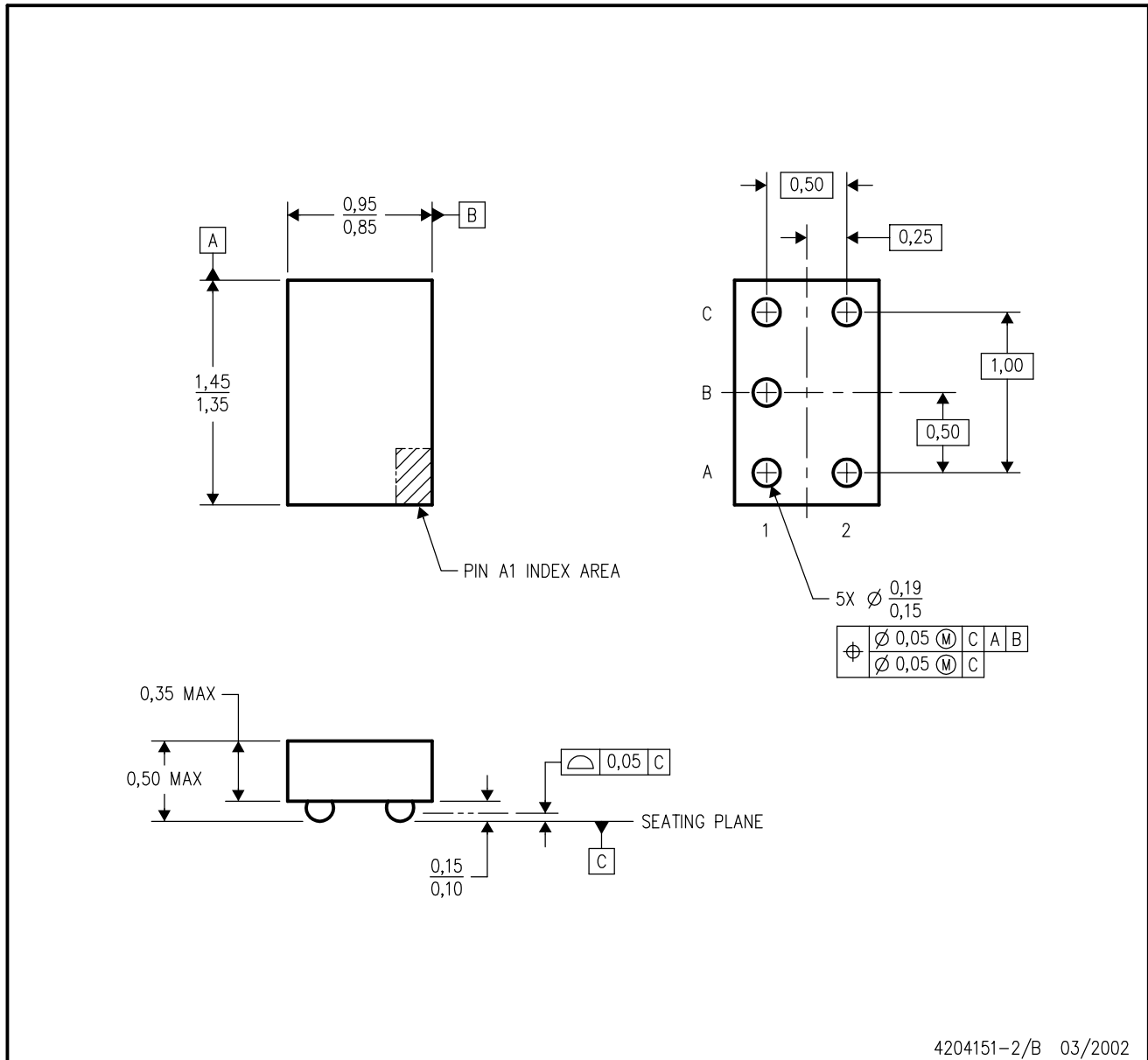


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

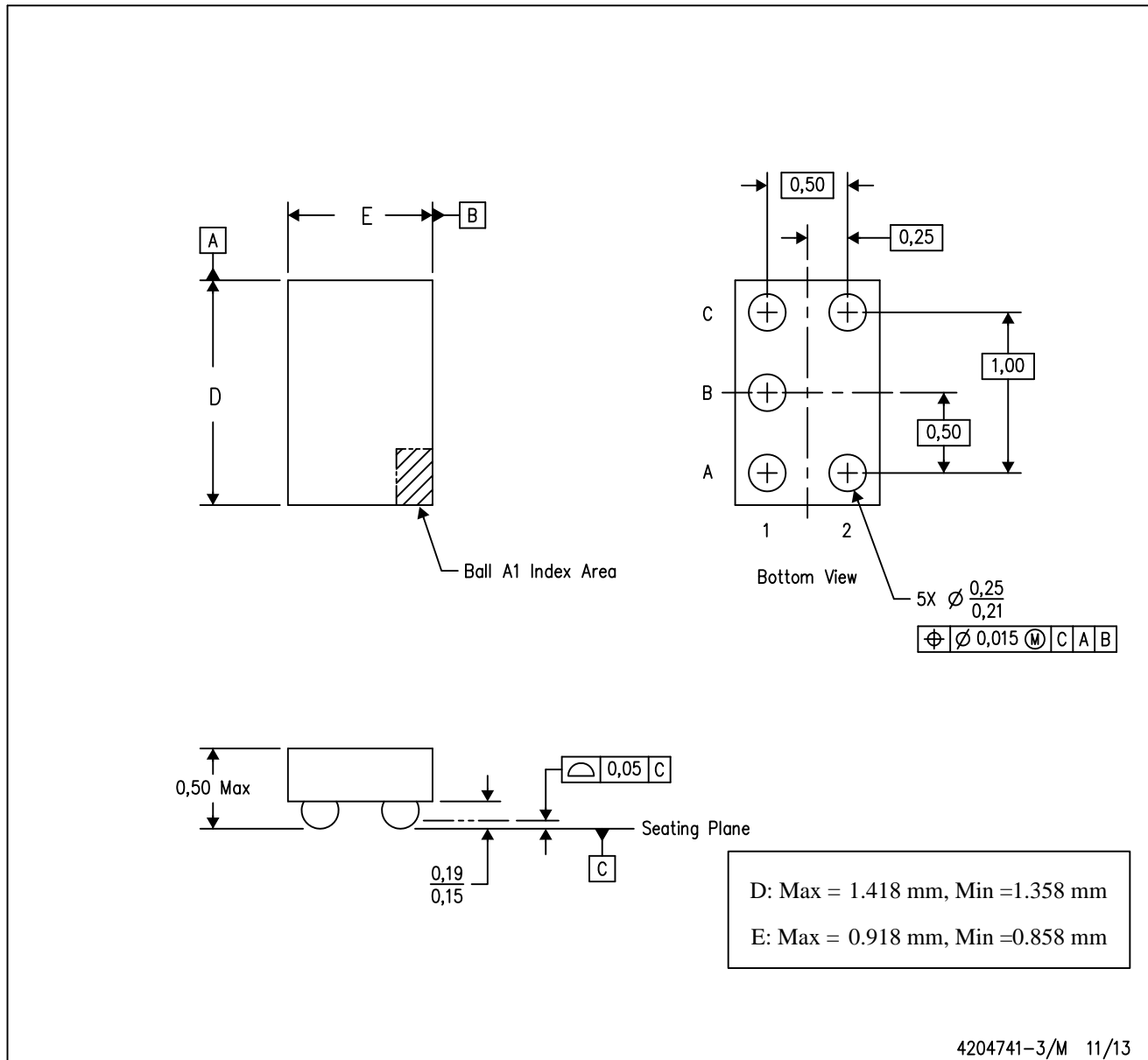


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YZP (R-XBGA-N5)

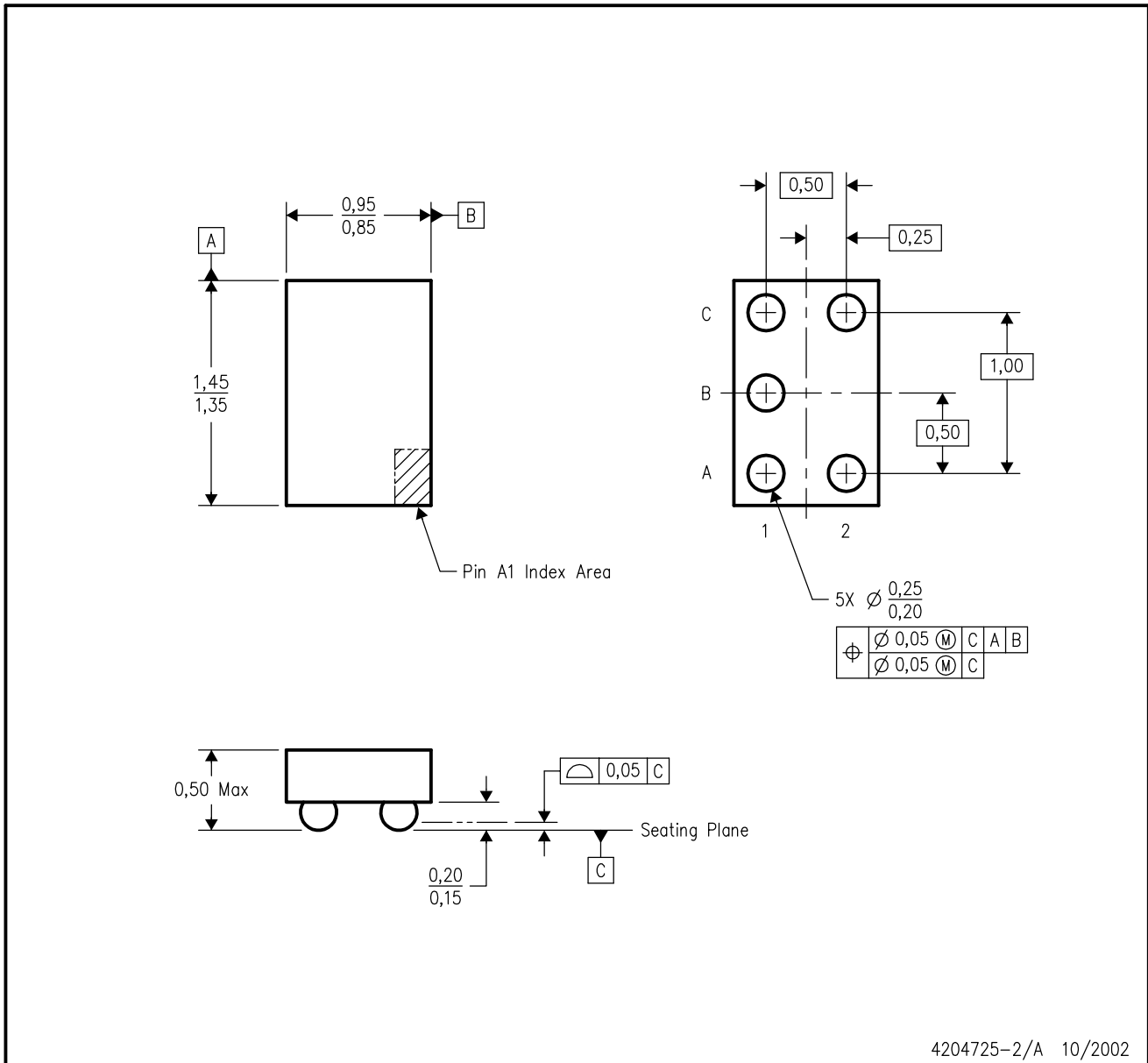
DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204725-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

NanoStar is a trademark of Texas Instruments.

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