

54ACT16952, 74ACT16952 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS159C – JANUARY 1991 – REVISED APRIL 1996

- Members of the Texas Instruments *Widebus*™ Family
- Inputs Are TTL-Voltage Compatible
- Noninverting Outputs
- Two 16-Bit, Back-to-Back Registers Store Data Flowing in Both Directions
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

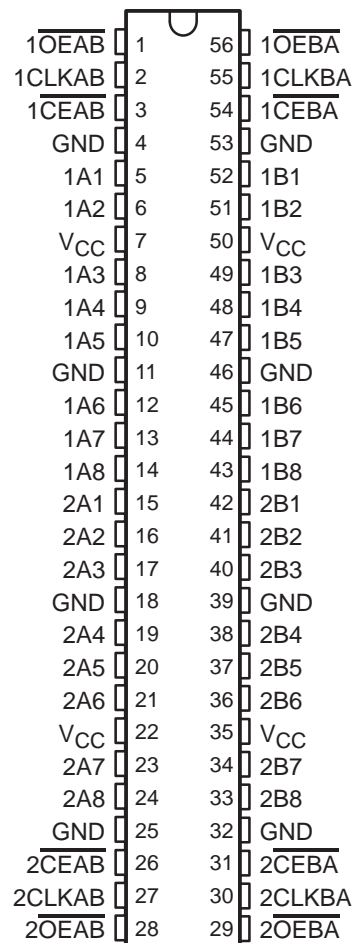
description

The 'ACT16952 are 16-bit registered transceivers that contain two sets of D-type flip-flops for temporary storage of data flowing in either direction. They can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable (\overline{CEAB} or \overline{CEBA}) input is low. Taking the output-enable (\overline{OEAB} or \overline{OEBA}) input low accesses the data on either port. To avoid false clocking of the flip-flops, \overline{CEAB} (or \overline{CEBA}) should not be switched from low to high while CLKAB (or CLKBA) is low.

The 74ACT16952 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16952 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16952 is characterized for operation from –40°C to 85°C.

54ACT16952 . . . WD PACKAGE
74ACT16952 . . . DL PACKAGE
(TOP VIEW)



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**TEXAS
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FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{\text{CEAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	
H	X	L	X	B_0^{\ddagger}
X	H	L	X	B_0^{\ddagger}
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

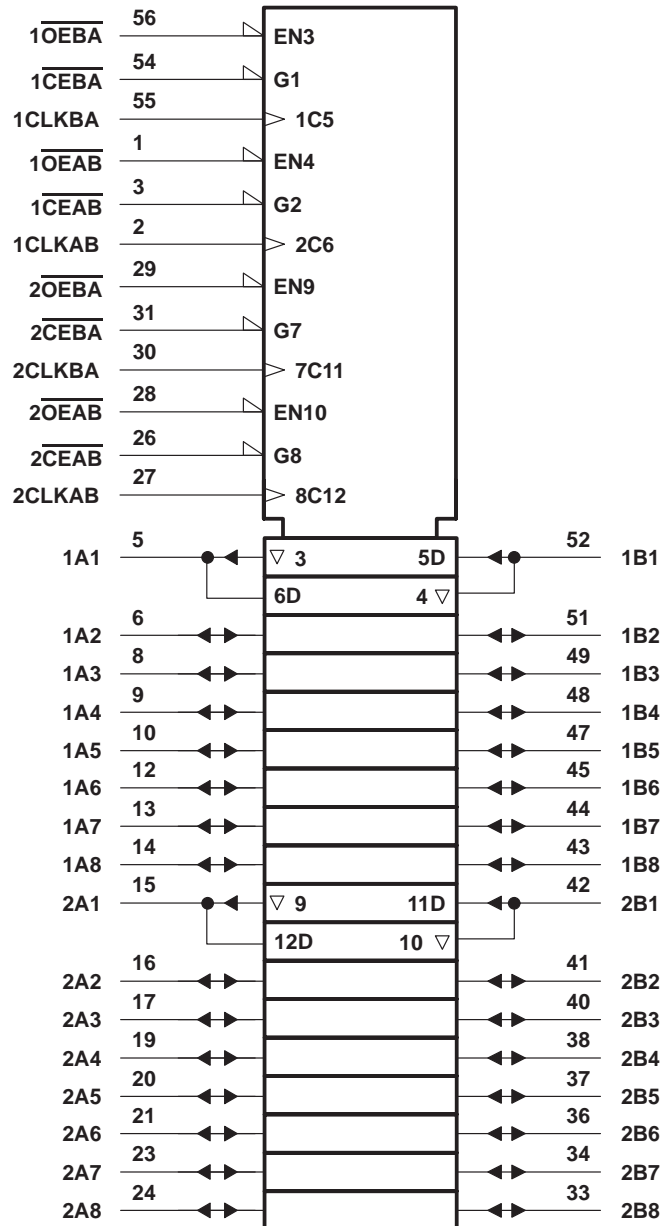
† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{\text{CEBA}}$, CLKBA, and $\overline{\text{OEBA}}$.

‡ Level of B before the indicated steady-state input conditions were established

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logic symbol†

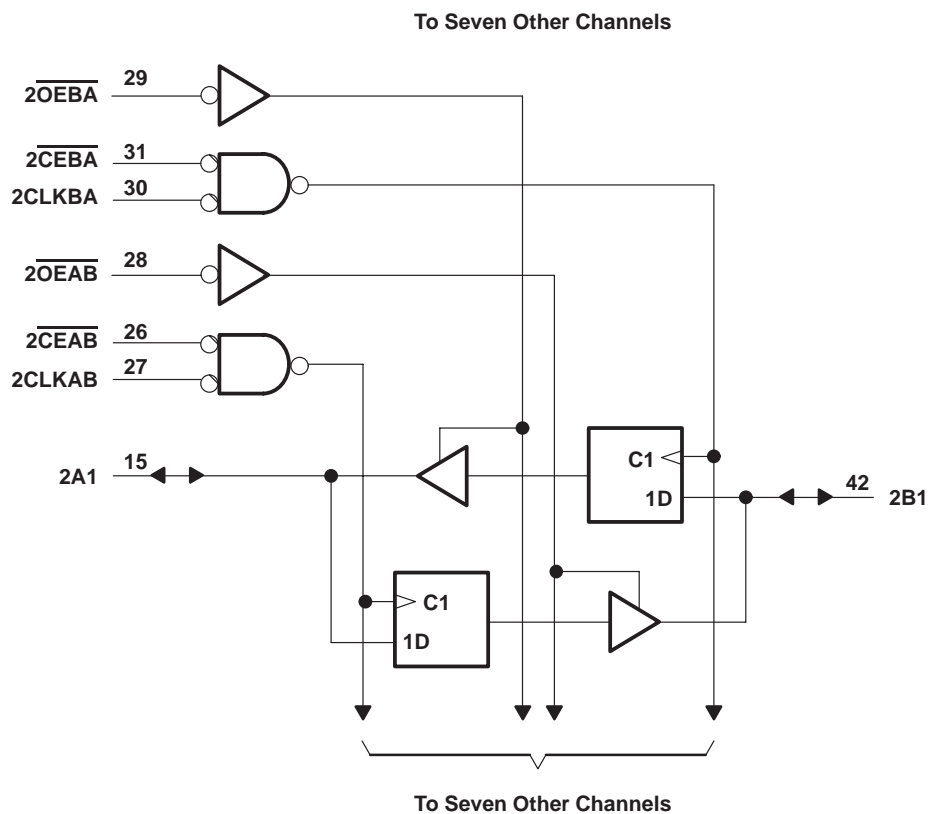
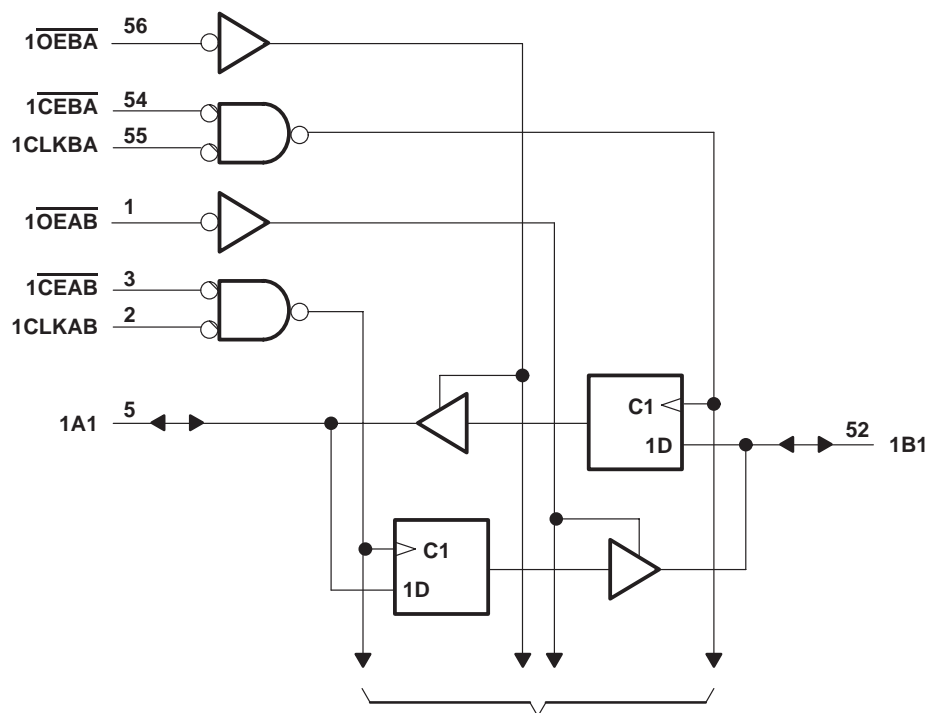


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Maximum package power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

	54ACT16952			74ACT16952			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_I Input voltage	0		V_{CC}	0		V_{CC}	V
V_O Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH} High-level output current			–24			–24	mA
I_{OL} Low-level output current			24			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	0		10	ns/V
T_A Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT16952		74ACT16952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	I _{OH} = -50 mA†	5.5 V								
	I _{OH} = -75 mA†	5.5 V				3.85		3.85		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	I _{OL} = 50 mA†	5.5 V								
	I _{OL} = 75 mA†	5.5 V					1.65		1.65	
I _I	Control inputs	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1	µA
I _{OZ} ‡	A or B ports	V _O = V _{CC} or GND	5.5 V		±0.5		±5		±5	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V		8		80		80	µA
ΔI _{CC} §		One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V		0.9		1		1	mA
C _i	Control inputs	V _I = V _{CC} or GND	5 V		3					pF
C _{io}	A or B ports	V _O = V _{CC} or GND	5 V		12					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

**timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted)**

			T _A = 25°C		54ACT16952		74ACT16952		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	75	0	75	0	75	MHz
t _w	Pulse duration, CLK high or low		6.7		6.7		6.7		ns
t _{su}	Setup time before CLK↑	Data	5		5		5		ns
		CEAB or CEBA	6.5		6.5		6.5		
t _h	Hold time after CLK↑	Data	1		1		1		ns
		CEAB or CEBA	0		0		0		

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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT16952		74ACT16952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75			75		75		MHz
t_{PLH}	CLK	A or B	4.7	8.5	10.7	4.7	11.8	4.7	11.8	ns
t_{PHL}			4.9	8.7	10.5	4.9	11.7	4.9	11.7	
t_{PLH}	$\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$	A or B	4.7	8.5	10.7	4.7	11.8	4.7	11.8	ns
t_{PHL}			4.9	8.7	10.5	4.9	11.7	4.9	11.7	
t_{PZH}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	3.4	8.1	10.2	3.4	11.2	3.4	11.2	ns
t_{PZL}			4.2	9.6	11.8	4.2	13	4.2	13	
t_{PHZ}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	5.2	7.5	8.9	5.2	9.4	5.2	9.4	ns
t_{PLZ}			4.5	6.7	8.2	4.5	8.7	4.5	8.7	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	55	pF

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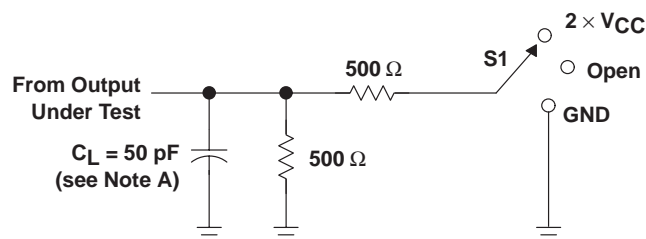


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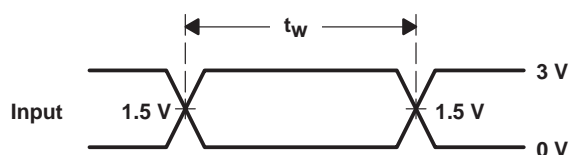
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PARAMETER MEASUREMENT INFORMATION

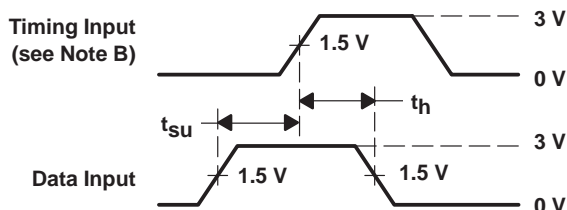


LOAD CIRCUIT

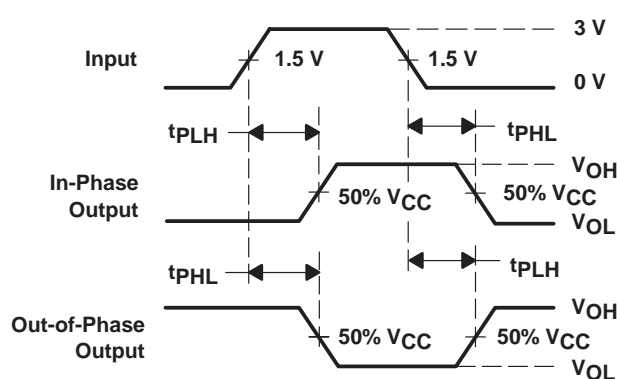
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



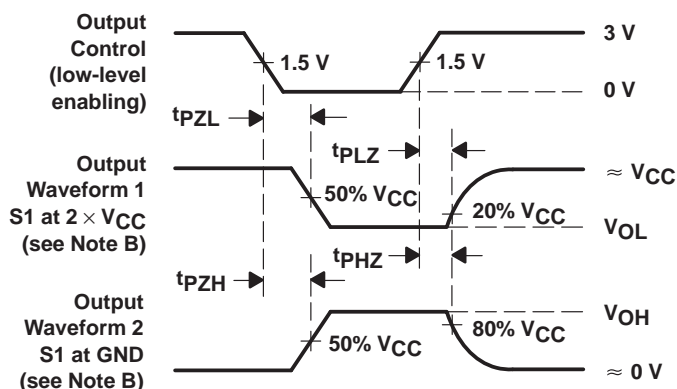
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74ACT16952DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ACT16952DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ACT16952DLR	ACTIVE	SSOP	DL	56		TBD	Call TI	Call TI	
74ACT16952DLRG4	ACTIVE	SSOP	DL	56		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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