MC14027B

Dual J-K Flip-Flop

The MC14027B dual J–K flip–flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip–flop. These devices may be used in control, register, or toggle functions.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Logic Edge−Clocked Flip−Flop Design
- Logic State is Retained Indefinitely with Clock Level Either High or Low; Information is Transferred to the Output Only on the Positive−Going Edge of the Clock Pulse
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4027B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Temperature Derating: "D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
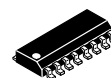
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
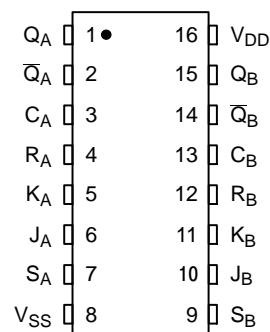
PIN ASSIGNMENT
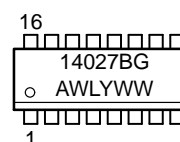
|			
Q_A	1●	16	V_{DD}
$\overline{Q}_A$	2	15	Q_B
C_A	3	14	$\overline{Q}_B$
R_A	4	13	C_B
K_A	5	12	R_B
J_A	6	11	K_B
S_A	7	10	J_B
V_{SS}	8	9	S_B

MARKING DIAGRAM

16
14027BG
○ AWLYWW
1

A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week
G = Pb−Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.
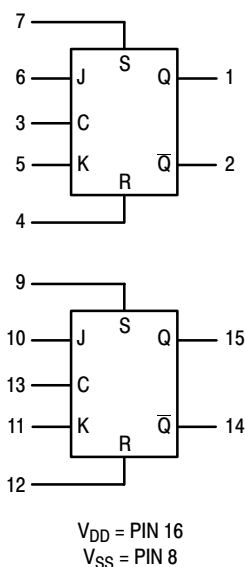
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TRUTH TABLE

Inputs						Outputs*	
$C^\dagger$	J	K	S	R	$Q_n{}^\ddagger$	Q_{n+1}	$\overline{Q_{n+1}}$
⌐_	1	X	0	0	0	1	0
⌐_	X	0	0	0	1	1	0
⌐_	0	X	0	0	0	0	1
⌐_	X	1	0	0	1	0	1
⌐_	1	1	0	0	Qo	$\overline{Qo}$	Qo
‾‾L	X	X	0	0	X	Q_n	$\overline{Q_n}$
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

No Change

X = Don't Care
$\dagger$ = Level Change
$\ddagger$ = Present State
* = Next State

BLOCK DIAGRAM

V_{DD} = PIN 16
V_{SS} = PIN 8

ORDERING INFORMATION

Device	Package	Shipping†
MC14027BDG	SOIC−16 (Pb−Free)	48 Units / Rail
NLV14027BDG*	SOIC−16 (Pb−Free)	48 Units / Rail
MC14027BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14027BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	"0" Level	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
$V_{in} = 0$ or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	–3.0 –0.64 –1.6 –4.2	– – – –	–2.4 –0.51 –1.3 –3.4	–4.2 –0.88 –2.25 –8.8	– – – –	–1.7 –0.36 –0.9 –2.4	– – – –	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mAdc
Input Current		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Capacitance ($V_{in} = 0$)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	– – –	1.0 2.0 4.0	– – –	0.002 0.004 0.006	1.0 2.0 4.0	– – –	30 60 120	µAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	$I_T = (0.8 \text{ µA/kHz}) f + I_{DD}$ $I_T = (1.6 \text{ µA/kHz}) f + I_{DD}$ $I_T = (2.4 \text{ µA/kHz}) f + I_{DD}$							µAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.002.
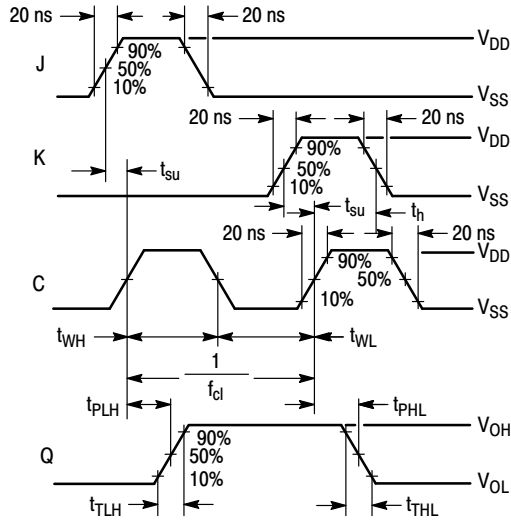
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SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

| Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 12.5 ns	t_{TLH}, t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Times** Clock to Q, Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	175 75 50	350 150 100	ns
Set to Q, Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		5.0 10 15	– – –	175 75 50	350 150 100	
Reset to Q, Q t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		5.0 10 15	– – –	350 100 75	450 200 150	
Setup Times	t_{su}	5.0 10 15	140 50 35	70 25 17	– – –	ns
Hold Times	t_h	5.0 10 15	140 50 35	70 25 17	– – –	ns
Clock Pulse Width	t_{WH}, t_{WL}	5.0 10 15	330 110 75	165 55 38	– – –	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	– – –	3.0 9.0 13	1.5 4.5 6.5	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	– – –	– – –	15 5.0 4.0	μs
Removal Times Set	t_{rem}	5 10 15	90 45 35	10 5 3	– – –	ns
Reset		5 10 15	50 25 20	– 30 – 15 – 10	– – –	
Set and Reset Pulse Width	t_{WH}	5.0 10 15	250 100 70	125 50 35	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
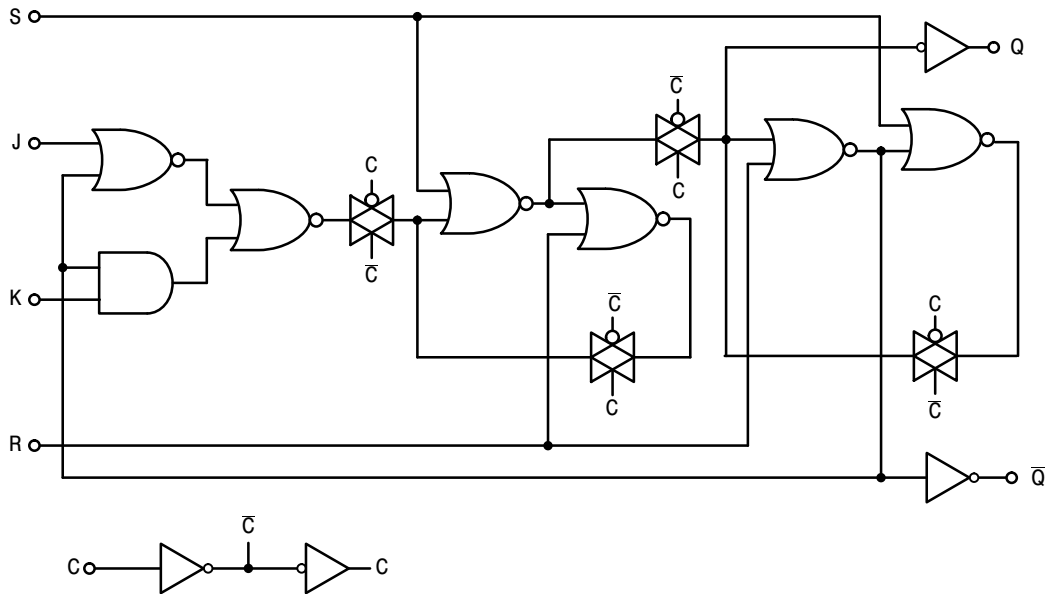
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Inputs R and S low.
For the measurement of t_{WH}, I/f_{cl}, and P_D
the Inputs J and K are kept high.

**Figure 1. Dynamic Signal Waveforms
(J, K, Clock, and Output)**
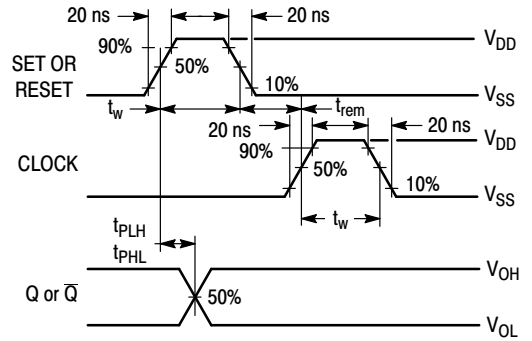
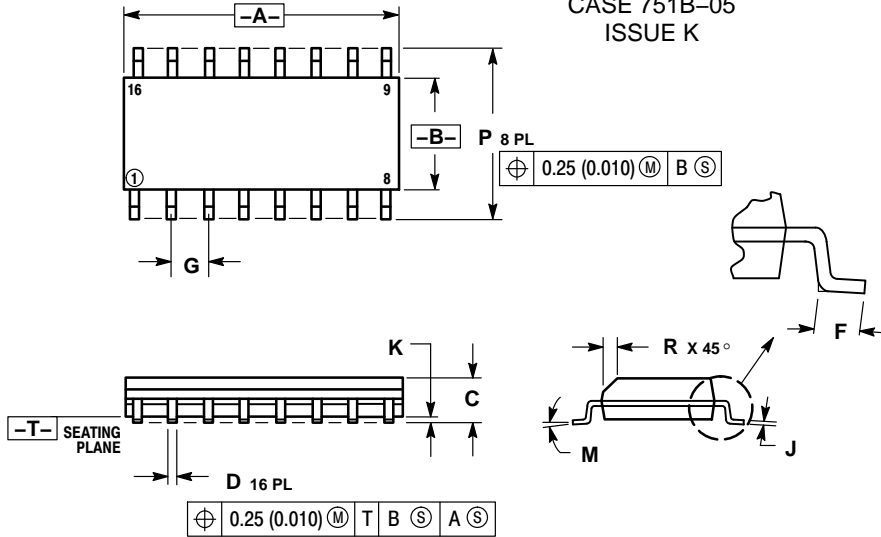**Figure 2. Dynamic Signal Waveforms
(Set, Reset, Clock, and Output)**

LOGIC DIAGRAM
(1/2 of Device Shown)

MC14027B

PACKAGE DIMENSIONS

SOIC–16
**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE K

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS
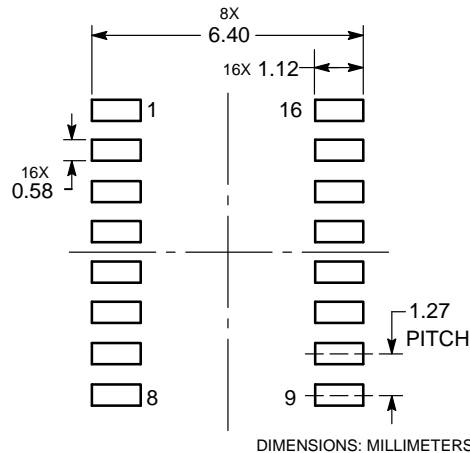
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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