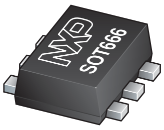


NX3008PBKV

30 V, 220 mA dual P-channel Trench MOSFET

Rev. 1 — 29 July 2011 | Product data sheet

1. Product profile

1.1 General description

Dual P-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Low threshold voltage
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

1.4 Quick reference data

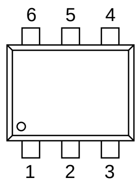
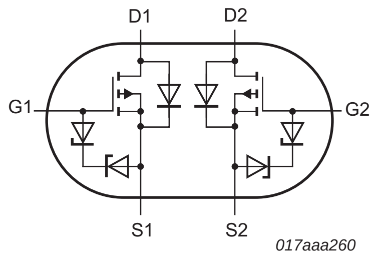
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-30	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-	-220	mA
Static characteristics (per transistor)							
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -200 mA; T_j = 25 °C		-	2.8	4.1	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 SOT666 (SOT666)	
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX3008PBKV	SOT666	plastic surface-mounted package; 6 leads	SOT666

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
NX3008PBKV	AB

[1] % = placeholder for manufacturing site code

5. Limiting values

Table 5. Limiting values

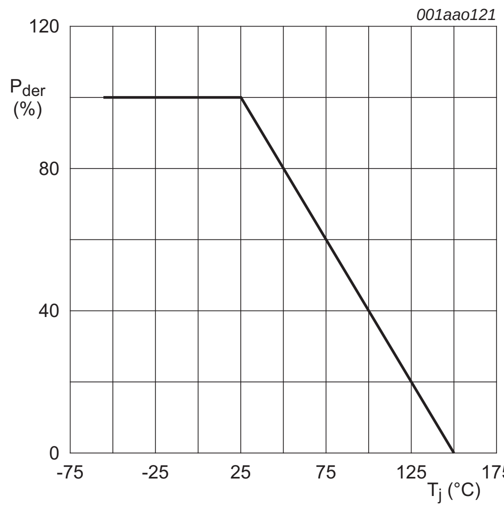
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	T_j = 25 °C		-	-30	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-220	mA
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-140	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \leq$ 10 µs		-	-0.9	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	330	mW
			[1]	-	390	mW
		T_{sp} = 25 °C		-	1090	mW
Per device						
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	500	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-220	mA
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

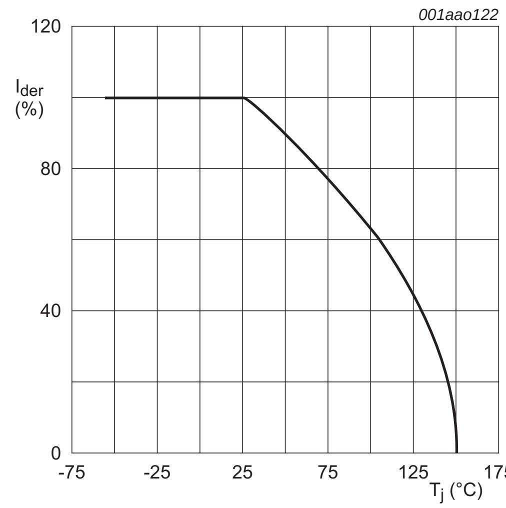
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



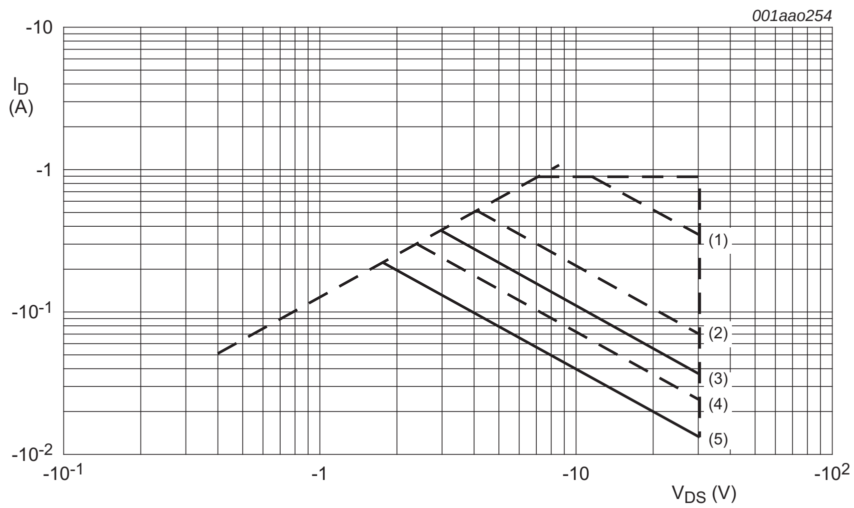
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} is a single pulse

(1) t_p = 1 ms

(2) t_p = 10 ms

(3) DC; T_{sp} = 25 °C

(4) t_p = 100 ms

(5) DC; T_{amb} = 25 °C; 1 cm^2 drain mounting pad

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

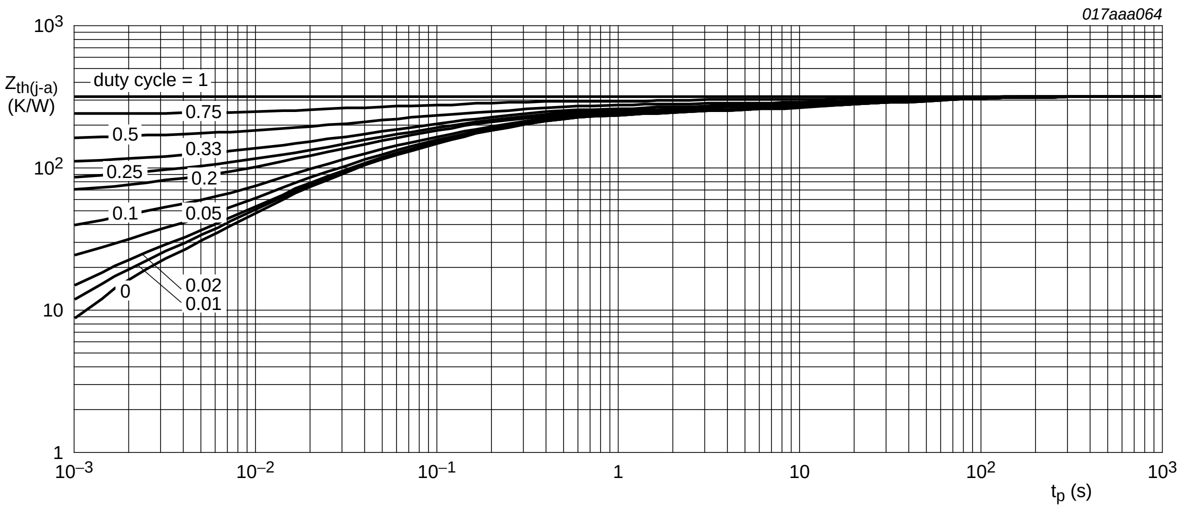
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	330	380	K/W
			[2]	-	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	115	K/W

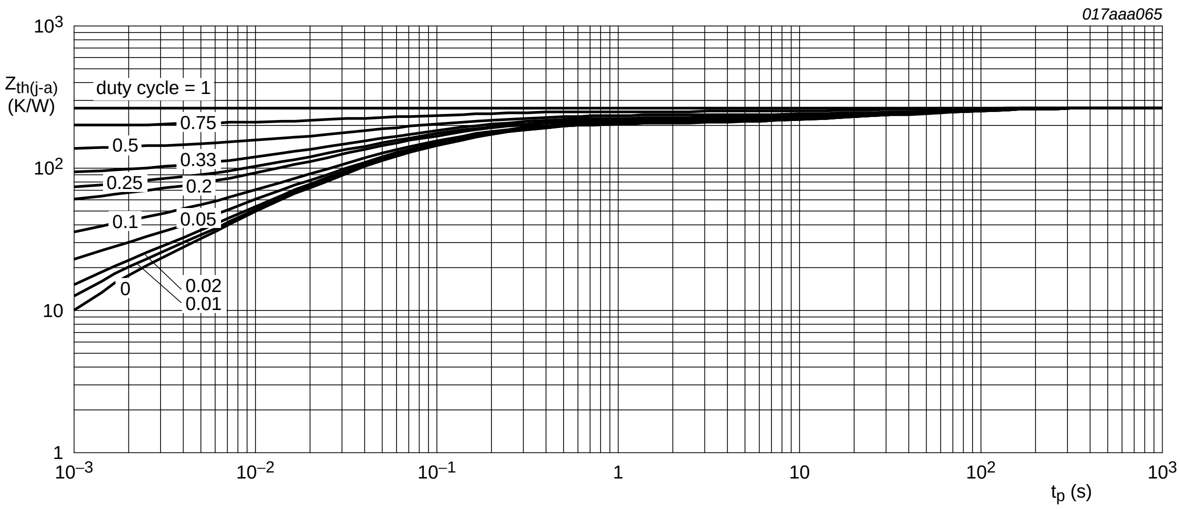
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.



FR4 PCB; standard footprint

Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



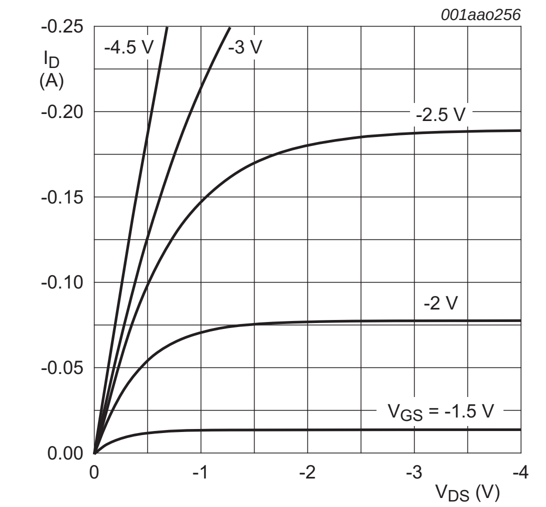
FR4 PCB, mounting pad for drain 1 cm^2

Fig 5. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

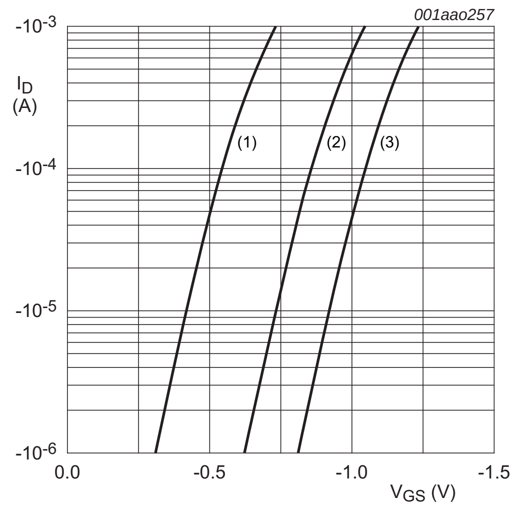
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C	-30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS}; T_j = 25 °C	-0.6	-0.9	-1.1	V
I_{DSS}	drain leakage current	V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	-1	µA
		V_{DS} = -30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	-10	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	-0.2	-1	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	-0.2	-1	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-10	-	nA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-10	-	nA
		V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-1	-	nA
		V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-1	-	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -200 mA; T_j = 25 °C	-	2.8	4.1	Ω
		V_{GS} = -4.5 V; I_D = -200 mA; T_j = 150 °C	-	5.3	7.8	Ω
		V_{GS} = -2.5 V; I_D = -10 mA; T_j = 25 °C	-	5.3	6.5	Ω
g_{fs}	forward transconductance	V_{DS} = -10 V; I_D = -200 mA; T_j = 25 °C	-	160	-	mS
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	V_{DS} = -15 V; I_D = -200 mA; V_{GS} = -4.5 V; T_j = 25 °C	-	0.55	0.72	nC
Q_{GS}	gate-source charge		-	0.23	-	nC
Q_{GD}	gate-drain charge		-	0.09	-	nC
C_{iss}	input capacitance	V_{DS} = -15 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	31	46	pF
C_{oss}	output capacitance		-	6.5	-	pF
C_{rss}	reverse transfer capacitance		-	2.3	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -20 V; R_L = 250 Ω; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	19	38	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	65	130	ns
t_f	fall time		-	38	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	I_S = -200 mA; V_{GS} = 0 V; T_j = 25 °C	-0.47	-0.88	-1.2	V



T_j = 25 °C

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



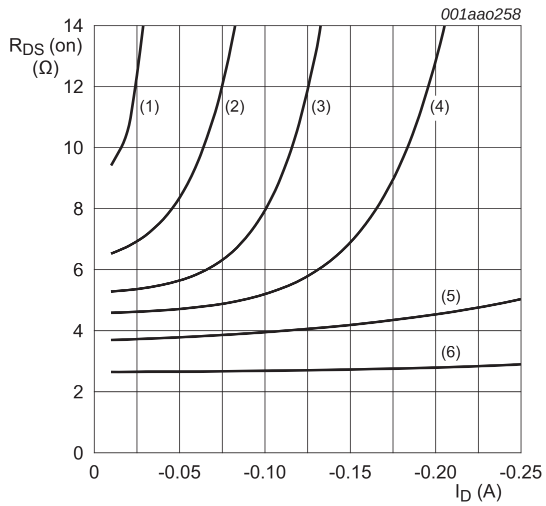
T_j = 25 °C; V_{DS} = -5 V

(1) minimum values

(2) typical values

(3) maximum values

Fig 7. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

(1) V_{GS} = -1.75 V

(2) V_{GS} = -2.0 V

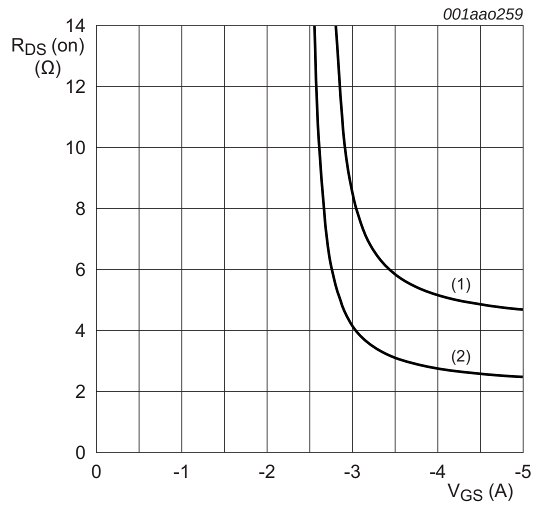
(3) V_{GS} = -2.25 V

(4) V_{GS} = -2.5 V

(5) V_{GS} = -3.0 V

(6) V_{GS} = -4.5 V

Fig 8. Drain-source on-state resistance as a function of drain current; typical values

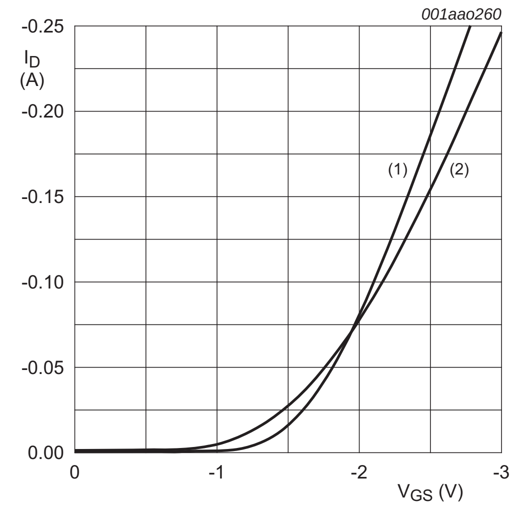


I_D = -200 mA

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

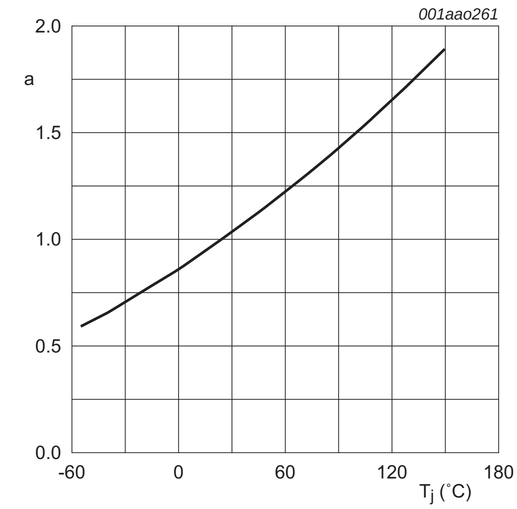


$V_{DS} > I_D \times R_{DSon}$

(1) T_j = 25 °C

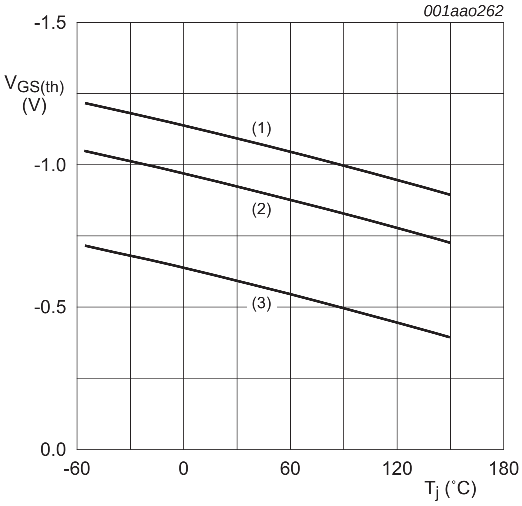
(2) T_j = 150 °C

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



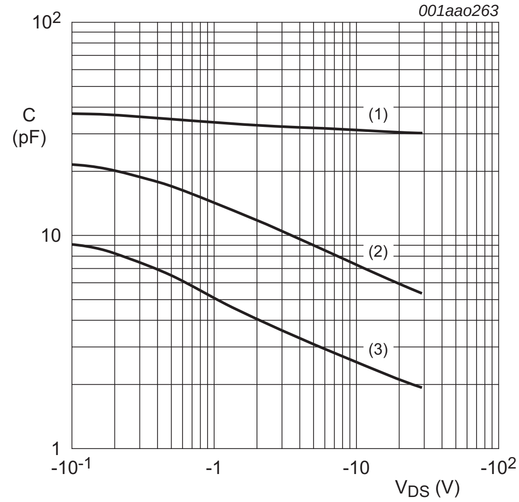
I_D = -0.25 mA; $V_{DS} = V_{GS}$

(1) maximum values

(2) typical values

(3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



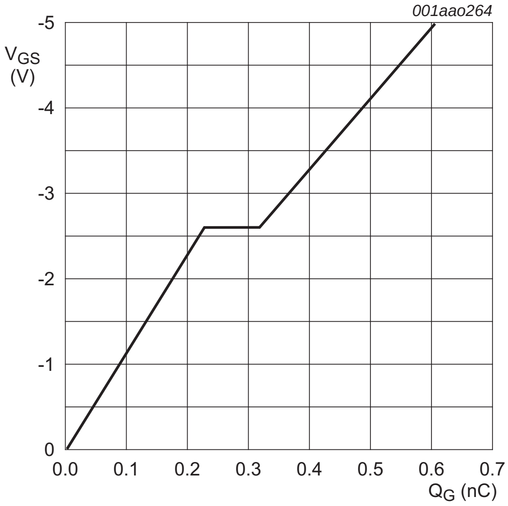
f = 1 MHz; V_{GS} = 0 V

(1)C_{iss}

(2)C_{oss}

(3)C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = -200 mA; V_{DS} = -15 V; T_{amb} = 25 °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

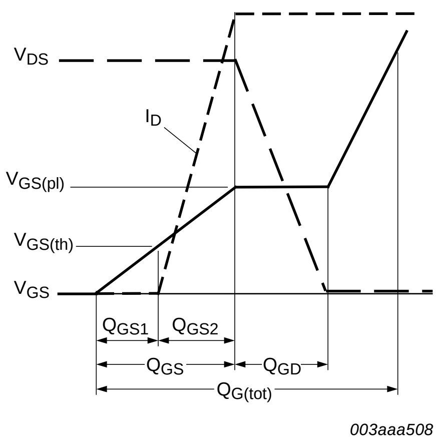
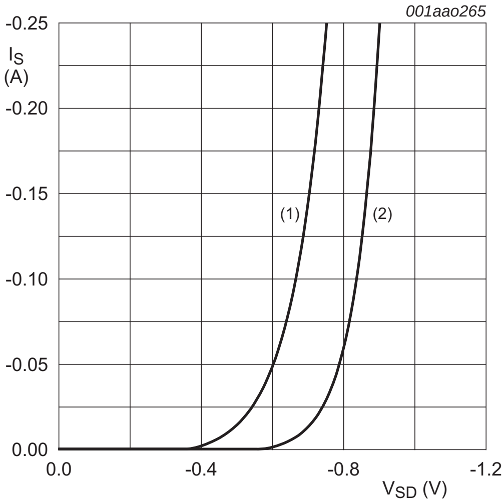


Fig 15. Gate charge waveform definitions



V_{GS} = 0 V

(1) T_j = 150 °C

(2) T_j = 25 °C

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information

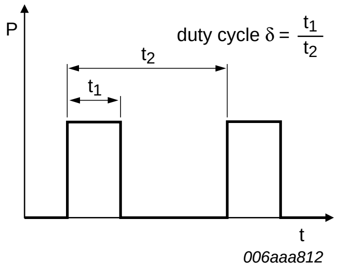


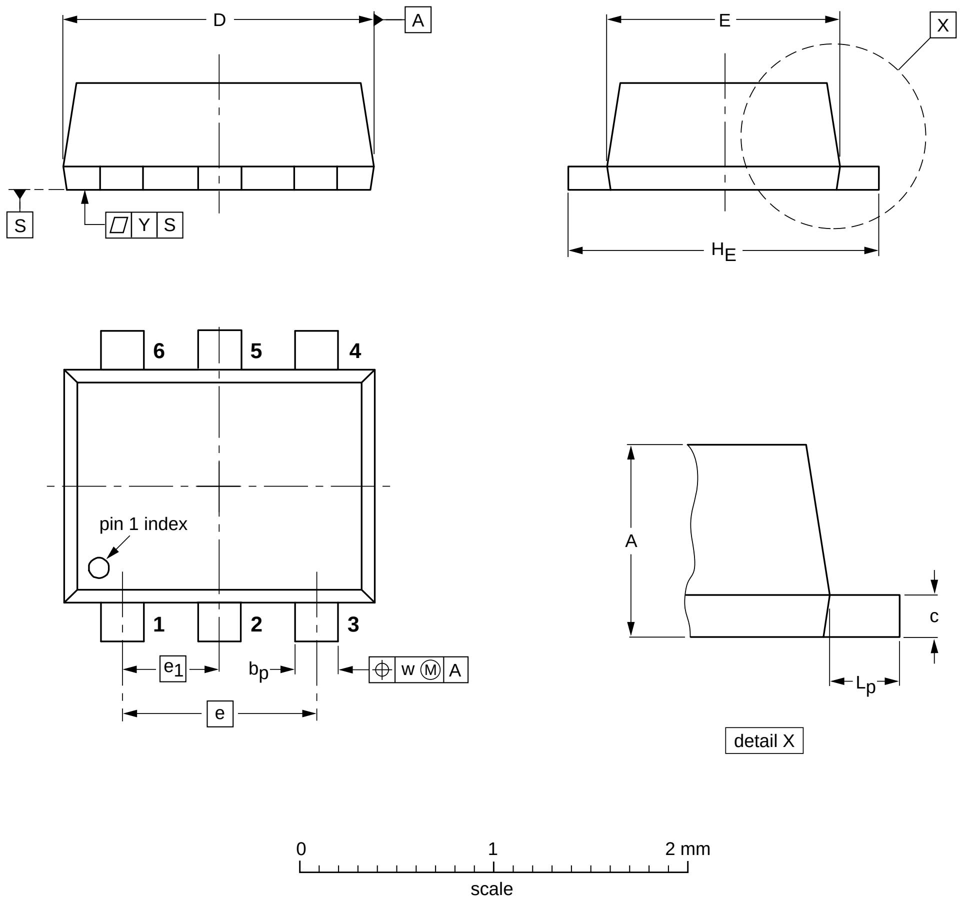
Fig 17. Duty cycle definition

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

Plastic surface-mounted package; 6 leads **SOT666**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT666						~~04-11-08~~ 06-03-16

Fig 18. Package outline SOT666 (SOT666)

10. Soldering

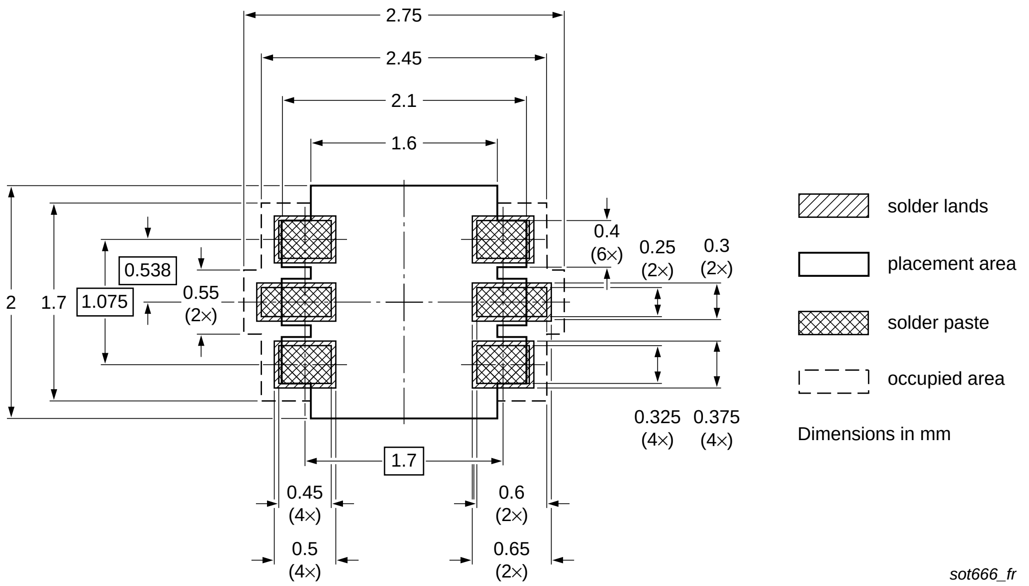


Fig 19. Reflow soldering footprint for SOT666 (SOT666)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3008PBKV v.1	20110729	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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Date of release: 29 July 2011
Document identifier: NX3008PBKV

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