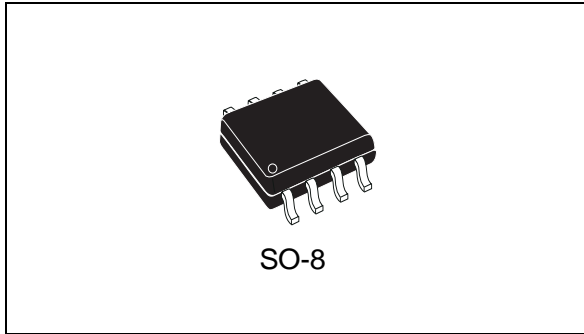


OMNIFET III fully protected low-side driver

Datasheet - production data


Description

The VNLD5300-E is a monolithic device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to the battery. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. Output current limitation protects the device in an overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the device to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

Features

| Type | V _{clamp} | R _{DS(on)} | I _D |
|------------|--------------------|---------------------|----------------|
| VNLD5300-E | 41 V | 300 mΩ | 2 A |

- Drain current: 2 A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- Compliant with European directive 2002/95/EC
- Open drain status output

Table 1. Devices summary

| Package | Order codes | |
|---------|-------------|---------------|
| | Tube | Tape and reel |
| SO-8 | VNLD5300-E | VNLD5300TR-E |

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1 Block diagrams and pins configurations

Figure 1. Block diagram

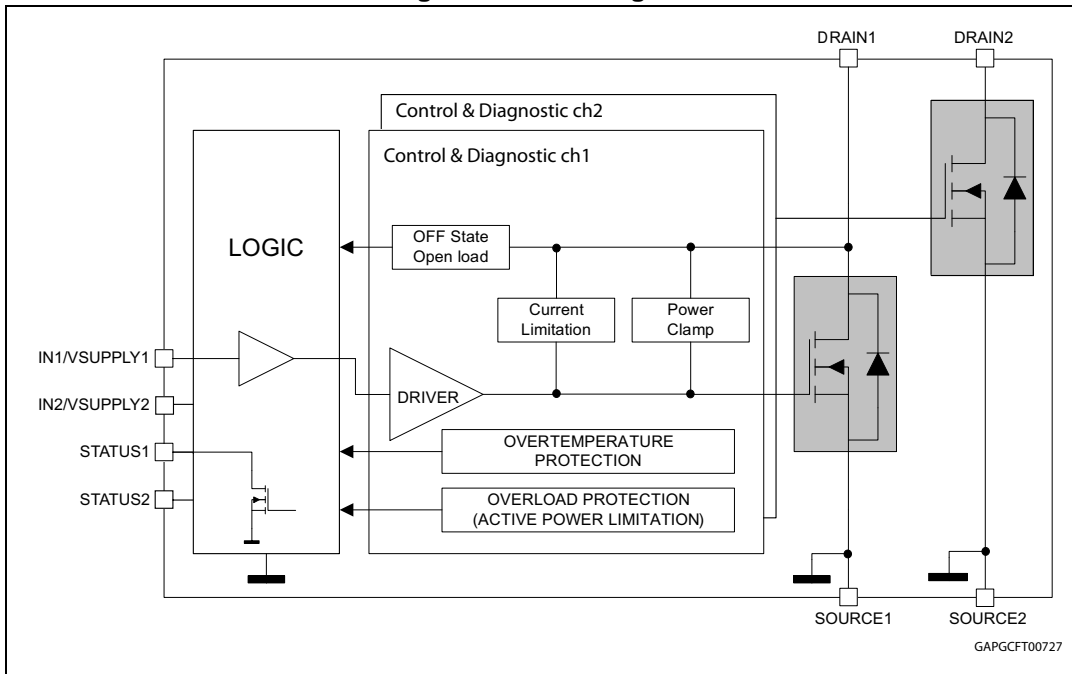


Table 2. Pin function

| Name | Function |
|---|--|
| IN _{1,2} /VSUPPLY _{1,2} | Voltage controlled input pin with hysteresis, CMOS compatible. They control output switch state. |
| DRAIN _{1,2} | PowerMOS drain. |
| SOURCE _{1,2} | PowerMOS source and ground reference for the control section. |
| STATUS _{1,2} | Open drain digital diagnostic pin. |

Figure 2. Current and voltage conventions

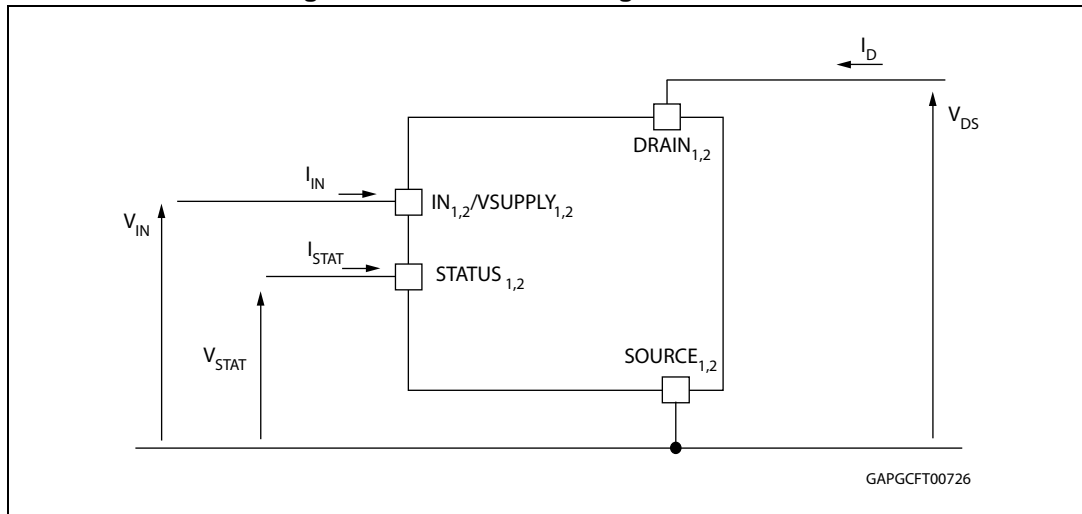


Figure 3. Configuration diagrams (top view)

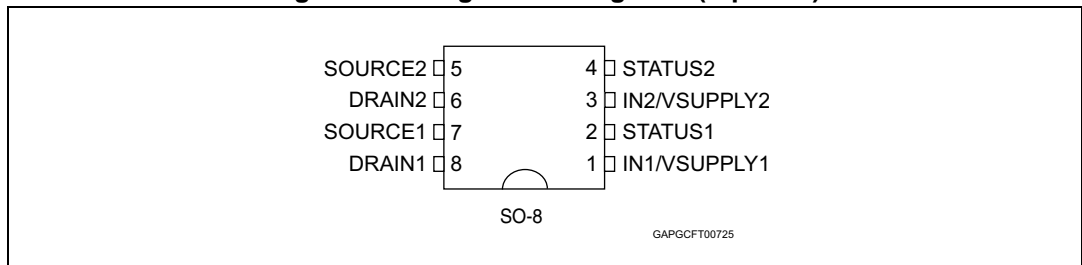


Table 3. Suggested connections for unused and n.c. pins

| Connection / pin | STATUS _{1,2} | N.C. | INPUT _{1,2} |
|------------------|-----------------------|------|------------------------|
| Floating | X ⁽¹⁾ | X | X |
| To ground | Not allowed | X | Through 10 kΩ resistor |

1. X: do not care.

2 Electical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------|---|--------------------|--------------|
| V_{DS} | Drain-source voltage ($V_{IN} = 0$ V) | Internally clamped | V |
| I_D | DC drain current | Internally limited | A |
| $-I_D$ | Reverse DC drain current | 6 | A |
| I_S | DC supply current | -1 to 10 | mA |
| I_{IN} | DC input current | -1 to 10 | mA |
| I_{STAT} | DC status current | -1 to 10 | mA |
| V_{ESD1} | Electrostatic discharge ($R = 1.5$ k Ω ; $C = 100$ pF) – DRAIN – SUPPLY, INPUT, STATUS | 5000 4000 | V |
| V_{ESD2} | Electrostatic discharge on output pin only ($R = 330$ Ω , $C = 150$ pF) | 2000 | V |
| T_j | Junction operating temperature | -40 to 150 | $^{\circ}$ C |
| T_{stg} | Storage temperature | -55 to 150 | $^{\circ}$ C |
| E_{AS} | Single pulse avalanche energy ($L = 19$ mH, $T_j = 150^{\circ}$ C, $R_L = 0$, $I_{OUT} = I_{limL}$) | 26 | mJ |

2.2 Thermal data

Table 5. Thermal data

| Symbol | Parameter | Maximum value | Unit |
|---------------|-------------------------------------|---------------|----------------|
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 115 | $^{\circ}$ C/W |

2.3 Electrical characteristics

Values specified in this section are for $V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V to } 5.5 \text{ V}$, $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise stated.

Table 6. PowerMOS section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------|--------------------------------------|---|------|------|------|---------------|
| R_{ON} | ON-state resistance | $I_{\text{D}} = 0.8 \text{ A}$; $T_j = 25^\circ\text{C}$; $V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V}$ | | 300 | | m Ω |
| | | $I_{\text{D}} = 0.8 \text{ A}$; $T_j = 150^\circ\text{C}$; $V_{\text{supply}} = V_{\text{IN}} = 4.5 \text{ V}$ | | | 600 | |
| V_{CLAMP} | Drain-source clamp voltage | $V_{\text{IN}} = 5 \text{ V}$; $I_{\text{D}} = 0.8 \text{ A}$ | 41 | 46 | 52 | V |
| V_{CLTH} | Drain-source clamp threshold voltage | $V_{\text{IN}} = 0 \text{ V}$; $I_{\text{D}} = 2 \text{ mA}$ | 36 | | | V |
| I_{DSS} | OFF-state output current | $V_{\text{IN}} = 0 \text{ V}$; $V_{\text{DS}} = 13 \text{ V}$; $T_j = 25^\circ\text{C}$ | 0 | | 3 | μA |
| | | $V_{\text{IN}} = 0 \text{ V}$; $V_{\text{DS}} = 13 \text{ V}$; $T_j = 125^\circ\text{C}$ | 0 | | 5 | |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|--|------|------|------|------|
| V_{SD} | Forward on voltage | $I_{\text{D}} = 0.8 \text{ A}$; $V_{\text{IN}} = 0 \text{ V}$ | — | 0.8 | — | V |

Table 8. Input section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|-------------------------------|--|------|------|------|---------------|
| I_{ISS} | Supply current from input pin | ON-state: $V_{\text{supply}} = V_{\text{IN}} = 5 \text{ V}$; $V_{\text{DS}} = 0 \text{ V}$ | | 30 | 65 | μA |
| | | OFF-state; $T_j = 25^\circ\text{C}$; $V_{\text{IN}} = V_{\text{DRAIN}} = 0 \text{ V}$; | | | | |
| V_{ICL} | Input clamp voltage | $I_{\text{S}} = 1 \text{ mA}$ | 5.5 | | 7 | V |
| | | $I_{\text{S}} = -1 \text{ mA}$ | | -0.7 | | |
| V_{INTH} | Input threshold voltage | $V_{\text{DS}} = V_{\text{IN}}$; $I_{\text{D}} = 1 \text{ mA}$ | 1 | | 3.5 | V |

Table 9. Status pin

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------|------------------------------|--|------|------|------|---------------|
| V_{STAT} | Status low output voltage | $I_{\text{STAT}} = 1 \text{ mA}$ | | | 0.5 | V |
| I_{LSTAT} | Status leakage current | Normal operation; $V_{\text{STAT}} = 5 \text{ V}$ | | | 10 | μA |
| C_{STAT} | Status pin input capacitance | Normal operation; $V_{\text{STAT}} = 5 \text{ V}$ | | | 100 | pF |
| V_{STCL} | Status clamp voltage | $I_{\text{STAT}} = 1 \text{ mA}$ | 5.5 | | 7 | V |
| | | $I_{\text{STAT}} = -1 \text{ mA}$ | | -0.7 | | |

Table 10. Switching characteristics⁽¹⁾

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|-------------------------------------|--|------|-------|------|---------|
| $t_{d(ON)}$ | Turn-on delay time | $R_L = 16 \Omega, V_{CC} = 13 V^{(2)}$ | — | 6 | — | μs |
| $t_{d(OFF)}$ | Turn-off delay time | $R_L = 16 \Omega, V_{CC} = 13 V^{(2)}$ | — | 3 | — | μs |
| t_r | Rise time | $R_L = 16 \Omega, V_{CC} = 13 V^{(2)}$ | — | 11 | — | μs |
| t_f | Fall time | $R_L = 16 \Omega, V_{CC} = 13 V^{(2)}$ | — | 3 | — | μs |
| W_{ON} | Switching energy losses at turn-on | $R_L = 16 \Omega, V_{CC} = 13 V^{(2)}$ | — | 0.028 | — | mJ |
| W_{OFF} | Switching energy losses at turn-off | $R_L = 16 \Omega, V_{CC} = 13 V^{(2)}$ | — | 0.006 | — | mJ |
| Q_g | Total gate charge | $V_{supply} = V_{IN} = 5 V$ | — | 0.6 | — | nC |

1. See [Figure 5: Application schematic](#).
2. See [Figure 4: Switching characteristics](#).

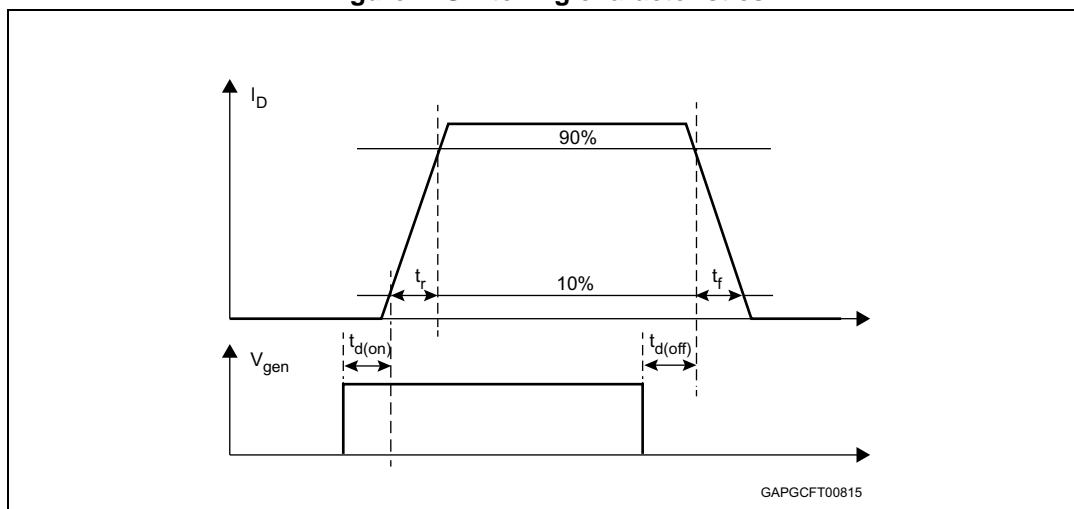
Table 11. Protection and diagnostics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------|--|--|--------------|--------------|------|-------------|
| I_{limH} | DC short-circuit current | $V_{DS} = 13 V;$ $V_{supply} = V_{IN} = 5 V$ | 2 | 2.8 | 3.8 | A |
| I_{limL} | Short-circuit current during thermal cycling | $V_{DS} = 13 V; T_R < T_j < T_{TSD};$ $V_{supply} = V_{IN} = 5 V$ | | 1.4 | | A |
| t_{dimL} | Step response current limit | $V_{DS} = 13 V; V_{input} = 5 V$ | | 7 | | μs |
| T_{TSD} | Shutdown temperature | | 150 | 175 | 200 | $^{\circ}C$ |
| T_R | Reset temperature | | $T_{RS} + 1$ | $T_{RS} + 5$ | | $^{\circ}C$ |
| T_{RS} | Thermal reset of STATUS | | 135 | | | $^{\circ}C$ |
| T_{HYST} | Thermal hysteresis ($T_{TSD} - T_R$) | | | 7 | | $^{\circ}C$ |

Table 12. Truth table

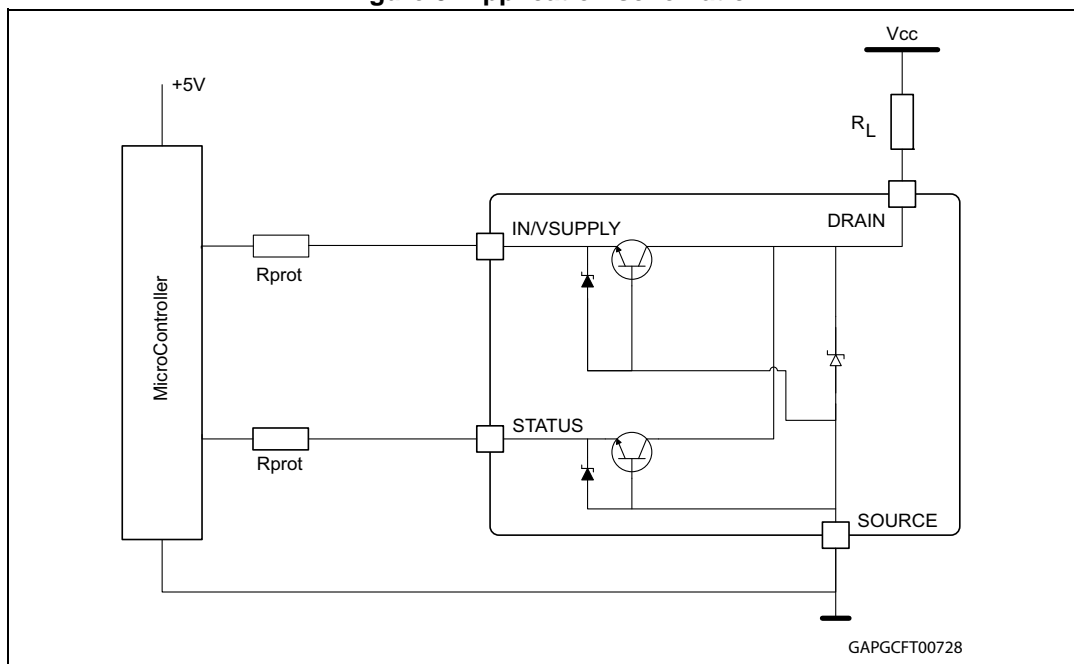
| Conditions | INPUT | DRAIN | STATUS |
|--------------------|-------|-------|--------|
| Normal operation | L | H | H |
| | H | L | H |
| Current limitation | L | H | H |
| | H | X | H |
| Overtemperature | L | H | H |
| | H | H | L |
| Undervoltage | L | H | X |
| | H | H | X |

Figure 4. Switching characteristics



3 Application information

Figure 5. Application schematic



3.1 MCU I/O protection

ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up^(a). The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the LSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os:

Equation 1:

$$\frac{0.7}{I_{latchup}} \leq R_{prot} \leq \frac{(V_{OH\mu C} - V_{IH})}{I_{IH\ max}}$$

Let:

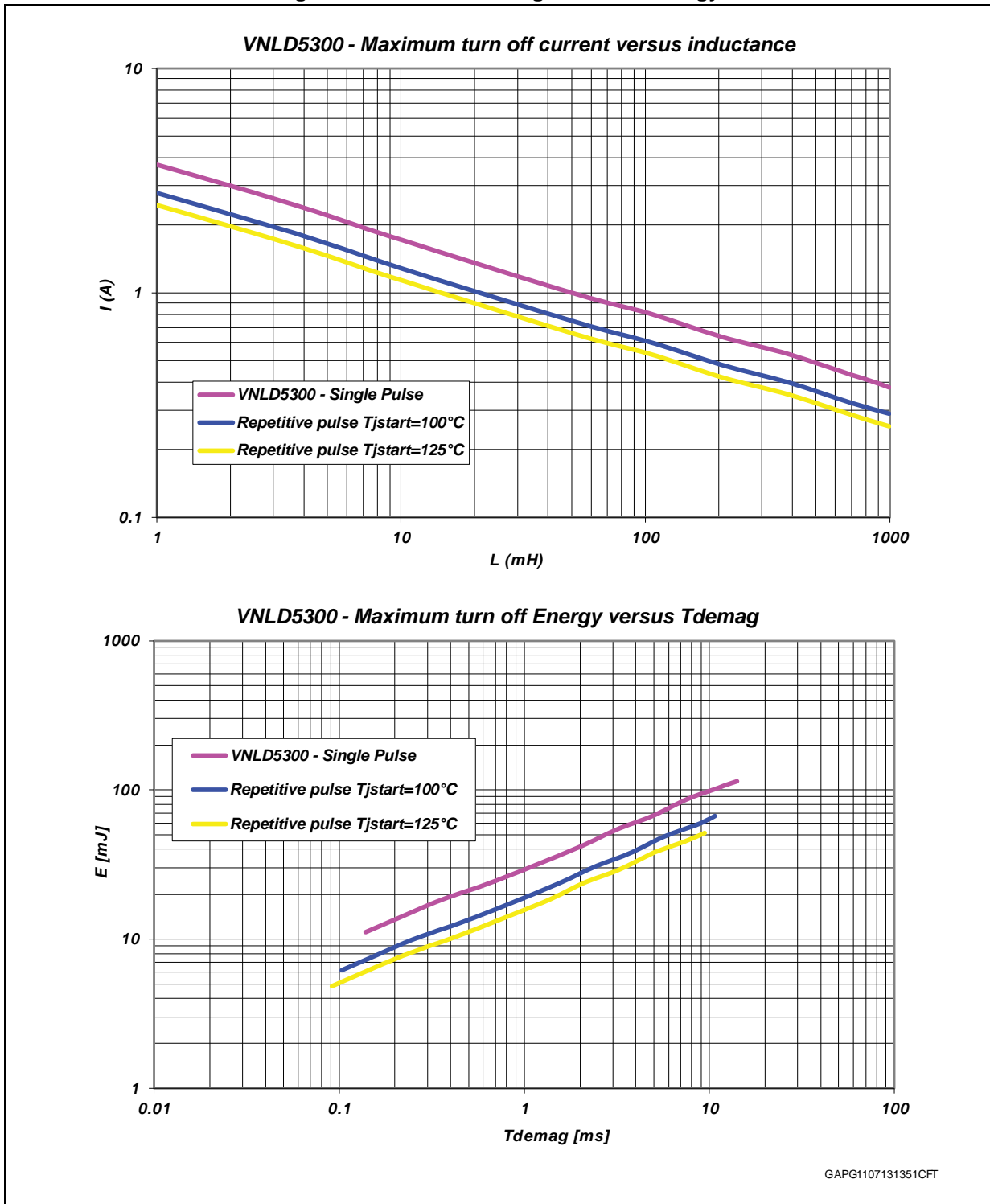
- $I_{latchup} \geq 20\ \text{mA}$
- $V_{OH\mu C} \geq 4.5\ \text{V}$
- $35\ \Omega \leq R_{prot} \leq 100\ \text{K}\Omega$

Then, the recommended value is $R_{prot} = 1\ \text{K}\Omega$

Figure 6 shows the turn-off current drawn during the demagnetization.

a. In case of negative transient on the drain pin.

Figure 6. Maximum demagnetization energy

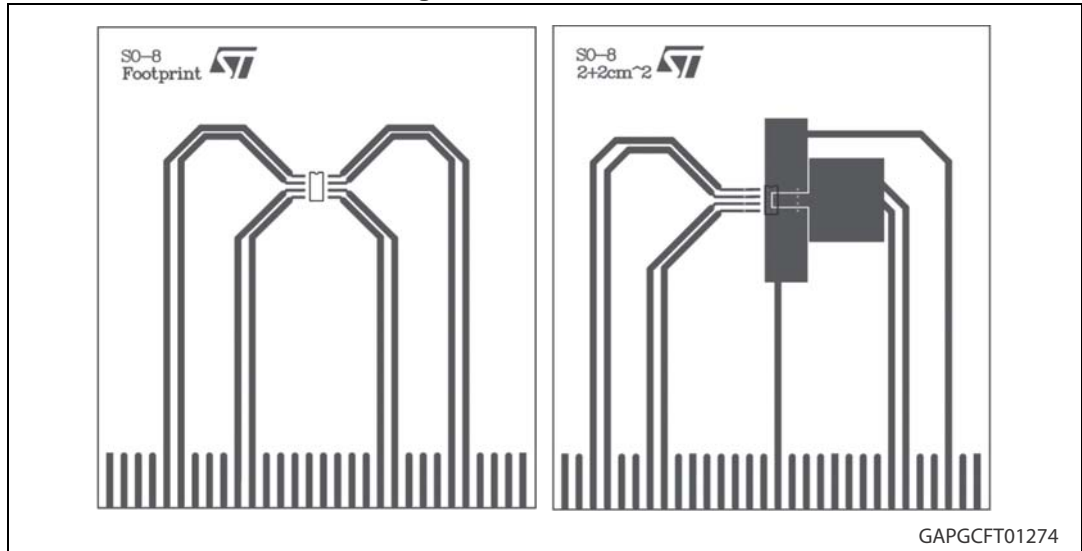


1. Values are generated with $R_L = 0\Omega$.
 In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 SO-8 thermal data

Figure 7. SO-8 PC board



1. Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 78 mm x 86 mm; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal via separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm).

Figure 8. $R_{thj-amb}$ vs PCB copper area in open box free air condition

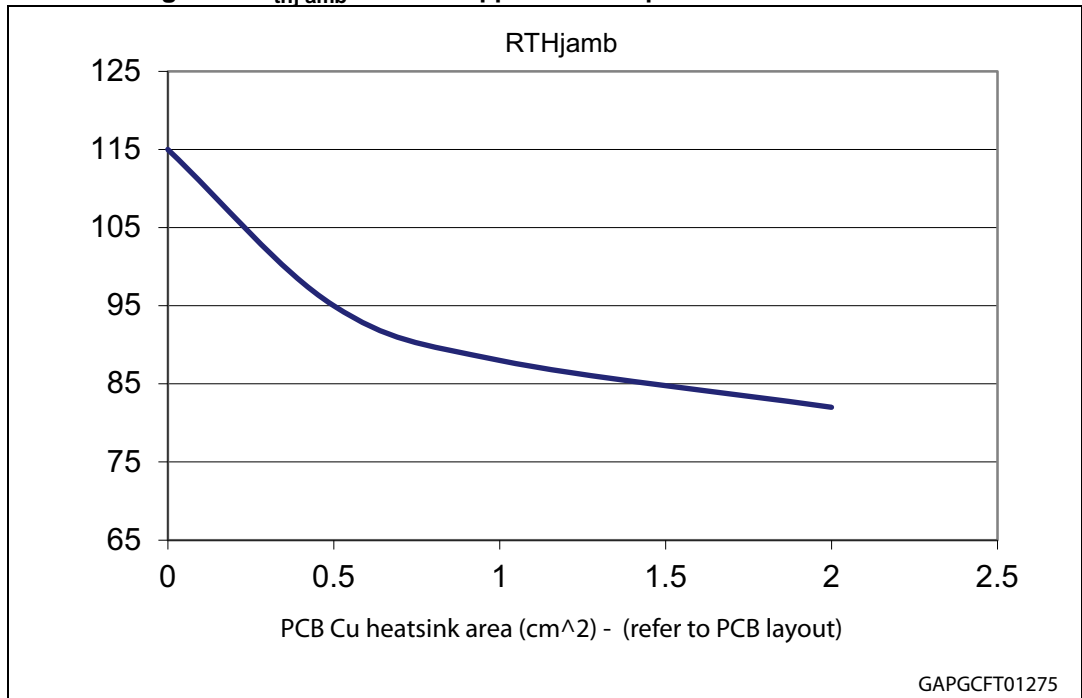
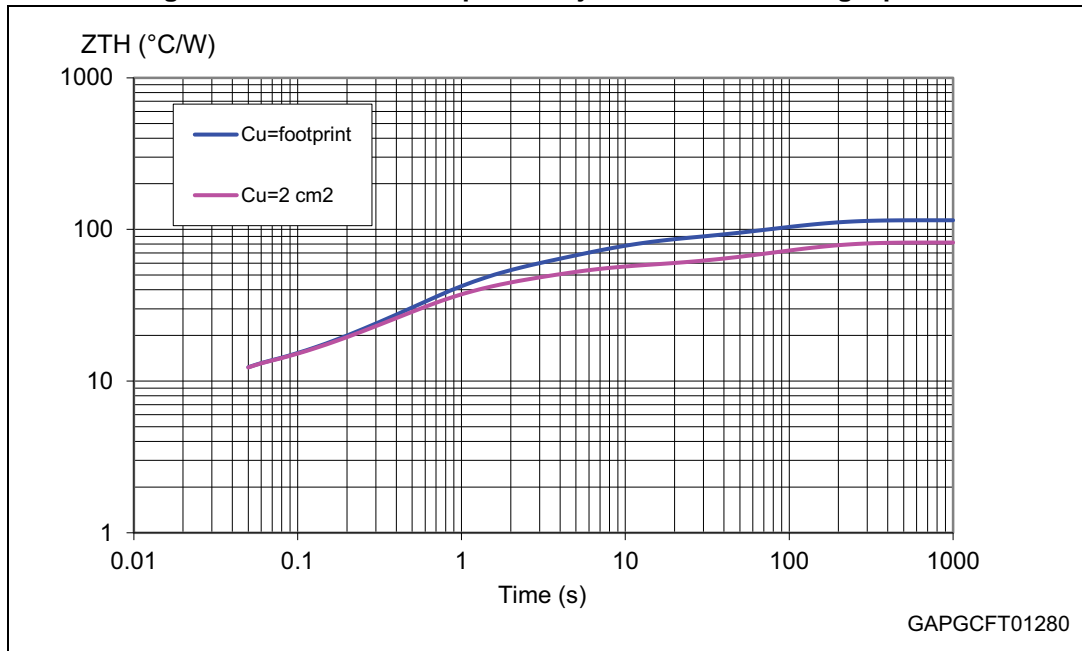


Figure 9. SO-8 thermal impedance junction ambient single pulse

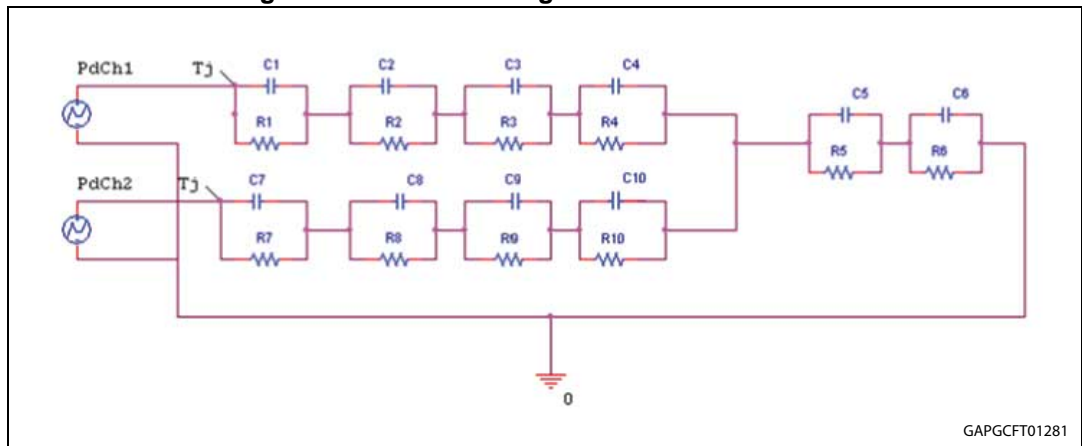


Equation 2:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 10. Thermal fitting model of a LSD in SO-8



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 13. Thermal parameters

| Area/island (cm ²) | Footprint | 2 |
|--------------------------------|-----------|---------|
| R1 = R7 (°C/W) | 2.8 | 2.8 |
| R2 = R8 (°C/W) | 3.7 | 3.7 |
| R3 = R9 (°C/W) | 3.5 | 3.5 |
| R4 = R10 (°C/W) | 34 | 25 |
| R5 (°C/W) | 36 | 20 |
| R6 (°C/W) | 35 | 27 |
| C1 = C7 (W.s/°C) | 0.00002 | 0.00002 |
| C2 = C8 (W.s/°C) | 0.001 | 0.001 |
| C3 = C9 (W.s/°C) | 0.005 | 0.005 |
| C4 = C10 (W.s/°C) | 0.02 | 0.02 |
| C5 (W.s/°C) | 0.15 | 0.15 |
| C6 (W.s/°C) | 2.5 | 3.5 |

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 SO-8 mechanical data

Figure 11. SO-8 package dimensions

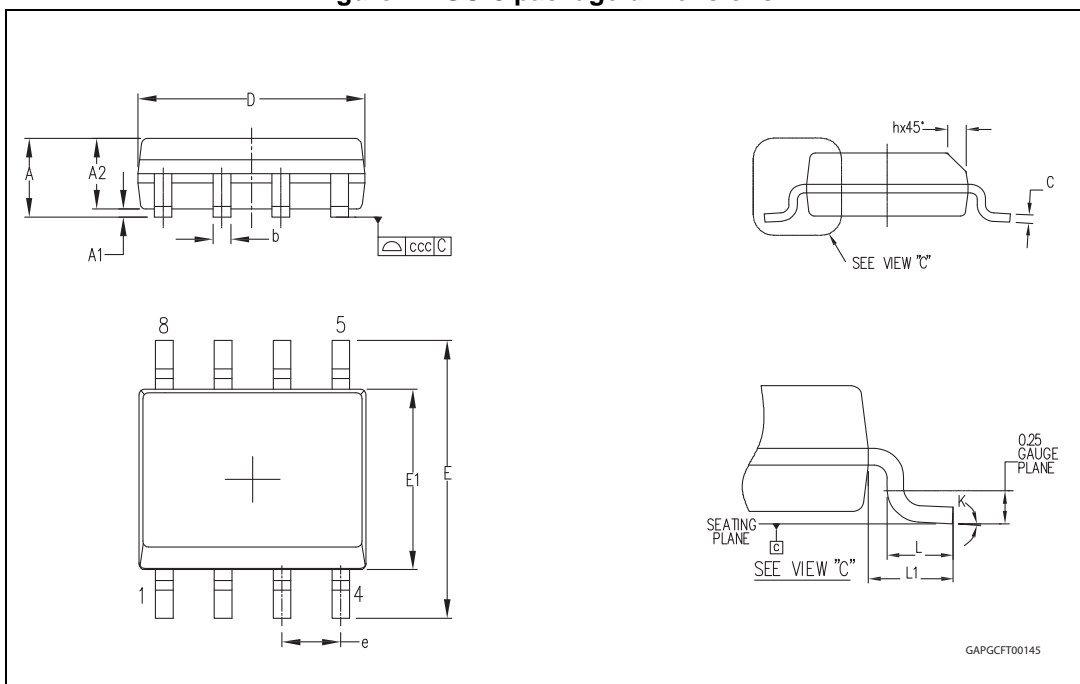


Table 14. SO-8 mechanical data

| Symbol | Millimeters | | |
|-------------------|-------------|------|------|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.28 | | 0.48 |
| c | 0.17 | | 0.23 |
| D ⁽¹⁾ | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 ⁽²⁾ | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | | 1.04 | |
| k | 0° | | 8° |
| ccc | | | 0.10 |

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

5.3 SO-8 packing information

Figure 12. SO-8 tube shipment (no suffix)

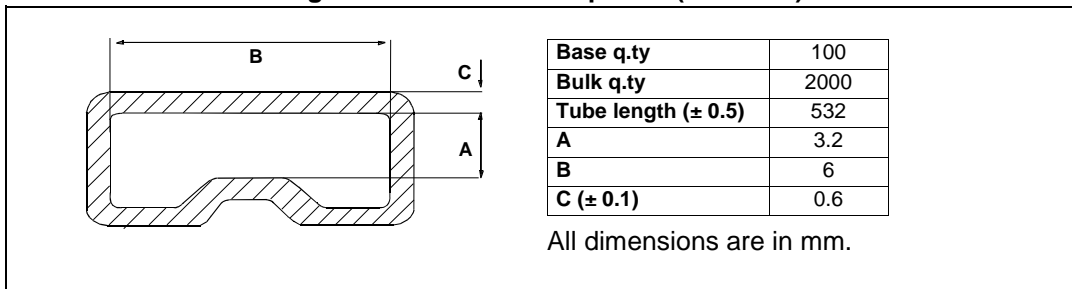
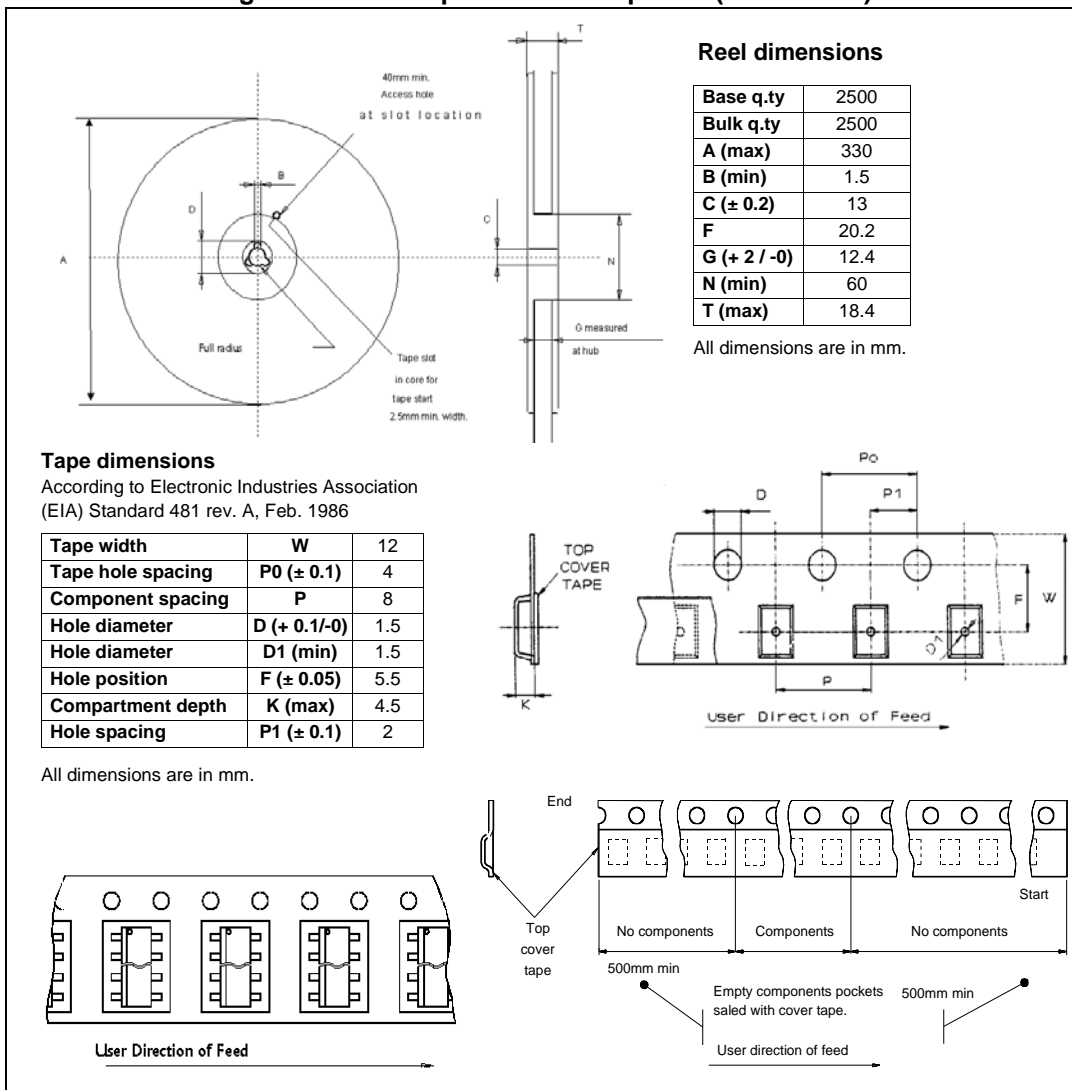


Figure 13. SO-8 tape and reel shipment (suffix “TR”)



6 Revision history

Table 15. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 28-Jun-2012 | 1 | Initial release. |
| 25-Mar-2013 | 2 | <p><i>Table 6: PowerMOS section:</i></p> <ul style="list-style-type: none"> – R_{ON}: added typical value, removed maximum value <p><i>Table 10: Switching characteristics:</i></p> <ul style="list-style-type: none"> – Updated typical values <p><i>Table 11: Protection and diagnostics:</i></p> <ul style="list-style-type: none"> – t_{dlimL}: updated typical value <p><i>Table 12: Truth table:</i></p> <ul style="list-style-type: none"> – Output voltage $< V_{OL}$: removed conditions |
| 05-Jun-2013 | 3 | <p><i>Table 5: Thermal data:</i></p> <ul style="list-style-type: none"> – $R_{thj-amb}$: updated value <p><i>Table 6: PowerMOS section:</i></p> <ul style="list-style-type: none"> – V_{CLAMP}: updated test conditions <p><i>Table 8: Input section:</i></p> <ul style="list-style-type: none"> – I_{ISS}: updated value <p>Updated <i>Section 3.1: MCU I/O protection</i></p> <p>Updated <i>Chapter 4: Package and PC board thermal data</i></p> |
| 18-Jul-2013 | 4 | <p><i>Table 4: Absolute maximum ratings:</i></p> <ul style="list-style-type: none"> – $-I_D$: updated value – E_{AS}: updated parameter value <p><i>Table 10: Switching characteristics:</i></p> <ul style="list-style-type: none"> – $t_{d(ON)}$, t_r, t_f, W_{ON}, W_{OFF}: updated typical values <p>Added <i>Figure 6: Maximum demagnetization energy</i></p> |
| 18-Sep-2013 | 5 | Updated disclaimer. |

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