APDS-9130
Digital Proximity Sensor

Data Sheet

Description

The APDS-9130 provides IR LED and a complete proximity detection system in a single 8 pin package. The proximity function offers plug and play detection to 100 mm (without front glass) thus eliminating the need for factory calibration of the end equipment or sub-assembly. The proximity detection feature operates well from bright sunlight to dark rooms. The wide dynamic range also allows for operation in short distance detection behind dark glass such as a cell phone.

The proximity function is targeted specifically towards near field proximity applications. In cell phones, the proximity detection can detect when the user positions the phone close to their ear. The device is fast enough to provide proximity information at a high repetition rate needed when answering a phone call. This provides both improved "green" power saving capability and the added security to lock the computer when the user is not present. The addition of the micro-optics lenses within the module, provide highly efficient transmission and reception of infrared energy which lowers overall power dissipation.

Ordering Information

Part Number	Packaging	Quantity
APDS-9130	Tape & Reel	2500 per reel
APDS-9130-140	Tape & Reel	1000 per reel
APDS-9130-200	Tape & Reel	1000 per reel

Features

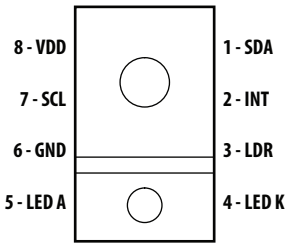
IR LED and Proximity Detector in an Optical Module

- Proximity Detection
  - Fully Calibrated to 100 mm Detection
  - Integrated IR LED and Synchronous LED Driver
  - Eliminates "Factory Calibration" of Prox
- Programmable Wait Timer
  - Wait State Power – 90 µA Typical
  - Programmable from 2.7 ms to > 8 sec
- I^2C Interface Compatible
  - Up to 400 kHz (I^2C Fast-Mode)
  - Dedicated Interrupt Pin
- Sleep Mode Power - 2.2 µA Typical
- Small Package L3.94 x W2.36 x H1.35 mm

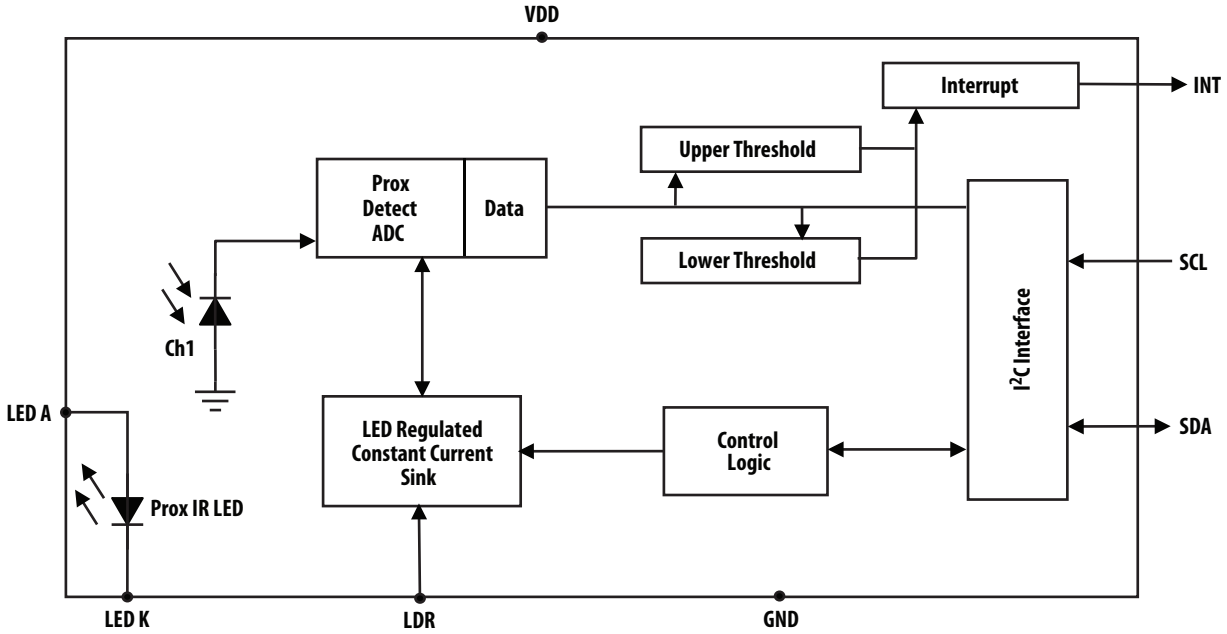
Applications

- Cell Phone Touch-screen Disable
- Notebook/Monitor Security
- Automatic Speakerphone Enable
- Automatic Menu Pop-up
- Digital Camera Eye Sensor

Package Diagram



Functional Block Diagram



Detailed Description

The APDS-9130 device provides on-chip Ch1 diode, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine and an I^2C interface. Each device has one Ch1 infrared-responding (IR) photodiode.

Communication to the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the APDS-9130 device is inherently more immune to noise when compared to an analog interface.

The APDS-9130 provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a proximity value. An interrupt is generated when the value of proximity conversion exceeds either an upper or lower threshold. Additionally, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for proximity.

Proximity detection is fully provided with an 850 nm IR LED. An internal LED driver (LDR) pin, is jumper connected to the LED cathode (LED K) to provide a factory calibrated proximity of 100 +/- 20 mm. This is accomplished with a proprietary current calibration technique that accounts for all variances in silicon, optics, package and most importantly IR LED output power. This will eliminate or greatly reduce the need for factory calibration that is required for most discrete proximity sensor solutions. While the APDS-9130 is factory calibrated at a given pulse count, the number of proximity LED pulses can be programmed from 1 to 255 pulses, which will allow greater proximity distances to be achieved. Each pulse has a 16 µs period.

I/O Pins Configuration

PIN	NAME	TYPE	DESCRIPTION
1	SDA	I/O	I^2C serial data I/O terminal – serial data I/O for I^2C.
2	INT	O	Interrupt – open drain.
3	LDR	I	LED driver for proximity emitter – up to 100 mA, open drain.
4	LEDK	O	LED Cathode, connect to LDR pin in most systems to use internal LED driver circuit
5	LEDA	I	LED Anode, connect to V_{BATT} on PCB
6	GND		Power supply ground. All voltages are referenced to GND.
7	SCL	I	I^2C serial clock input terminal – clock signal for I^2C serial data.
8	V_{DD}		Power Supply voltage.

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Parameter	Symbol	Min	Max	Units	Test Conditions
Power Supply voltage	V_{DD}		3.8	V	[1]
Digital voltage range		-0.5	3.8	V	
Digital output current	I_O	-1	20	mA	
Storage temperature range	Tstg	-40	85	°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note:

1. All voltages are with respect to GND.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating Ambient Temperature	T_A	-30		85	°C
Supply voltage	V_{DD}	2.2	3.0	3.6	V
Supply Voltage Accuracy, V_{DD} total error including transients		-3		+3	%
LED Supply Voltage	V_{BATT}	2.5		4.5	V

Operating Characteristics, V_{DD} = 3 V, T_A = 25° C (unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply current [1]	I_{DD}		195	250	µA	Active
			90			Wait Mode
			2.2	4.0		Sleep Mode
INT SDA output low voltage	V_{OL}	0		0.4	V	3 mA sink current
		0		0.6		6 mA sink current
Leakage current, SDA, SCL, INT Pins	I_{LEAK}	-5		5	µA	
Leakage current, LDR Pin	I_{LEAK}	-10		10	µA	
SCL, SDA input high voltage	V_{IH}	1.25		VDD	V	
SCL, SDA input low voltage	V_{IL}			0.54	V	

Note:
1. The power consumption is raised by the programmed amount of Proximity LED Drive during the 8 us the LED pulse is on. The nominal and maximum values are shown under Proximity Characteristics. There the I_{DD} supply current is I_{DD} Active + Proximity LED Drive programmed value.

Proximity Characteristics, V_{DD} = 3 V, T_A = 25° C, PGAIN = 1, PEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions	
I_{DD} Supply current – LDR Pulse On		3		mA		
ADC Conversion Time Step Size	2.58	2.73	2.9	ms	PTIME = 0xff	
ADC Number of Integration Steps		1		steps	PTIME = 0xff	
Full Scale ADC Counts			1023	counts	PTIME = 0xff	
Proximity IR LED Pulse Count	0		255	pulses		
Proximity Pulse Period		16.0		µs		
Proximity Pulse – LED On Time		7.3		µs		
Proximity LED Drive		100		mA	PDRIVE = 0	I_{SINK} Sink current @ 600 mV, LDR Pin
		50			PDRIVE = 1	
		25			PDRIVE = 2	
		12.5			PDRIVE = 3	
Proximity ADC count value, no object		100	200	counts	Dedicated power supply VBatt = 3 V LED driving 8 pulses, PDRIVE = 00, PGAIN = 10, open view (no glass) and no reflective object above the module. [1]	
Proximity ADC count value, 100 mm distance object	450	520	590	counts	Reflecting object – 73 mm x 83 mm Kodak 90% grey card, 100 mm distance, LED driving 8 pulses, PDRIVE = 00, PGAIN = 10, open view (no glass) above the module. Tested value is the average of 5 consecutive readings. [1]	

Note:
1. 100 mA and 8 pulses are the recommended driving conditions. For other driving conditions, contact Avago Field Sales.

IR LED Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Peak Wavelength, λ_P		850		nm	I_F = 20 mA
Spectrum Width, Half Power, $\Delta\lambda$		40		nm	I_F = 20 mA
Optical Rise Time, T_R		20		ns	I_F = 100 mA
Optical Fall Time, T_F		20		ns	I_F = 100 mA

Wait Characteristics, V_{DD} = 3 V, T_A = 25 °C, Gain = 16, WEN = 1 (unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Wait Step Size		2.73	2.9	ms	WTIME = 0×ff
Wait Number of Step	1		256	steps	

AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted) *

Parameter	Symbol	Min.	Max.	Unit
Clock frequency (I^2C-bus only)	f_{SCL}	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t_{HDSTA}	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	µs
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	µs
Data hold time	$t_{HD;DAT}$	60	–	ns
Data set-up time	$t_{SU;DAT}$	100	–	ns
LOW period of the SCL clock	t_{LOW}	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	–	µs
Clock/data fall time	t_f	20	300	ns
Clock/data rise time	t_r	20	300	ns
Input pin capacitance	C_i	–	10	pF

* Specified by design and characterization; not production tested.

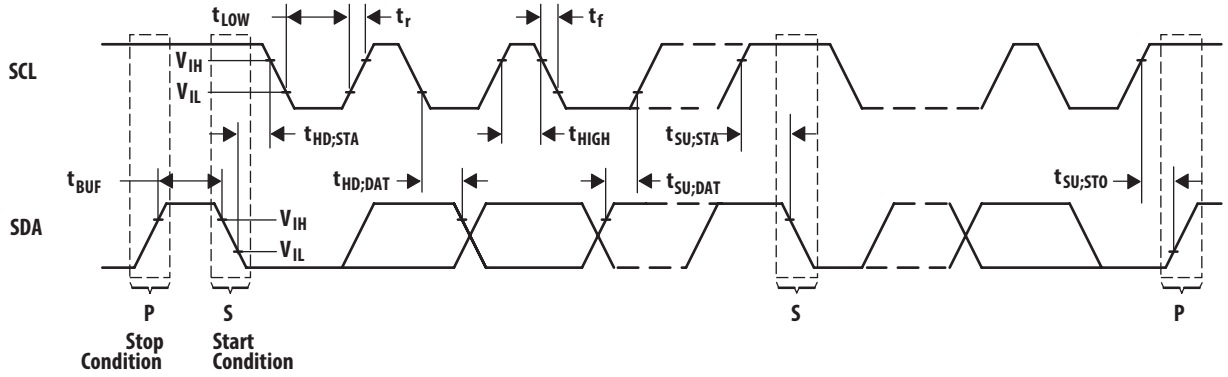


Figure 1. Timing Diagrams

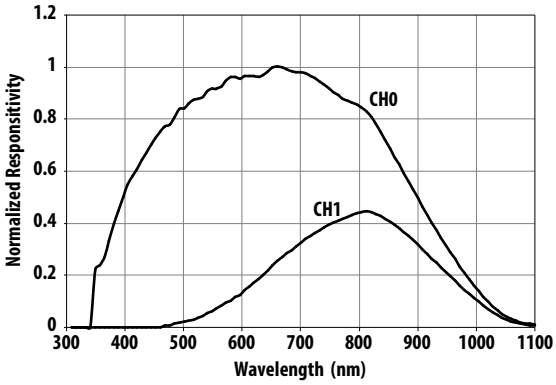


Figure 2. Spectral Response

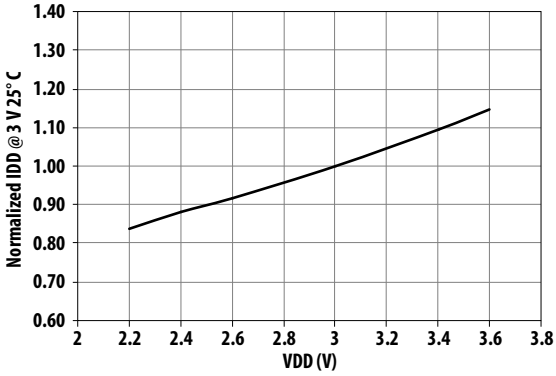


Figure 3a. Normalized IDD vs. VDD

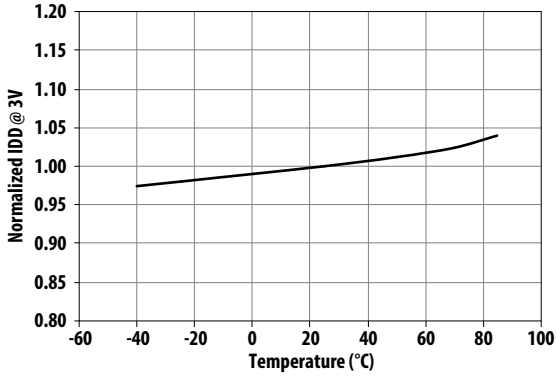


Figure 3b. Normalized IDD vs. Temperature

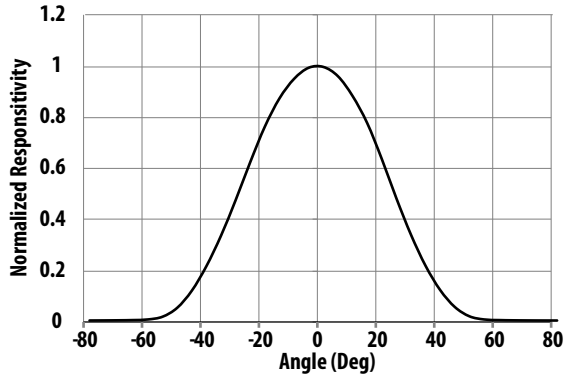


Figure 4a. Normalized PD Responsitivity vs. Angular Displacement

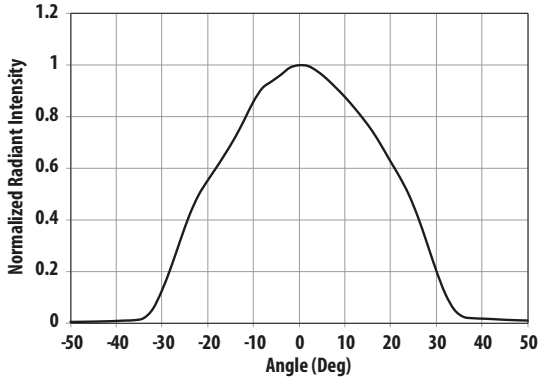


Figure 4b. Normalized LED Angular Emitting Profile

PRINCIPLES OF OPERATION

System State Machine

An internal state machine provides system control of the proximity detection, and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected on the I2C bus, the device transitions to the Idle state where it checks the Enable register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a proximity function is enabled. Once enabled, the device will execute the Prox and Wait states in sequence as indicated in Figure 5. Upon completion and return to Idle, the device will automatically begin a new prox–wait cycle as long as PON and PEN remain enabled.

If the Prox function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I2C command is received.

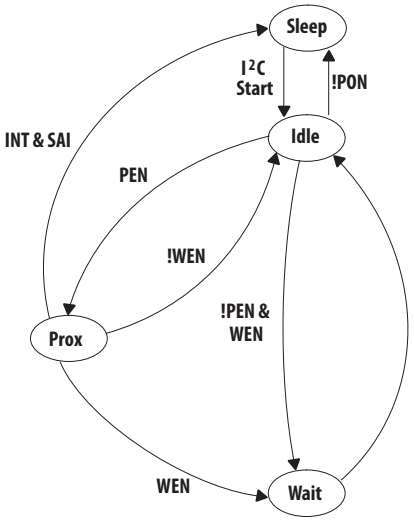


Figure 5. Simplified State Diagram

Proximity Detection

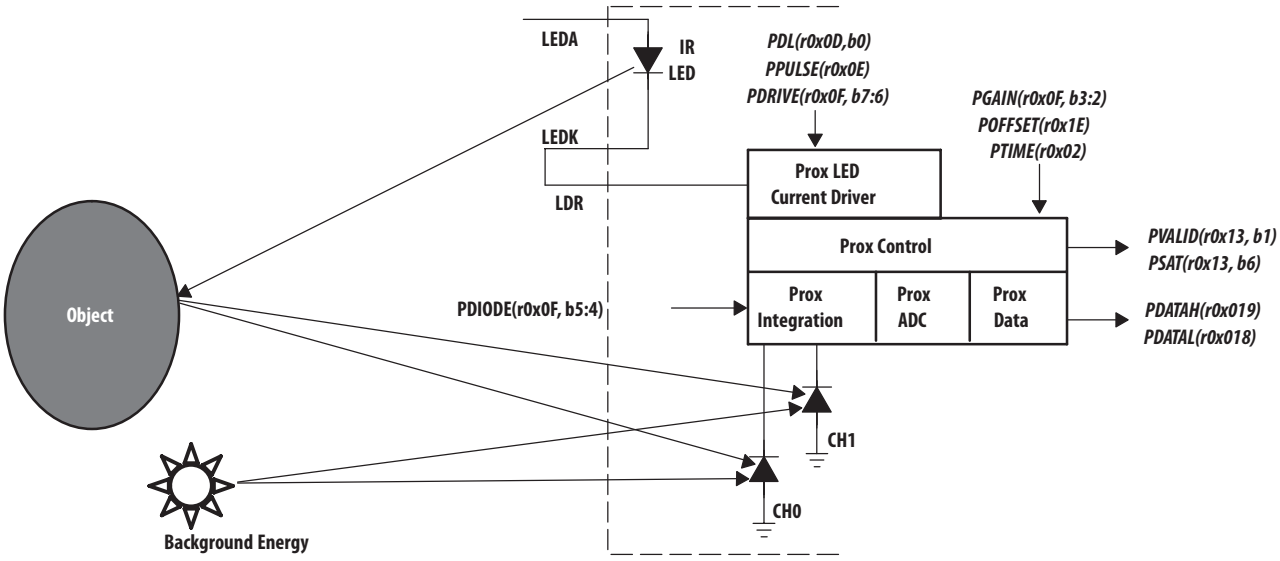


Figure 6. Proximity Detection

Proximity detection is accomplished by measuring the amount of IR energy, from the internal IR LED, reflected off an object to determine its distance. The internal proximity IR LED is driven by the integrated proximity LED current driver as shown in Figure 6.

The LED current driver, output on the LDR terminal, provides a regulated current sink that eliminates the need for an external current limiting resistor. The combination of proximity LED drive strength (PDRIVE) and proximity drive level (PDL) determine the drive current. PDRIVE sets the drive current to 100 mA, 50 mA, 25 mA, or 12.5 mA when PDL is not asserted. However, when PDL is asserted, the drive current is reduced by a factor of 9.

Referring to the Detailed State Machine figure, the LED current driver pulses the IR LED as shown in Figure 7 during the Prox Accum state. Figure 7 also illustrates that the LED On pulse has a fixed width of 7.3 µs and period of 16.0 µs. So, in addition to setting the proximity drive current, 1 to 255 proximity pulses (PPULSE) can be programmed. When deciding on the number of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of PPULSE.

Figure 6 illustrates light rays emitting from the internal IR LED, reflecting off an object, and being absorbed by the CH1 photodiodes. The proximity diode selector (PDIODE) selects Ch1 diode for a given proximity measurement. Note that PDIODE must be set for proximity detection to work.

Referring again to Figure 7, the reflected IR LED and the background energy is integrated during the LED On time, then during the LED Off time, the integrated background energy is subtracted from the LED On time energy, leaving the IR LED energy to accumulate from pulse to pulse. The proximity gain (PGAIN) determines the integration rate, which can be programmed to 1×, 2×, 4×, or 8× gain. At power up, PGAIN defaults to 1× gain, which is recommended for most applications. For reference, PGAIN equal to 4× is comparable to the APDS-9900's 1× gain setting. During LED On time integration, the proximity saturation bit in the Status register (0x13) will be set if the integrator saturates. This condition can occur if the proximity gain is set too high for the lighting conditions, such as in the presence of bright sunlight. Once asserted, PSAT will remain set until a special function proximity interrupt clear command is received from the host (see command register).

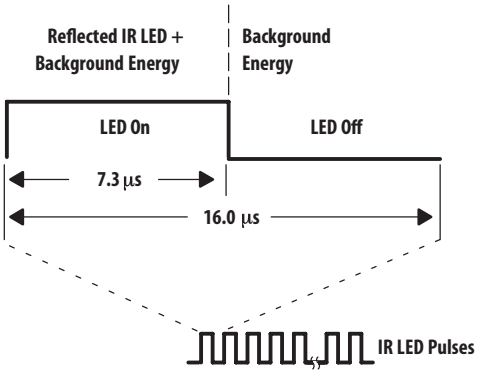


Figure 7. Proximity LED Current Driver Waveform

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. ADC scaling is controlled by the proximity ADC conversion time (PTIME) which is programmable from 1 to 256 2.73-ms time units. However, depending on the application, scaling the proximity data will equally scale any accumulated noise. Therefore, in general, it is recommended to leave PTIME at the default value of one 2.73 ms ADC conversion time (0xFF).

In many practical proximity applications, a number of optical system and environmental conditions can produce an offset in the proximity measurement result. To counter these effects, a proximity offset (POFFSET) is provided which allows the proximity data to be shifted positive or negative.

Once the first proximity cycle has completed, the proximity valid (PVALID) bit in the Status register will be set and remain set until the proximity detection function is disabled (PEN).

Optical Design Considerations

The APDS-9130 simplifies the optical system design by eliminating the need for light pipes and improves system optical efficiency by providing apertures and package shielding which will reduce crosstalk when placed in the final system. By reducing the IR LED to glass surface crosstalk, proximity performance is greatly improved and enables a wide range of cell phone applications utilizing the APDS-9130. The module package design has been optimized for minimum package foot print and short distance proximity of 100 mm typical. The spacing between the glass surface and package top surface is critical to controlling the crosstalk. If the package to top surface spacing gap, window thickness and transmittance are met, there should be no need to add additional components (such as a barrier) between the LED and photodiode. Thus with some simple mechanical design implementations, the APDS-9130 will perform well in the end equipment system.

APDS-9130 Module Optimized design parameters:

- Window thickness, t ≤ 1.0 mm
- Air gap, g ≤ 1.0 mm [1]
- Assuming window IR transmittance 90%

Note:
1. Applications with an air gap from 0.5 mm to 1.0 mm are recommended to use Poffset Register (0x1E) in their factory calibration.

The APDS-9130 is available in a low profile package that contains optics that provide optical gain on both the LED and the sensor side of the package. The device has a package Z height of 1.35 mm and will support an air gap of ≤ 1.0 mm between the glass and the package. The assumption of the optical system level design is that glass surface above the module is ≤ 1.0 mm.

By integrating the micro-optics in the package, the IR energy emitted can be reduced thus conserving the precious battery life in the application.

The system designer can optimize his designs for slim form factor Z height as well as improve the proximity sensing, save battery power, and disable the touch screen in a cellular phone.

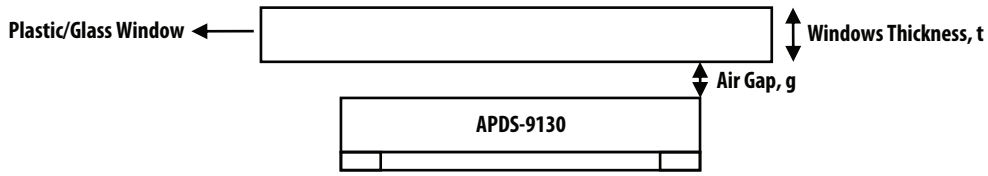


Figure 8. Proximity Detection

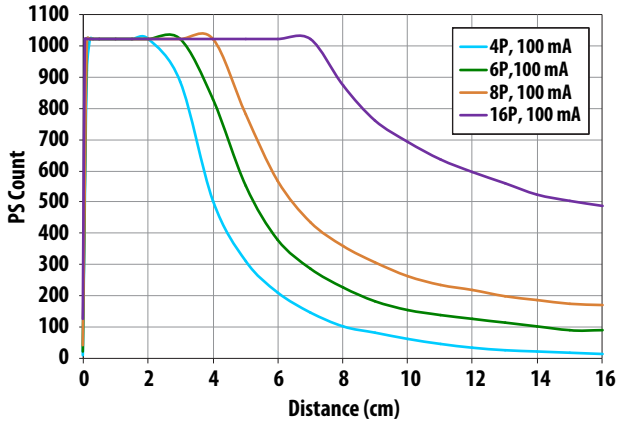


Figure 9a. PS Output vs. Distance at 100 mA, PGAIN = 10, at various Pulse Count. No glass in front of the module, 18% Kodak Grey Card.

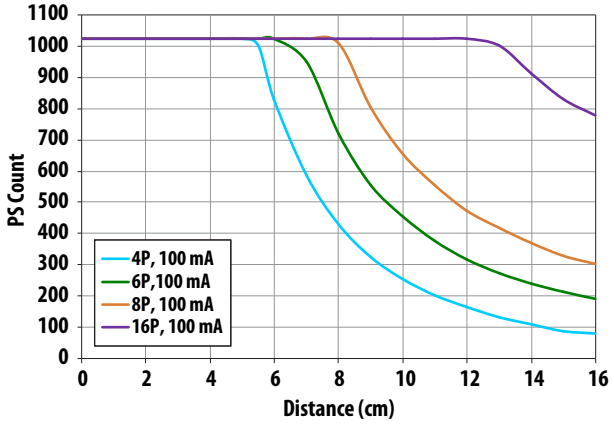


Figure 9b. PS Output vs. Distance at 100 mA, PGAIN = 10, at various Pulse Count. No glass in front of the module, 90% Kodak Grey Card.

Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for proximity values outside of a user-defined range. While the interrupt function is always enabled and its status is available in the status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) fields in the enable register (0x00).

Four 16-bit interrupt threshold registers allow the user to set limits below and above a desired proximity range. An out-of-range proximity interrupt can be generated when the proximity data (PDATA) falls below the proximity interrupt low threshold (PILTx) or exceeds the proximity interrupt high threshold (PIHTx).

It is important to note that the thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range proximity occurrences before an interrupt is generated. The persistence filter register (0x0C) allows the user to set the proximity persistence filter (PPERS) values. See the persistence filter register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see command register).

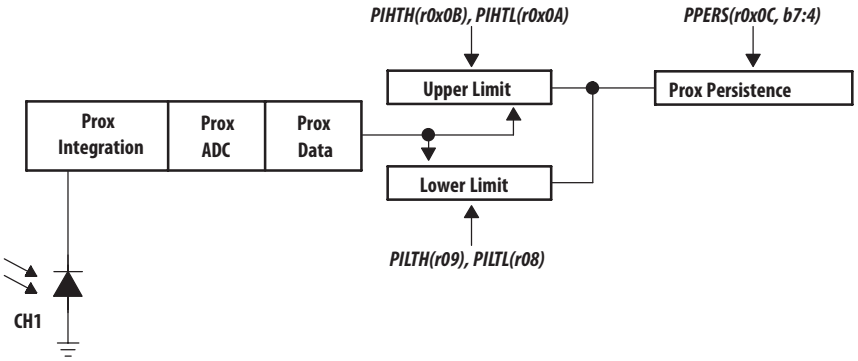


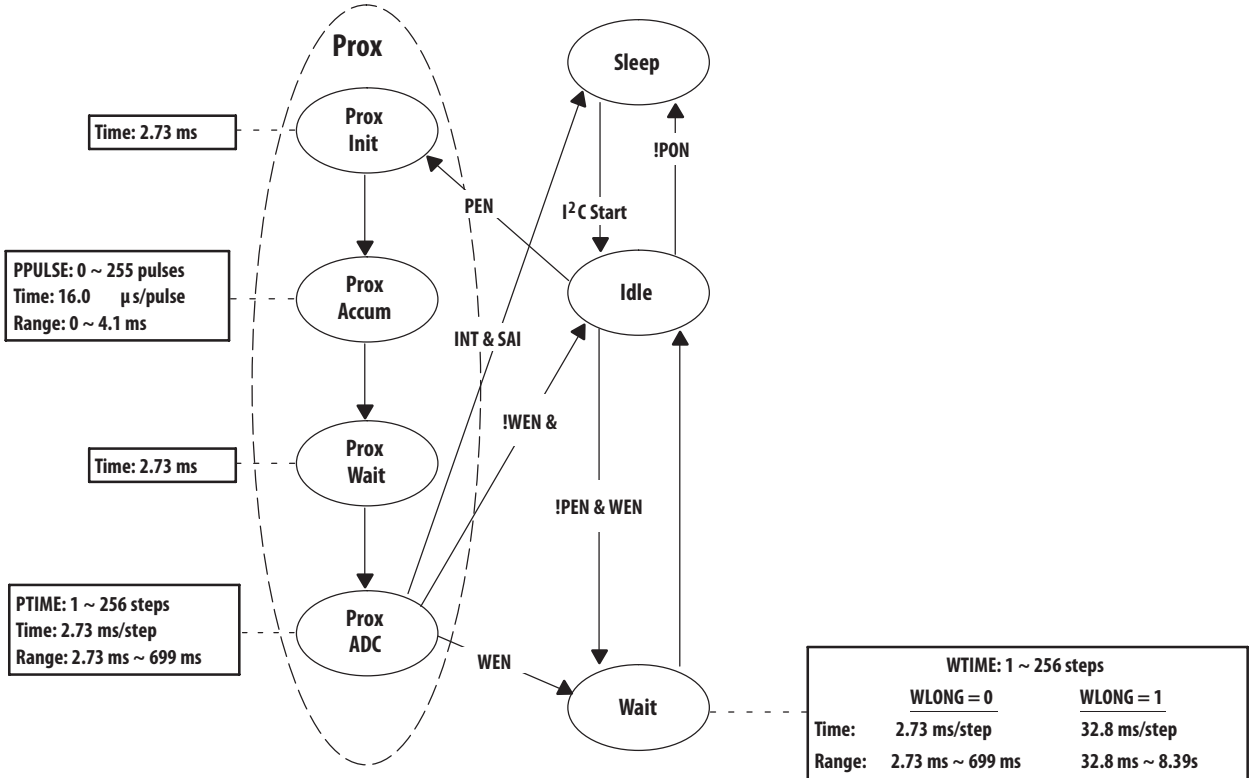
Figure 10. Programmable Interrupt

State Diagram

The system state machine shown in Figure 5 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features, which affect the state machine cycle time, and provides details to determine system level timing. Upon VDD power on, it is recommended to wait at least 4.5ms before issuing the I2C command.

When the proximity detection feature is enabled (PEN), the state machine transitions through the Prox Init, Prox Accum, Prox Wait, and Prox ADC states. The Prox Init and Prox Wait times are a fixed 2.73 ms, whereas the Prox Accum time is determined by the number of proximity LED pulses (PPULSE) and the Prox ADC time is determined by the integration time (PTIME). The formulas to determine the Prox Accum and Prox ADC times are given in the associated boxes in Figure 11. If an interrupt is generated as a result of the proximity cycle, it will be asserted at the end of the Prox ADC state and transition to the Sleep state if SAI is enabled.

When the power management feature is enabled (WEN), the state machine will transition in turn to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12× when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 11.



Note: PON, PEN, WEN, AEN, and SAI are fields in the Enable register (0x00).

Figure 11. Extended State Diagram

Power Management

Power consumption can be managed with the Wait state, because the Wait state typically consumes only 90 µA of IDD current. An example of the power management feature is given below. With the assumptions provided in the example, average IDD is estimated to be 157 µA.

Power Management

SYSTEM STATE MACHINE STATE	PROGRAMMABLE PARAMETER	PROGRAMMED VALUE	DURATION	TYPICAL CURRENT
Prox Init			2.73 ms	0.195 mA
Prox Accum	PPULSE	0x04	0.064 ms	
Prox Accum – LED On			0.029 ms (Note 1)	103 mA
Prox Accum – LED OFF			0.035 ms (Note 2)	0.195 mA
Prox Wait			2.73 ms	0.195 mA
Prox ADC	PTIME	0xFF	2.73 ms	0.195 mA
Wait	WTIME WLONG	0xEE 0	49.2 ms	0.090 mA

Notes:
1. Prox Accum – LED On time = 7.3 µs per pulse × 4 pulses = 29.3µs = 0.029 ms
2. Prox Accum – LED Off time = 8.7 µs per pulse × 4 pulses = 34.7µs = 0.035 ms

Average IDD Current = ((0.029 × 103) + (0.035 x 0.195) + (2.73 × 0.195) + (49.2 × 0.195) + (2.73 × 0.195 × 2)) / 57 = 157 µA

Keeping with the same programmed values as the example, the table below shows how the average IDD current is affected by the Wait state time, which is determined by WEN, WTIME, and WLONG. Note that the worst-case current occurs when the Wait state is not enabled.

Average IDD Current

WEN	WTIME	WLONG	WAIT STATE	AVERAGE IDD CURRENT
0	n/a	n/a	0 ms	557 µA
1	0xFF	0	2.73 ms	441 µA
1	0xEE	0	49.2 ms	157 µA
1	0x00	0	699 ms	96 µA
1	0x00	1	8389 ms	91 µA

Basic Software Operation

The following pseudo-code shows how to do basic initialization of the APDS-9130.

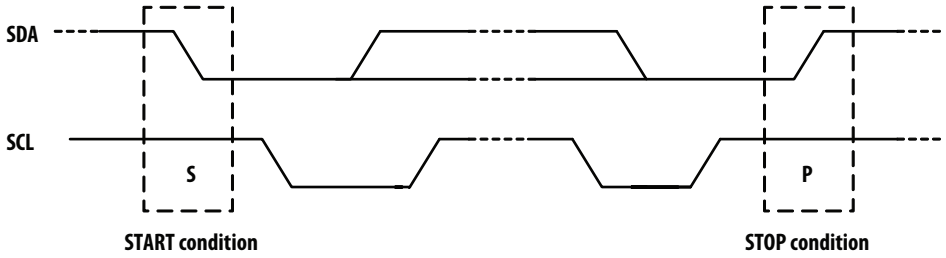
```
uint8 PIME, WTIME, PPULSE;
WTIME = 0xff; // 2.7 ms – minimum Wait time
PTIME = 0xff; // 2.7 ms – minimum Prox integration time
PPULSE = 1; // Minimum prox pulse count

WriteRegData(0, 0); //Disable and Powerdown
WriteRegData (2, PTIME);
WriteRegData (3, WTIME);
WriteRegData (0xe, PPULSE);

uint8 PDRIVE, PDIODE, PGAIN;
PDRIVE = 0; //100mA of LED Power
PDIODE = 0x20; // CH1 Diode
PGAIN = 0; //1x Prox gain
WriteRegData (0xf, PDRIVE | PDIODE | PGAIN);

uint8 WEN, PEN, PON;
WEN = 8; // Enable Wait
PEN = 4; // Enable Prox
PON = 1; // Enable Power On
WriteRegData (0, WEN | PEN | PON); // WriteRegData(0,0x0f);

Wait(12); //Wait for 12 ms

int CH0_data, CH1_data, Prox_data;

CH0_data = Read_Word(0x14);
CH1_data = Read_Word(0x16);
Prox_data = Read_Word(0x18);

WriteRegData(uint8 reg, uint8 data)
{
        m_I2CBus.WriteI2C(0x39, 0x80 | reg, 1, &data);
}

uint16 Read_Word(uint8 reg);
{
        uint8 barr[2];
        m_I2CBus.ReadI2C(0x39, 0xA0 | reg, 2, ref barr);
        return (uint16)(barr[0] + 256 * barr[1]);
}
```

I²C Protocol

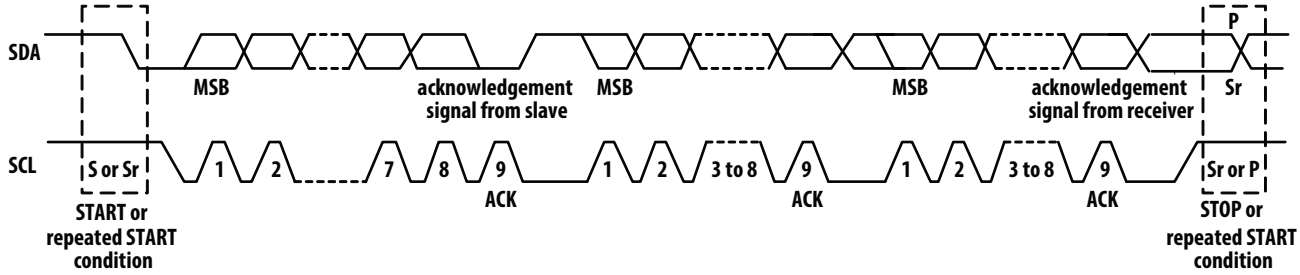
Interface and control of the APDS-9130 is accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0x39 hex using 7 bit addressing protocol. (Contact factory for other addressing options.)

The I²C standard provides for three types of bus transaction: read, write and a combined protocol. During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5 bit register address. The control commands can also be used to clear interrupts. For a complete description of I²C protocols, please review the I²C Specification at: http://www.NXP.com

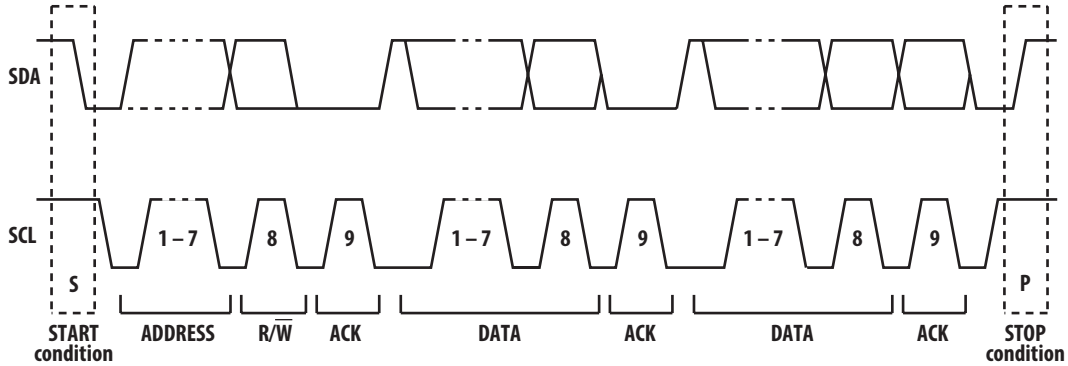
Start and Stop conditions



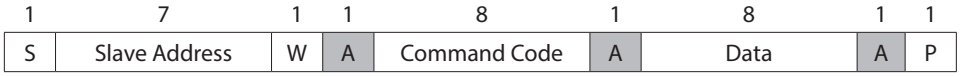
Data transfer on I²C-bus



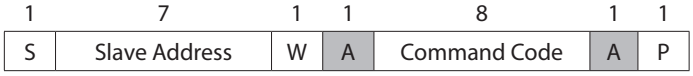
A complete data transfer



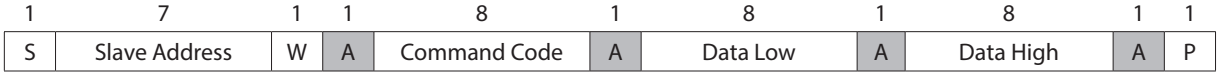
A	Acknowledge (0)
N	Not Acknowledged (1)
P	Stop Condition
R	Read (1)
S	Start Condition
Sr	Repeated Start Condition
W	Write (0)
…	Continuation of protocol
☐	Master-to-Slave
▒	Slave-to-Master



I²C Write Protocol

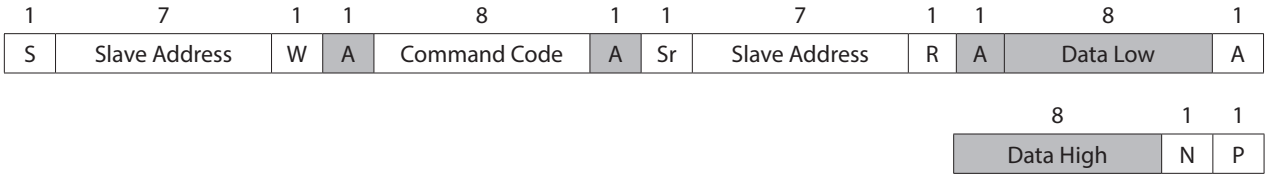


I²C Write Protocol (Clear Interrupt)



I²C Write Word Protocol

I²C Read Protocol – Combined Format



I²C Read Word Protocol

Register Set

The APDS-9130 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

ADDRESS	RESISTER NAME	R/W	REGISTER FUNCTION	Reset Value
–	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enable of states and interrupts	0x00
0x02	PTIME	R/W	Proximity ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold hi byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt hi threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt hi threshold hi byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPULSE	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Gain control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x18	PDATAL	R	Proximity ADC low data register	0x00
0x19	PDATAH	R	Proximity ADC high data register	0x00
0x1E	POFFSET	R/W	Proximity offset register	- -

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I²C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

	7	6	5	4	3	2	1	0	
COMMAND	CMD	TYPE		ADD					–

FIELD	BITS	DESCRIPTION	
COMMAND	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**INTEGRATION TIME**
		00	Repeated Byte protocol transaction
		01	Auto-Increment protocol transaction
		10	Reserved – Do not use
		11	Special function – See description below
		Byte protocol will repeatedly read the same register with each data access. Block protocol will provide auto-increment function to read successive bytes.	
ADD	4:0	Address register/special function register. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write or read transactions:	
		FIELD VALUE	**READ VALUE**
		00000	Normal – no action
		00101	Proximity interrupt clear
		00110	Reserved - Do not write
		00111	Proximity interrupt clear
		other	Reserved – Do not write
		Proximity Interrupt Clear. Clears any pending Proximity interrupt. This special function is self clearing.	

Enable Register (0x00)

The ENABLE register is used primarily to power the APDS-9130 device on/off, enable functions, and interrupts.

	7	6	5	4	3	2	1	0	Address
ENABLE	Reserved	SAI	PIEN	Reserved	WEN	PEN	Reserved	PON	0x00

FIELD	BITS	DESCRIPTION
Reserved	7	Reserved. Write as 0.
SAI	6	Sleep after interrupt. When asserted, the device will power down at the end of a proximity cycle if an interrupt has been generated.
PIEN	5	Proximity Interrupt Mask. When asserted, permits proximity interrupts to be generated.
Reserved	4	Reserved. Write as 0
WEN	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity Enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
Reserved	1	Reserved. Write as 0
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

Proximity Time Control Register (0x02)

The proximity timing register controls the integration time of the proximity ADC in 2.73 ms increments. It is recommended that this register be programmed to a value of 0xff (1 cycle, 1023 bits).

FIELD	BITS	DESCRIPTION			
PTIME	7:0	VALUE	CYCLES	TIME	Max Count
		0xff	1	2.73 ms	1023

Wait Time Register (0x03)

Wait time is set 2.73 ms increments unless the WLONG bit is asserted in which case the wait times are 12x longer. WTIME is programmed as a 2's complement number.

FIELD	BITS	DESCRIPTION			
WTIME	7:0	REGISTER VALUE	WALL TIME	TIME (WLONG = 0)	TIME (WLONG = 1)
		0xff	1	2.73 ms	0.033 sec
		0xb6	74	202 ms	2.4 sec
		0x00	256	699 ms	8.4 sec

Note. The Proximity Wait Time Register should be configured before PEN and/or AEN is/are asserted.

Proximity Interrupt Threshold Register (0x08 – 0x0B)

The proximity interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity ADC channel low threshold lower byte
PILTH	0x09	7:0	Proximity ADC channel low threshold upper byte
PIHTL	0x0A	7:0	Proximity ADC channel high threshold lower byte
PIHTH	0x0B	7:0	Proximity ADC channel high threshold upper byte

Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time.

	7	6	5	4	3	2	1	0	
PERS	PPERS				Reserved				0x0c

FIELD	BITS	DESCRIPTION		
PPERS	7:4	Proximity interrupt persistence. Controls rate of proximity interrupt to the host processor.		
		FIELD VALUE	**MEANING**	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every	Every proximity cycle generates an interrupt
		0001	1	1 consecutive proximity values out of range
		…	…	…
		1111	15	15 consecutive proximity values out of range
Reserved.	3:0	Reserved. Write as 0		

Configuration Register (0x0D)

The configuration register sets the proximity LED drive level and wait long time.

	7	6	5	4	3	2	1	0	
CONFIG	Reserved					Reserved	WLONG	PDL	0x0D

FIELD	BITS	DESCRIPTION
Reserved	7:3	Reserved. Write as 0.
Reserved	2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12x from that programmed in the WTIME register.
PDL	0	Proximity drive level. When asserted, the proximity LDR drive current is reduced by 9.

Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that the LDR pin will generate during the Prox Accum state. The pulses are generated at a 62.5 kHz rate. 100 mA and 8 pulses are the recommended driving conditions. For other driving conditions, contact Avago Field Sales.

	7	6	5	4	3	2	1	0	
PPULSE	PPULSE								0x0E

FIELD	BITS	DESCRIPTION
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

	7	6	5	4	3	2	1	0	
CONTROL	PDRIVE		PDIODE		PGAIN		Reserved		0x0F

FIELD	BITS	DESCRIPTION		
PDRIVE	7:6	LED Drive Strength.		
		FIELD VALUE	**LED STRENGTH — PDL = 0**	**LED STRENGTH — PDL = 1**
		00	100 mA	11.1 mA
		01	50 mA	5.6 mA
		10	25 mA	2.8 mA
		11	12.5 mA	1.4 mA
PDIODE	5:4	Proximity Diode Select.		
		FIELD VALUE	**DIODE SELECTION**	
		00	Reserved	
		01	Reserved	
		10	Proximity uses the Ch1 diode	
		11	Reserved	
PGAIN	3:2	Proximity Gain Control.		
		FIELD VALUE	**Proximity GAIN VALUE**	
		00	1X Gain	
		01	2X Gain	
		10	4X Gain	
		11	8X Gain	
Reserved	1:0	Reserved. Write as 0		

Device ID Register (0x12)

The ID register provides the value for the part number. The ID register is a read-only register.

	7	6	5	4	3	2	1	0	
ID	Device ID								0x12

FIELD	BITS	DESCRIPTION
ID	7:0	Part number identification
		0x39 = APDS-9130

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

	7	6	5	4	3	2	1	0	
STATUS	Reserved	PSAT	PINT	Reserved	Reserved	Reserved	PVALID	Reserved	0x13

FIELD	BITS	DESCRIPTION
Reserved	7	Reserved.
PSAT	6	Proximity Saturation. Indicates that the proximity measurement is saturated
PINT	5	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.
Reserved	4	Reserved.
Reserved	3:2	Reserved.
PVALID	1	PS Valid. Indicates that the PS has completed an integration cycle.
Reserved	0	Reserved.

Proximity DATA Register (0x18 – 0x19)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two byte read I^2C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

Proximity Offset Register (0x1E)

The 8-bit proximity offset register provides compensation for proximity offsets caused by device variations, optical crosstalk, and other environmental factors. Proximity offset is a sign-magnitude value where the sign bit, bit 7, determines if the offset is negative (bit 7 = 0) or positive (bit 7 = 1). The magnitude of the offset compensation depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE). Because a number of environmental factors contribute to proximity offset, this register is best suited for use in an adaptive closed-loop control system.

	7	6	5	4	3	2	1	0	Address
POFFSET	SIGN	MAGINITUDE							0x1E

FIELD	BITS	DESCRIPTION
SIGN	7	Proximity Offset Sign. The offset sign shifts the proximity data negative when equal to 0 and positive when equal to 1.
MAGNITUDE	6:0	Proximity Offset Magnitude. The offset magnitude shifts the proximity data positive or negative, depending on the proximity offset sign. The actual amount of the shift depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE).

Application Information: Hardware

In a proximity sensing system, the included IR LED can be pulsed with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Averaging of multiple proximity samples is recommended to reduce the proximity noise.

The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LEDA pin, the key goal can be met. Place a 1 µF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LEDA pin, and at least 10 µF of bulk capacitance to supply the 100 mA current surge. This may be distributed as two 4.7 µF capacitors.

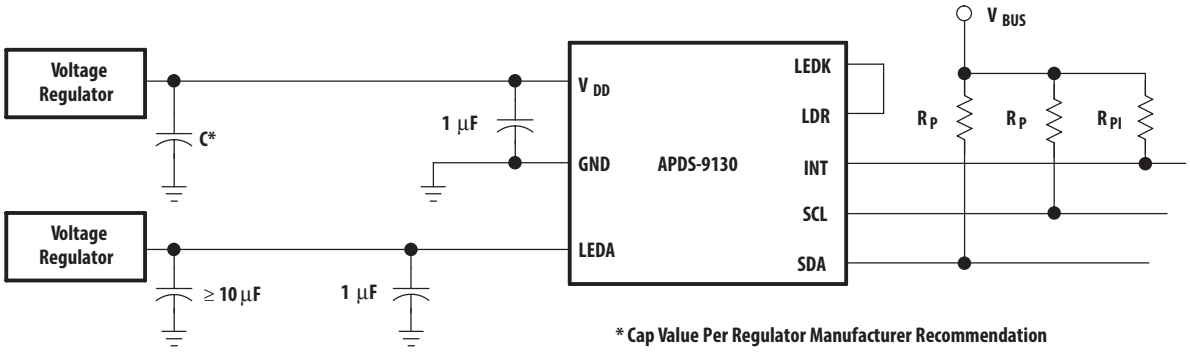


Figure 12a. Proximity Sensing Using Separate Power Supplies

If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22 Ω resistor in series with the V_{DD} supply line and a 1 µF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

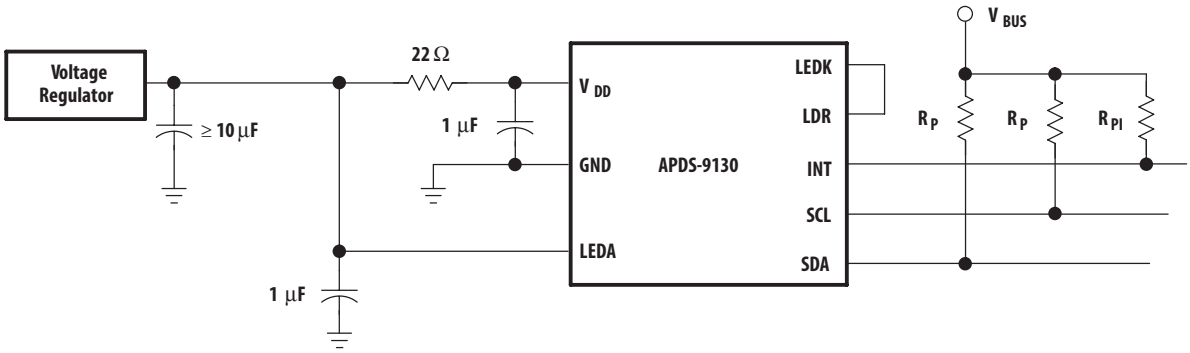
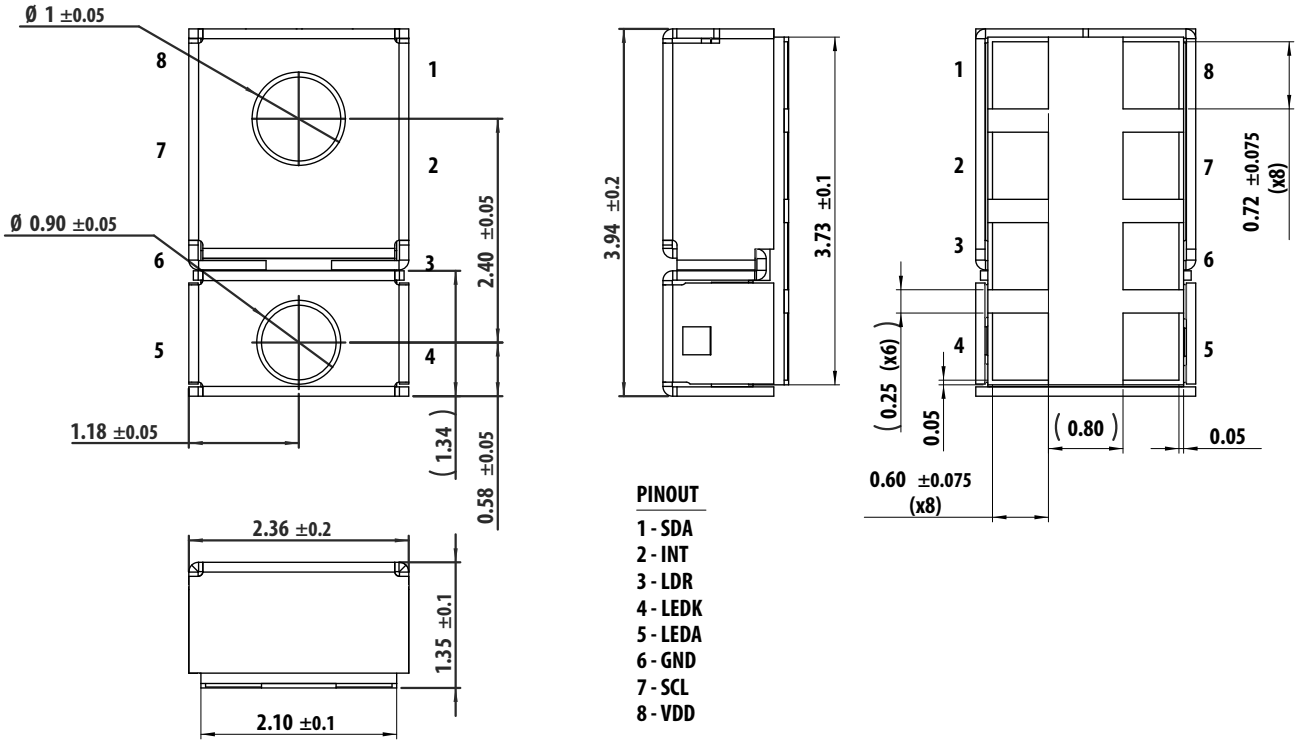


Figure 12b. Proximity Sensing Using Single Power Supply

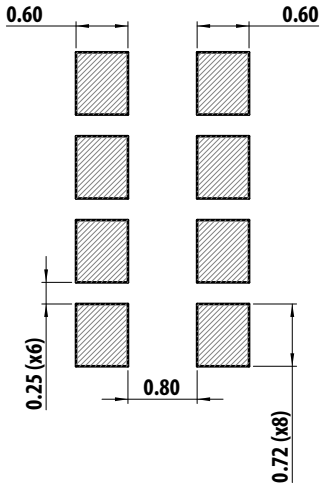
V_{BUS} in the above figures refers to the I²C bus voltage. The I²C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (R_P) value is a function of the I²C bus speed, the I²C bus voltage, and the capacitive load. A 10 kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

Package Outline Dimensions



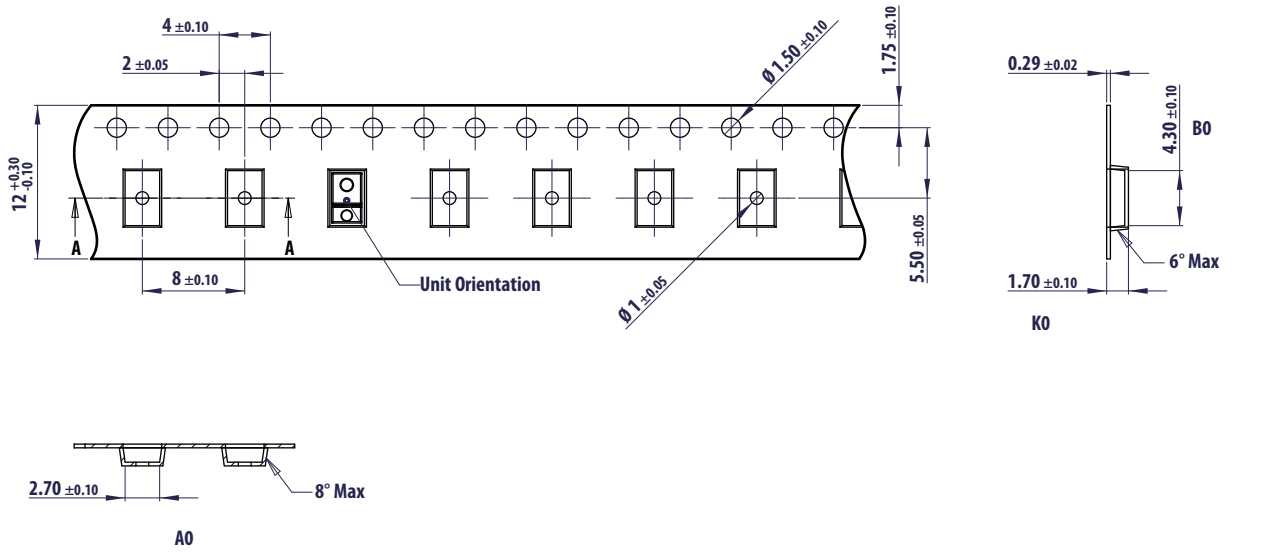
PCB Pad Layout

Suggested PCB pad layout guidelines for the Dual Flat No-Lead surface mount package are shown below.



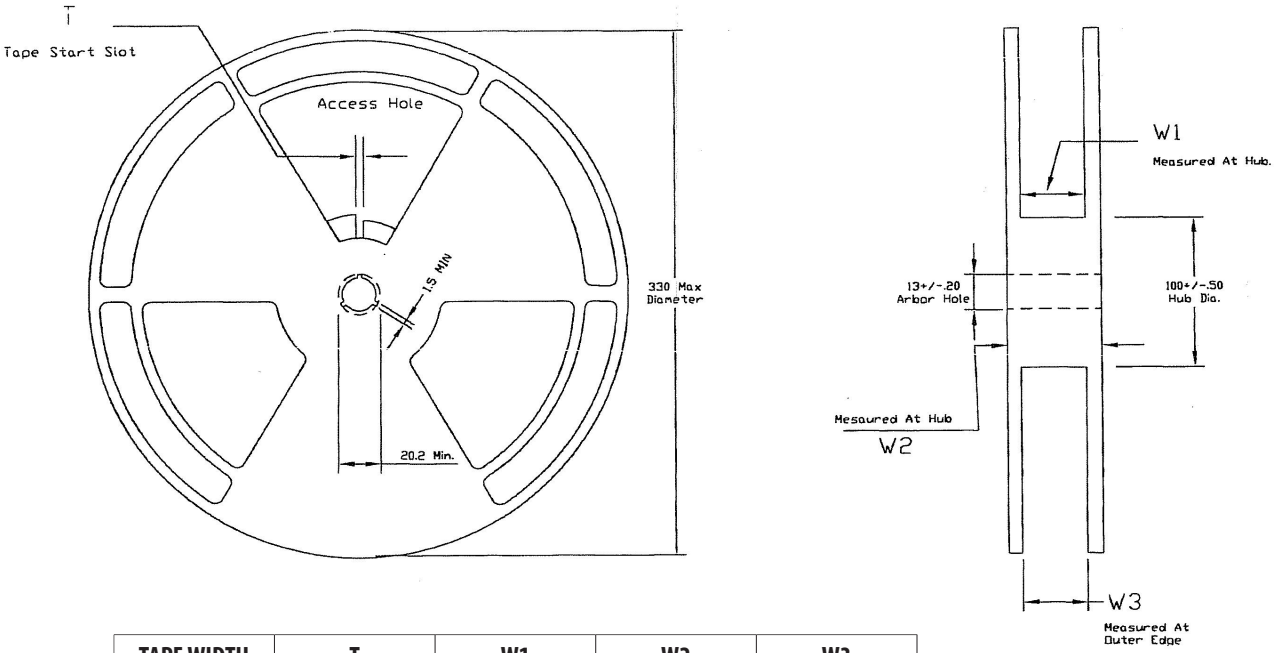
Notes: all linear dimensions are in mm.

Tape Dimensions



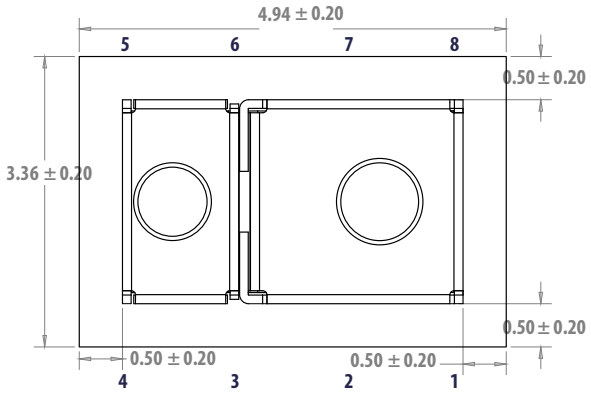
All dimensions unit: mm

Reel Dimensions

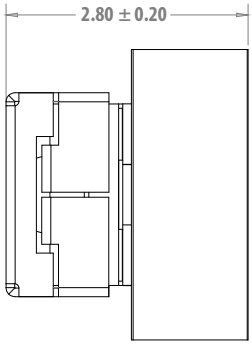


TAPE WIDTH	T	W1	W2	W3
12MM	4+/- .50	12.4 + 2.0 - 0.0	18.4 MAX	11.9 MIN 15.4 MAX

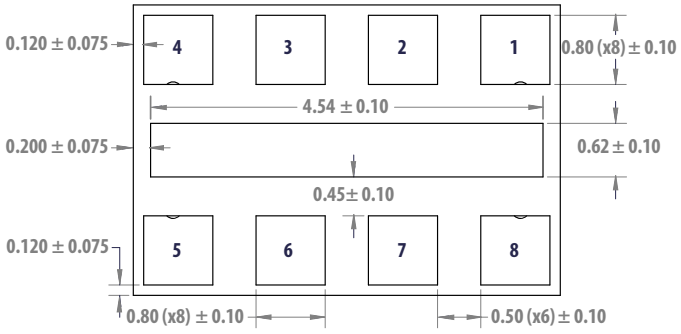
Package Outline Dimensions for Option -140



Top View

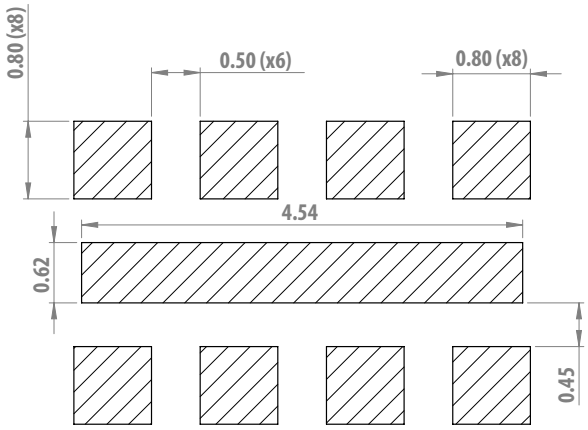


Side View

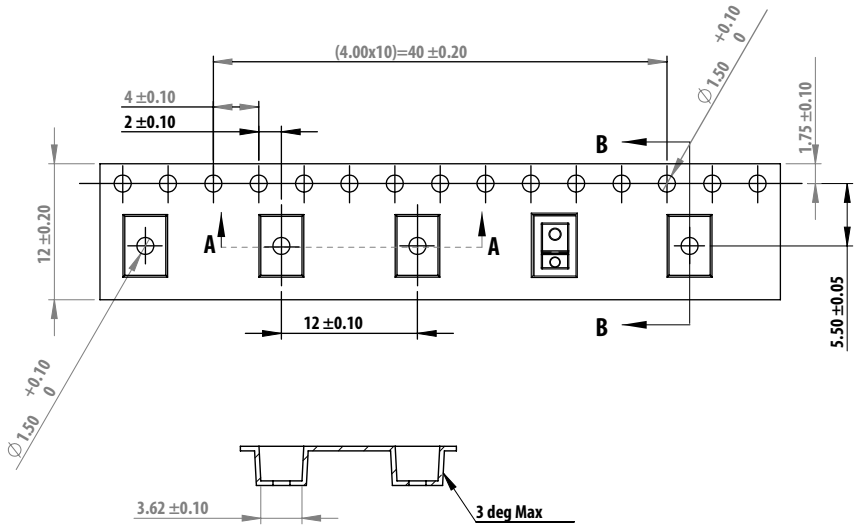


Bottom View

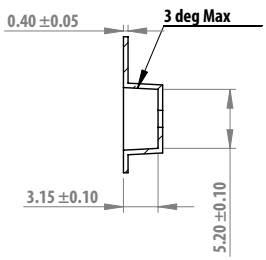
PCB Pad Layout for Option -140



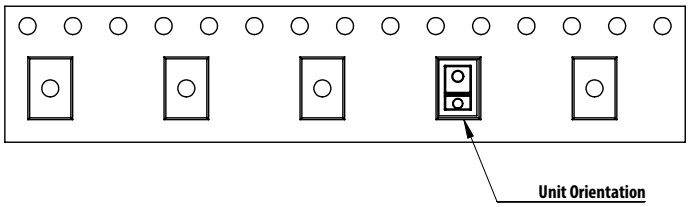
Tape Dimensions for Option -140



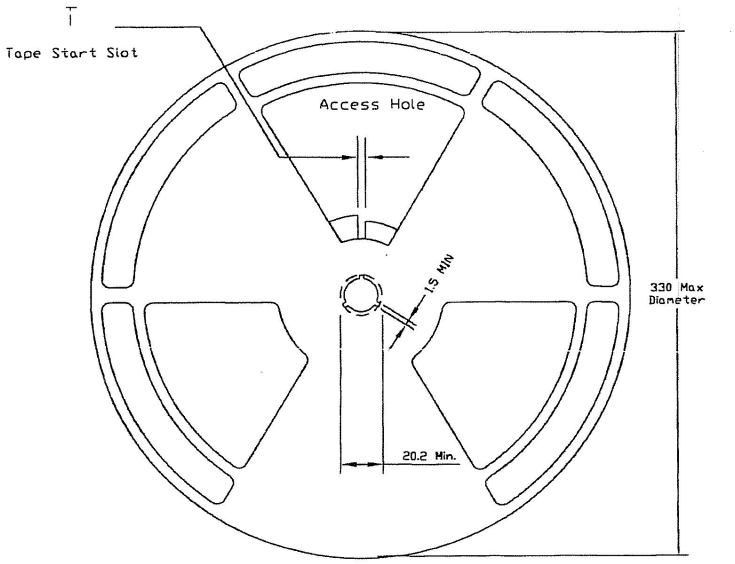
SECTION A-A

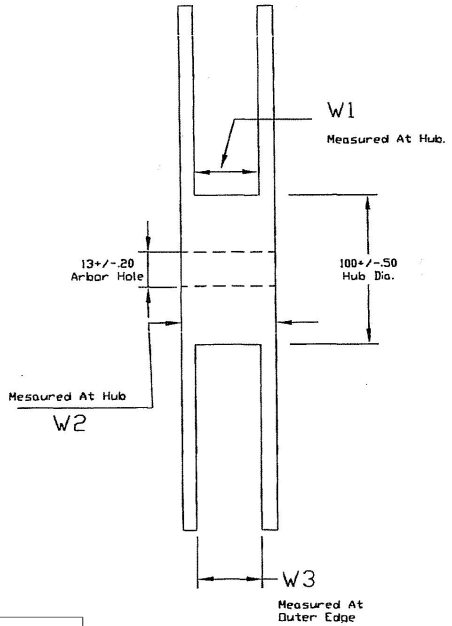


SECTION B-B



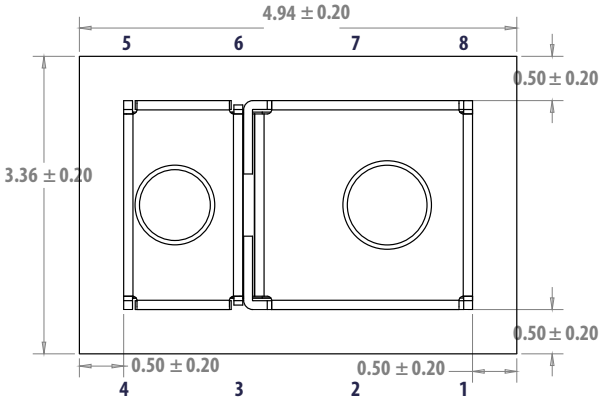
Reel Dimensions for Option -140



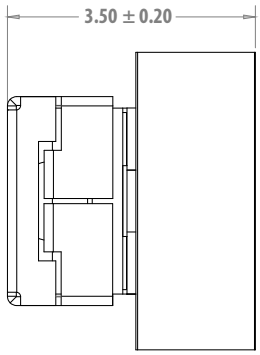


TAPE WIDTH	T	W1	W2	W3
12MM	4+/- .50	12.4 + 2.0 - 0.0	18.4 MAX	11.9 MIN 15.4 MAX

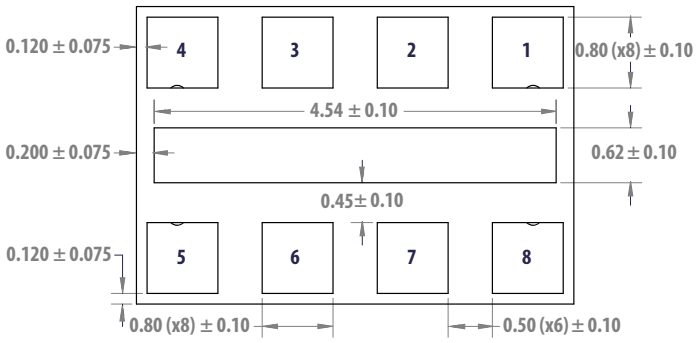
Package Outline Dimensions for Option -200



Top View

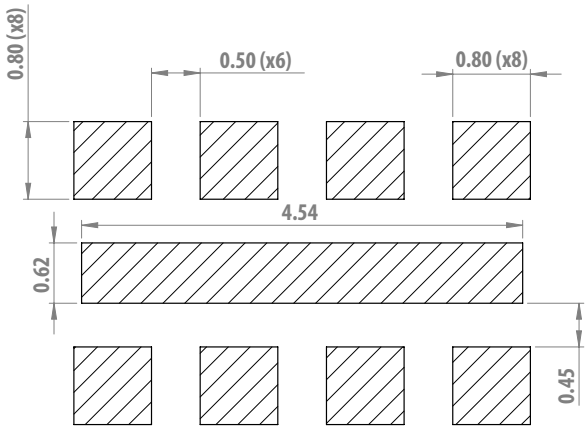


Side View

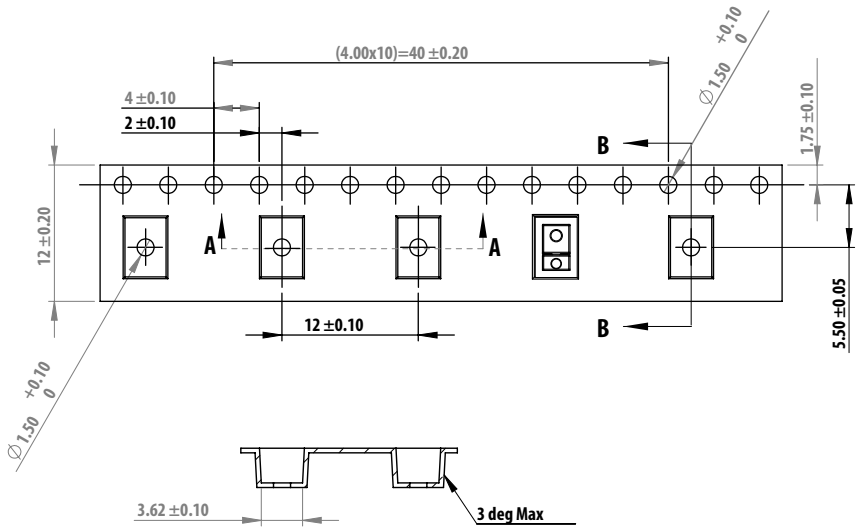


Bottom View

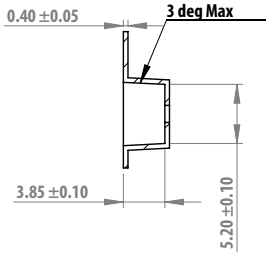
PCB Pad Layout for Option -200



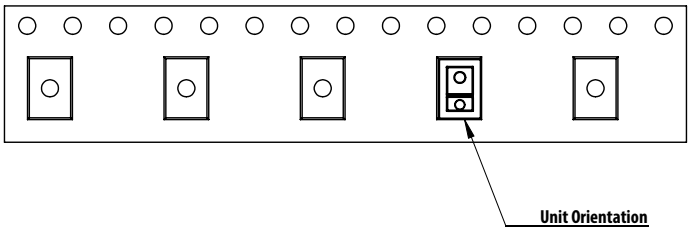
Tape Dimensions for Option -200



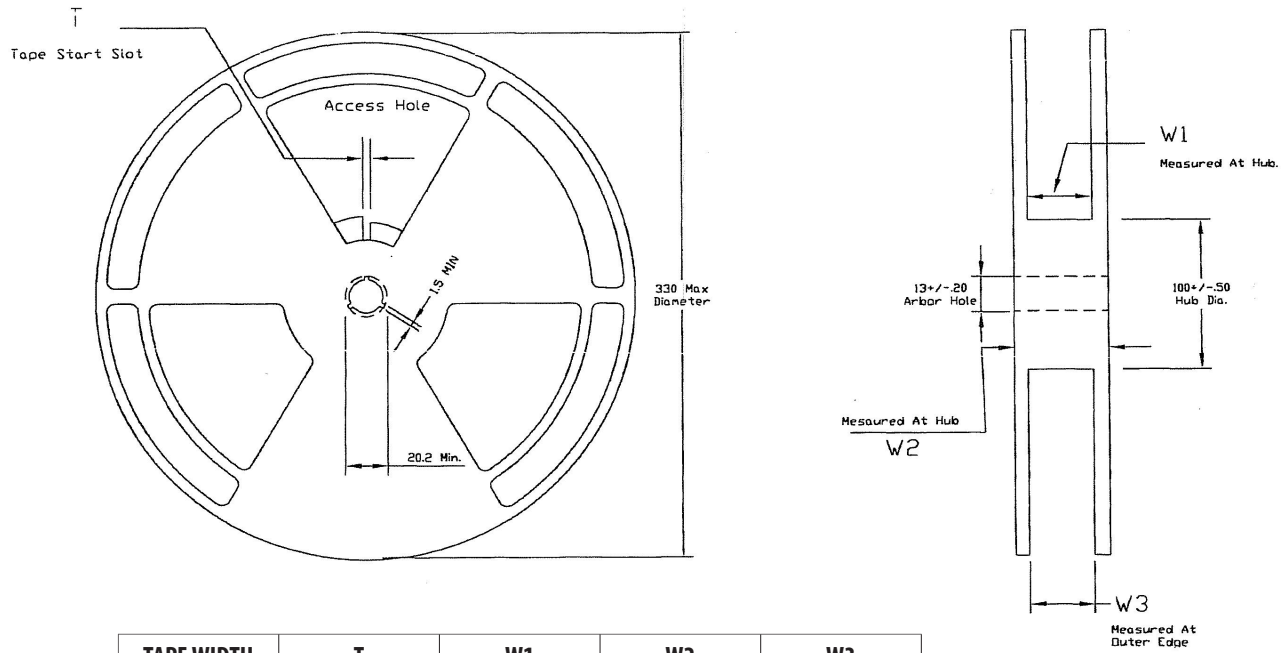
SECTION A-A



SECTION B-B



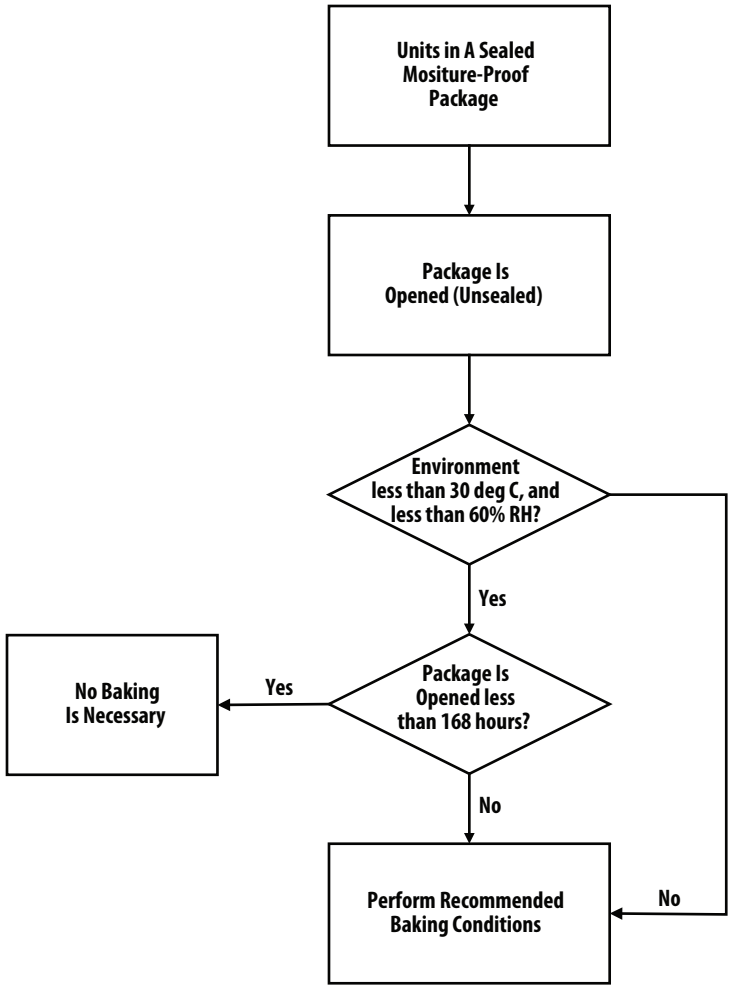
Reel Dimensions for Option -200



TAPE WIDTH	T	W1	W2	W3
12MM	4+/- .50	12.4 + 2.0 - 0.0	18.4 MAX	11.9 MIN 15.4 MAX

Moisture Proof Packaging

All APDS-9130 options are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.



Baking Conditions:

Package	Temperature	Time
In Reel	60° C	48 hours
In Bulk	100° C	4 hours

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

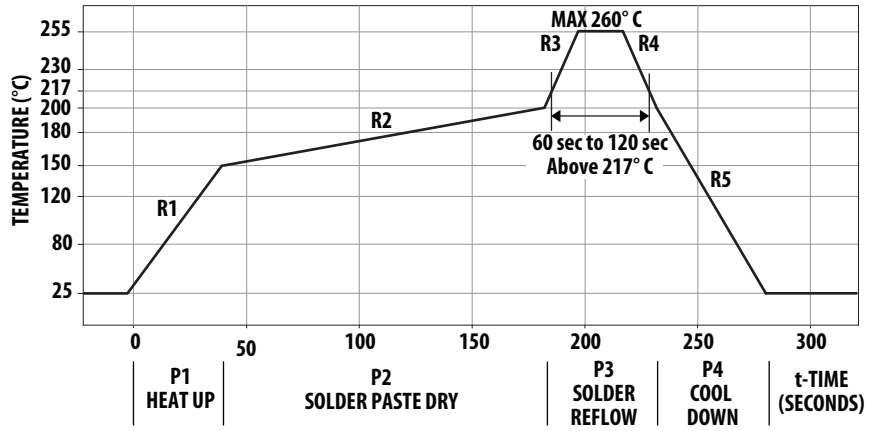
Recommended Storage Conditions:

Storage Temperature	10° C to 30° C
Relative Humidity	below 60% RH

Time from unsealing to soldering:

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25° C to 150° C	3° C/s
Solder Paste Dry	P2, R2	150° C to 200° C	100 s to 180s
Solder Reflow	P3, R3	200° C to 260° C	3° C/s
	P3, R4	260° C to 200° C	-6° C/s
Cool Down	P4, R5	200° C to 25° C	-6° C/s
Time maintained above liquidus point , 217° C		> 217° C	60 s to 120 s
Peak Temperature		260° C	–
Time within 5° C of actual Peak Temperature		> 255° C	20 s to 40 s
Time 25° C to Peak Temperature		25° C to 260° C	8 mins

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and component pins are heated to a temperature of 150° C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3° C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260° C (500° F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 120 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25° C (77° F) should not exceed 6° C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

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