

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10V to 20V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability of 1.9A/2.3A typical
- Leadfree, RoHS compliant
- Automotive qualified\*

### Typical Applications

- Piezo injection
- Electric Power Steering
- Fan and compressor
- Starter/alternator

### Product Summary

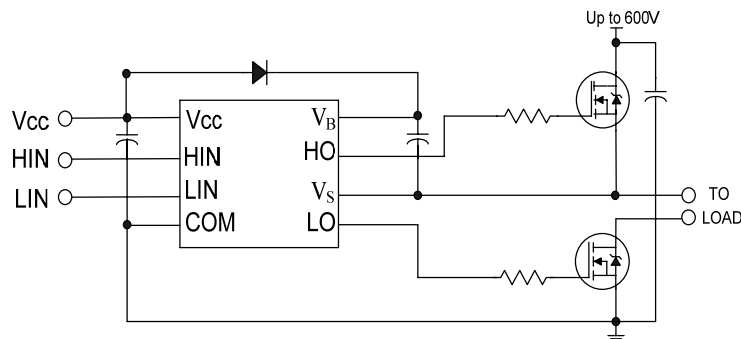
|   |                          |
|---|--------------------------|
| Topology                                    | High and Low Side Driver |
| $V_{\text{OFFSET}}$                         | $\leq 600\text{V}$       |
| $V_{\text{OUT}}$                            | 10V – 20V                |
| $I_{\text{O+}} \& I_{\text{O-}}$ (typical)  | 1.9A & 2.3A              |
| $t_{\text{on}} \& t_{\text{off}}$ (typical) | 135ns                    |

### Package Options



8 - Lead SOIC  
AUIRS21811S

### Typical Connection Diagram



**AUIRS21811S**

(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

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## Description

The AUIRS21811S is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600V.

## Feature Comparison: AUIRS21811/AUIRS2181/AUIRS2183/AUIRS2184

| Part  | Input Logic                  | Cross-Conduction Prevention logic | Dead-Time               | Ground Pins          | Ton/Toff (typical) |
|-------|------------------------------|-----------------------------------|-------------------------|----------------------|--------------------|
| 21811 | HIN/LIN                      | No                                | none                    | COM                  | 135/135 ns         |
| 2181  | HIN/LIN                      | No                                | none                    | COM                  | 160/200 ns         |
| 21814 |                              |                                   |                         | V <sub>SS</sub> /COM |                    |
| 2183  | HIN/ $\overline{\text{LIN}}$ | Yes                               | Internal 500ns          | COM                  | 180/220 ns         |
| 21834 |                              |                                   | Programmable 0.4 – 5 us | V <sub>SS</sub> /COM |                    |
| 2184  | $\overline{\text{IN}}$ /SD   | Yes                               | Internal 500ns          | COM                  | 600/230 ns         |
| 21844 |                              |                                   | Programmable 0.4 – 5 us | V <sub>SS</sub> /COM |                    |

**Qualification Information<sup>†</sup>**

|                                   |                      |   |
|-----------------------------------|----------------------|---|
| <b>Qualification Level</b>        |                      | Automotive<br>(per AEC-Q100 <sup>††</sup> )   |
|                                   |                      | Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. |
| <b>Moisture Sensitivity Level</b> |                      | MSL3 <sup>†††</sup> 260°C<br>(per IPC/JEDEC J-STD-020)  |
| <b>ESD</b>                        | Machine Model        | Class M3 (Pass +/-250V)<br>(per AEC-Q100-003)   |
|                                   | Human Body Model     | Class H2 (Pass +/-2500V)<br>(per AEC-Q100-002)  |
|                                   | Charged Device Model | Class C5 (Pass +/-1250V)<br>(per AEC-Q100-011)  |
| <b>RoHS Compliant</b>             |                      | Yes   |

<sup>†</sup> Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

<sup>††</sup> Exceptions to AEC-Q100 requirements are noted in the qualification report.

<sup>†††</sup> Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

### Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM lead. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

| Symbol     | Definition  | Min         | Max            | Units                     |
|------------|---|-------------|----------------|---------------------------|
| $V_B$      | High side floating absolute voltage                     | -0.3        | 620            | V                         |
| $V_S$      | High side floating supply offset voltage                | $V_B - 25$  | $V_B + 0.3$    |                           |
| $V_{HO}$   | High side floating output voltage                       | $V_S - 0.3$ | $V_B + 0.3$    |                           |
| $V_{CC}$   | Low side and logic fixed supply voltage                 | -0.3        | 20             |                           |
| $V_{LO}$   | Low side output voltage                                 | -0.3        | $V_{CC} + 0.3$ |                           |
| $V_{IN}$   | Logic input voltage (HIN & LIN)                         | COM - 0.3   | $V_{CC} + 0.3$ |                           |
| $dV_S/dt$  | Allowable offset supply voltage transient               | —           | 50             | V/ns                      |
| $P_D$      | Package power dissipation @ $T_A \leq 25^\circ\text{C}$ | —           | 0.625          | W                         |
| $R_{thJA}$ | Thermal resistance, junction to ambient                 | —           | 200            | $^\circ\text{C}/\text{W}$ |
| $T_J$      | Junction temperature                                    | —           | 150            | $^\circ\text{C}$          |
| $T_S$      | Storage temperature                                     | -50         | 150            |                           |
| $T_L$      | Lead temperature (soldering, 10 seconds)                | —           | 300            |                           |

### Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions.  $V_S$  and offset rating are tested with all supplies biased at 15V differential.

| Symbol   | Definition                                 | Min        | Max        | Units            |
|----------|--|------------|------------|------------------|
| $V_B$    | High side floating supply absolute voltage | $V_S + 10$ | $V_S + 20$ | V                |
| $V_S$    | High side floating supply offset voltage   | †          | 600        |                  |
| $V_{HO}$ | High side floating output voltage          | $V_S$      | $V_B$      |                  |
| $V_{CC}$ | Low side and logic fixed supply voltage    | 10         | 20         |                  |
| $V_{LO}$ | Low side output voltage                    | 0          | $V_{CC}$   |                  |
| $V_{IN}$ | Logic input voltage (HIN & LIN)            | COM        | $V_{CC}$   |                  |
| $T_A$    | Ambient temperature                        | -40        | 125        | $^\circ\text{C}$ |

† Logic operational for  $V_S$  of -5V to +600V. Logic state held for  $V_S$  of -5V to  $-V_{BS}$ . (Please refer to Figure 4 for more details).

## Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  with bias conditions of  $V_{CC} = V_{BS} = 15\text{V}$ ,  $V_S = \text{COM}$ ,  $C_L = 1000\text{pF}$ .

| Symbol    | Definition                          | Min | Typ | Max | Units | Test Conditions                    |
|-----------|-------------------------------------|-----|-----|-----|-------|------------------------------------|
| $t_{on}$  | Turn-on propagation delay           | —   | 135 | 230 | ns    | $V_S = 0\text{V}$                  |
| $t_{off}$ | Turn-off propagation delay          | —   | 135 | 230 |       | $V_S = 0\text{V}$ or $600\text{V}$ |
| MT        | Delay matching, HO & LO turn-on/off | —   | —   | 35  |       |                                    |
| $t_r$     | Turn-on rise time                   | —   | —   | 60  |       | $V_S = 0\text{V}$                  |
| $t_f$     | Turn-off fall time                  | —   | —   | 35  |       | $V_S = 0\text{V}$                  |

## Static Electrical Characteristics

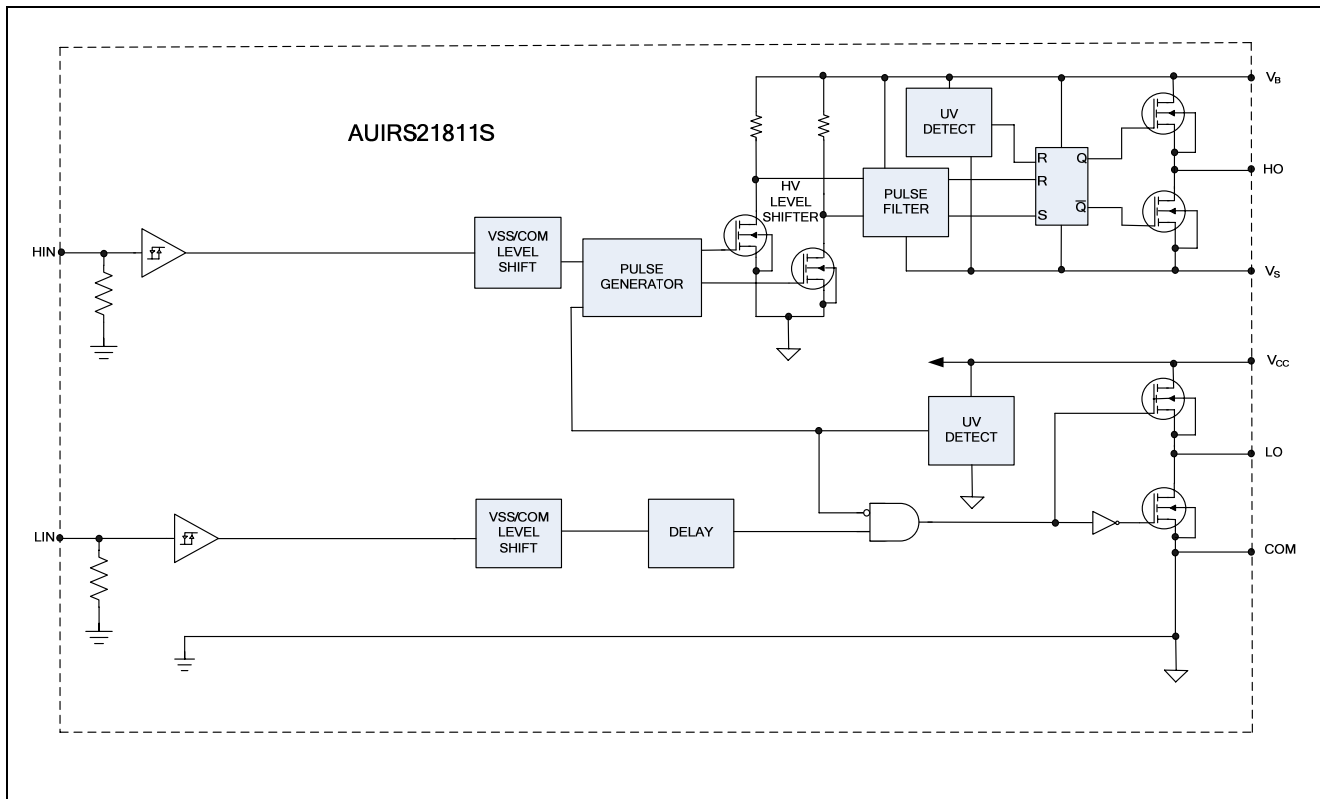
Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  with bias conditions of  $V_{CC} = V_{BS} = 15\text{V}$  and  $V_S = \text{COM}$ . The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}/\text{COM}$  and are applicable to the respective input leads: HIN and LIN. The  $V_O$  and  $I_O$  parameters are referenced to  $V_S/\text{COM}$  and are applicable to the respective output leads: HO and LO.

| Symbol                     | Definition   | Min | Typ | Max | Units         | Test Conditions   |
|----------------------------|--|-----|-----|-----|---------------|---|
| $V_{IH}$                   | Logic “1” input voltage  | 2.5 | —   | —   | V             | $V_{CC} = 10\text{V}$ to $20\text{V}$   |
| $V_{IL}$                   | Logic “0” input voltage  | —   | —   | 0.8 |               |   |
| $V_{OH}$                   | High level output voltage, $V_{BIAS} - V_O$                        | —   | —   | 1.4 |               | $I_O = 0\text{mA}$  |
| $V_{OL}$                   | Low level output voltage, $V_O$                                    | —   | —   | 0.2 |               | $I_O = 20\text{mA}$   |
| $I_{LK}$                   | Offset supply leakage current                                      | —   | —   | 50  | $\mu\text{A}$ | $V_B = V_S = 600\text{V}$   |
| $I_{QBS}$                  | Quiescent $V_{BS}$ supply current                                  | 25  | 80  | 200 |               | $V_{IN} = 0\text{V}$ or $5\text{V}$   |
| $I_{QCC}$                  | Quiescent $V_{CC}$ supply current                                  | 55  | 130 | 260 |               |   |
| $I_{IN+}$                  | Logic “1” input bias current                                       | —   | 25  | 60  |               | $V_{IN} = 5\text{V}$  |
| $I_{IN-}$                  | Logic “0” input bias current                                       | —   | —   | 1.0 |               | $V_{IN} = 0\text{V}$  |
| $V_{CCUV+}$<br>$V_{BSUV+}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold | 8.0 | 8.9 | 9.8 | V             |   |
| $V_{CCUV-}$<br>$V_{BSUV-}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold | 7.4 | 8.2 | 9.0 |               |   |
| $V_{CCUVH}$<br>$V_{BSUVH}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage Hysteresis               | 0.3 | 0.7 | —   |               |   |
| $I_{O25+}^{(†)}$           | Output high short circuit pulsed current                           | 1.4 | 1.9 | —   | A             | $V_O = 0\text{V}$ ,<br>$PW \leq 10\mu\text{s}$ ,<br>$T_J = 25^{\circ}\text{C}$  |
| $I_{O25-}^{(†)}$           | Output low short circuit pulsed current                            | 1.8 | 2.3 | —   |               | $V_O = 15\text{V}$ ,<br>$PW \leq 10\mu\text{s}$ ,<br>$T_J = 25^{\circ}\text{C}$ |
| $I_{O+}^{(†)(††)}$         | Output high short circuit pulsed current                           | 1.2 | —   | —   |               | $V_O = 0\text{V}$ ,<br>$PW \leq 10\mu\text{s}$                                  |
| $I_{O-}^{(†)(††)}$         | Output low short circuit pulsed current                            | 1.5 | —   | —   |               | $V_O = 15\text{V}$ ,<br>$PW \leq 10\mu\text{s}$                                 |

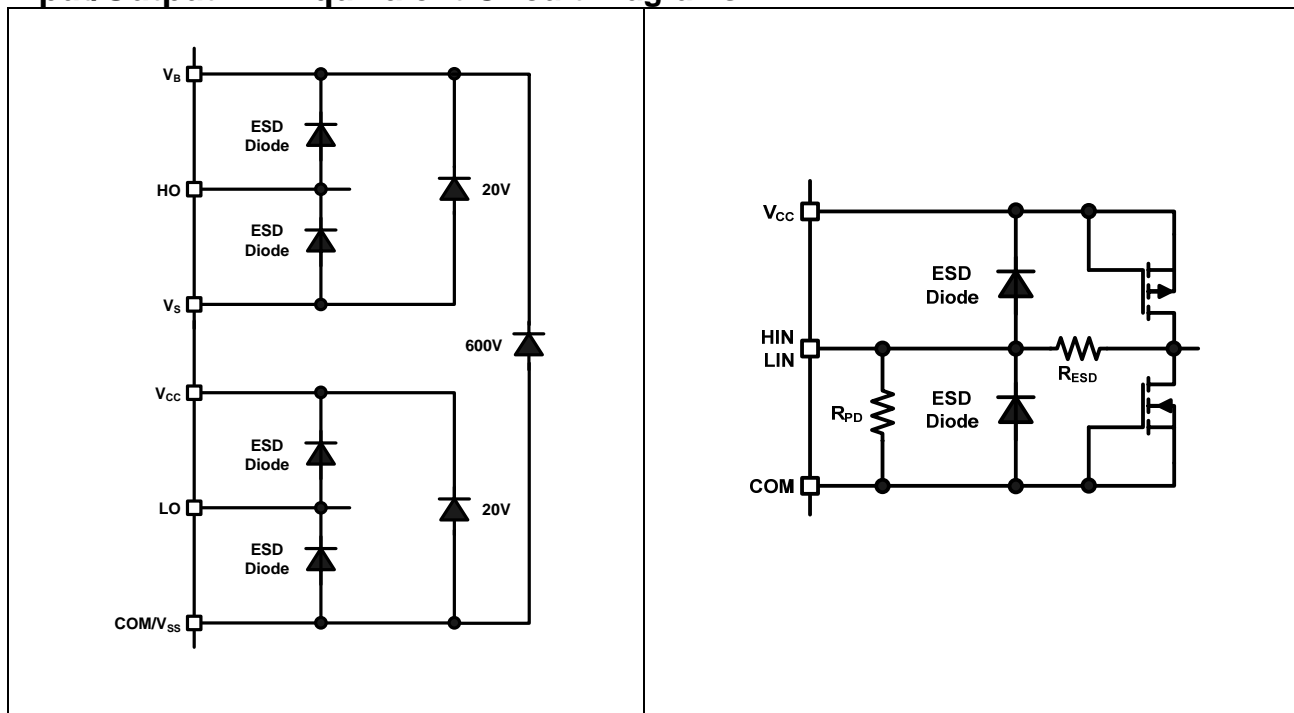
(†) Guaranteed by design

(††)  $I_{O+}$  and  $I_{O-}$  decrease with rising temperature

## Functional Block Diagrams



### Input/Output Pin Equivalent Circuit Diagrams

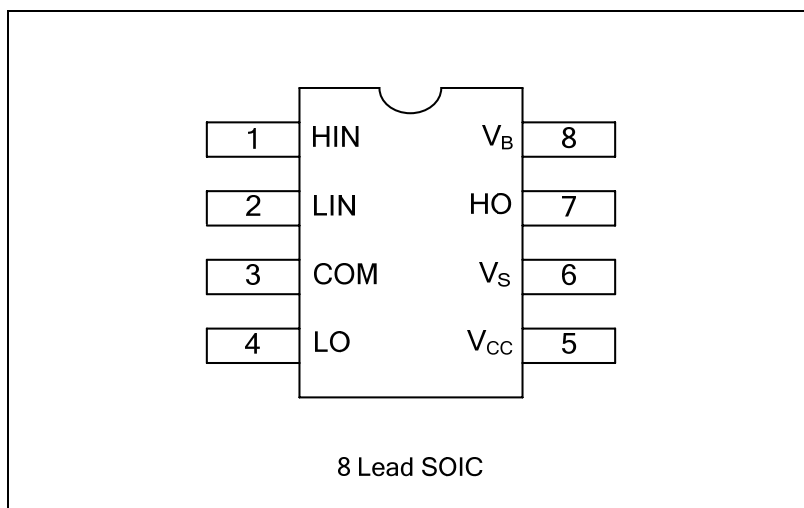




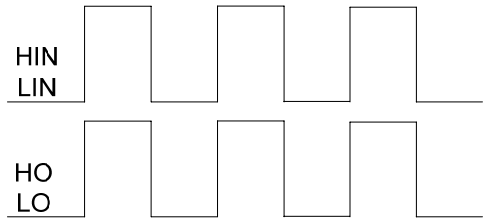
## Lead Definitions: AUIRS21811S

| Pin# | Symbol          | Description  |
|------|-----------------|--|
| 1    | HIN             | Logic input for high-side driver output (HO), in phase |
| 2    | LIN             | Logic input for low-side driver output (LO), in phase  |
| 3    | COM             | Low-side return  |
| 4    | LO              | Low-side gate drive output                             |
| 5    | V <sub>CC</sub> | Low-side and logic fixed supply                        |
| 6    | V <sub>S</sub>  | High-side floating supply return                       |
| 7    | HO              | High-side gate drive output                            |
| 8    | V <sub>B</sub>  | High-side floating supply                              |

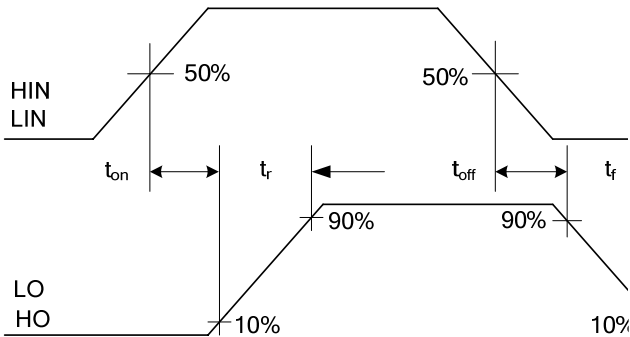
## Lead Assignments



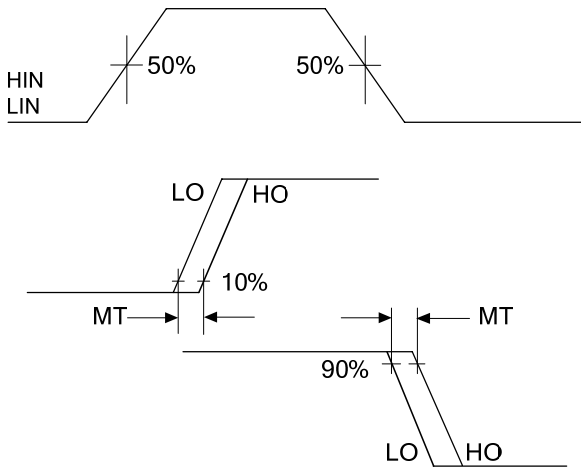
**Application Information and Additional Details**



**Figure 1. Input/Output Timing Diagram**



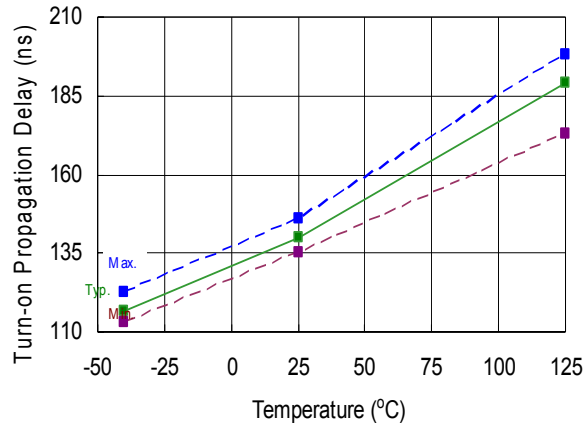
**Figure 2. Switching Time Waveform Definitions**



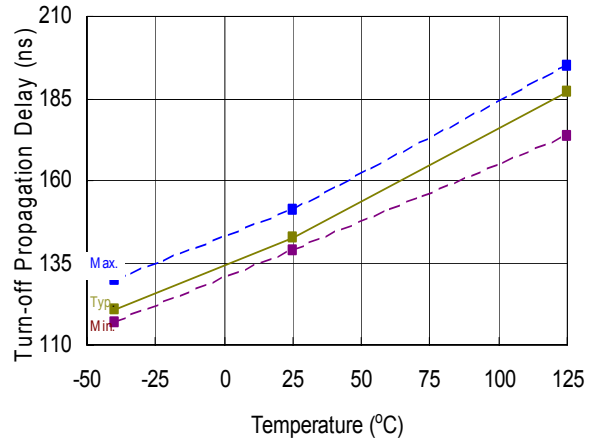
**Figure 3. Delay Matching Waveform Definitions**

## Parameter Temperature Trends

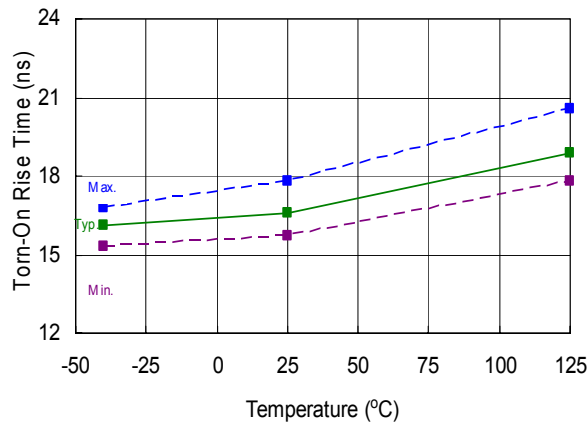
Figures 4-16 provide information on the experimental performance of the AUIRS21811S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the curves. Each line in the graphs consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).



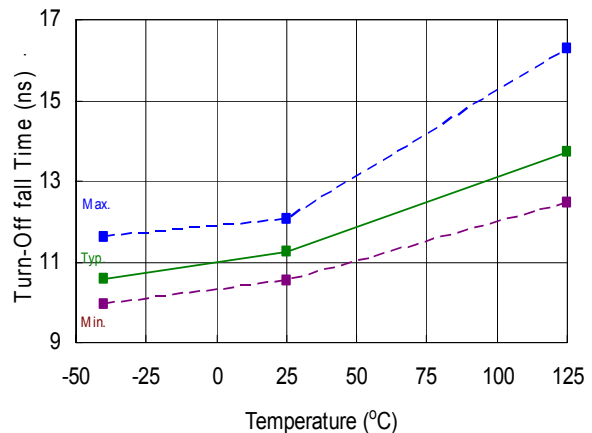
**Figure 4. Turn-On Propagation Delay vs. Temperature**



**Figure 5. Turn-Off Propagation Delay vs. Temperature**



**Figure 6. Turn-On Rise Time vs. Temperature**



**Figure 7. Turn-Off Fall Time vs. Temperature**

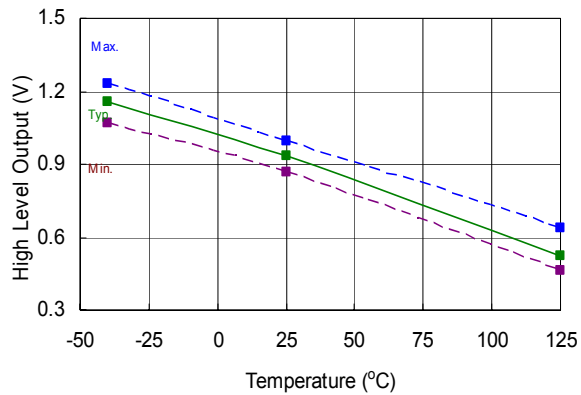


Figure 8. High Level Output Voltage vs. Temperature ( $I_o = 0$  mA)

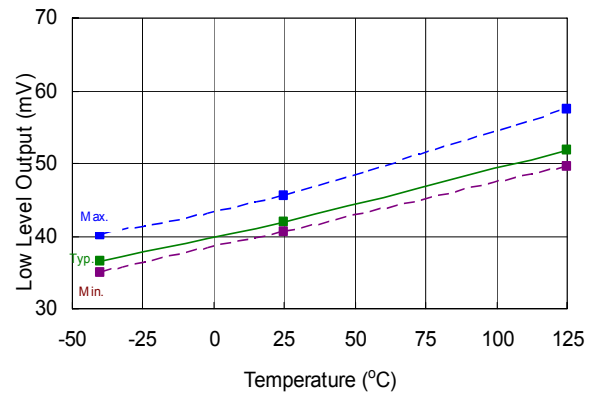


Figure 9. Low Level Output vs. Temperature

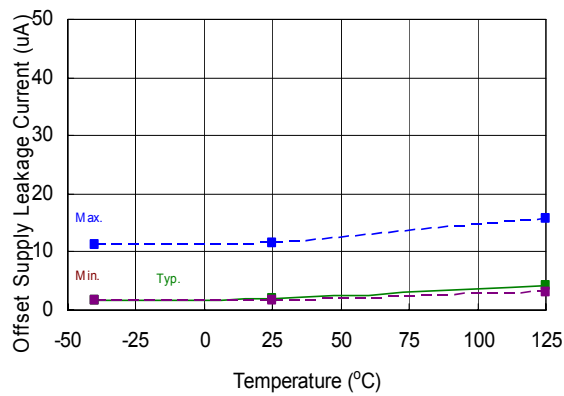


Figure 10. Offset Supply Leakage Current vs. Temperature

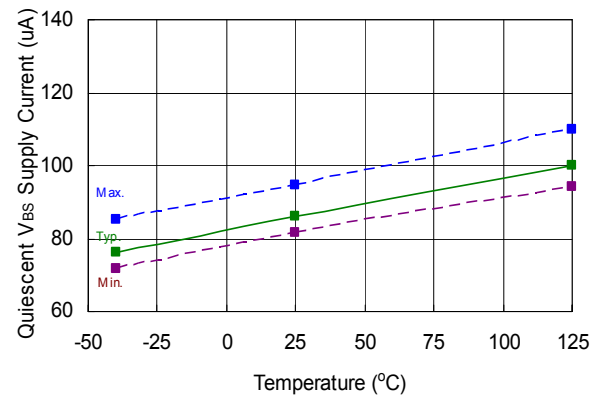


Figure 11.  $V_{BS}$  Supply Current vs. Temperature

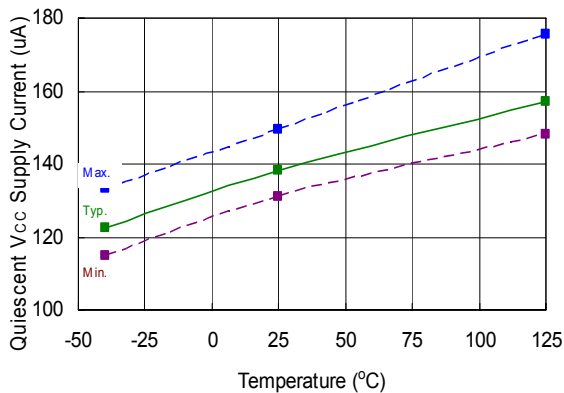


Figure 12.  $V_{CC}$  Supply Current vs. Temperature

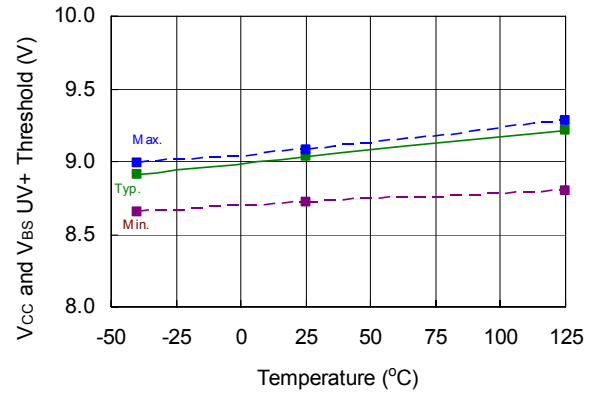


Figure 13.  $V_{CC}$  Undervoltage Threshold (+) vs. Temperature

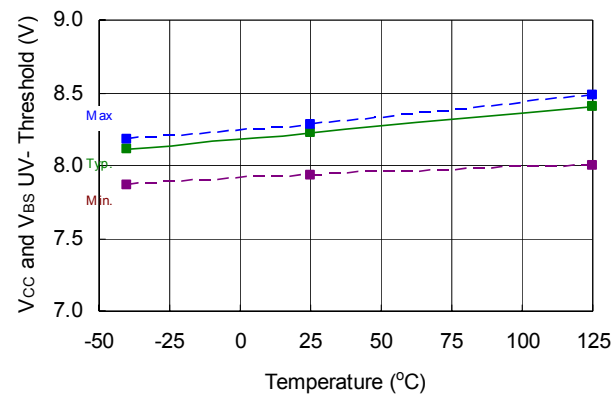


Figure 14.  $V_{CC}$  Undervoltage Threshold (-) vs. Temperature

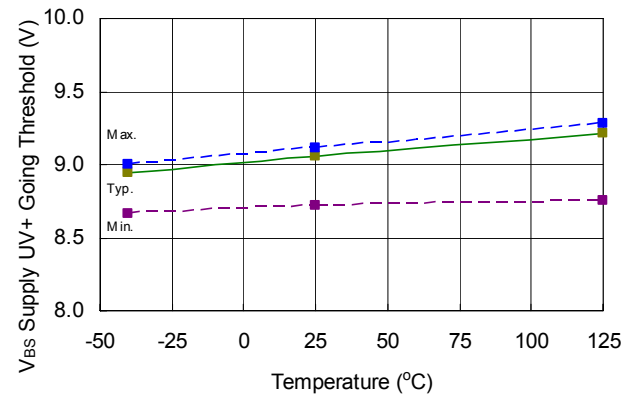


Figure 15.  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature

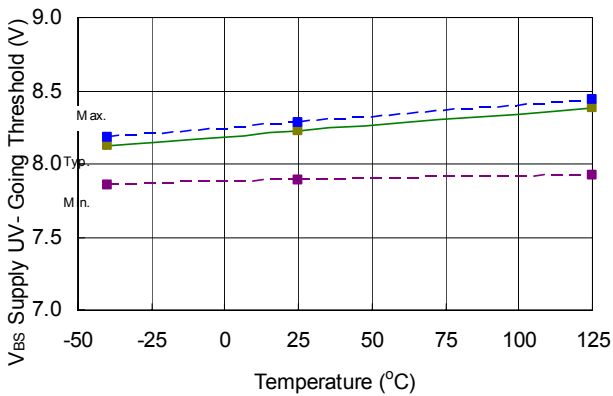
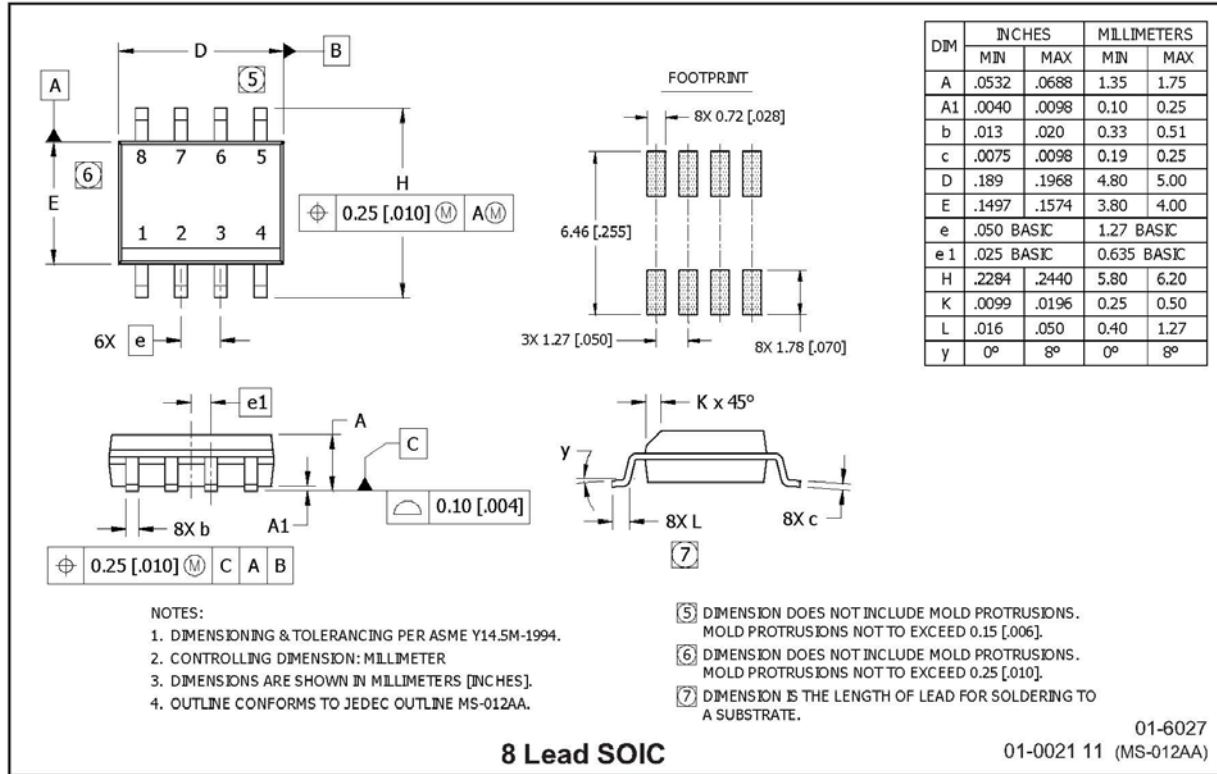
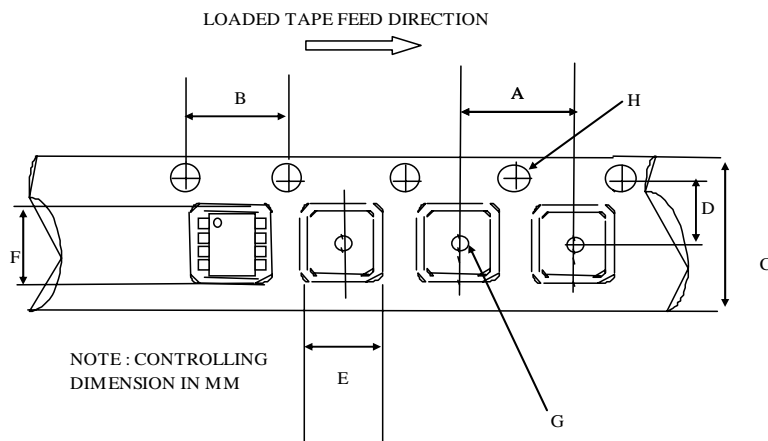


Figure 16.  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature

**Package Details: SOIC 8**

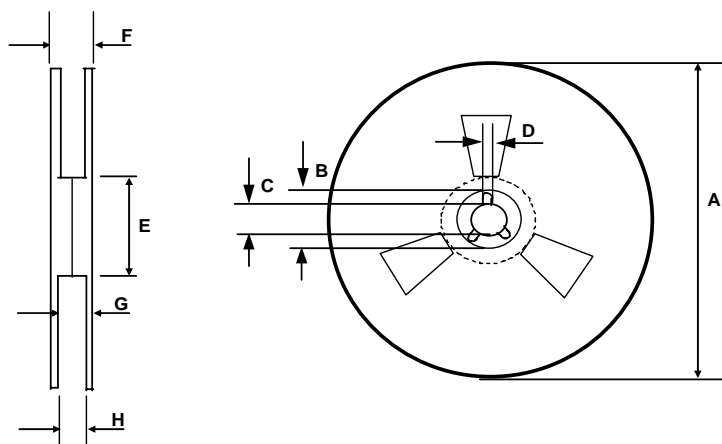


**Tape and Reel Details: SOIC8**



**CARRIER TAPE DIMENSION FOR 8SOICN**

| Code | Metric |       | Imperial |       |
|------|--------|-------|----------|-------|
|      | Min    | Max   | Min      | Max   |
| A    | 7.90   | 8.10  | 0.311    | 0.318 |
| B    | 3.90   | 4.10  | 0.153    | 0.161 |
| C    | 11.70  | 12.30 | 0.46     | 0.484 |
| D    | 5.45   | 5.55  | 0.214    | 0.218 |
| E    | 6.30   | 6.50  | 0.248    | 0.255 |
| F    | 5.10   | 5.30  | 0.200    | 0.208 |
| G    | 1.50   | n/a   | 0.059    | n/a   |
| H    | 1.50   | 1.60  | 0.059    | 0.062 |

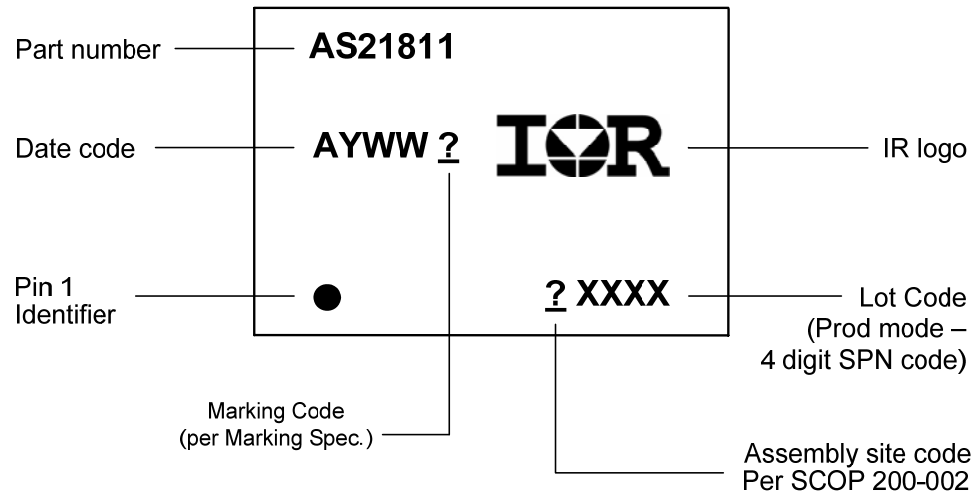


**REEL DIMENSIONS FOR 8SOICN**

| Code | Metric |        | Imperial |        |
|------|--------|--------|----------|--------|
|      | Min    | Max    | Min      | Max    |
| A    | 329.60 | 330.25 | 12.976   | 13.001 |
| B    | 20.95  | 21.45  | 0.824    | 0.844  |
| C    | 12.80  | 13.20  | 0.503    | 0.519  |
| D    | 1.95   | 2.45   | 0.767    | 0.096  |
| E    | 98.00  | 102.00 | 3.858    | 4.015  |
| F    | n/a    | 18.40  | n/a      | 0.724  |
| G    | 14.50  | 17.10  | 0.570    | 0.673  |
| H    | 12.40  | 14.40  | 0.488    | 0.566  |

**Part Marking Information**

**SOIC8:**





## Order Information

| Base Part Number | Package Type | Standard Pack |          | Complete Part Number |
|------------------|--------------|---------------|----------|----------------------|
|                  |              | Form          | Quantity |                      |
| AUIRS21811       | SOIC8N       | Tube/Bulk     | 95       | AUIRS21811S          |
|                  |              | Tape and Reel | 2500     | AUIRS21811STR        |

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**WORLD HEADQUARTERS:**

233 Kansas St., El Segundo, California 90245  
Tel: (310) 252-7105

**Revision History**

| <b>Date</b> | <b>Change by</b> | <b>Comment</b>   |
|-------------|------------------|--|
| 8/6/08      | CIC              | First draft: all changes wrt AUIRS2181(4)(S) datasheet<br>Updated all references to IC name<br>Changed references of ton/toff to reflect requested 120ns/120ns spec<br>Updated expected $I_{QBS}$ and $I_{QCC}$ specs  |
| 9/8/08      | CIC              | Changed product summary topology to "Half-Bridge"<br>Changed product summary $I_{O+}$ & $I_{O-}$ from typ values to min values<br>Removed reference to deadtime in the product summary<br>Removed typical applications section<br>Removed references to other parts in feature comparison section<br>Changed $V_{IN}$ from 2.7V min to 2.5V min<br>Changed $V_{OH}$ from 1.2V max to 1.4V max<br>Changed $V_{OL}$ from 0.1V max to 0.2V max<br>Updated functional block diagrams<br>Updated lead definitions and lead assignments, added device label for lead assignment<br>Added typical application diagram section<br>Added simplified block diagram section<br>Added input/output pin equivalent diagrams<br>Added in application info and additional details section<br>Added in parameter temperature trend section |
| 10/31/08    | CIC              | Changed VB max to 620V (align with rest of 20V clamp drivers spec)   |
| 2/24/09     | CIC              | Updated the qual table (showing "TBD" for ESD/LU ratings)  |
| 2/26/09     | CIC              | Removed IRS218114  |
| 3/10/09     | CIC              | Removed Simplified Block Diagram<br>Removed Typical Application Diagram<br>Removed Parameter Temp Trend Section<br>Updated page number references  |
| 3/23/09     | CIC              | Changed $I_{O+/-}$ units to A from mA  |
| 5/20/09     | CIC              | Added ESD and LU ratings   |
| 6/9/09      | APBU             | Front page: "Logic and power ground +/- 5V offset" sentence erased (only one ground exists).<br>Page 3: "designed for minimum driver cross-conduction" sentence erased.<br>Page 5, 6, 8: Vss related sentences erased or modified (Vss does not exist).  |
| 7/17/09     | CIC              | Removed min spec on $I_{O+/-}$ parameters<br>Changed typ ton/toff to 135ns   |
| 9/08/09     | APBU             | Added Typical Applications on front page, Extended Feature comparison table, added junction temperature range in Dynamic and Static electrical characteristic tables.  |
| 9/14/09     | APBU             | Added tri-temp plots, added ESD passing threshold voltage, corrected $I_{O+/-}$ & $T_{on/off}$ typical value on front page to be consistent with data in table   |
| 9/15/09     | APBU             | Corrected list of Typical Applications on front page   |
| 9/16/09     | APBU             | Dyn el. Char table: Max turn on and off prop. Delay changed from 180 ns to 210 ns, removed temperature range from Statics and Dynamic Electrical Characteristic tables   |
| 9/16/09     | CIC              | Change the year to 2009 in header<br>Separated Marking info and order info in two pages  |
| 9/17/09     | CIC              | Fixed ESD passing thresholds   |
| 10/6/09     | APBU             | LU rating to "tbd", added SOA page, updated marking, updated table of content, added guaranteed by design note for $I_{O+/-}$ parameters, removed typ. $t_r/t_f$ ,   |
| 10/08/09    | APBU             | Removed SOA page and updated table of content.   |
| 10/09/09    | APBU             | Changed Max turn on/off to 230ns to allow for tri-temp variations  |

|              |      |   |
|--------------|------|---|
| 1/6/2010     | APBU | Removed Latch Up Rating from Qual Info page; updated ton/toff typical in comparison table for AUIRS2181(4)S to 160/200ns & for AUIRS2184(4)S to 600/230ns; modified disclaimer under Absolute Max. Rating; added Important Notice |
| 2/24/10      | APBU | Page 6: Added $I_{O25+}$ and $I_{O25-}$ specification and the note  |
| 05/07/10     | APBU | Corrected topology to High and Low Side driver on front page.   |
| 28 July 2010 | APBU | Clamp voltage changed from 25V to 20V in input output pin equivalent circuit diagram.   |

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➤ Address :

401 Building No.5, JiuGe Business Center, Lane 2301, Yishan Rd  
Minhang District, Shanghai , China

➤ Sales :

Direct     +86 (21) 6401-6692  
  
Email        amall@ameya360.com  
  
QQ            800077892  
  
Skype        ameyasales1 ameyasales2

➤ Customer Service :

Email        service@ameya360.com

➤ Partnership :

Tel            +86 (21) 64016692-8333  
  
Email        mkt@ameya360.com