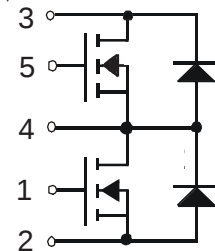


Trench Gate HiperFET Power MOSFET

FMM50-025TF

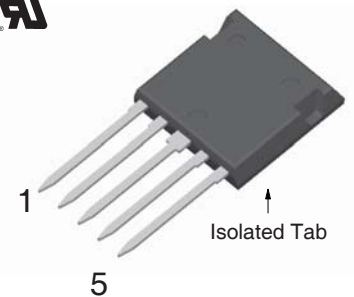
Phase Leg Topology

N-Channel



$$\begin{aligned} V_{DSS} &= 250V \\ I_{D25} &= 30A \\ R_{DS(on)} &\leq 60m\Omega \\ t_{rr(typ)} &= 84ns \end{aligned}$$

ISOPLUS i4-Pak™



Symbol	Test Conditions	Maximum Ratings	
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
V_{ISOLD}	50/60Hz, RMS, t = 1min, Leads-to-Tab	2500	V~
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
F_C	Mounting Force	20..120/ 4.5..27	N/lb.

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	250	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	250	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	30	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	130	A
I_A	$T_C = 25^\circ\text{C}$	25	A
E_{AS}	$T_C = 25^\circ\text{C}$	400	mJ
dV/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$	15	V/ns
P_D	$T_C = 25^\circ\text{C}$	125	W

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
C_p	Coupling Capacitance Between Shorted Pins and Mounting Tab in the Case		40	pF
d_s, d_A	Pin - Pin	1.7		mm
d_s, d_A	Pin - Backside Metal	5.5		mm
Weight			9	g

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
 - UL Recognized Package
 - Isolated Mounting Surface
 - 2500V Electrical Isolation
- Avalanche Rated
- Low Q_g
- Low Drain-to-Tab capacitance
- Low package inductance

Advantages

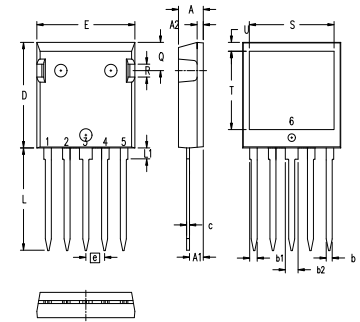
- Low Gate Drive Requirement
- High power density
- Fast Intrinsic Rectifier
- Low Drain to Ground Capacitance
- Fast Switching

Applications

- DC and AC Motor Drives
- UPS, Solar and Wind Power Inverters
- Synchronous Rectifiers
- Multi-Phase DC to DC Converters
- Industrial Battery Chargers
- Switching Power Supplies

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V, I_D = 1mA$	250		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.5		4.5 V
I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			1 μA 150 μA
$R_{DS(on)}$	$V_{GS} = 10V, I_D = 25A$, Note 1			60 m Ω
g_{fs}	$V_{DS} = 10V, I_D = 25A$, Note 1	35	58	S
C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1\text{ MHz}$		4000	pF
C_{oss}			410	pF
C_{rss}			60	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 15V, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 25A$ $R_G = 5\Omega$ (External)		14	ns
t_r			25	ns
$t_{d(off)}$			47	ns
t_f			25	ns
$Q_{g(on)}$	$V_{GS} = 10V, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 25A$		78	nC
Q_{gs}			19	nC
Q_{gd}			22	nC
R_{thJC}				1.0 $^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$

ISOPLUS i4-Pak™ Outline



NOTE: Bottom heatsink meets 3000 Volts AC 1 sec isolation to the other pins.

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
b2	.100	.110	2.54	2.79
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0V$			30 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			200 A
V_{SD}	$I_F = 50A, V_{GS} = 0V$, Note 1			1.5 V
t_{rr}	$I_F = 25A, -di/dt = 250A/\mu s$ $V_R = 100V, V_{GS} = 0V$		84	ns
I_{RM}			15.4	A
Q_{RM}			650	nC

Note 1. Pulse test, $t \leq 300\mu s$, duty cycle, $d \leq 2\%$.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

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