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May 25, 2006 FN8117.1

Dual Voltage Monitor with Integrated CPU Supervisor and System Battery Switch

FEATURES

- Dual voltage detection and reset assertion
  - —Three standard reset threshold settings (4.6V/2.9V, 4.6V/2.6V, 2.9V/1.6V)
  - —V_{TRIP2} programmable down to 0.9V
  - —Adjust low voltage reset threshold voltages using special programming sequence
  - —Reset signal valid to V_{CC} = 1V
  - —Monitor two voltages or detect power fail
- Battery switch backup
- V_{OUT}: 5mA to 50mA from V_{CC}; or 250µA from V_{BATT}
- Fault detection register
- Selectable power-on reset timeout (0.05s, 0.2s, 0.4s, 0.8s)
- Selectable watchdog timer interval (25ms, 200ms, 1.4s, off)
- Debounced manual reset input
- Low power CMOS
  - —25µA typical standby current, watchdog on
  - —6µA typical standby current, watchdog off
  - —1µA typical battery current in backup mode
- 4Kbits of EEPROM
  - —16 byte page write mode
  - —Self-timed write cycle
  - —5ms write cycle time (typical)
- Built-in inadvertent write protection
  - —Power-up/power-down protection circuitry
  - —Block lock protect 0 or 1/2, of EEPROM
- 400kHz 2-wire interface
- 2.7V to 5.5V power supply operation
- Available packages
  - —14 Ld SOIC, TSSOP
- Pb-free plus anneal available (RoHS compliant)
- Monitor voltages: 5V to 1.6V
- Memory security
- Battery switch backup
- V_{OUT} 5mA to 50mA

APPLICATIONS

- Communications equipment
  - —Routers, hubs, switches
  - —Disk arrays
- Industrial systems
  - —Process control
  - —Intelligent instrumentation
- Computer systems
  - —Desktop computers
  - —Network servers

X40420, X40421

Standard V_{TRIP1} Level	Standard V_{TRIP2} Level	Suffix
4.6V (±1%)	2.9V(±1.7%)	-A
4.6V (±1%)	2.6V (±2%)	-B
2.9V(±1.7%)	1.6V (±3%)	-C

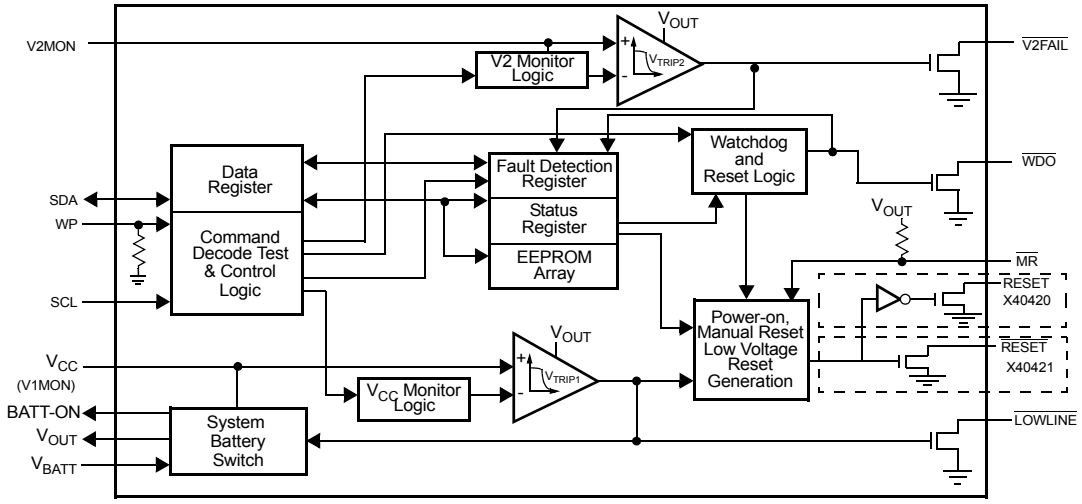
See “Ordering Information” for more details
For Custom Settings, call Intersil.

DESCRIPTION

The X40420, X40421 combines power-on reset control, watchdog timer, supply voltage supervision, and secondary supervision, manual reset, and Block Lock™ protect serial EEPROM in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying voltage to V_{CC} activates the power-on reset circuit which holds RESET/$\overline{\text{RESET}}$ active for a period of time. This allows the power supply and system oscillator to stabilize before the processor can execute code.

BLOCK DIAGRAM



Ordering Information

PART NUMBER* WITH RESET	PART MARKING	PART NUMBER* WITH RESET	PART MARKING	MONITORED V_{CC} SUPPLIES	V_{TRIP1} RANGE	V_{TRIP2} RANGE	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
X40420S14-C	X40420S C	X40421S14-C	X40421S C	1.6 to 3.6	2.9V ±50mV	1.6V ±50mV	0 to 70	14 Ld SOIC (150 mil)	MDP0027
X40420S14I-C	X40420S IC	X40421S14I-C	X40421S IC				-40 to +85	14 Ld SOIC (150 mil)	MDP0027
X40420V14-C	X4042 0VC	X40421V14-C	X40421V C				0 to 70	14 Ld TSSOP (4.4mm)	M14.173
X40420V14I-C	X4042 0VIC	X40421V14I-C	X40421V IC				-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X40420S14-B	X40420S B	X40421S14-B	X40421S B	2.6 to 5.5	4.6V ±50mV	2.6V ±50mV	0 to 70	14 Ld SOIC (150 mil)	MDP0027
X40420S14Z-B (Note)	X40420S ZB	X40421S14Z-B (Note)	X40421S ZB				0 to 70	14 Ld SOIC (150 mil) (Pb-free)	MDP0027
X40420S14I-B	X40420S IB	X40421S14I-B	X40421S IB				-40 to +85	14 Ld SOIC (150 mil)	MDP0027
X40420S14IZ-B (Note)	X40420S ZIB	X40421S14IZ-B (Note)	X40421S ZIB				-40 to +85	14 Ld SOIC (150 mil) (Pb-free)	MDP0027
X40420V14-B	X4042 0VB	X40421V14-B	X40421V B				0 to 70	14 Ld TSSOP (4.4mm)	M14.173
X40420V14Z-B (Note)	X4042 0VZB	X40421V14Z-B (Note)	X40421V ZB				0 to 70	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X40420V14I-B	X4042 0VIB	X40421V14I-B	X40421V IB				-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X40420V14IZ-B (Note)	X4042 0VZIB	X40421V14IZ-B (Note)	X40421V ZIB				-40 to +85	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X40420S14-A	X40420S A	X40421S14-A	X40421S A	2.9 to 5.5		2.9V ±50mV	0 to 70	14 Ld SOIC (150 mil)	MDP0027
X40420S14Z-A (Note)	X40420S ZA	X40421S14Z-A (Note)	X40421S ZA				0 to 70	14 Ld SOIC (150 mil) (Pb-free)	MDP0027
X40420S14I-A	X40420S IA	X40421S14I-A	X40421S IA				-40 to +85	14 Ld SOIC (150 mil)	MDP0027
X40420S14IZ-A (Note)	X40420S ZIA	X40421S14IZ-A (Note)	X40421S ZIA				-40 to +85	14 Ld SOIC (150 mil) (Pb-free)	MDP0027
X40420V14Z-A (Note)	X4042 0VZA	X40421V14Z-A (Note)	X40421V ZA				0 to 70	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173
X40420V14-A	X4042 0VA	X40421V14-A	X40421V A				0 to 70	14 Ld TSSOP (4.4mm)	M14.173
X40420V14I-A	X4042 0VIA	X40421V14I-A	X40421V IA				-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X40420V14IZ-A (Note)	X4042 0VZIA	X40421V14IZ-A (Note)	X40421V ZIA				-40 to +85	14 Ld TSSOP (4.4mm) (Pb-free)	M14.173

*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Low V_{CC} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{CC} falls below the minimum V_{TRIP1} point. RESET/$\overline{\text{RESET}}$ is active until V_{CC} returns to proper operating level and stabilizes. A second voltage monitor circuit tracks the unregulated supply to provide a power fail warning or monitors different power supply voltage. Three common low voltage combinations are available, however, Intersil's unique circuits allows the threshold for either voltage monitor to be reprogrammed to meet special needs or to fine-tune the threshold for applications requiring higher precision.

A manual reset input provides debounce circuitry for minimum reset component count.

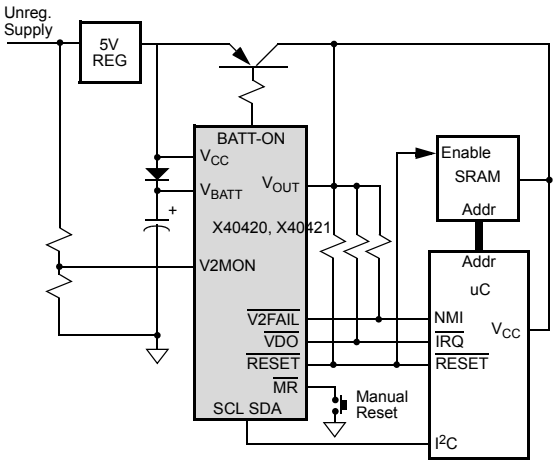
A battery switch circuit compares V_{CC} with V_{BATT} input and connects V_{OUT} to whichever is higher. This provides voltage to external SRAM or other circuits in the event of main power failure. The X40420, X40421 can drive 50mA from V_{CC} to 250µA from V_{BATT}. The device only switches to V_{BATT} when V_{CC} drops below the low V_{CC} voltage threshold and V_{BATT}.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{\text{WDO}}$ signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The memory portion of the device is a CMOS Serial EEPROM array with Intersil's Block Lock protection. The array is internally organized as x 8. The device features an 2-wire interface and software protocol allowing operation on a two-wire bus.

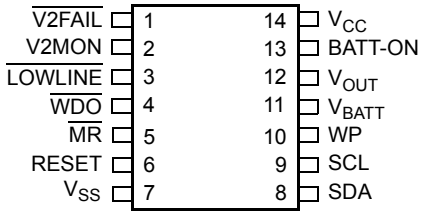
The device utilizes Intersil's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

Example Application

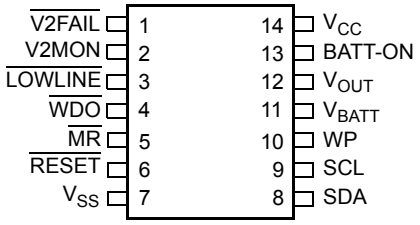


PIN CONFIGURATION

X40420
14-Pin SOIC, TSSOP



X40421
14-Pin SOIC, TSSOP



PIN DESCRIPTION

Pin	Name	Function
1	$\overline{\text{V2FAIL}}$	**V2 Voltage Fail Output.** This open drain output goes LOW when V2MON is less than V_{TRIP2} and goes HIGH when V2MON exceeds V_{TRIP2}. There is no power-up reset delay circuitry on this pin.
2	V2MON	**V2 Voltage Monitor Input.** When the V2MON input is less than the V_{TRIP2} voltage, $\overline{\text{V2FAIL}}$ goes LOW. This input can monitor an unregulated power supply with an external resistor divider or can monitor a second power supply with no external components. Connect V2MON to V_{SS} or V_{CC} when not used.
3	$\overline{\text{LOWLINE}}$	**Early Low V_{CC} Detect.** This open drain output signal goes LOW when $V_{CC} < V_{TRIP1}$. When $V_{CC} > V_{TRIP1}$, this pin is pulled high with the use of an external pull up resistor.
4	$\overline{\text{WDO}}$	**$\overline{\text{WDO}}$ Output.** $\overline{\text{WDO}}$ is an active LOW, open drain output which goes active whenever the watchdog timer goes active.
5	$\overline{\text{MR}}$	**Manual Reset Input.** Pulling the $\overline{\text{MR}}$ pin LOW initiates a system reset. The RESET/$\overline{\text{RESET}}$ pin will remain HIGH/LOW until the pin is released and for the t_{PURST} thereafter. It has an internal pull up resistor.

PIN DESCRIPTION (Continued)

Pin	Name	Function
6	$\overline{\text{RESET}}$/ RESET	**$\overline{\text{RESET}}$ Output.** (X40421) This open drain pin is an active LOW output which goes LOW whenever V_{CC} falls below V_{TRIP1} voltage or if manual reset is asserted. This output stays active for the programmed time period (t_{PURST}) on power-up. It will also stay active until manual reset is released and for t_{PURST} thereafter. **RESET Output.** (X40420) This pin is an active HIGH open drain output which goes HIGH whenever V_{CC} falls below V_{TRIP1} voltage or if manual reset is asserted. This output stays active for the programmed time period (t_{PURST}) on power-up. It will also stay active until manual reset is released and for t_{PURST} thereafter.
7	V_{SS}	Ground
8	SDA	**Serial Data.** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. This pin requires a pull up resistor and the input buffer is always active (not gated). **Watchdog Input.** A HIGH to LOW transition on the SDA (while SCL is toggled from HIGH to LOW and followed by a stop condition) restarts the Watchdog timer. The absence of this transition within the watchdog time out period results in WDO going active.
9	SCL	**Serial Clock.** The Serial Clock controls the serial bus timing for data input and output.
10	WP	**Write Protect.** WP HIGH prevents writes to any location in the device (including all the registers). It has an internal pull down resistor. (>10MΩ typical)
11	V_{BATT}	**Battery Supply Voltage.** This input provides a backup supply in the event of a failure of the primary V_{CC} voltage. The V_{BATT} voltage typically provides the supply voltage necessary to maintain the contents of SRAM and also powers the internal logic to “stay awake.” If the battery is not used, connect V_{BATT} to ground.
12	V_{OUT}	**Output Voltage. (V)** $V_{OUT} = V_{CC}$ if $V_{CC} > V_{TRIP1}$. IF $V_{CC} < V_{TRIP1}$ then $V_{OUT} = V_{CC}$ if $V_{CC} > V_{BATT} + 0.03V$ else $V_{OUT} = V_{BATT}$ (ie if $V_{CC} < V_{BATT} - 0.03V$) **Note:** There is hysteresis around $V_{BATT} \pm 0.03V$ point to avoid oscillation at or near the switchover voltage. A capacitance of 0.1µF must be connected to V_{OUT} to ensure stability.
13	BATT-ON	**Battery On.** This CMOS output goes HIGH when the V_{OUT} switches to V_{BATT} and goes LOW when V_{OUT} switches to V_{CC}. It is used to drive an external PNP pass transistor when $V_{CC} = V_{OUT}$ and current requirements are greater than 50mA. The purpose of this output is to drive an external transistor to get higher operating currents when the V_{CC} supply is fully functional. In the event of a V_{CC} failure, the battery voltage is applied to the V_{OUT} pin and the external transistor is turned off. In this “backup condition,” the battery only needs to supply enough voltage and current to keep SRAM devices from losing their data–there is no communication at this time.
14	V_{CC}	Supply Voltage

PRINCIPLES OF OPERATION

Power-on Reset

Applying power to the X40420, X40421 activates a Power-on Reset Circuit that pulls the RESET/$\overline{\text{RESET}}$ pins active. This signal provides several benefits.

– It prevents the system microprocessor from starting to operate with insufficient voltage.

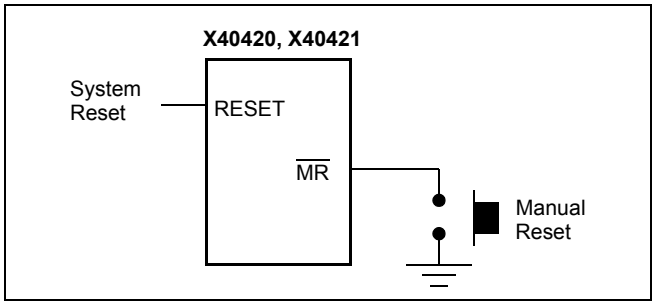
– It prevents the processor from operating prior to stabilization of the oscillator.

– It allows time for an FPGA to download its configuration prior to initialization of the circuit.

– It prevents communication to the EEPROM, greatly reducing the likelihood of data corruption on power-up.

When V_{CC} exceeds the device V_{TRIP1} threshold value for t_{PURST} (selectable) the circuit releases the $\overline{\text{RESET}}$ (X40421) and RESET (X40420) pin allowing the system to begin operation.

Figure 1. Connecting a Manual Reset Push-Button



Manual Reset

By connecting a push-button directly from $\overline{\text{MR}}$ to ground, the designer adds manual system reset capability. The $\overline{\text{MR}}$ pin is LOW while the push-button is closed and RESET/$\overline{\text{RESET}}$ pin remains LOW for t_{PURST} or till the push-button is released and for t_{PURST} thereafter. A weak pull up resistor is connected to the $\overline{\text{MR}}$ pin.

Low Voltage V1 Monitoring

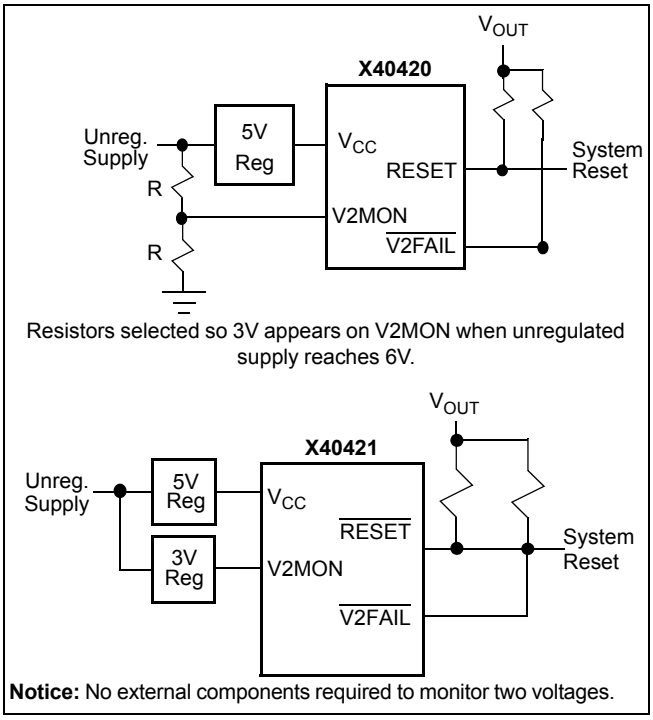
During operation, the X40420, X40421 monitors the V_{CC} level and asserts RESET if supply voltage falls below a preset minimum V_{TRIP1}. The RESET signal prevents the microprocessor from operating in a power fail or brownout condition. The V1FAIL signal remains active until the voltage drops below 1V. It also remains active until V_{CC} returns and exceeds V_{TRIP1} for t_{PURST}.

Low Voltage V2 Monitoring

The X40420, X40421 also monitors a second voltage level and asserts $\overline{\text{V2FAIL}}$ if the voltage falls below a preset minimum V_{TRIP2}. The $\overline{\text{V2FAIL}}$ signal is either ORed with RESET to prevent the microprocessor from operating in a power fail or brownout condition or used to interrupt the microprocessor with notification of an impending power failure. The $\overline{\text{V2FAIL}}$ signal remains active until the V_{CC} drops below 1V (V_{CC} falling). It also remains active until V2MON returns and exceeds V_{TRIP2}.

V2MON voltage monitor is powered by V_{OUT}. If V_{CC} and V_{BATT} go away, V2MON cannot be monitored.

Figure 2. Two Uses of Multiple Voltage Monitoring



Notice: No external components required to monitor two voltages.

WATCHDOG TIMER

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the SDA and SCL pins. A standard read or write sequence to any slave address byte restarts the watchdog timer and prevents the $\overline{\text{WDO}}$ signal to go active. A minimum sequence to reset the watchdog timer requires four microprocessor instructions namely, a Start, Clock Low, Clock High and Stop. The state of two nonvolatile control bits in the Status Register determine the watchdog timer period. The microprocessor can change these watchdog bits by writing to the X40420, X40421 control register.

Figure 3. V_{TRIPX} Set/Reset Conditions

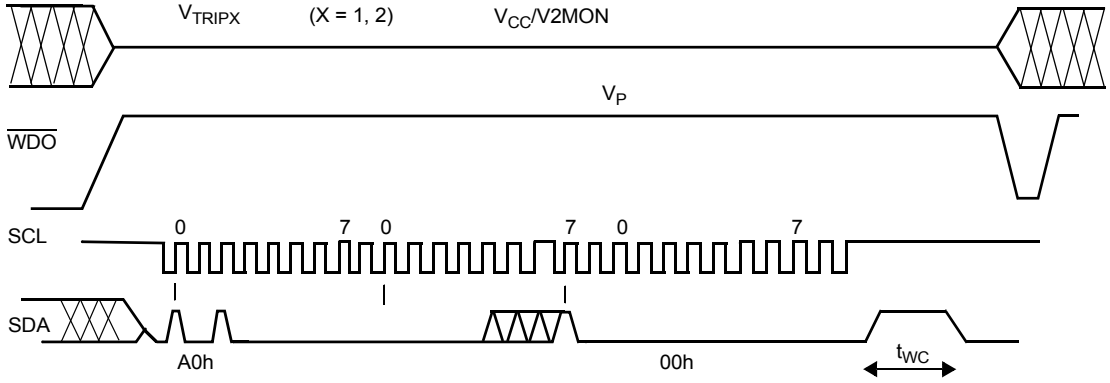
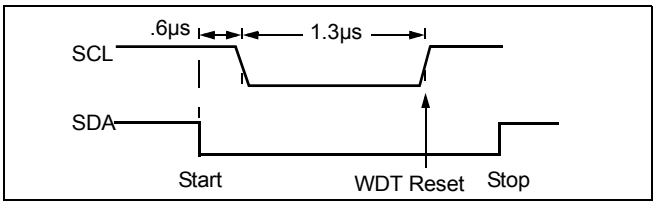


Figure 4. Watchdog Restart



V1 AND V2 THRESHOLD PROGRAM PROCEDURE (OPTIONAL)

The X40420, X40421 is shipped with standard V1 and V2 threshold (V_{TRIP1}, V_{TRIP2}) voltages. These values will not change over normal operating and storage conditions. However, in applications where the standard thresholds are not exactly right, or if higher precision is needed in the threshold value, the X40420 trip points may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.

Setting a V_{TRIPx} Voltage (x = 1, 2)

There are two procedures used to set the threshold voltages (V_{TRIPx}), depending if the threshold voltage to be stored is higher or lower than the present value. For example, if the present V_{TRIPx} is 2.9 V and the new V_{TRIPx} is 3.2 V, the new voltage can be stored directly into the V_{TRIPx} cell. If however, the new setting is to be lower than the present setting, then it is necessary to "reset" the V_{TRIPx} voltage before setting the new value.

Setting a Higher V_{TRIPx} Voltage (x = 1, 2)

To set a V_{TRIPx} threshold to a new voltage which is higher than the present threshold, the user must apply the desired V_{TRIPx} threshold voltage to the corresponding input pin (Vcc(V1MON) or V2MON). Then, a program-ming voltage (Vp) must be applied to the $\overline{WDO}$ pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h, followed by the Byte Address 01h for V_{TRIP1}, and 09h for V_{TRIP2}, and a 00h Data Byte in order to program V_{TRIPx}.

The STOP bit following a valid write operation initiates the programming sequence. Pin $\overline{WDO}$ must then be brought LOW to complete the operation.

To check if the V_{TRIPX} has been set, set VXMON to a value slightly greater than V_{TRIPX} (that was previously set). Slowly ramp down VXMON and observe when the corresponding outputs (LOWLINE and $\overline{V2FAIL}$) switch. The voltage at which this occurs is the V_{TRIPX} (actual).

CASE A

Now if the desired V_{TRIPX} is greater than the V_{TRIPX} (actual), then add the difference between V_{TRIPX} (desired) - V_{TRIPX} (actual) to the original V_{TRIPX} desired. This is your new V_{TRIPX} that should be applied to VXMON and the whole sequence should be repeated again (see Figure 5).

CASE B

Now if the V_{TRIPX} (actual), is higher than the V_{TRIPX} (desired), perform the reset sequence as described in the next section. The new V_{TRIPX} voltage to be applied to VXMON will now be: V_{TRIPX} (desired) - (V_{TRIPX} (actual) - V_{TRIPX} (desired)).

Note: 1. This operation does not corrupt the memory array.

2. Set V_{CC} = 5V, when V_{TRIP2} is being programmed

Setting a Lower V_{TRIPx} Voltage (x = 1, 2)

In order to set V_{TRIPx} to a lower voltage than the present value, then V_{TRIPx} must first be "reset" according to the procedure described in the following section. Once V_{TRIPx} has been "reset", then V_{TRIPx} can be set to the desired voltage using the procedure described in "Setting a Higher V_{TRIPx} Voltage".

Resetting the V_{TRIPx} Voltage

To reset a V_{TRIPx} voltage, apply the programming voltage (Vp) to the $\overline{WDO}$ pin before a START condition is set up on SDA. Next, issue on the SDA pin the Slave Address A0h followed by the Byte Address 03h for V_{TRIP1} and 0Bh for V_{TRIP2}, followed by 00h for the Data Byte in order to reset V_{TRIPx}. The STOP bit following a valid write operation initiates the programming sequence. Pin $\overline{WDO}$ must then be brought LOW to complete the operation.

After being reset, the value of V_{TRIPx} becomes a nominal value of 1.7V or lesser.

Note: This operation does not corrupt the memory array.

System Battery Switch

As long as V_{CC} exceeds the low voltage detect threshold V_{TRIP}, V_{OUT} is connected to V_{CC} through a 5Ω (typical) switch. When the V_{CC} has fallen below $V1_{TRIP}$, then V_{CC} is applied to V_{OUT} if V_{CC} is or equal to or greater than V_{BATT} - 0.03V. When V_{CC} drops to less than V_{BATT} - 0.03V, then V_{OUT} is connected to V_{BATT} through an 80Ω (typical) switch. V_{OUT} typically supplies the system static RAM voltage, so the switchover circuit operates to protect the contents of the static RAM during a power failure. Typically, when V_{CC} has failed, the SRAMs go into a lower power state and draw much less current than in their active mode. When V_{CC} returns, V_{OUT} switches back to V_{CC} when V_{CC} exceeds V_{BATT} + 0.03V. There is a 60mV hysteresis around this battery switch threshold to prevent oscillations between supplies.

While V_{CC} is connected to V_{OUT} the BATT-ON pin is pulled LOW. The signal can drive an external PNP transistor to provide additional current to the external circuits during normal operation.

Operation

The device is in normal operation with V_{CC} as long as $V_{CC} > V_{TRIP1}$. It switches to the battery backup mode when V_{CC} goes away.

Condition	Mode of Operation
$V_{CC} > V_{TRIP1}$	Normal Operation
$V_{CC} > V_{TRIP1}$ & $V_{BATT} = 0$	Normal Operation without battery backup capability
$0 \le V_{CC} \le V_{TRIP1}$ and $V_{CC} < V_{BATT}$	Battery Backup mode; RESET signal is asserted. No communication to the device is allowed.

Control Register

The Control Register provides the user a mechanism for changing the Block Lock and Watchdog Timer settings. The Block Lock and Watchdog Timer bits are nonvolatile and do not change when power is removed.

The Control Register is accessed with a special preamble in the slave byte (1011) and is located at address 1FFh. It can only be modified by performing a byte write operation directly to the address of the register and only one data byte is allowed for each register write operation. Prior to writing to the Control Register, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps. See "Writing to the Control Registers" on page 9.

The user must issue a stop, after sending this byte to the register, to initiate the nonvolatile cycle that stores WD1, WD0, PUP1, PUP0, and BP. The X40420 will not acknowledge any data bytes written after the first byte is entered.

The state of the Control Register can be read at any time by performing a random read at address 01Fh, using the special preamble. Only one byte is read by each register read operation. The master should supply a stop condition to be consistent with the bus protocol, but a stop is not required to end this operation.

7	6	5	4	3	2	1	0
PUP1	WD1	WD0	BP	0	RWEL	WEL	PUP0

RWEL: Register Write Enable Latch (Volatile)

The RWEL bit must be set to “1” prior to a write to the Control Register.

Figure 5. Sample V_{TRIP} Reset Circuit

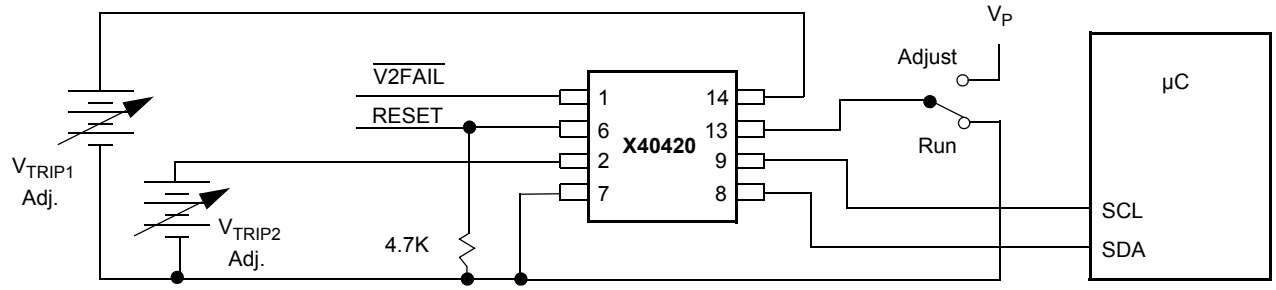
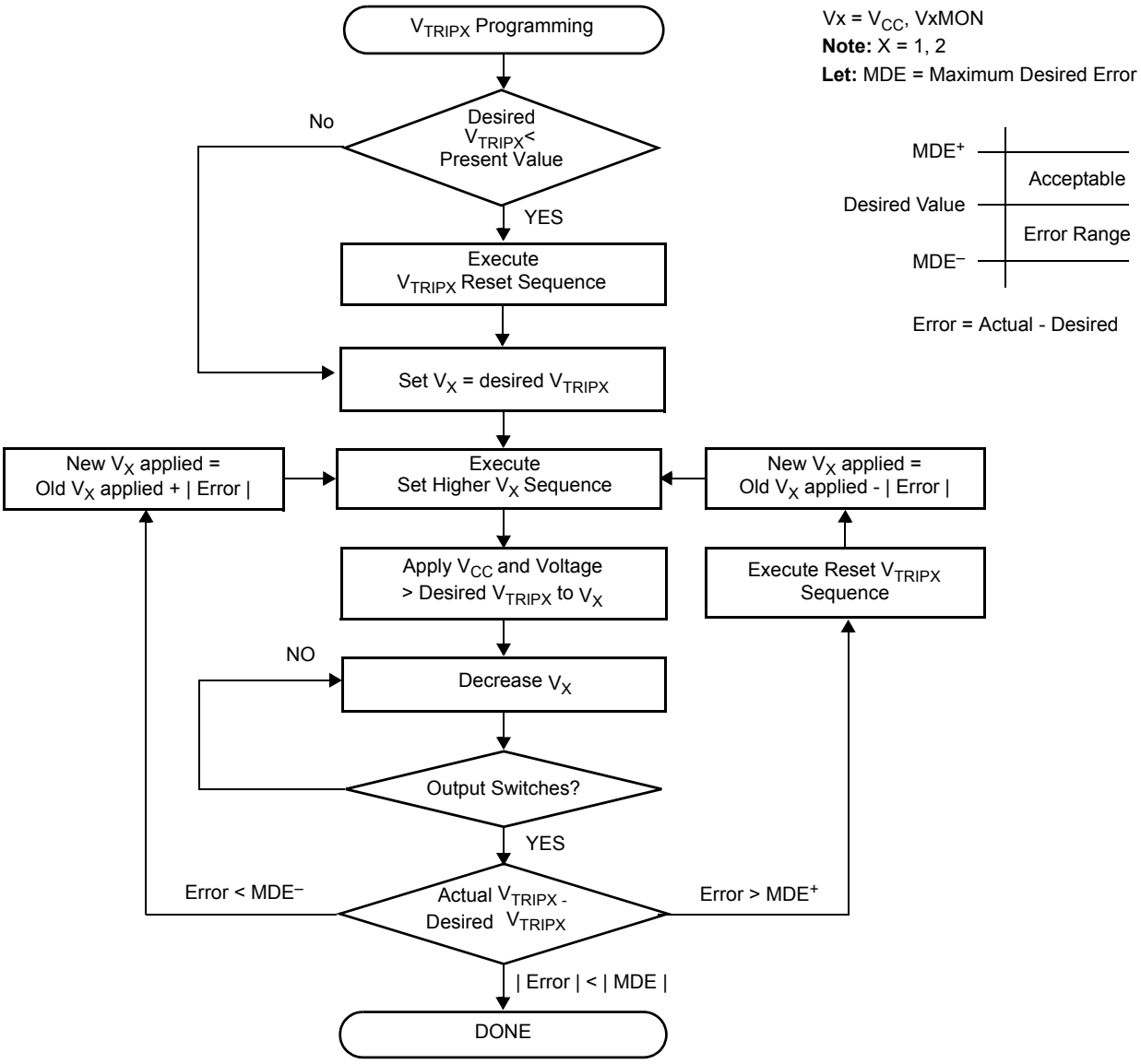


Figure 6. V_{TRIPX} Set/Reset Sequence (X = 1, 2)



WEL: Write Enable Latch (Volatile)

The WEL bit controls the access to the memory and to the Register during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to any address, including any control registers will be ignored (no acknowledge will be issued after the Data Byte). The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the control register.

Once set, WEL remains set until either it is reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the control register) or until the part powers up again. Writes to the WEL bit do not cause a high voltage write cycle, so the device is ready for the next operation immediately after the stop condition.

BP: Block Protect Bit (Nonvolatile)

The Block Protect Bits BP determines which blocks of the array are write protected. A write to a protected block of memory is ignored. The block protect bit will prevent write operations to half the array segment.

BP	Protected Addresses (Size)	Memory Array Lock
0	None	None
1	100h – 1FFh (256 bytes)	Upper Half of Memory Array

PUP1, PUP0: Power-uppower-up Bits (Nonvolatile)

The Power-up bits, PUP1 and PUP0, determine the t_{PURST} time delay. The nominal power-up times are shown in the following table.

PUP1	PUP0	Power-on Reset Delay (t_{PURST})
0	0	50ms
0	1	200ms (default)
1	0	400ms
1	1	800ms

WD1, WD0: Watchdog Timer Bits

The bits WD1 and WD0 control the period of the Watchdog Timer. The options are shown below.

WD1	WD0	Watchdog Time Out Period
0	0	1.4 seconds
0	1	200 milliseconds
1	0	25 milliseconds
1	1	disabled (factory default)

Writing to the Control Registers

Changing any of the nonvolatile bits of the control and trickle registers requires the following steps:

– Write a 02H to the Control Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceded by a start and ended with a stop).

– Write a 06H to the Control Register to set the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation proceeded by a start and ended with a stop).

– Write a one byte value to the Control Register that has all the control bits set to the desired state. The Control register can be represented as *qxys* 001*r* in binary, where *xy* are the WD bits, and st are the BP bits and *qr* are the power-up bits. This operation proceeded by a start and ended with a stop bit. Since this is a nonvolatile write cycle it will take up to 10ms to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to '1' in this third step (*qxys* 011*r*) then the RWEL bit is set, but the WD1, WD0, PUP1, PUP0, and BP bits remain unchanged. Writing a second byte to the control register is not allowed. Doing so aborts the write operation and returns a NACK.

– A read operation occurring between any of the previous operations will not interrupt the register write operation.

– The RWEL bit cannot be reset without writing to the nonvolatile control bits in the control register, power cycling the device or attempting a write to a write protected block.

To illustrate, a sequence of writes to the device consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits in the Control Register to 0. A sequence of [02H, 06H, 06H] will leave the nonvolatile bits unchanged and the RWEL bit remains set.

Note: 1. t_{PURST} is set to 200ms as factory default.
2. Watchdog timer bits are shipped disabled.

Fault Detection Register (FDR)

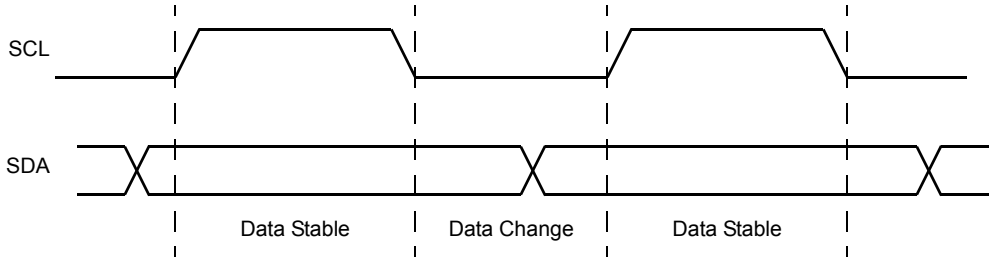
The Fault Detection Register provides the user the status of what causes the system reset active. The Manual Reset Fail, Watchdog Timer Fail and Three Low Voltage Fail bits are volatile

7	6	5	4	3	2	1	0
LV1F	LV2F	0	WDF	MRF	0	0	0

The FDR is accessed with a special preamble in the slave byte (1011) and is located at address 0FFh. It can only be modified by performing a byte write operation directly to the address of the register and only one data byte is allowed for each register write operation.

There is no need to set the WEL or RWEL in the control register to access this fault detection register.

Figure 7. Valid Data Changes on the SDA Bus



At power-up, the Fault Detection Register is defaulted to all “0”. The system needs to initialize this register to all “1” before the actual monitoring take place. In the event of any one of the monitored sources failed. The corresponding bits in the register will change from a “1” to a “0” to indicate the failure. At this moment, the system should perform a read to the register and noted the cause of the reset. After reading the register the system should reset the register back to all “1” again. The state of the Fault Detection Register can be read at any time by performing a random read at address 0FFh, using the special preamble.

The FDR can be read by performing a random read at 0FFh address of the register at any time. Only one byte of data is read by the register read operation.

MRF: Manual Reset Fail Bit (Volatile)

The MRF bit will set to “0” when Manual Reset input goes active.

WDF: Watchdog Timer Fail Bit (Volatile)

The WDF bit will set to “0” when WDO goes active.

LV1F: Low V_{CC} Reset Fail Bit (Volatile)

The LV1F bit will be set to “0” when V_{CC} (V1MON) falls below V_{TRIP1}.

LV2F: Low V2MON Reset Fail Bit (Volatile)

The LV2F bit will be set to “0” when V2MON falls below V_{TRIP2}.

Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

Serial Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 7.

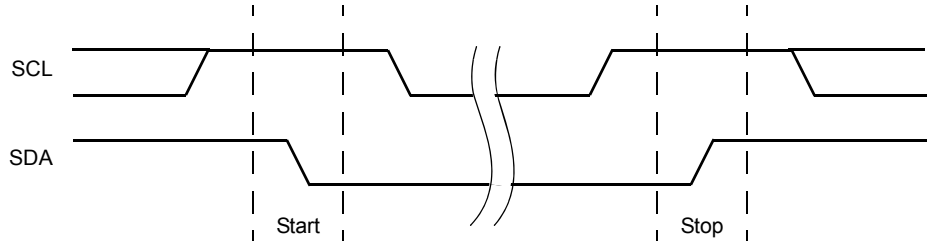
Serial Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 8.

Serial Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 8.

Figure 8. Valid Start and Stop Conditions



Serial Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. See Figure 9.

The device will respond with an acknowledge after recognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for the Slave Address Byte when the Device Identifier and/or Select bits are incorrect.

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

Serial Write Operations

Byte Write

For a write operation, the device requires the Slave Address Byte and a Word Address Byte. This gives the master access to any one of the words in the array. After receipt of the Word Address Byte, the device responds with an acknowledge, and awaits the next eight bits of data. After receiving the 8 bits of the Data Byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 12.

A write to a protected block of memory will suppress the acknowledge bit.

Figure 9. Acknowledge Response From Receiver

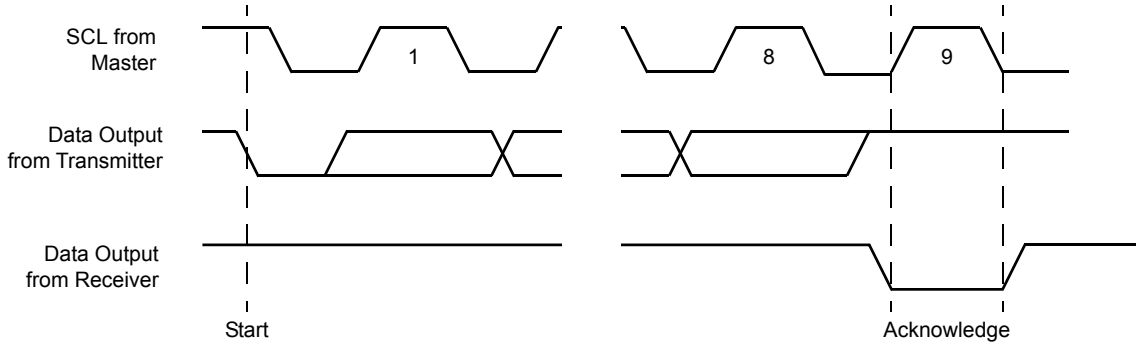
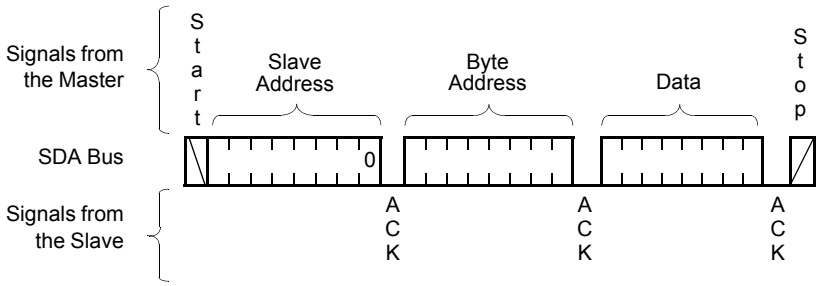


Figure 10. Byte Write Sequence



Page Write

The device is capable of a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the device will respond with an acknowledge, and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it “rolls over” and goes back to ‘0’ on the same page.

This means that the master can write 16 bytes to the page starting at any location on that page. If the master begins writing at location 10, and loads 12 bytes, then the first 6 bytes are written to locations 10 through 15, and the last 6 bytes are written to locations 0 through 5. Afterwards, the address counter would point to location 6 of the page that was just written. If the master supplies more than 16 bytes of data, then new data overwrites the previous data, one byte at a time.

Figure 11. Page Write Operation

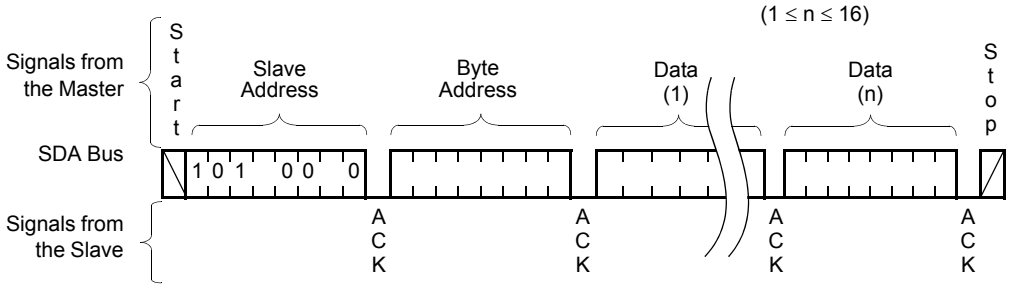
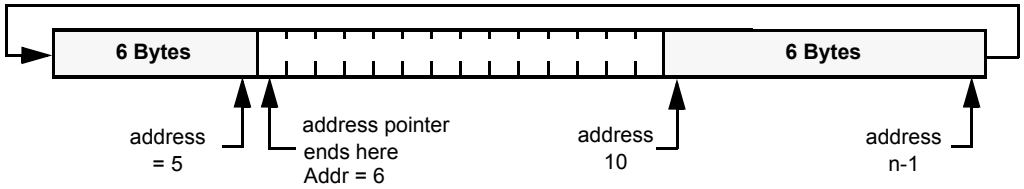


Figure 12. Writing 12 bytes to a 16-byte Page Starting at Location 10



The master terminates the Data Byte loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. See Figure 11 for the address, acknowledge, and data transfer sequence.

Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte plus the subsequent ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte plus its associated ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be effected.

Acknowledge Polling

The disabling of the inputs during high voltage cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master's byte load operation, the device initiates the internal high voltage cycle. Acknowledge polling can be initiated immediately. To do this, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. See Figure 13.

Serial Read Operations

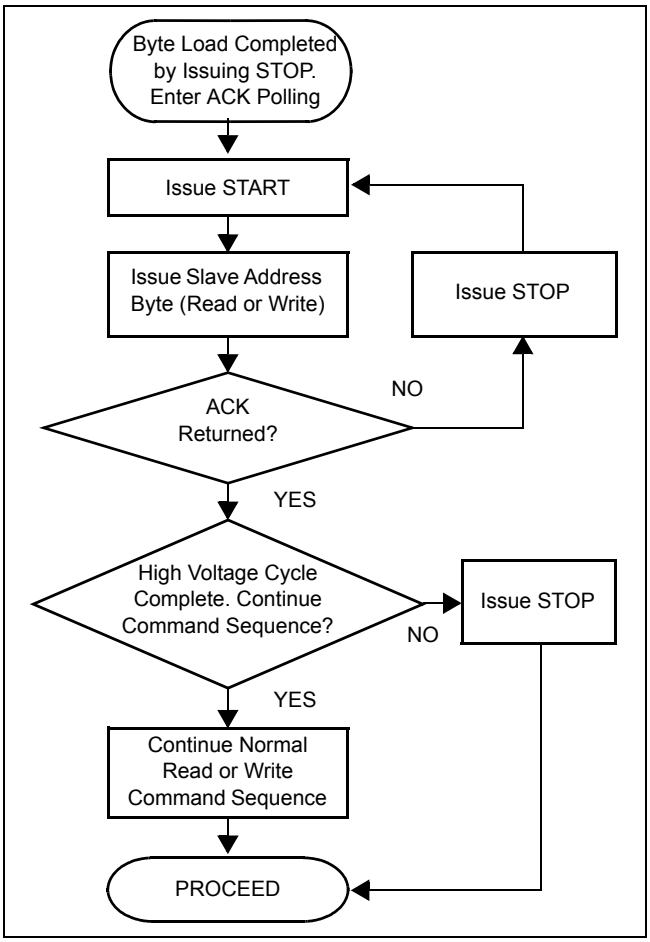
Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power-up, the address of the address counter is undefined, requiring a read or write operation for initialization.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. See Figure 14 for the address, acknowledge, and data transfer sequence.

Figure 13. Acknowledge Polling Sequence



It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition and the Slave Address Byte, receives an acknowledge, then issues the Word Address Bytes. After acknowledging receipts of the Word Address Bytes, the master immediately issues another start condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. See Figure 15 for the address, acknowledge, and data transfer sequence.

A similar operation called “Set Current Address” where the device will perform this operation if a stop is issued instead of the second start is shown in Figure 15. The device will go into standby mode after the stop and all bus activity will be ignored until a start is detected. This operation loads the new address into the address counter. The next Current Address Read operation will read from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first Data Byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter “rolls over” to address 0000_H and the device continues to output data for each acknowledge received. See Figure 17 for the acknowledge and data transfer sequence.

SERIAL DEVICE ADDRESSING

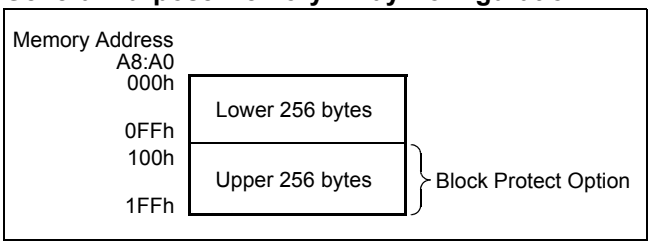
Memory Address Map

CR, Control Register, CR7: CR0
Address: $1FF_{hex}$

FDR, Fault DetectionRegister, FDR7: FDR0
Address: $0FF_{hex}$

General Purpose Memory Organization, A8:A0
Address: 00h to 1FFh

General Purpose Memory Array Configuration



Slave Address Byte

Following a start condition, the master must output a Slave Address Byte. This byte consists of several parts:

– a device type identifier that is always “1010” when accessing the array and “1011” when accessing the control register and fault detection register.

– two bits of “0”.

– one bit that becomes the MSB of the memory address X_4.

– last bit of the slave command byte is a R/$\overline{W}$ bit. The R/$\overline{W}$ bit of the Slave Address Byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. See Figure 16.

Figure 14. Current Address Read Sequence

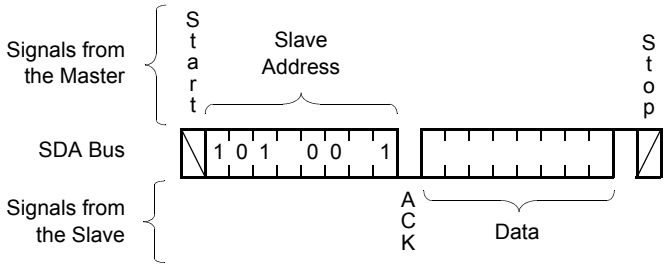


Figure 15. Random Address Read Sequence

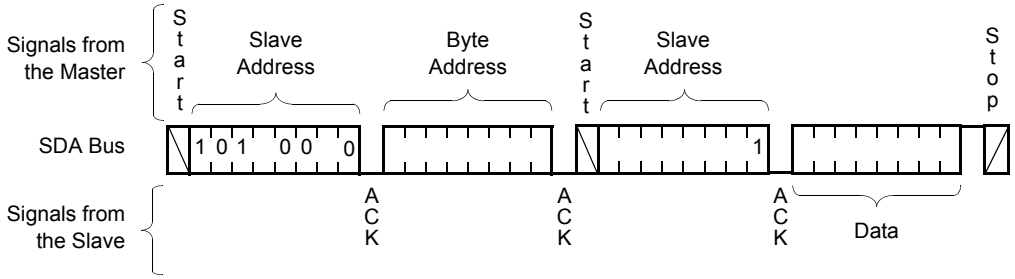


Figure 16. X40410/11 Addressing

	Slave Byte							
General Purpose Memory	1	0	1	0	0	0	A8	R/$\overline{W}$
Control Register	1	0	1	1	0	0	1	R/$\overline{W}$
Fault Detection Register	1	0	1	1	0	0	0	R/$\overline{W}$

	Word Address							
General Purpose Memory	A7	A6	A5	A4	A3	A2	A1	A0
Control Register	1	1	1	1	1	1	1	1
Fault Detection Register	1	1	1	1	1	1	1	1

Word Address

The word address is either supplied by the master or obtained from an internal counter.

Operational Notes

The device powers-up in the following state:

– The device is in the low power standby state.

– The WEL bit is set to ‘0’. In this state it is not possible to write to the device.

– SDA pin is the input mode.

– RESET/$\overline{\text{RESET}}$ Signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

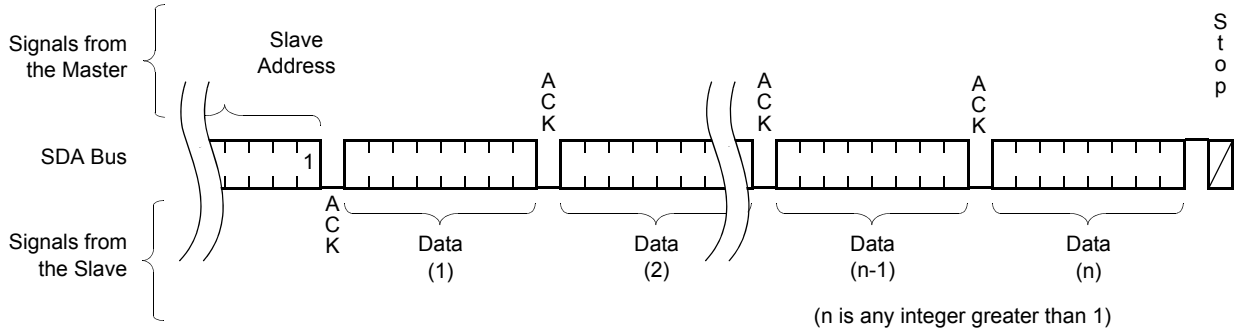
– The WEL bit must be set to allow write operations.

– The proper clock count and bit sequence is required prior to the stop bit in order to start a nonvolatile write cycle.

– A three step sequence is required before writing into the Control Register to change Watchdog Timer or Block Lock settings.

– The WP pin, when held HIGH, prevents all writes to the array and all the Register.

Figure 17. Sequential Read Sequence



ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature..... -65°C to +150°C
Voltage on any pin with
respect to V_{SS} ..... -1.0V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10s) ..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C

Version	Chip Supply Voltage	Monitored Voltages*
-A or -B	2.7V to 5.5V	2.6 to 5.5V
-C	2.7V to 5.5V	1.6V to 3.6V

*See ordering Info

D.C. OPERATING CHARACTERISTICS

(Over the recommended operating conditions unless otherwise specified)

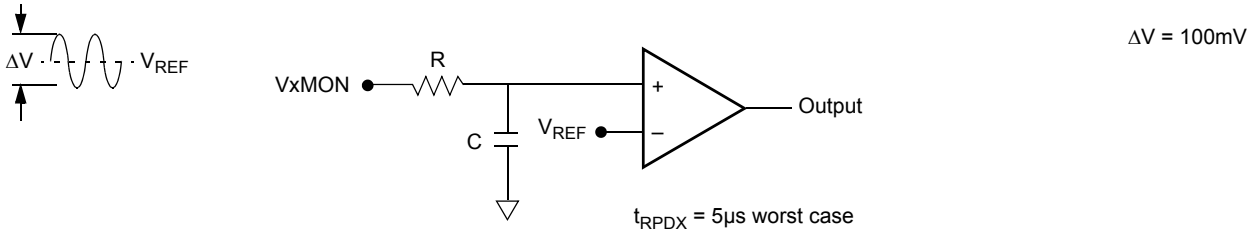
Symbol	Parameter	Min.	Typ.(5)	Max.	Unit	Test Conditions
I_{CC1}(1)	Active Supply Current (V_{CC}) Read (Excludes I_{OUT})			1.5	mA	$V_{IL} = V_{CC}$ x 0.1 $V_{IH} = V_{CC}$ x 0.9, f_{SCL} = 400kHz
I_{CC2}(1)	Active Supply Current (V_{CC}) Write Non Volatile Memory (Excludes I_{OUT})			3.0	mA	
I_{SB1}(1)(7)	Standby Current (V_{CC}) AC (WDT off)		6	10	µA	$V_{IL} = V_{CC}$ x 0.1 VIH = V_{CC} x 0.9 f_{SCL}, f_{SDA} = 400kHz
I_{SB2}(2)(7)	Standby Current (V_{CC}) DC (WDT on)		25	30	µA	$V_{SDA} = V_{SCL} = V_{CC}$ Others = GND or V_{CC}
I_{BATT1}(3)(7)	V_{BATT} Current (Excludes I_{OUT})		0.4	1	µA	$V_{OUT} = V_{CC}$
I_{BATT2}(7)	V_{BATT} Current (Excludes I_{OUT}) (Battery Backup Mode)			6	µA	V_{BATT} = 2.8V V_{OUT} = Open
V_{OUT1}(7)	Output Voltage ($V_{CC} > V_{BATT}$ + 0.03V or $V_{CC} > V_{TRIP1}$)	V_{CC}-0.05V V_{CC}-0.5V			V	I_{OUT} = 5mA (4.5-5.5V) I_{OUT} = 50mA (4.5-5.5V)
V_{OUT2}(7)	Output Voltage ($V_{CC} < V_{BATT}$ – 0.03V and $V_{CC} < V_{TRIP1}$) {Battery Backup}	V_{BATT}-0.2			V	I_{OUT} = 250µA
V_{OLB}	Output (BATT-ON) LOW Voltage			0.4	V	I_{OL} = 3.0mA (4.5-5.5V)
V_{OHB}	Output (BATT-ON) HIGH Voltage	V_{OUT}-0.8			V	I_{OH} = -0.4mA (4.5-5.5V)
V_{BSH}(7)	Battery Switch Hysteresis ($V_{CC} < V_{TRIP1}$)		30 -30		mV	Power-up Power-down
I_{LI}	Input Leakage Current (SCL, $\overline{MR}$, WP)			10	µA	V_{IL} = GND to V_{CC}
I_{LO}	Output Leakage Current (SDA, $\overline{V2FAIL}$, $\overline{WDO}$, $\overline{RESET}$)			10	µA	V_{SDA} = GND to V_{CC} Device is in Standby(2)
V_{IL}(3)	Input LOW Voltage (SDA, SCL, $\overline{MR}$, WP)	-0.5		V_{CC} x 0.3	V	
V_{IH}(3)	Input HIGH Voltage (SDA, SCL, $\overline{MR}$, WP)	V_{CC} x 0.7		V_{CC} + 0.5	V	

D.C. OPERATING CHARACTERISTICS (Continued)
(Over the recommended operating conditions unless otherwise specified)

Symbol	Parameter	Min.	Typ.(5)	Max.	Unit	Test Conditions
V_{HYS}(7)	Schmitt Trigger Input Hysteresis • Fixed input level • V_{CC} related level	 0.2 .05 x V_{CC}			 V V	
V_{OL}	Output LOW Voltage (SDA, RESET/ RESET, LOWLINE, V2FAIL, WDO)			0.4	V	I_{OL} = 3.0mA (2.7-5.5V) I_{OL} = 1.8mA (2.4-3.6V)
V_{CC} Supply						
V_{TRIP1}(6)	V_{CC} Reset Trip Point Voltage Range	2.0		4.75	V	
		4.55	4.6	4.65		A, B Version
		2.85	2.9	2.95		C Version
t_{RPDL}(7)	V_{TRIP1} to $\overline{LOWLINE}$			5	µS	
Second Supply Monitor						
V_{TRIP2}(6)	V2MON Reset Trip Point Voltage Range	0.9		3.5	V	
		2.85	2.9	2.95		A Version
		2.55	2.6	2.65		B Version
		1.55	1.6	1.65		C Version
t_{RPD2}(7)	V_{TRIP2} to $\overline{V2FAIL}$			5	µS	

Notes: (1) The device enters the Active state after any start, and remains active until: 9 clock cycles later if the Device Select Bits in the Slave Address Byte are incorrect; 200ns after a stop ending a read operation; or t_{WC} after a stop ending a write operation.
(2) The device goes into Standby: 200ns after any stop, except those that initiate a high voltage write cycle; t_{WC} after a stop that initiates a high voltage cycle; or 9 clock cycles after any start that is not followed by the correct Device Select Bits in the Slave Address Byte.
(3) Negative numbers indicate charging current, positive numbers indicate discharge current.
(4) V_{IL} Min. and V_{IH} Max. are for reference only and are not tested.
(5) At 25°C, V_{CC} = 3V.
(6) See ordering information for standard programming levels. For custom programming levels, contact factory.
(7) Based on characterization data only.

EQUIVALENT INPUT CIRCUIT FOR VxMON (x = 1, 2)

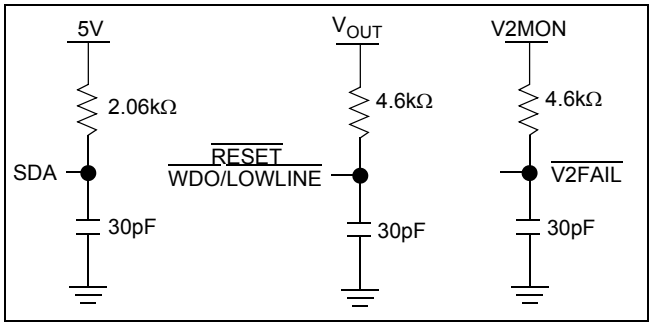


CAPACITANCE

Symbol	Parameter	Max.	Unit	Test Conditions
C_{OUT}(1)	Output Capacitance (SDA, RESET, $\overline{RESET}$/$\overline{LOWLINE}$, V2FAIL, WDO)	8	pF	V_{OUT} = 0V
C_{IN}(1)	Input Capacitance (SCL, WP)	6	pF	V_{IN} = 0V

Note: (1) This parameter is not 100% tested.

EQUIVALENT A.C. OUTPUT LOAD CIRCUIT FOR V_{CC} = 5V



A.C. TEST CONDITIONS

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing levels	V_{CC} x 0.5
Output load	Standard output load

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

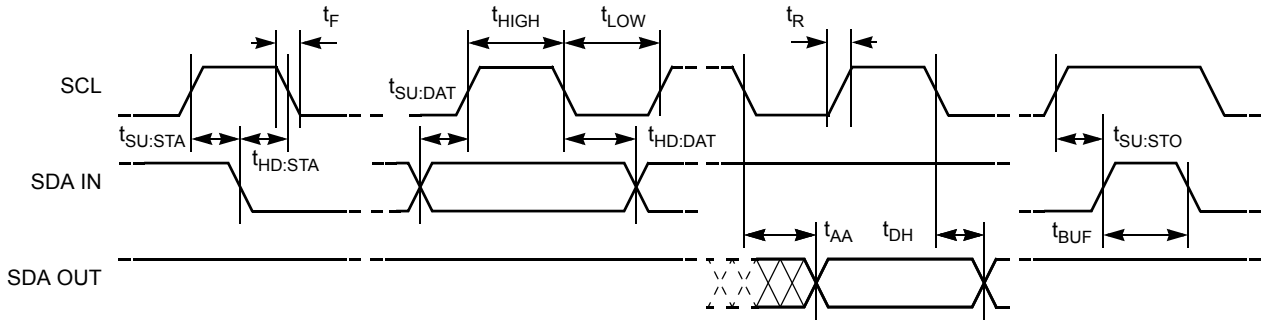
A.C. CHARACTERISTICS

Symbol	Parameter	400kHz		Unit
		Min.	Max.	
f_{SCL}	SCL Clock Frequency		400	kHz
t_{IN}	Pulse width Suppression Time at inputs	50		ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus free before start of new transmission	1.3		µs
t_{LOW}	Clock LOW Time	1.3		µs
t_{HIGH}	Clock HIGH Time	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time	0.6		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
$t_{SU:DAT}$	Data In Setup Time	100		ns
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{DH}	Data Output Hold Time	50		ns
t_R	SDA and SCL Rise Time	20 +.1Cb(1)	300	ns
t_F	SDA and SCL Fall Time	20 +.1Cb(1)	300	ns
$t_{SU:WP}$	$\overline{WP}$ Setup Time	0.6		µs
$t_{HD:WP}$	$\overline{WP}$ Hold Time	0		µs
Cb	Capacitive load for each bus line		400	pF

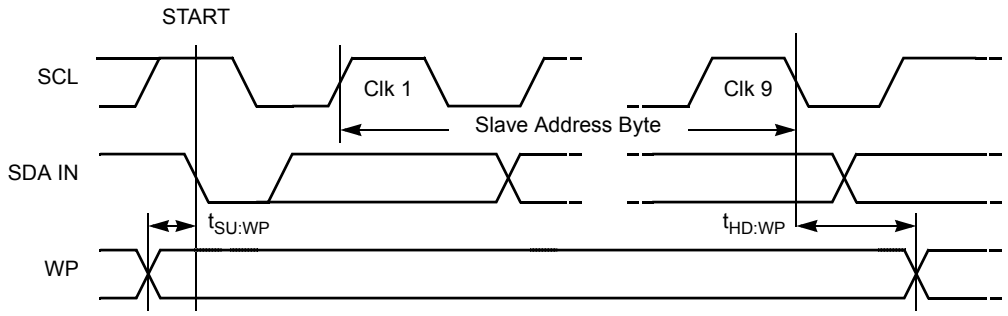
Note: (1) Cb = total capacitance of one bus line in pF.

TIMING DIAGRAMS

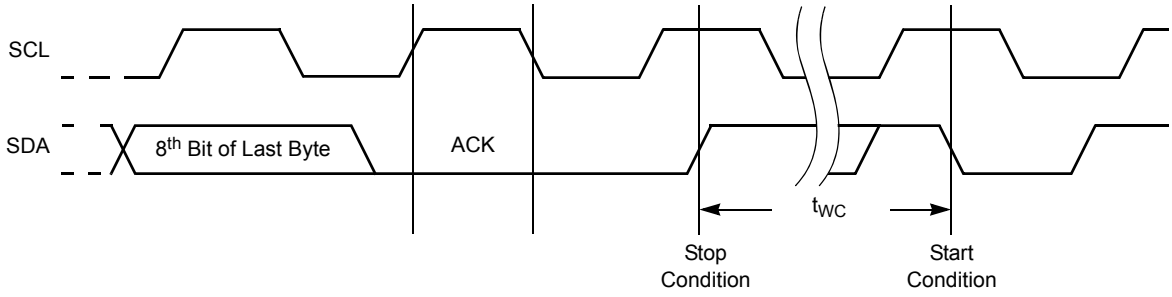
Bus Timing



WP Pin Timing



Write Cycle Timing

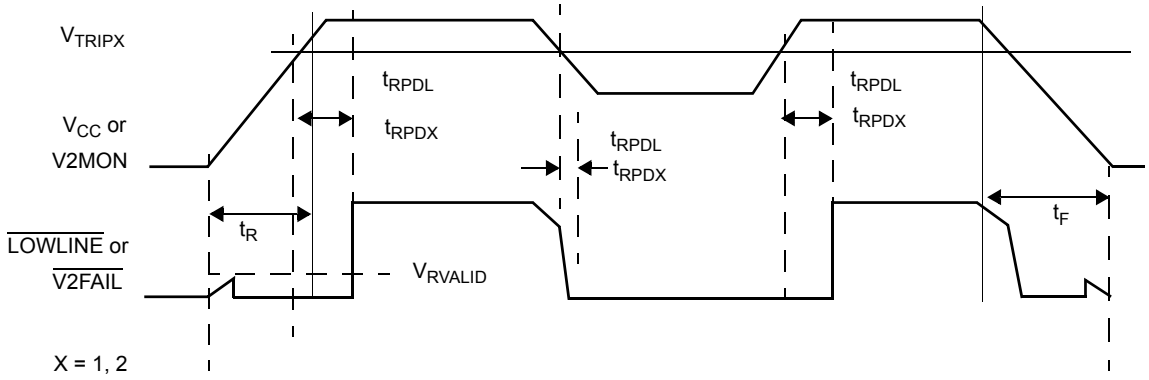


Nonvolatile Write Cycle Timing

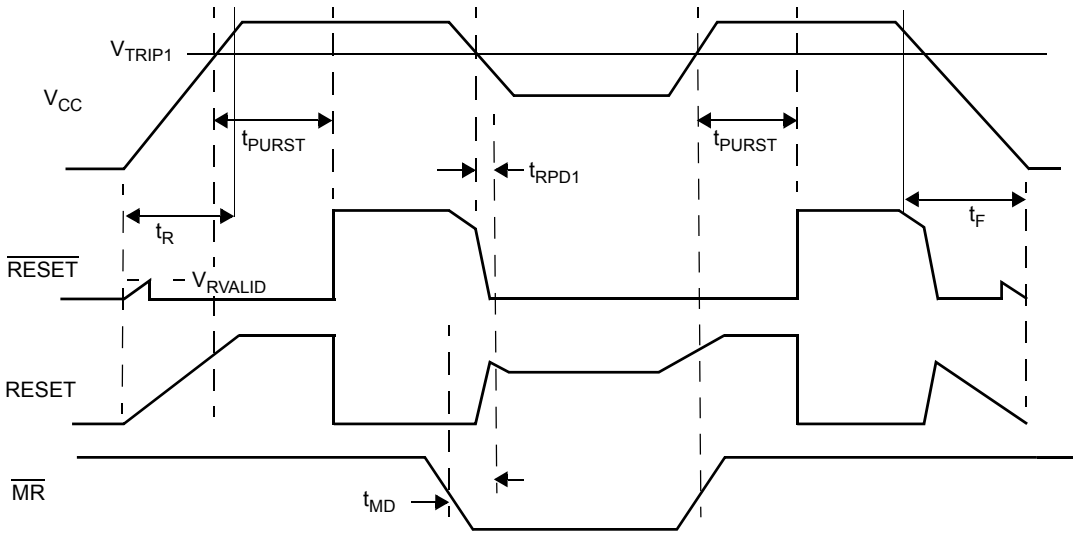
Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
t_{WC}(1)	Write Cycle Time		5	10	ms

Note: (1) t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

Power Fail Timings



RESET/$\overline{\text{RESET}}$/$\overline{\text{MR}}$ Timings

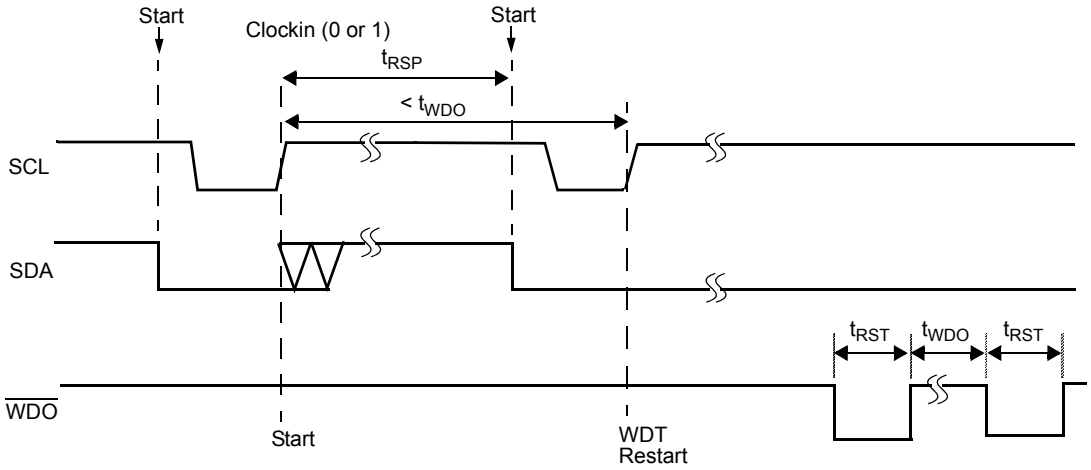


LOW VOLTAGE AND WATCHDOG TIMINGS PARAMETERS (@25°C, VCC = 5V)

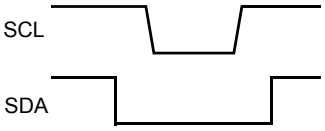
Symbol	Parameters	Min.	Typ.	Max.	Unit
t_{RPD1}(1) t_{RPDL}	V_{TRIP1} to $\overline{\text{RESET}}$/RESET (Power-down only) V_{TRIP1} to $\overline{\text{LOWLINE}}$			5	µs
t_{LR}(1)	$\overline{\text{LOWLINE}}$ to RESET/$\overline{\text{RESET}}$ delay (Power-down only) [= t_{RPD1}-t_{RPDL}]		500		ns
t_{RPD2}(1)	V_{TRIP2} to $\overline{\text{V2FAIL}}$			5	µs
t_{PURST}	Power-on Reset delay: PUP1=0, PUP0=0 PUP1=0, PUP0=1 (factory default) PUP1=1, PUP0=0 PUP1=1, PUP0=1		 50(1) 200 400(1) 800(1)		 ms ms ms ms
t_F	V_{CC}, V2MON Fall Time	20			mV/µs
t_R	V_{CC}, V2MON Rise Time	20			mV/µs
V_{RVALID}	Reset Valid V_{CC}	1			V
t_{MD}	$\overline{\text{MR}}$ to RESET/ $\overline{\text{RESET}}$ delay (activation only)	500			ns
t_{in1}	Pulse width Suppression Time for $\overline{\text{MR}}$	50			ns
t_{WDO}	Watchdog Timer Period: WD1=0, WD0=0 WD1=0, WD0=1 WD1=1, WD0=0 WD1=1, WD0=1 (factory default)		 1.4(1) 200(1) 25 OFF		 s ms ms
t_{RST1}	Watchdog Reset Time Out Delay WD1=0, WD0=0 WD1=0, WD0=1	100	200	300	ms
t_{RST2}	Watchdog Reset Time Out Delay WD1=1, WD0=0	12.5	25	37.5	ms
t_{RSP}	Watchdog timer restart pulse width	1			µs

Note: (1) Based on characterization data.

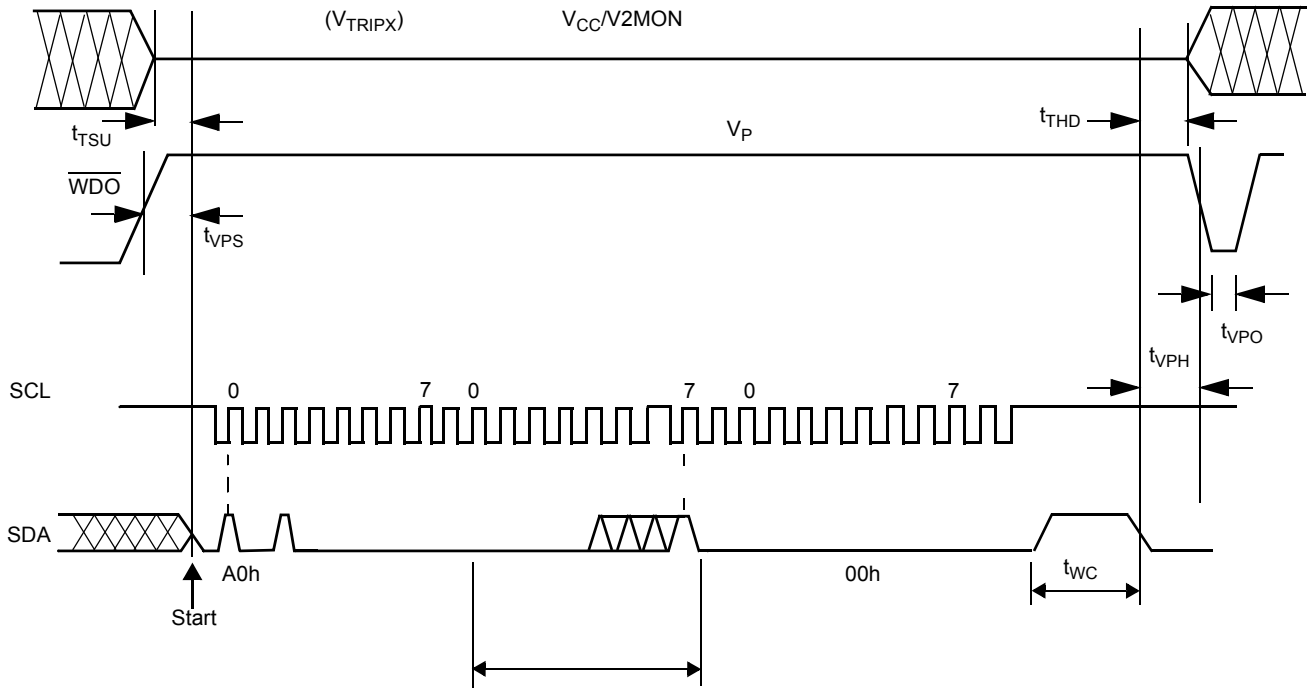
Watchdog Time Out For 2-Wire Interface



Minimum Sequence to Reset WDT



V_{TRIPX} Set/Reset Conditions



01h* sets V_{TRIP1} 03h* resets V_{TRIP1}
09h* sets V_{TRIP2} 0Bh* resets V_{TRIP2}

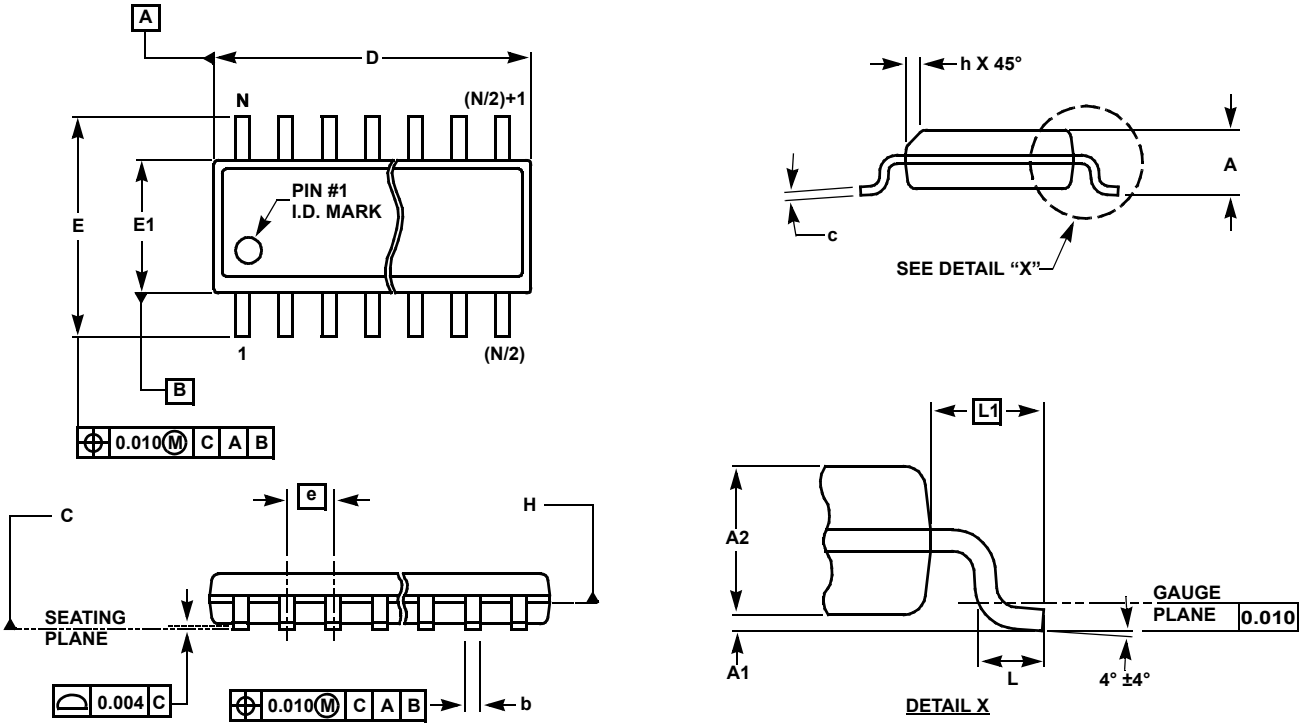
* all others reserved

V_{TRIP1}, V_{TRIP2} Programming Specifications: V_{CC} = 2.0-5.5V; Temperature = 25°C

Parameter	Description	Min.	Max.	Unit
t_{VPS}	$\overline{WDO}$ Program Voltage Setup time	10		µs
t_{VPH}	$\overline{WDO}$ Program Voltage Hold time	10		µs
t_{TSU}	V_{TRIPX} Level Setup time	10		µs
t_{THD}	V_{TRIPX} Level Hold (stable) time	10		µs
t_{WC}	V_{TRIPX} Program Cycle	10		ms
t_{VPO}	Program Voltage Off time before next cycle	1		ms
V_P	Programming Voltage	15	18	V
V_{TRAN1}	V_{TRIP1} Set Voltage Range	2.0	4.75	V
V_{TRAN2}	V_{TRIP2} Set Voltage Range	0.9	3.5	V
V_{tv}	V_{TRIPX} Set Voltage variation after programming (0-75°C).	-25	+25	mV
t_{VPS}	$\overline{WDO}$ Program Voltage Setup time	10		µs

V_{TRIPX} programming parameters are periodically sampled and are not 100% tested.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

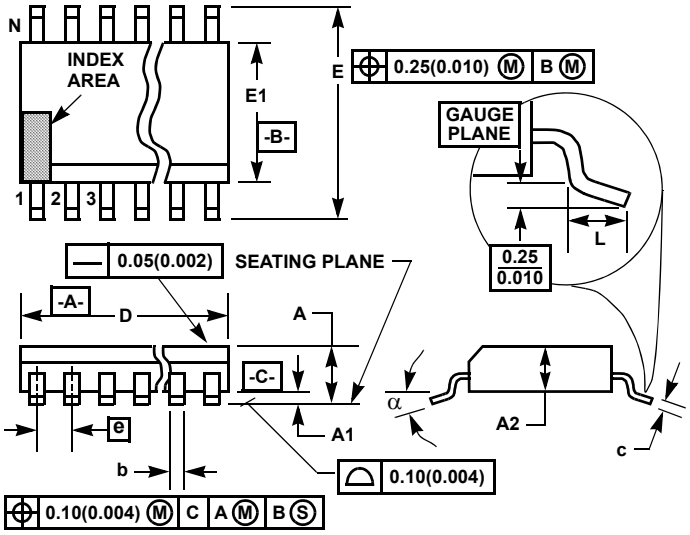
SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0°	8°	0°	8°	-

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